- **Project: Annual Handoff flow process at BlackChip Semiconductors (BCS)**

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Project Phase 1

Company Background:

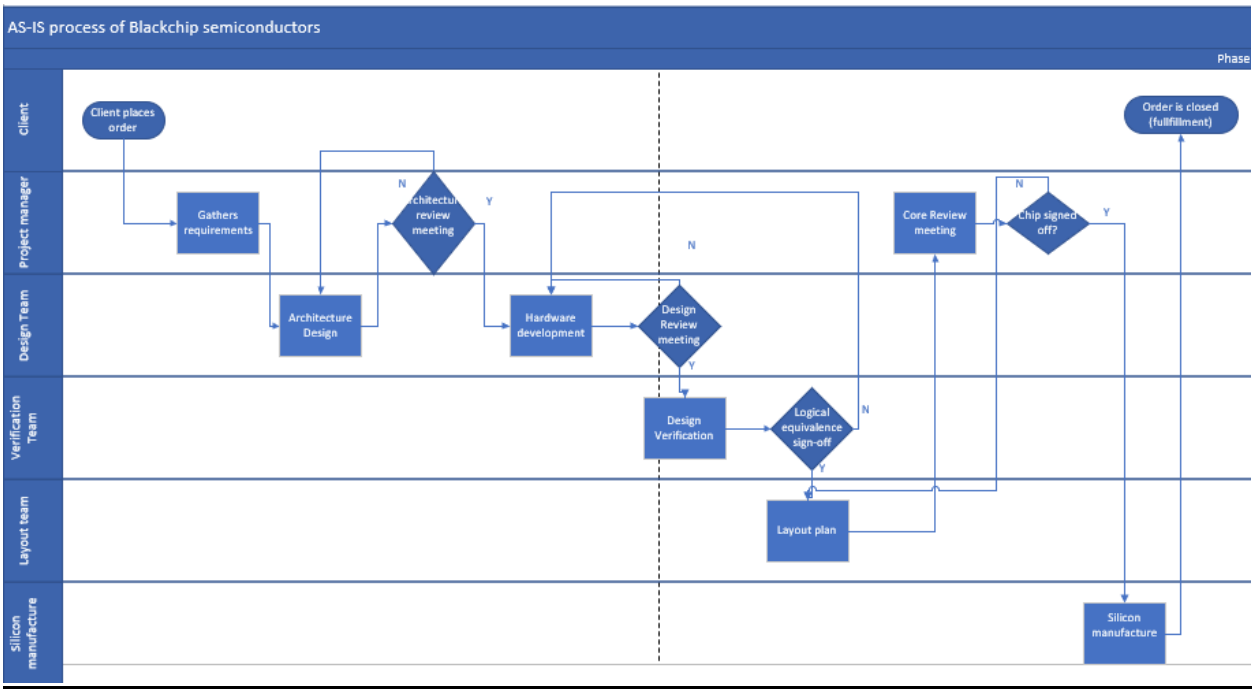
Blackchip is an upcoming semiconductor start-up specialized in developing low-cost hardware solutions for clients that are involved in Non-Profit activities. A typical project at BlackChip semiconductor starts with client placing a order and goes through several stages like
sales, management, design, verification, layout planning, silicon manufacturing.

Process and Actors:

Once the client places an order, the sales inventory gets updated and a program manager gathers requirements to communicate to the designated Design Team. There are frequent architecture review meetings that are held until architecture is finalized. Once the architecture is finalized then the sales team performs projected cost benefit analysis and parallely Design development begins. For each design cycle, the verification team works on finding bugs within the design. If any breaks are found, then design is handed off to the design team to fix the issues. Once sign-off is clean, the layout engineer places the entire design on layout (A 3D platform) to simulate the actual chip before manufacturing. Once the layout process is finished, A core review meeting is held to take care of any last-minute hiccups before proceeding to silicon manufacturing.Once silicon manufacturing completes, the sales team performs actual cost benefit analysis and the order is fulfilled to the customer.

- Client - Each client places orders based on their requirements. They can make multiple orders.
- Sales - They handle the inventory updates. They also work on Actual and Projected cost benefit analysis, profit or loss estimation during the entire project life cycle.
- Project manager (Management) - They receive the order and deliver the requirements to the appropriate design teams. They also conduct the review meetings across the teams.They are also part of signing-off of the project before delivering the order to silicon manufacturer
- Design & verification Team - They design the chips, involve in hardware development and after the designing, they conduct various verifications on those chips.
- Layout team - They perform chip planning on the designed and verified chips based.
- Silicon manufacture - Post Layouting, silicon manufacturer manufactures the chips based on the order count.

Swimlane Diagram: AS-IS:



Issues with Current Process:

The current process has some minor issues.

1) The communication between the Design and Verification team. There is no necessity of frequent design meetings if the verification stage is failed. For example, if a chip "A" has met all goals of power, performance and area and signed off by the design team and if the verification team found bugs then entire design resources are wasted.So, it's not ideal for the verification team to wait until design review meetings take place. It's best to have a strategy.
2) Once the layout planning is done, there are no meetings happening internally within the team. These meetings are necessary for any team before the final core review meeting to make sure that everything is perfect.

Solution:

BCS has come up with the solutions for those two problems.

→ For the first problem, combining the design and verification teams will resolve the dependencies among the two teams. Because they are interrelated, it's best practice to put them under the same actor.

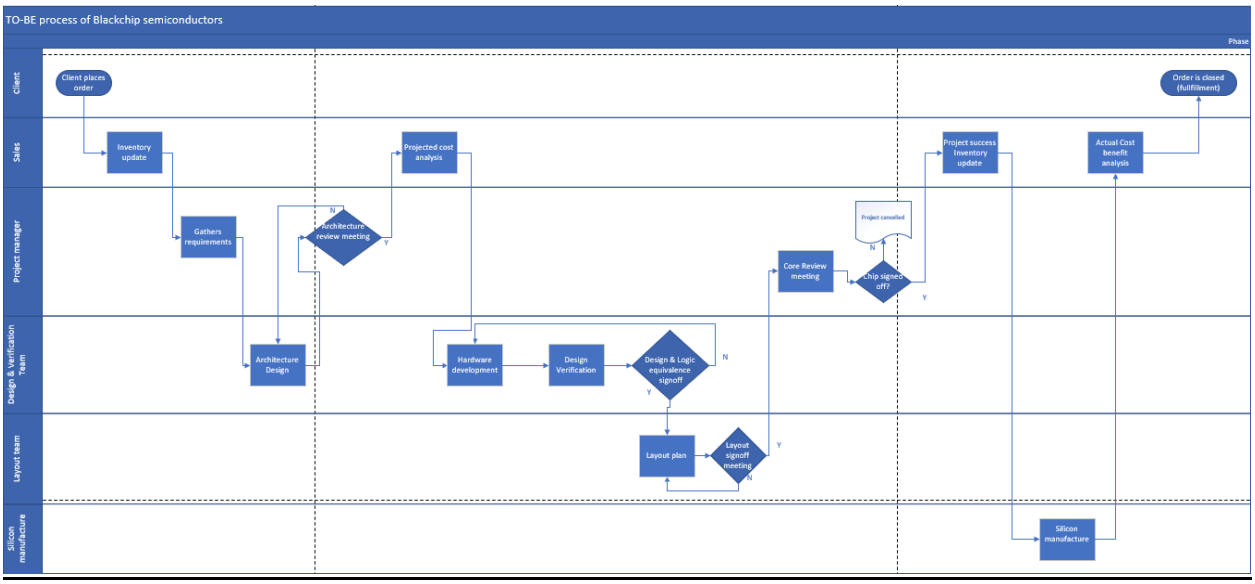
→ As far as the second problem is concerned, BCS planned to add a layout signoff meeting before the final core-review meeting. This might add some delay in the process, but it's necessary to have this meeting, because this makes the process more efficient before handing chips to the client.

Enablers:

The changes suggested above contribute to modifying Workflow Design and Information systems.

- [**Workflow Design**] Added sales as a new actor and additional process restructuring in Layout, Design and Verification for making the process more streamlined.
- [**Information systems**] Addition of actor “Sales" would create additional data which can be used to cost benefit analysis..

Swimlane Diagram: TO-BE:

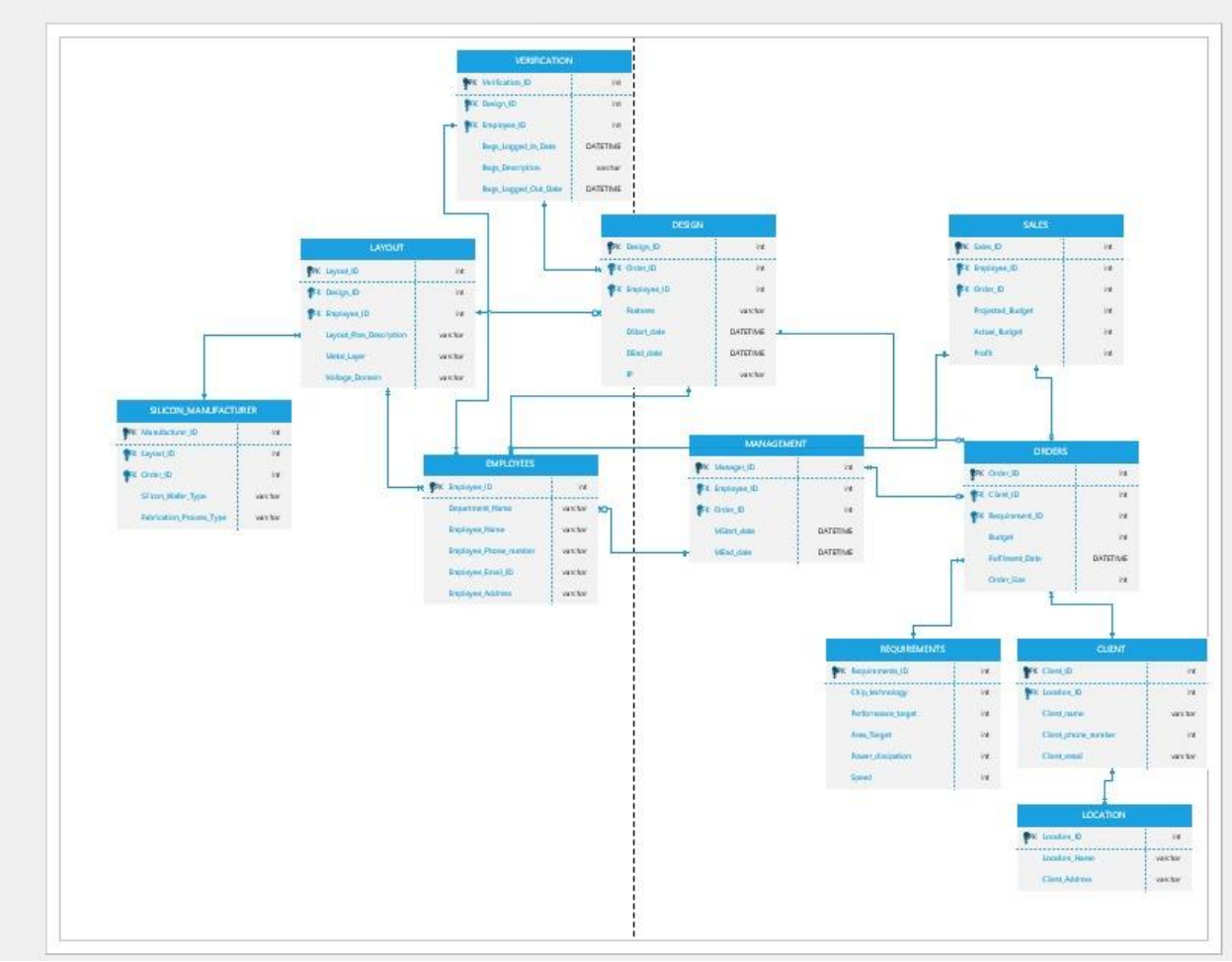


Detailed Description of the Business Rules and User Requirements:

- One order is placed by one and only one client, one client can place on or more orders.
- One client will be associated with one or more locations. Each location is associated with one client.
- One order will have one and only one requirement. Requirements will be for one or more orders.
- One order will be assigned to one and only one manager, Each manager may or maynot handle an order.
- One order will be assigned to one sales team, each sales team may or maynot handle an order.
- Each order will be assigned to one and only one design team, design teams will work on zero or more orders.
- Each Design will be verified only once, verification is done on one or more designs.
- Each verified design will have one and only layout, multiple designs can have many layouts.
- Each layout-design is manufactured by one silicon manufacturer. Each silicon manufacturer can manufacture many layout-designs.

- Each team like sales, management, design, verification ,layout have one or more employees. Each employee belongs to one and only one department team.

ERD Diagram:



Data dictionary:

Database	Attribute	Data type	Max field size	Key type	Accepts null value	Description
Client	client ID	Integer	10	Primary key	N	Unique IDs for all the clients
	Location ID	Integer	10	Foreign Key	N	Unique IDs for all the locations
	Client Name	varChar	30		N	Full name of client
	Client phone number	Integer	10		Y	Phone number of client
	Client email	varChar	15		N	Email of client
Locations	Location ID	integer	10	Primary key	N	Unique IDs for all locations
	Location Name	varChar	30		Y	Locations where client is established
	Client Address	varChar	255		N	Location address where client is established
Order	Order ID	integer	10	Primary key	N	Unique IDs for all the orders
	Client ID	integer	10	Foreign key	N	Unique IDs for all the clients
	Requirement ID	integer	10	Foreign key	N	Unique IDs for all requirements imposed by customers
	Budget	integer	10		N	Budget for the chip
	Fullfillment date	DATETIME	15		Y	Due date for the chip completion
	Order size	integer	10		Y	Number of chips required
Requirements	Requirements ID	integer	10	Primary key	N	Unique IDs for all requirements imposed by customers
	Chip technology	integer	5		Y	Chip technology is a number that specifies size of techn
	Performance target	integer	3		Y	Performance target is set per 100% to convey efficiency
	Area target	integer	5		N	Area target is a number in nn/mm size of chip
	Power dissipation	Integer	5		Y	Power dissipation is an integer typically in milli watts
	Speed	Integer	5		Y	Describes the performance rate of the chip typically in G
Employees	Employee ID	Integer	5	Primary key	N	Unique ID to identify all members of company
	Department name	varChar	30		N	department ID to know which team he belongs
	Employee name	varChar	30		N	Name of employee
	Employee phone number	varChar	10		Y	Phone number of employee
	Employee email ID	varChar	15		Y	Email ID of employee
	Employee Address	varChar	255		Y	Address of employee
Management	Manager_ID	Integer	10	Primary key	N	Unique ID for a manager
	Employee ID	Integer	10	Foreign Key	N	Unique ID for a employee
	Order_ID	Integer	10	Foreign Key	N	Unique ID for a order
	MStart date	DATETIME	15		Y	Start date of the project
	MEnd date	DATETIME	15		Y	End date of the project
Design	Design_ID	Integer	10	Primary key	N	Unqiue ID for a design
	Order_ID	Integer	10	Foreign Key	N	Unique ID for a order
	Employee ID	Integer	10	Foreign Key	N	Unique ID for a employee working on design
	Features	varChar	255		Y	Description of design features
	DStart date	DATETIME	15		Y	Start date of design
	DEnd date	DATETIME	15		Y	End date of design
	IP	varChar	10		Y	IP status of the design
Verification	Verification_ID	Integer	10	Primary key	N	Unique ID for a verification
	Employee ID	Integer	10	Foreign Key	N	Unique ID for an employee working on verification
	Design_ID	Integer	10	Foreign Key	N	Unique IDs for the designs
	Bugs logged-in-date	DATETIME	15		Y	Register to track the bugs that are found in design
	Bugs description	varChar	255		Y	Description of bugs that are identified
	Bugs logged-out-date	DATETIME	15		Y	Register to track closing dates of bugs that are found in
Layout	Layout_ID	Integer	10	Primary key	N	Unique IDs for the layouts
	Employee ID	Integer	10	Foreign Key	N	Unique ID of employees working on identifying bugs
	Design ID	Integer	10	Foreign Key	N	Unique ID for layout team to track the design they are l
	Layout plan description	varChar	255		Y	Description of chip planning like shape of chip etc.
	Metal layer	varChar	4		N	Metal layer describes type of mental used in chip layout
	Voltage domain	varChar	4		Y	Domain simulates type of power domain used for layou
Silicon manufacturer	Manufacturer ID	Integer	10	Primary Key	N	Unique ID for a manufacturing company
	Layout ID	Integer	10	Foreign Key	N	Unique ID for a layout
	Order ID	Integer	10	Foreign Key	N	Unique ID for an order
	Silicon wafer type	varChar	255		N	Description of the material type used for silicon manufa
	Fabrication process type	varChar	255		Y	Description of methodology type
Sales	Sales ID	Integer	10	Primary Key	N	Unique IDs for the sales
	Employee ID	Integer	10	Foreign Key	N	Unique IDs for all the employees
	Order ID	Integer	10	Foreign Key	N	Unique IDs for all the orders
	Projected Budget	Integer	10		N	Expected Budget for all the orders
	Actual Budget	Integer	10		N	Actual Budget for all the orders
	Profit	Integer	10		N	The overall profit for each order