wafer level chip-scale package; 49 bumps; $3.29 \times 3.29 \times 0.54$ mm (backside coating included)

8 February 2016

Package information

1. Package summary

Terminal position code B (bottom)

Package type descriptive code WLCSP

Package type industry code WLCSP

Package style descriptive codeUC (uncased chip)Package style suffix codeNA (not applicable)

Package body material type P (plastic)

Mounting method type S (surface mount)

Issue date 3-11-2014

Table 1. Package summary

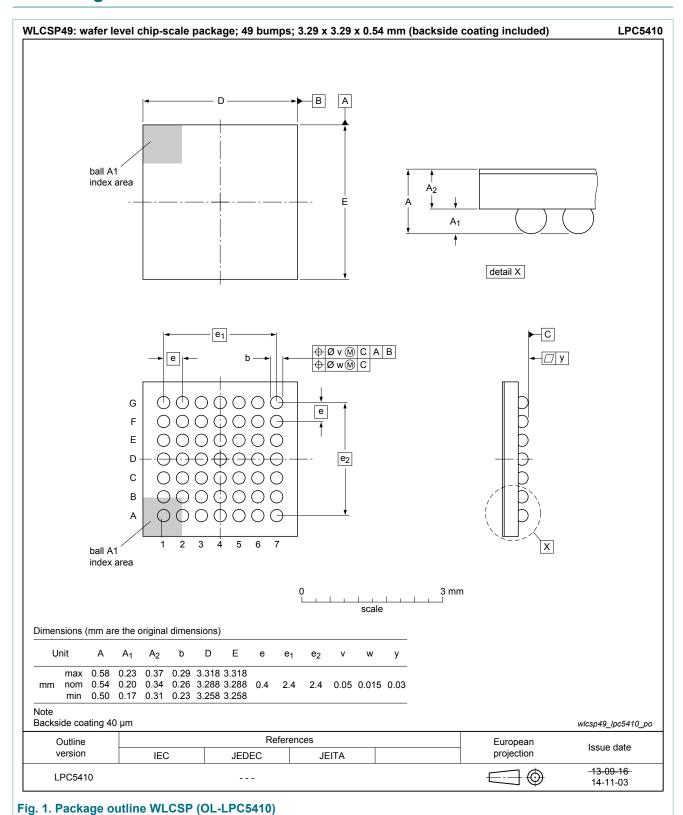
| Symbol | Parameter | Min | Тур | Nom | Max | Unit |
|--------|--------------------------------|-------|-----|-------|-------|------|
| D | package length | 3.258 | - | 3.288 | 3.318 | mm |
| E | package width | 3.258 | - | 3.288 | 3.318 | mm |
| Α | seated height | 0.5 | - | 0.54 | 0.58 | mm |
| е | nominal pitch | - | - | 0.4 | - | mm |
| n_2 | actual quantity of termination | - | - | 49 | - | |



NXP Semiconductors OL-LPC5410

wafer level chip-scale package; 49 bumps; 3.29 x 3.29 x 0.54 mm (backside coating included)

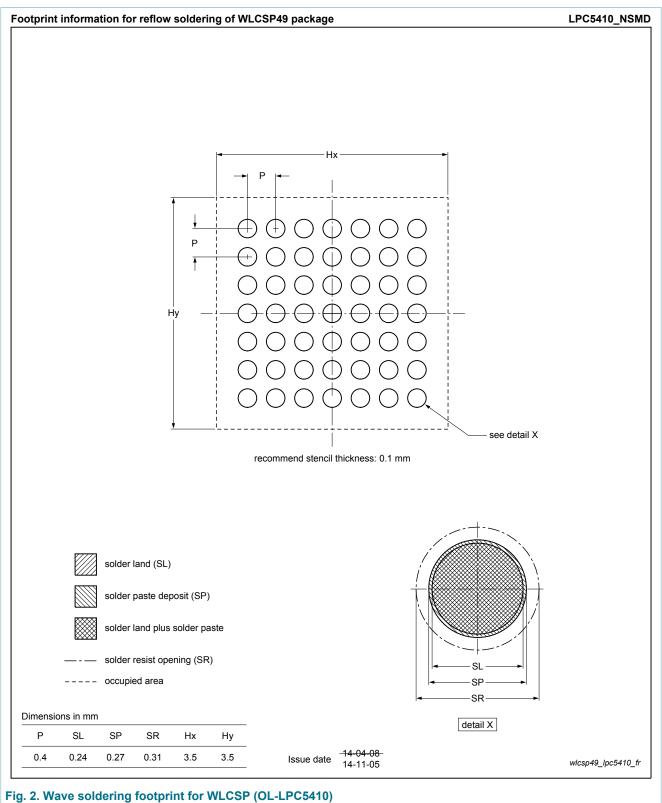
2. Package outline



NXP Semiconductors OL-LPC5410

> wafer level chip-scale package; 49 bumps; 3.29 x 3.29 x 0.54 mm (backside coating included)

3. Soldering



NXP Semiconductors OL-LPC5410

wafer level chip-scale package; 49 bumps; 3.29 x 3.29 x 0.54 mm (backside coating included)

4. Legal information

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

NXP Semiconductors OL-LPC5410

wafer level chip-scale package; 49 bumps; 3.29 x 3.29 x 0.54 mm (backside coating included)

5. Contents

| 1. | Package summary | . 1 |
|----|-------------------|-----|
| 2. | Package outline | . 2 |
| 3. | Soldering | . 3 |
| 4. | Legal information | . 4 |

For more information, please visit: http://www.nxp.com For sales office addresses, please send an email to: salesaddresses@nxp.com Date of release: 8 February 2016

[©] NXP Semiconductors N.V. 2016. All rights reserved