s_gate_pulses_1ph_1 (subcircuit)

Attributes

```
inputs: x1 x2
outputs: y1 y2
e_left_nodes:
e_right_nodes:
e_top_nodes:
e_bottom_nodes:
parameters:
  delt_min: 1e-6
  delt_nrml: 10e-6
  t_delay: 1e-3
  y_high: 1
```

Description

s_gate_pulses_1ph_1 is designed to generate signals required to drive a pair of switches in a "non-overlapping" manner. It compares inputs x1 and x2 and produces outputs y1 and y2. The value of y1 is y_high if x1 > x2; else, it is zero. For y2, the opposite is true; viz., y2 is equal to g_high if x1 < x2; else, it is zero. However, a delay is introduced between the transitions in y1 and y2 as depicted in Fig. 1.

The parameters delt_min, delt_nrml are used for controlling the simulator time steps (see documentation for cmpr_1_1).
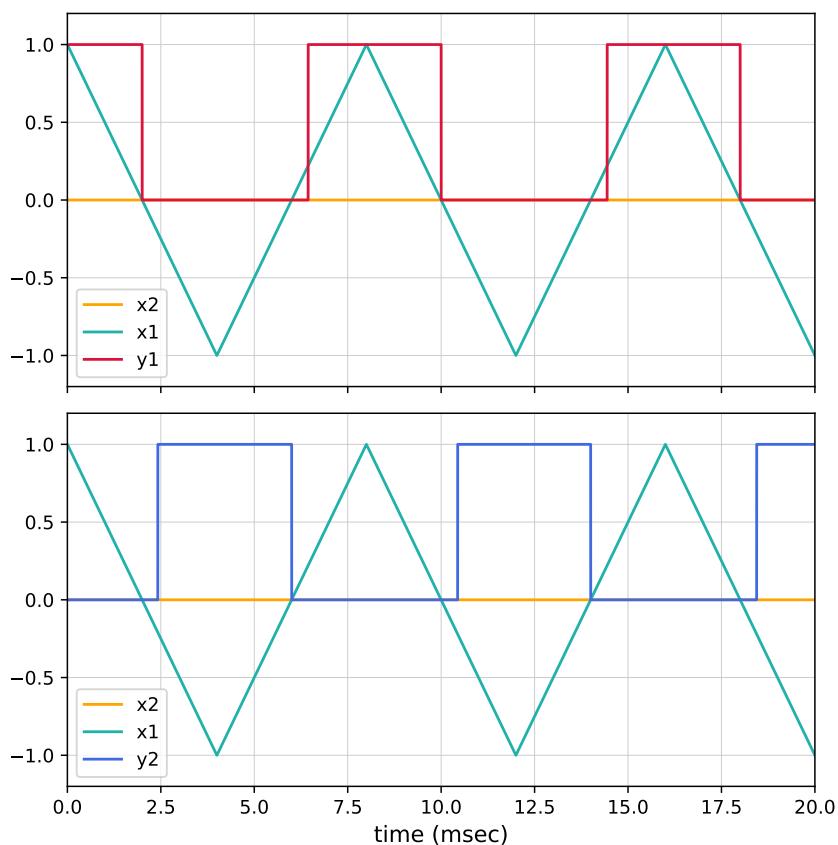

Figure 1: Sample waveforms obtained with s_gate_pulses_1ph_1. The parameter values are $\text{delt\_min} = 0.02\,\mu\text{s}$, $\text{delt\_nrml} = 0.2\,\text{ms}$, $\text{y\_high} = 1$, $\text{t\_delay} = 0.5\,\text{ms}$.