LAB REPORT- 1

CS 322 - COMPUTER PERIPHERALS AND INTERFACES

GROUP-12

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OBJECTIVE:

To identify all the peripheral devices including their name and functionality and to install the required software in a computer for the given kit(mps 85-3), run sample programs using them and also using the default keyboard give in kit.

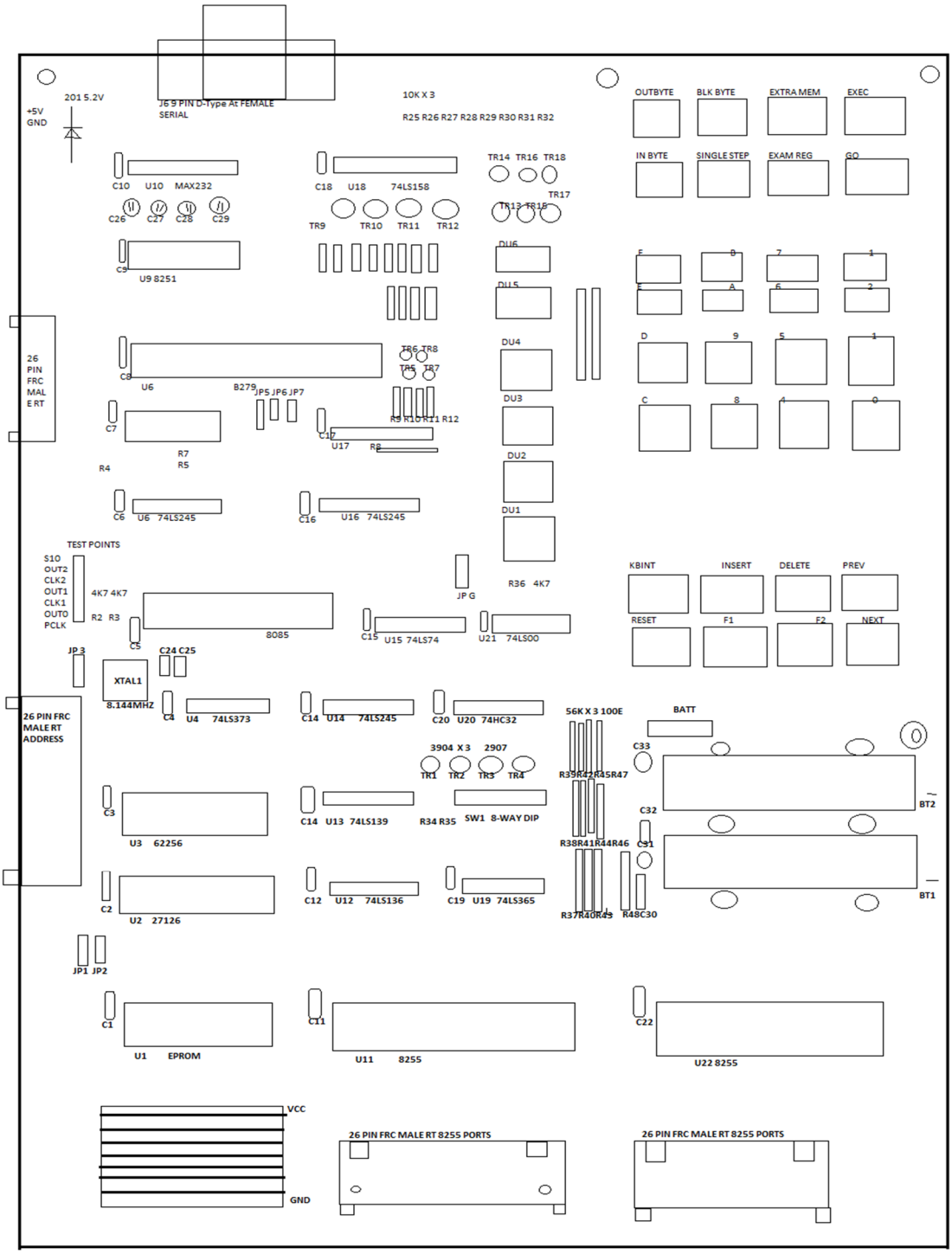
INSTALLED SOFTWARE:

The software that is installed is:

Drivers from Electro systems associates for mps 85-3.

BLOCK DIAGRAM:

MPS 85-3 BLOCK DIAGRAM



IDENTIFIED COMPONENTS AND PERIPHERALS:

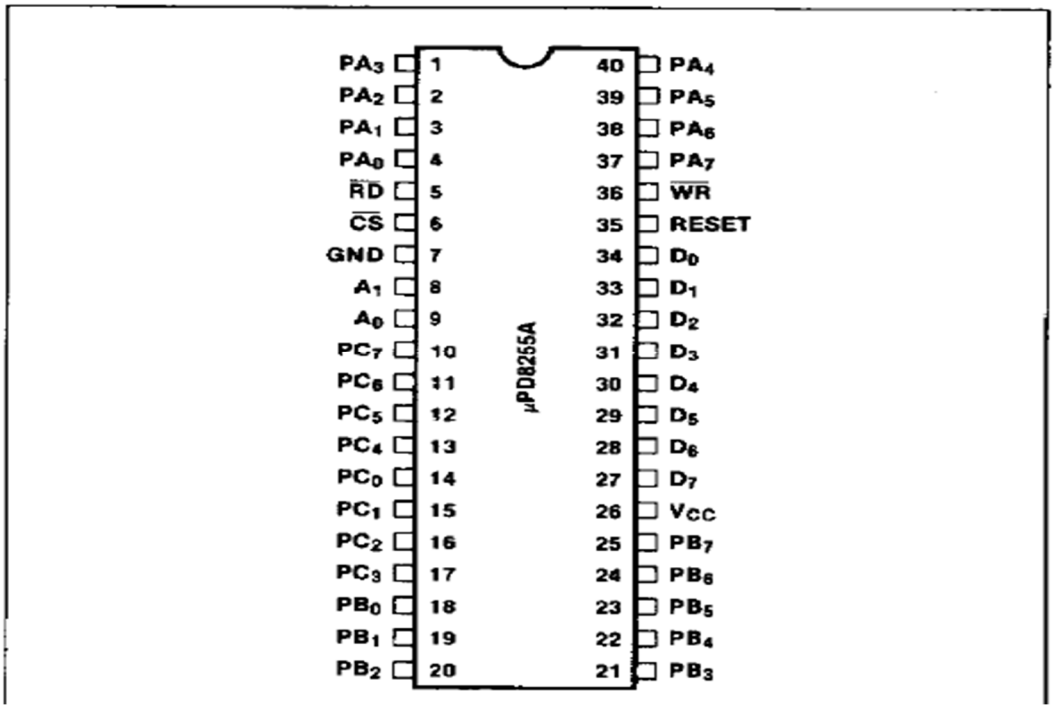
M80C85A (8-Bit CMOS Microprocessor):

The MSM80C85AH is a complete 8-bit parallel; central processor implemented in silicon gate C-MOS technology and compatible with MSM80C85A. It is designed with higher processing speed (max.5 MHz) and lower power consumption compared with MSM80C85A and power down mode is provided, thereby offering a high level of system integration.

D8255AC-5 (Programmable Peripheral Interface):

It is a general purpose programmable input/output device designed for use with 8085 microprocessors. 24 input output lines may be programmed in two groups of 12 and used in 3 modes of operation.

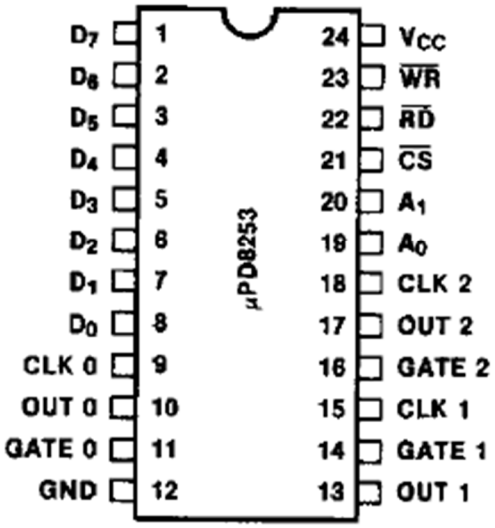
PIN CONFIGURATION:



D8253C-5 (Programmable Interval Timer):

It contains 3 independent programmable multi model 16 bit counters/timers. It is designed as a general purpose device fully compatible with 8080 family. It interfaces directly to the buses of the processor as an array of I/O ports.

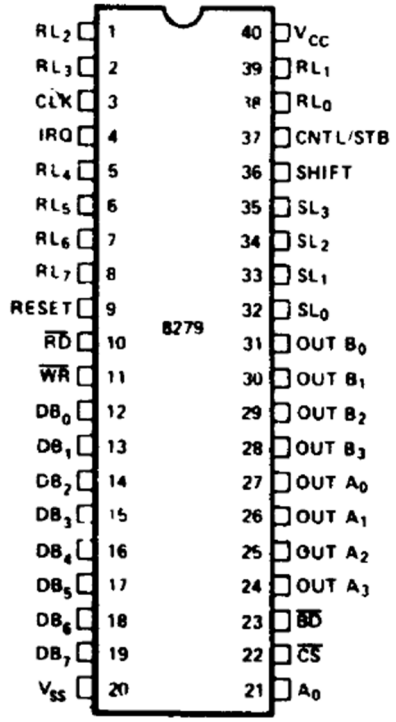
PIN CONFIGURATION**:**



KC8279P (Programmable Key Board Display Interface):

The Intel 8279 is a general purpose programmable keyboard and display I/O device interface designed for use with Intel microprocessors. The keyboard portion can provide a scanned interface to a 64 contact key matrix.

PIN CONFIGURATION:



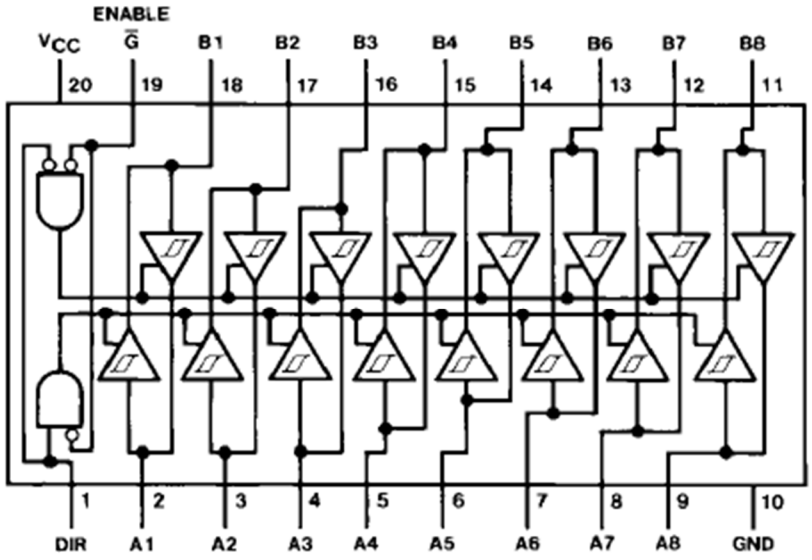
HD74HC32P:

It is Quad 2-input OR Gates. Some of its features are

1) High Speed Operation
2) High Output Current
3) Wide Operating Voltage
4) Low Input Current

DM74LS245N:

CONNECTION DIAGRAM**:**



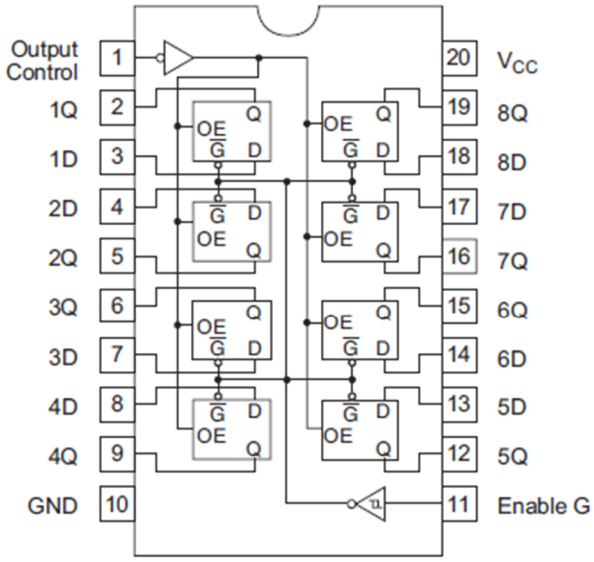
It is 3-STATE Octal Bus Transceiver. These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements. The device allows data transmission from the A Bus to the B Bus or from the B Bus to the A Bus depending upon the logic level at the direction control (DIR) input.

HD74LS373P:

The HD74LS373, 8-bit register features totem-pole three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide this register with the capacity of being connected directly to and driving the bus lines in a bus-organized system without need for interface or

pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, Bidirectional bus drivers, and working registers.

PIN CONFIGURATION**:**

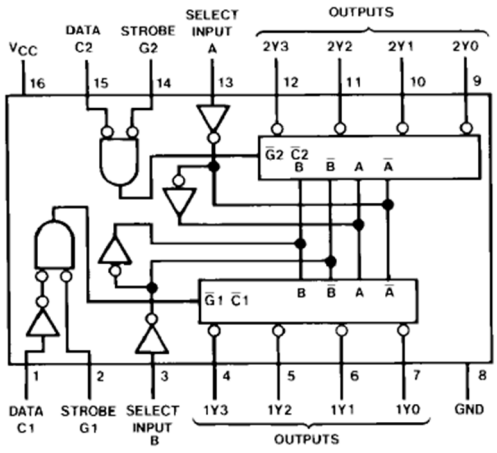


(Top view)

74LS155 (Dual 2-Line to 4-Line Decoders/De multiplexers):

These TTL circuits feature dual 1-line-to-4-line de multiplexers with individual strobes and common binary-address inputs in a single 16-pin package. When both sections are enabled by the strobes, the common address inputs sequentially select and route associated input data to the appropriate output of each section.

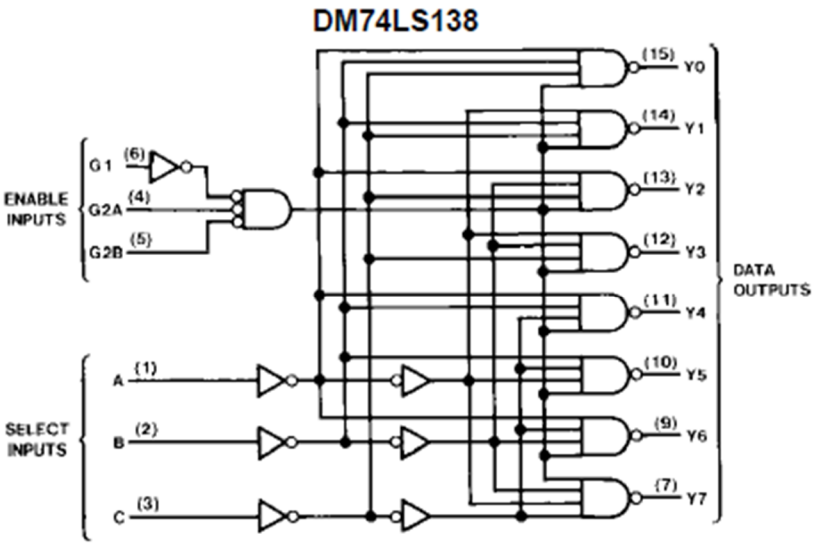
CONNECTION DIAGRAM:



DM74LS138:

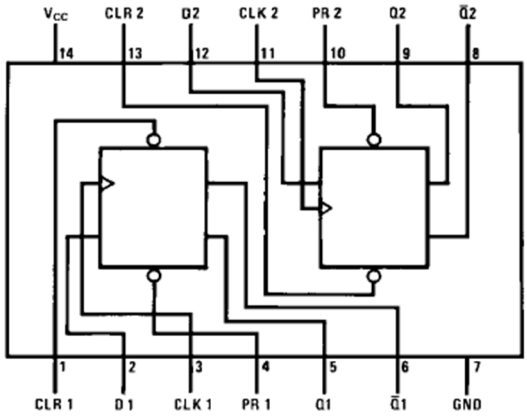
These Schottky-clamped circuits are designed to be used in high-performance memory-decoding or data-routing applications, requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding.

LOGIC DIAGRAMS:



S974ALS74N (Dual Positive-Edge-Triggered D Flip-Flops with Preset, Clear and Complementary Outputs):

This device contains two independent positive-edge-triggered D flip-flops with complementary outputs. The information on the D input is accepted by the flip-flops on the positive going edge

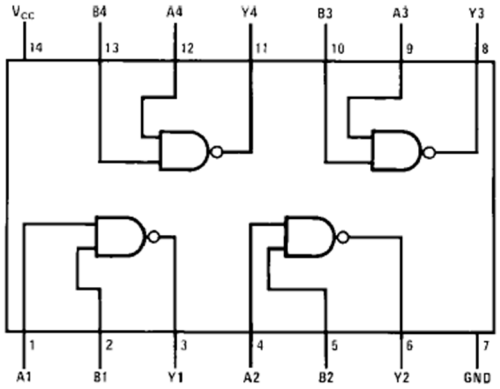


of the clock pulse.

D974LS00N (Quad 2-Input NAND Gate):

This device contains four independent gates each of which performs the logic NAND function.

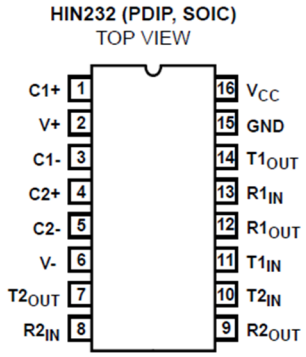
CONNECTION DIAGRAM:



HIN232CP:

The HIN230-HIN241 family of RS-232 transmitters/receivers interface circuits meets all EIA RS-232E and V.28 specifications, and is particularly suited for those applications where ±12V is not available. They require a single +5V power supply (except HIN231 and HIN239) and feature onboard charge pump voltage converters which generate +10V and -10V supplies from the 5V supply.

PIN CONFIGURATION:



CY62256L-70PC (Static Ram):

The CY62256 is a high-performance CMOS static RAM organized as 32K words by 8 bits. Easy memory expansion is provided by an active LOW chip enable (CE) and active LOW output

enable (OE) and three-state drivers. This device has an automatic power-down feature, reducing the power consumption by 99.9% when deselected.

SAMPLE PROGRAMS:

Some sample programs such as adding 2 numbers, subtracting 2 numbers, were done using kit's keyboard.

For example:

```
cpu "8085.tbl"

hof "int8"

org 9000h

mvi a,50h

mvi b,40h

add b

RST 5
```

SOFTWARE USED:

The following applications in the software were put to use:

C16 – for converting the assemble language program to hex code which is understandable by 8085 microprocessor.

Xt85 – for loading HEX code to the kit.