

Quartus Prime Lite Edition - /home/gshimabuko/Documents/Estudo/Coursera/Expanded\_Nios\_Training/Traffic\_Lights/DE10\_LITE/traffic\_lights - traffic\_lights

FileEditViewProjectAssignmentsProcessingToolsWindowHelp

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traffic\_lights

Tasks

Compilation

Task

✔▶▶Fitter (Place & Route)

✔▶▶Assembler (Generate programmm

✔▶▶Timing Analysis

✔▶▶EDA Netlist Writer

Edit Settings

Program Device (Open Programmer

Compilation Report - traffic\_lights

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Flow Summary

Flow Settings

Flow Non-Default Globi

Flow Elapsed Time

Flow OS Summary

Flow Log

Analysis & Synthesis

Fitter

Assembler

Flow Summary

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Flow Status

Quartus Prime Version

Revision Name

Top-level Entity Name

Family

Device

Timing Models

Total logic elements

Successful - Mon May 11 17:38:23 2020

18.1.0 Build 625 09/12/2018 SJ Lite Edition

traffic\_lights

toplevel

MAX 10

10M50DAF484C7G

Final

2,195 / 49,760 ( 4 % )

TasksProject Navigator

All

5

17

<<Filter>>

Find...

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Messages

TypeIDMessage

332102

Design is not fully constrained for setup requirements

332102

Design is not fully constrained for hold requirements

▶332102

Quartus Prime Timing Analyzer was successful. 0 errors, 16 warnings

▶332102

Running Quartus Prime EDA Netlist Writer

▶332102

Command: quartus\_eda --read\_settings\_files=off --write\_settings\_files=off traffic\_lights -c traffic\_lights

18236

Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM\_PARALLEL\_PROCESSORS in your QS

10905

Generated the EDA functional simulation netlist because it is the only supported netlist type for this device.

204019

Generated file traffic\_lights.vo in folder "/home/gshimabuko/Documents/Estudo/Coursera/Expanded\_Nios\_Training/Traffic\_Lights/DE10\_LITE/simulation/modelsim

▶204019

Quartus Prime EDA Netlist Writer was successful. 0 errors, 2 warnings

293000

Quartus Prime Full Compilation was successful. 0 errors, 75 warnings

SystemProcessing (328)

Tcl ConsoleMessages

100%00:01:24