8MMINI-BB

(i.MX8M Mini Customer Base Board)

Schematics DevBoard

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1. Interrupted lines coded with the same letter or letter combinations are electrically connected.

2. Device type number is for reference only. The number varies with the manufacturer.

3. Special signal usage:
   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

4. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

Preliminary - Subject to Change without Notice!

This board was designed for maximum flexibility in software development and demonstrates multiple functions possible with i.MX processors. Although best design practices have been applied, some areas may not be suitable for a mass-production design.

Revision History

Rev. Code	Date	By		Description
A	2018-03-16	Javen	1	initial version
B	2018-05-09	Javen	1	Add D308, D309, D310, U312, C337, R355, C338, D312, D313 to enable always 'ON' LDO
			2	Add U311, R356, R357, R358, R359, R343, D311, C341 to get accurate VBUS2 threshold
			3	Change U303, U306 part number to PTN5110NHQ to reduce the EN_SNK output debounce time
			4	Remove backup resistor R347, R348 and add C342-C344 for VBUS detect circuit
			5	Change U702 to NXP part:NX3P191, add TP701, TP704
			6	Install R502 to make the ENET IO voltage default to 1.8V
			7	Add R349, R350, R353, R354 for Type-C circuit debug
			8	Change C113 to 0.22uF, Add C161 to increase the time delay of PTN5110 VBUS/VDD
			9	Remove R712, D701, Q704, R716, R715 for PWM_LED.
			10	Add R216, R217, R218, R219 for SD2_nCD alternative design
			11	Add Q1001-Q1003, R1029-R1033, C1004 to control the audio board power sequence.
			12	Update bootcfg pull up resistors R1101/R1103/R1105/R1107/R1109/R1111/R1113/R1115/R1117/ R1119/R1121/R1123/R1125/R1127/R1129/R1131/R1133/R1135 to 4.7K OHM
			13	Add R1034 for power backup
C	2018-09-10	Javen	1	Update the Block Diagram and Power Tree;
			2	Change C301,C321 from 10uF to 4.7uF;
			3	DNP R315, R316;
			4	Add R632,DNP R626, D603 for PCIe L1SS support
			5	Add R1137-R1140, Change SW1101, SW1102 for BOOT_MODE2/3
			6	Update J201 PIN56 from GND to TEST_MODE net
			7	Change R101 from 1.5M OHM to 1.4M OHM to support VBUS < 5V case
			8	DNP R614,R615, Install R610,R611,R616,R617
C1	2018-11-29	Javen	1	Update L401,L501,L503,L601,L602,L901 to BLM18PG121SN1
			2	Change U702 to ADP191ACBZ-R7, U701 to IRM-V538M3/TR1 due to EOL
C2	2019-2-11	Javen	1	Update the Min/Typ/Max operating range for I.MX8M Mini power supplies;
			2	Add note for all IOs that internal pull up/down is not supported in 3.3V mode;

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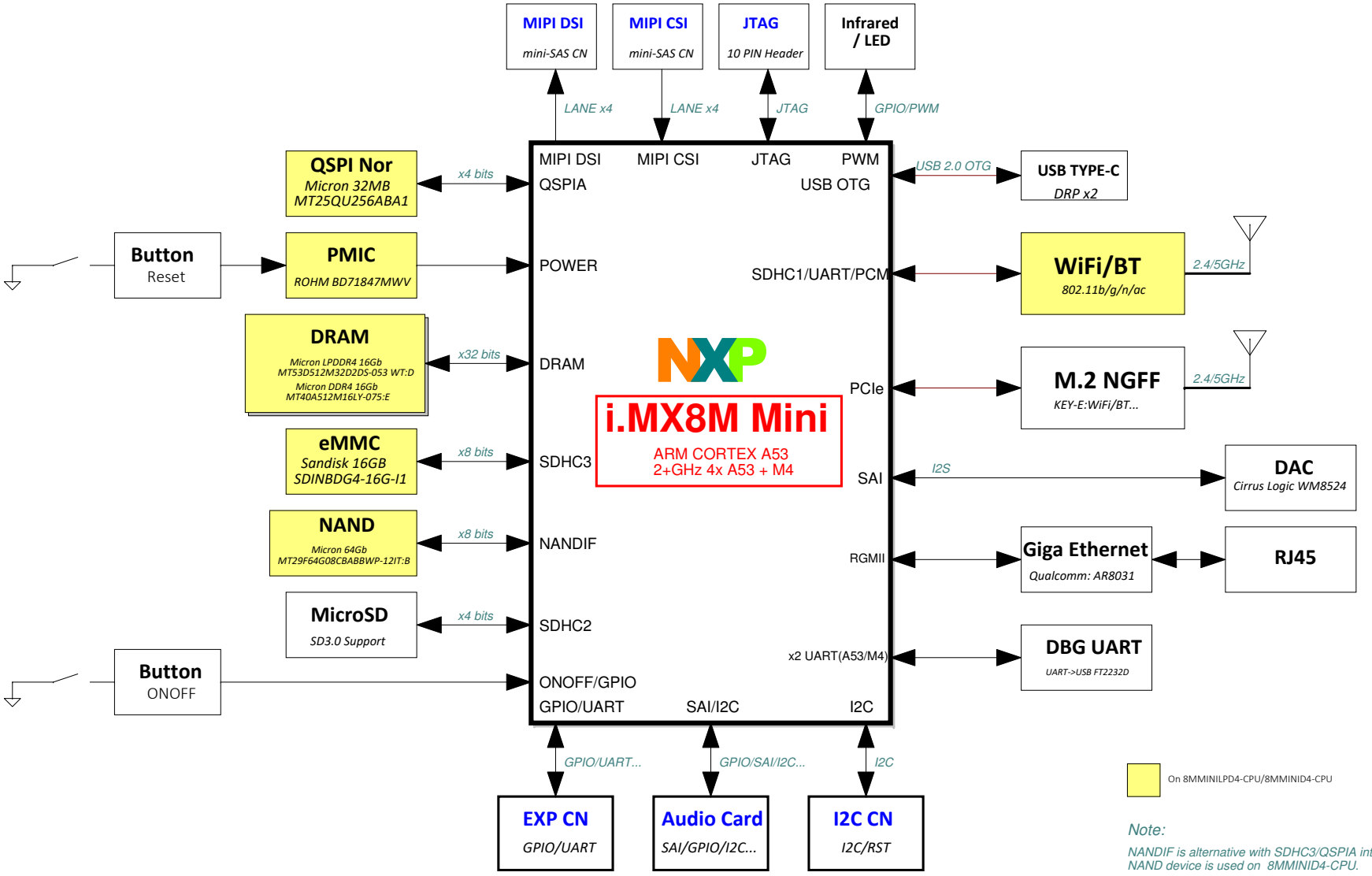
8MMINI-EVK

Block Diagram

8MMINILPD4-EVK	31409
├ 8MMINILPD4-CPU	31399
└ 8MMINI-BB	31407

8MMINID4-EVK	35105
├ 8MMINID4-CPU	35104
└ 8MMINI-BB	31407



On 8MMINILPD4-CPU/8MMINID4-CPU

Note:

NANDIF is alternative with SDHC3/QSPIA interface, NAND device is used on 8MMINID4-CPU.

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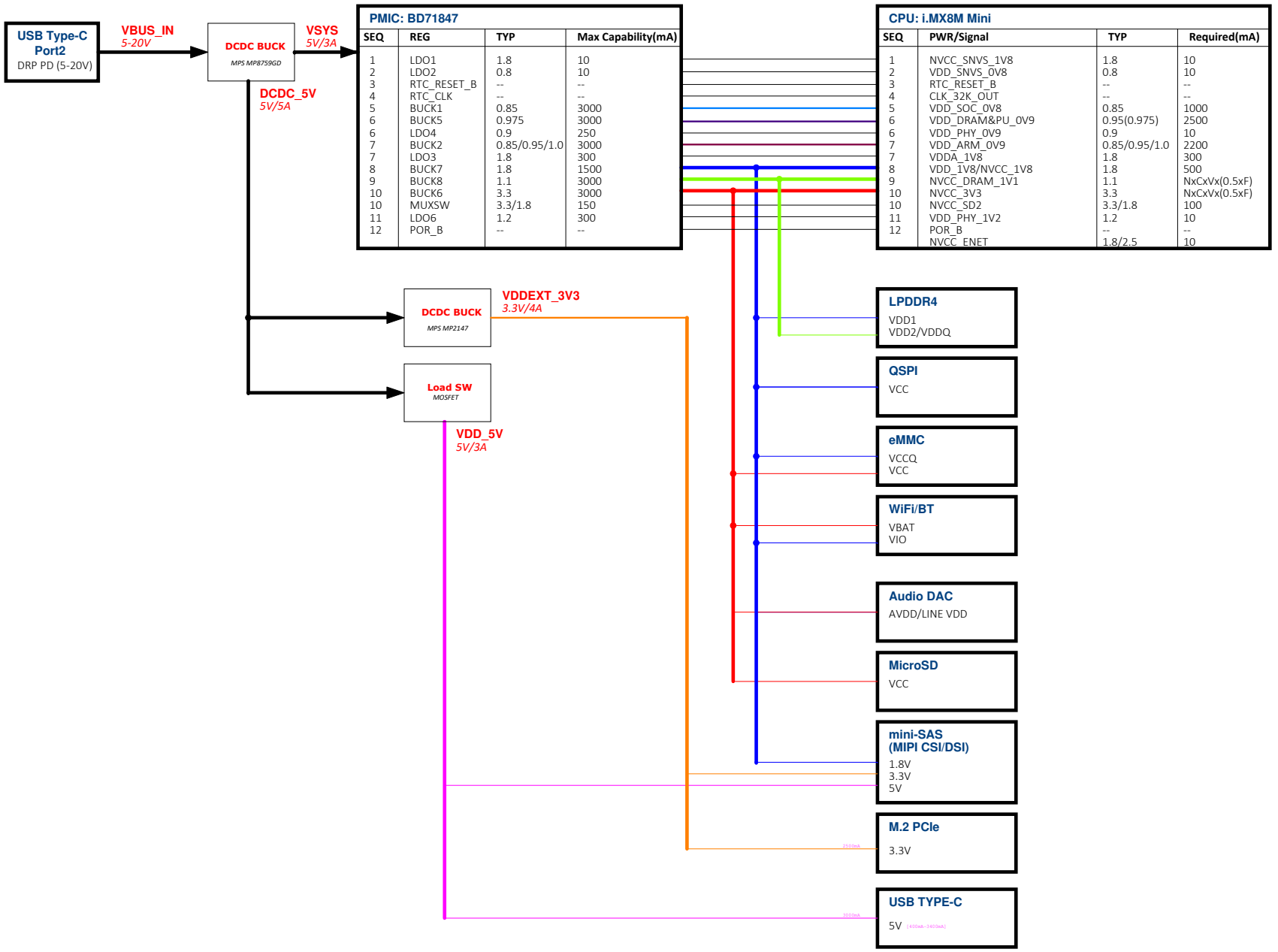
8MMINILPD4-EVK PWR TREE



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Approved: <Approver>	Size: Custom / Document Number: SCH-31407 PDF: SPF-31407	Rev: C2
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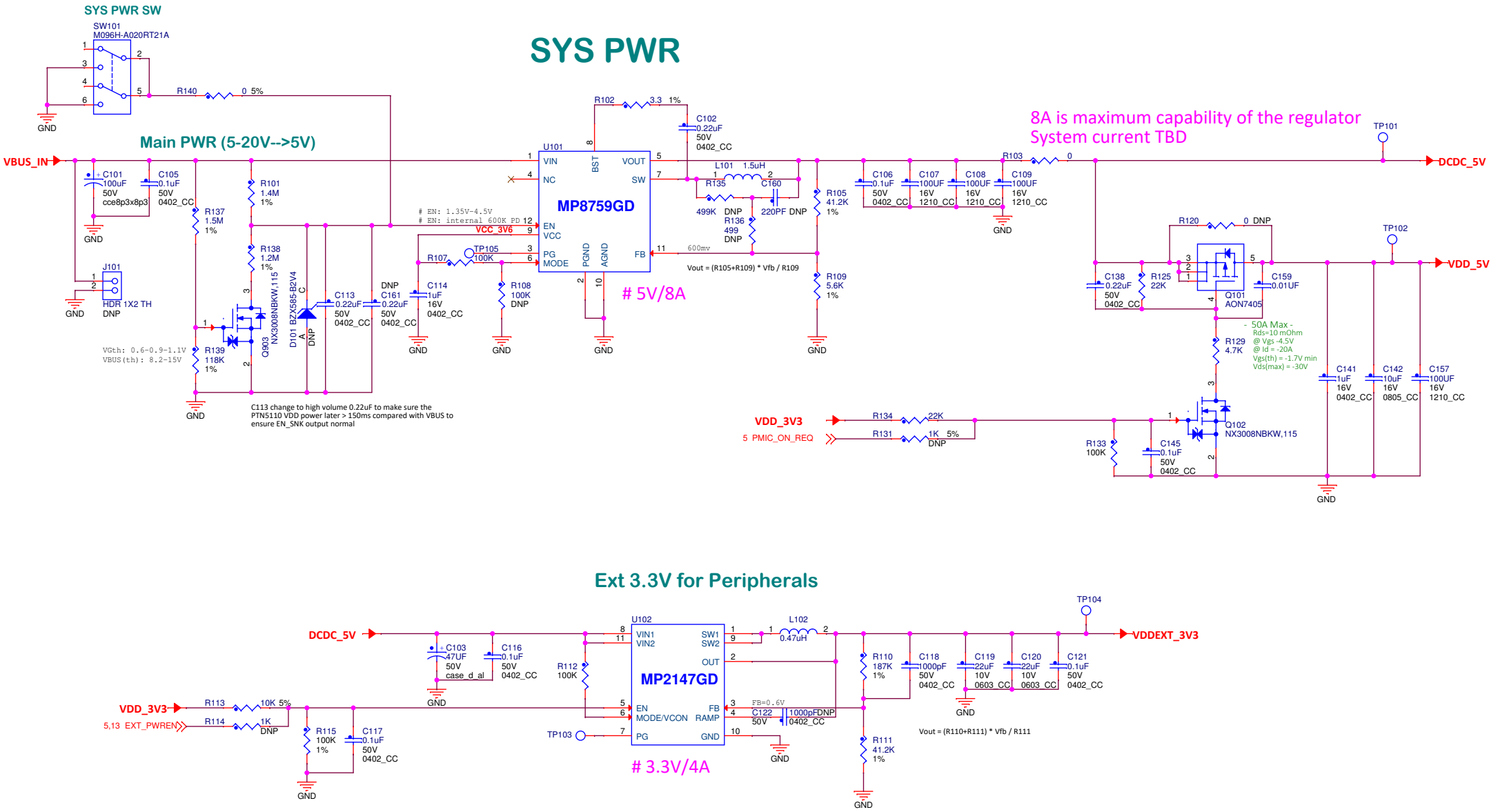
SYS PWR



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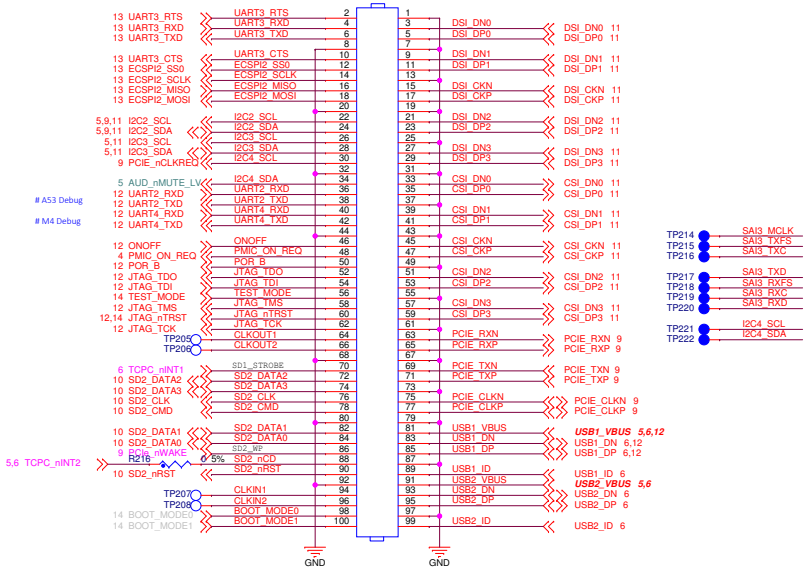
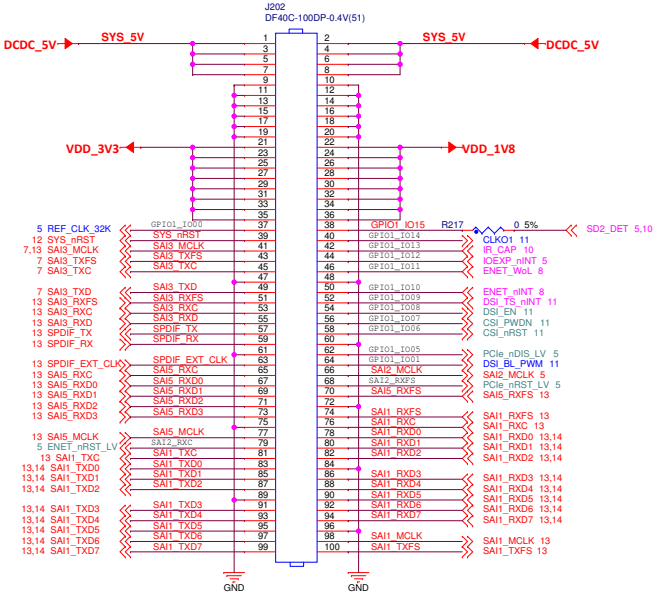
IO connector

Caution:
IO internal pull up/down is not supported in 3.3V mode, must disable the internal pull up/down via software and use external pull up/down resistors instead.
All IO pin groups are impacted except for XTAL, DDR, PCI, USB and MIPI PHY IO's.
See Errata e50080 for detailed information.

B2B Receptacle



B2B Header



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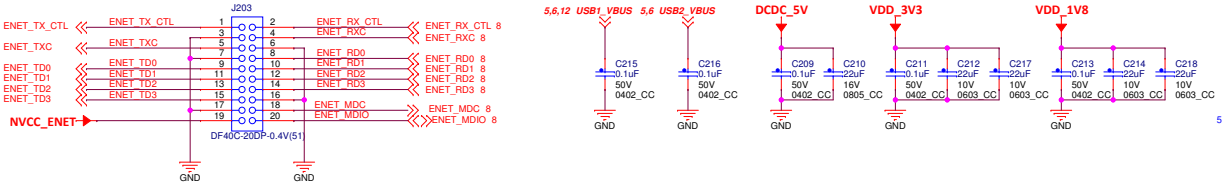
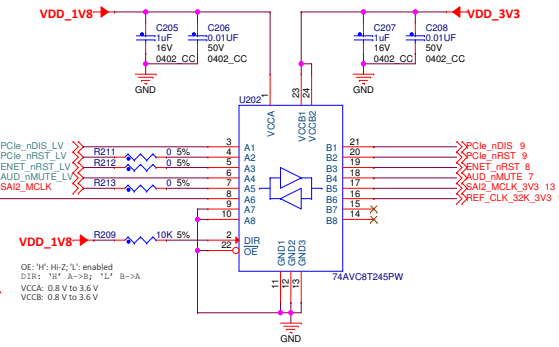
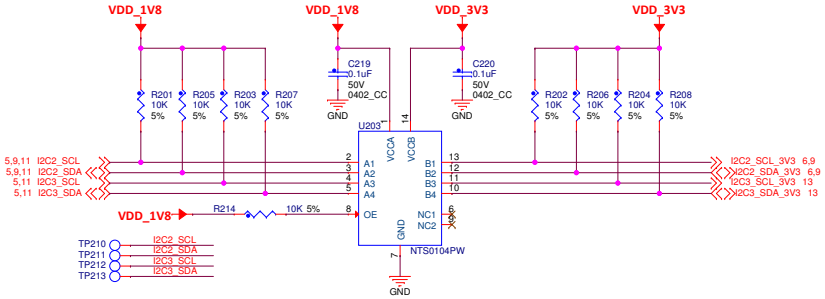
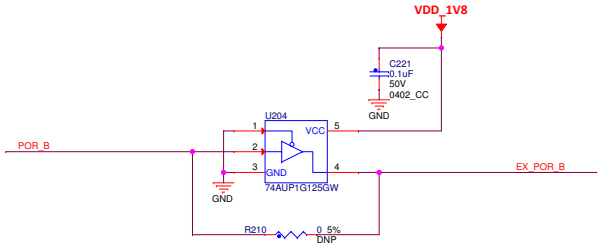


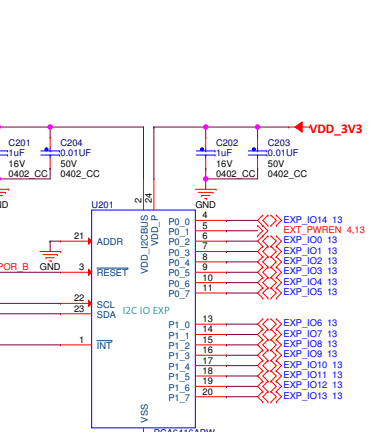


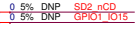
I2C2/3 Level shifter



POR_B Buffer







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USB1

USB1 IS NOT the power supply!

Always ON LDO

USB TYPE-C

5-20V

De-bounce | PWR SW OFF | PWR SW ON | Reboot

USB2

USB2 is the primary supply!

USB2 HOT SWAPPING NOT Supported !!!

USB TYPE-C

5-20V

True Table:

VBUS2_TH	EN_SNK2	EN_SNK1	3483_EN_SNK1
H	H	X	L
H	L	H	H
H	L	L	L
L	X	H	H
L	X	L	L

Short B2/C2/C1 for non-HDI routing

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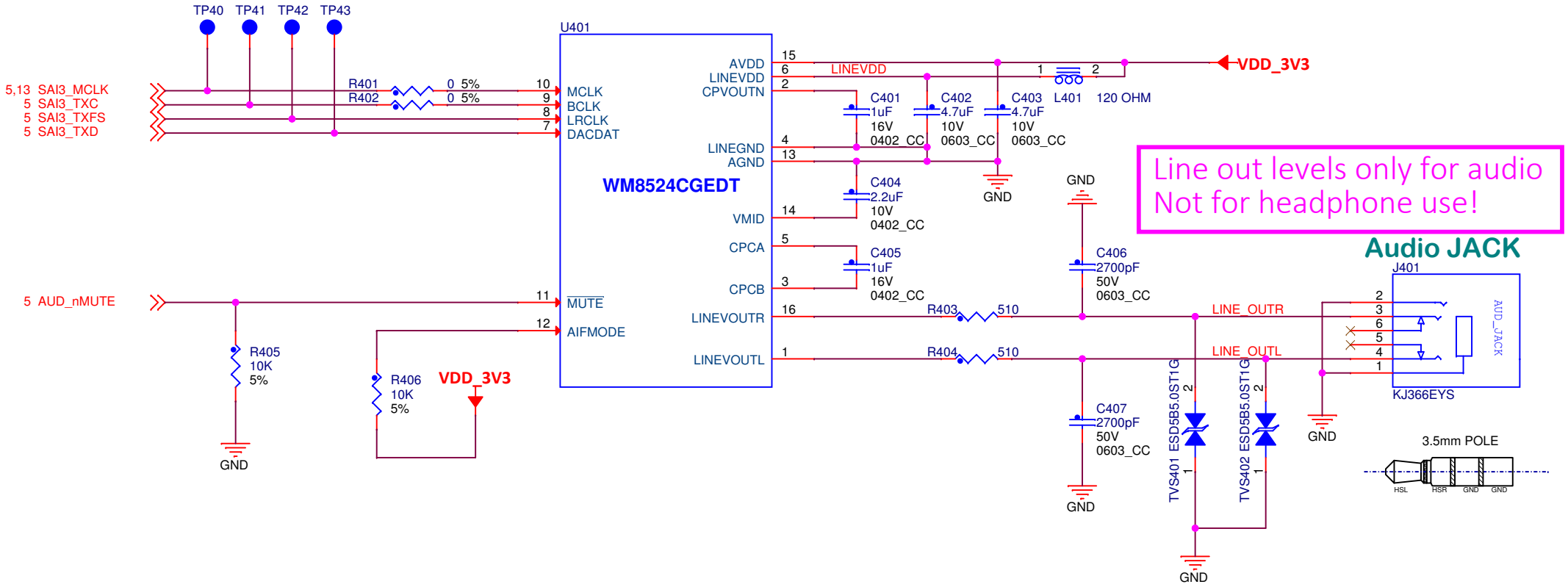
All IO pin groups are impacted except for XTAL, DDR, PCI, USB and MIPI PHY IO's.
See Errata e50080 for detailed information.

Audio DAC

24-bit 192kHz Stereo DAC 2Vrms Line Out



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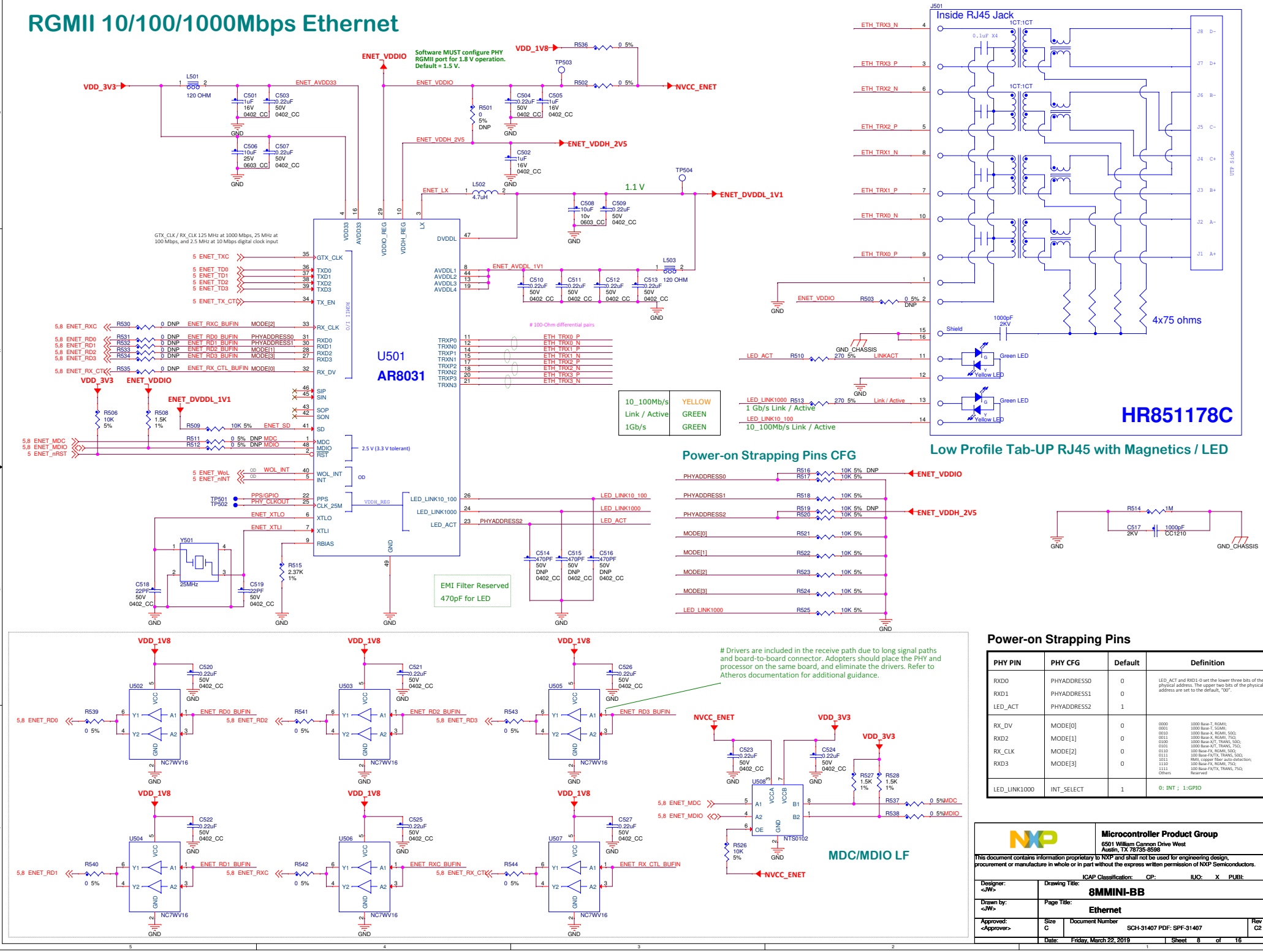
RGMII 10/100/1000Mbps Ethernet



Power-on Strapping Pins

PHY PIN	PHY CFG	Default	Definition
RXD0	PHYADDRESS0	0	LED_ACT and RXD1-0 set the lower three bits of the physical address. The upper two bits of the physical address are set to the default, "00".
RXD1	PHYADDRESS1	0	
LED_ACT	PHYADDRESS2	1	
RX_DV	MODE[0]	0	0000 1000 Base-T, RGMII; 0001 1000 Base-T, SGMII; 0010 1000 Base-X, RGMII, 50Ω; 0011 1000 Base-X, RGMII, 75Ω; 0100 1000 Base-X/T, TRANS, 50Ω; 0101 1000 Base-X/T, TRANS, 75Ω; 0110 100 Base-FX, RGMII, 50Ω; 0111 100 Base-FX/TX, TRANS, 50Ω; 1011 RMII, copper fiber auto-detection; 1110 100 Base-FX, RGMII, 75Ω; 1111 Others Reserved
RXD2	MODE[1]	0	
RX_CLK	MODE[2]	0	
RXD3	MODE[3]	0	
LED_LINK1000	INT_SELECT	1	0: INT ; 1:GPIO

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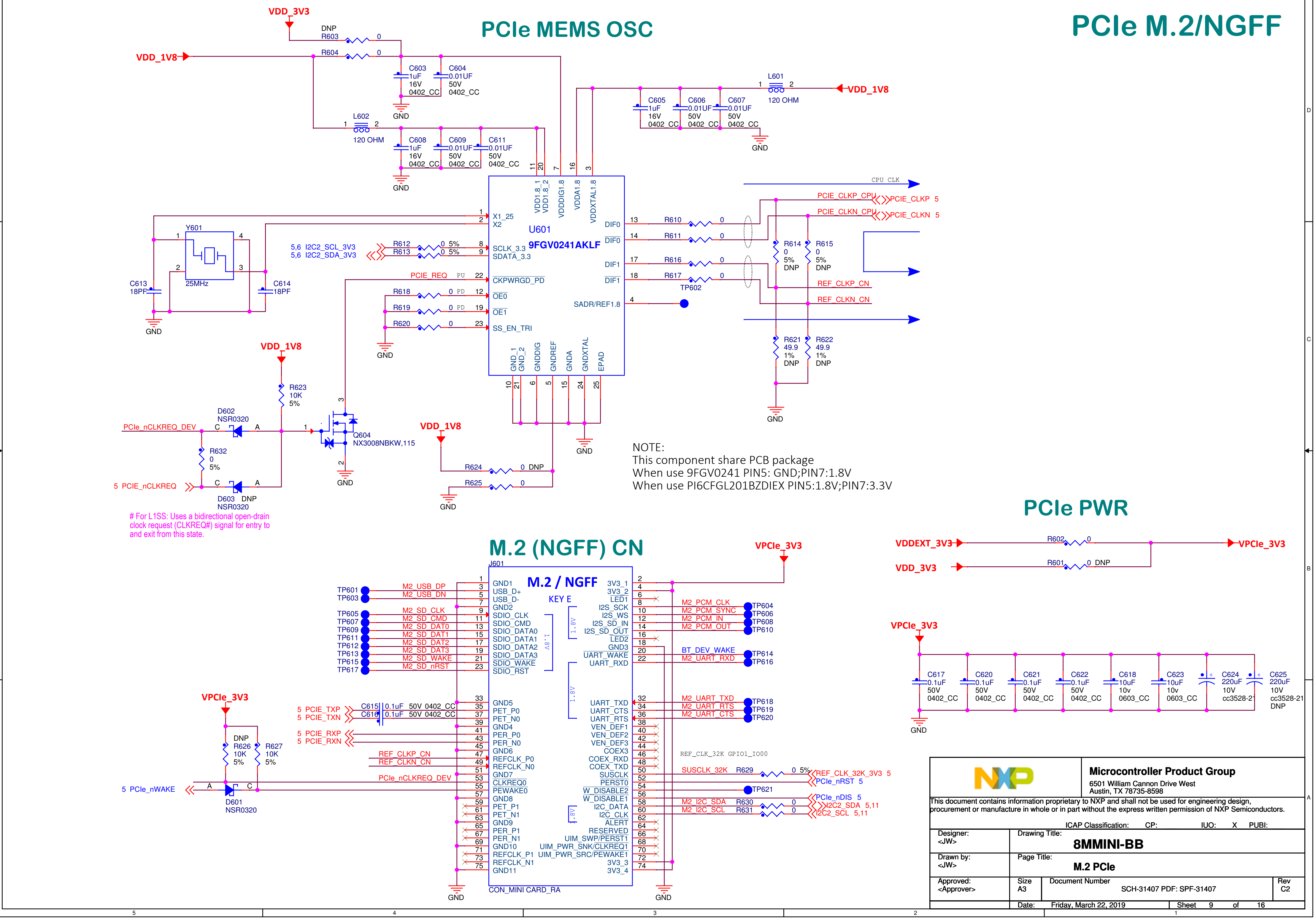
PCIe M.2/NGFF



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MicroSD/Infrared/LED

Caution:
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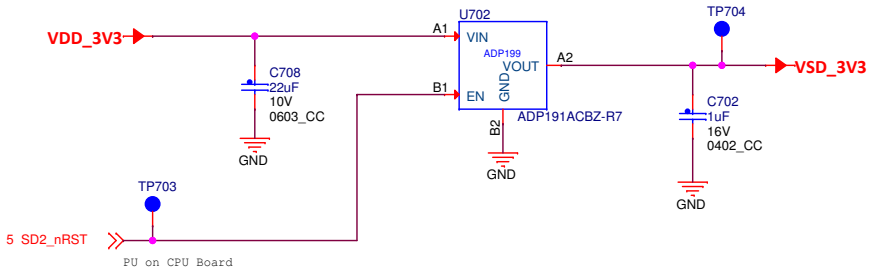
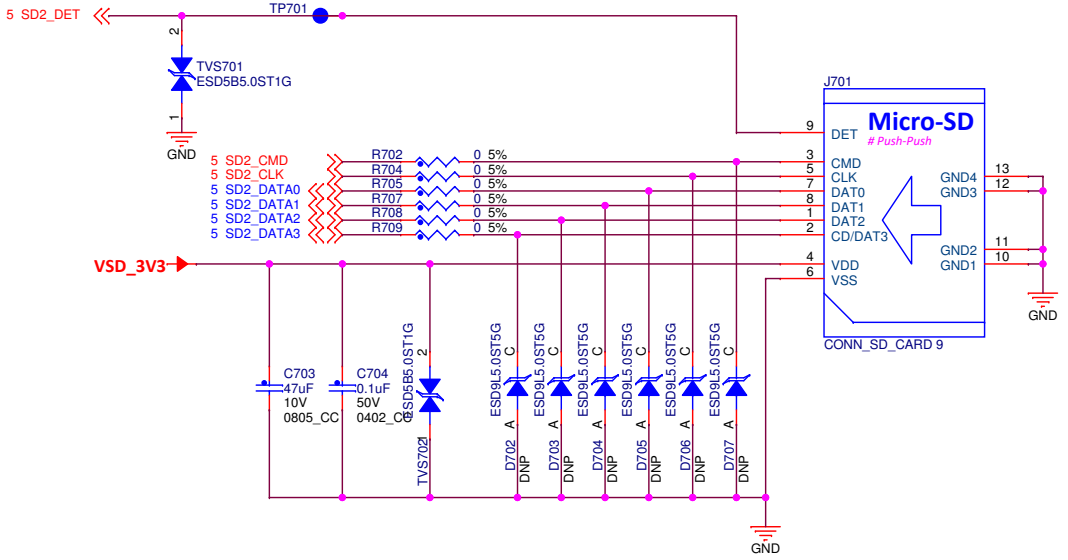
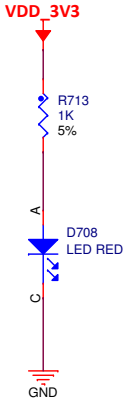
All IO pin groups are impacted except for XTAL, DDR, PCI, USB and MIPI PHY IO's.
See Errata e50080 for detailed information.

SD3.0 PWR

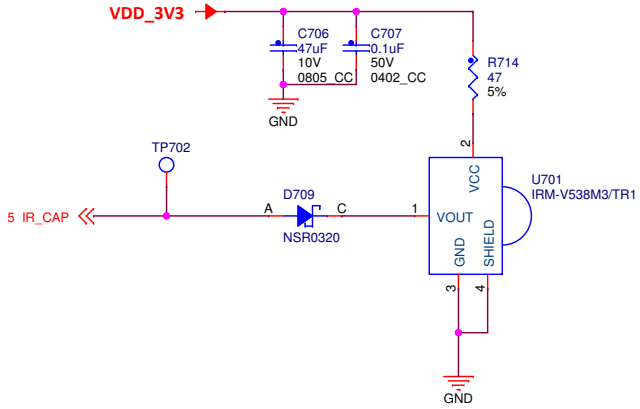




STATUS/PWR LED



Inferad Remote Control



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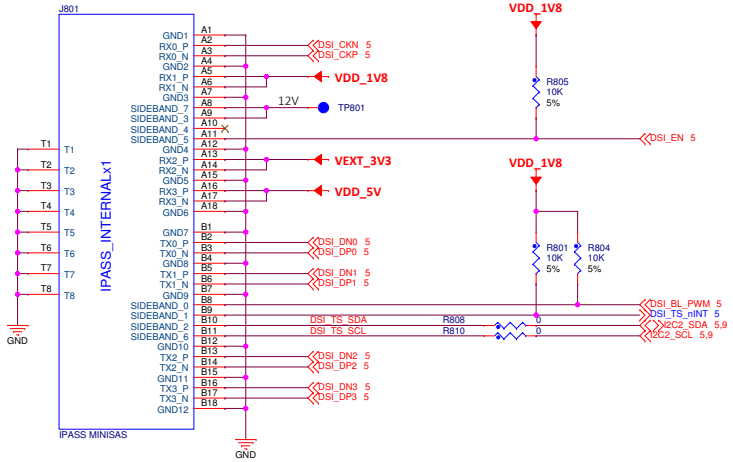
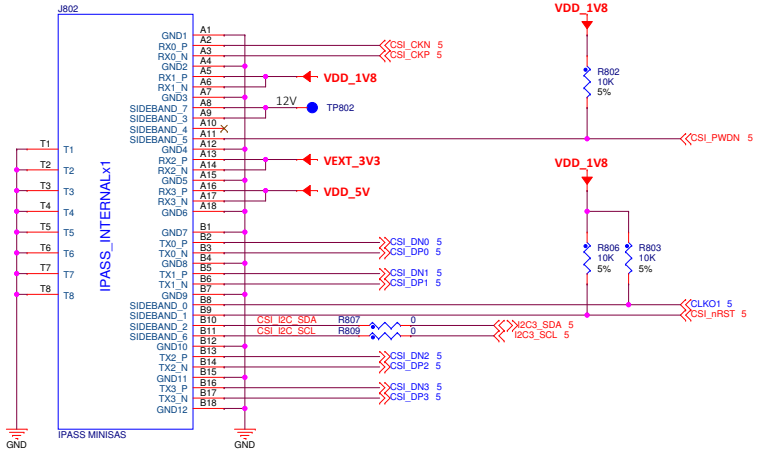
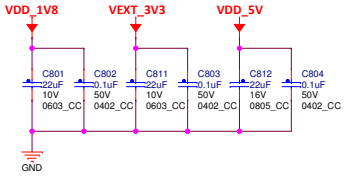
Camera/DSI LCD

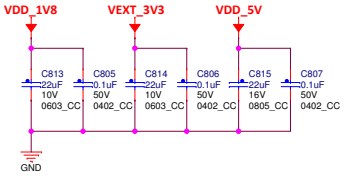
DSI LCD



Camera







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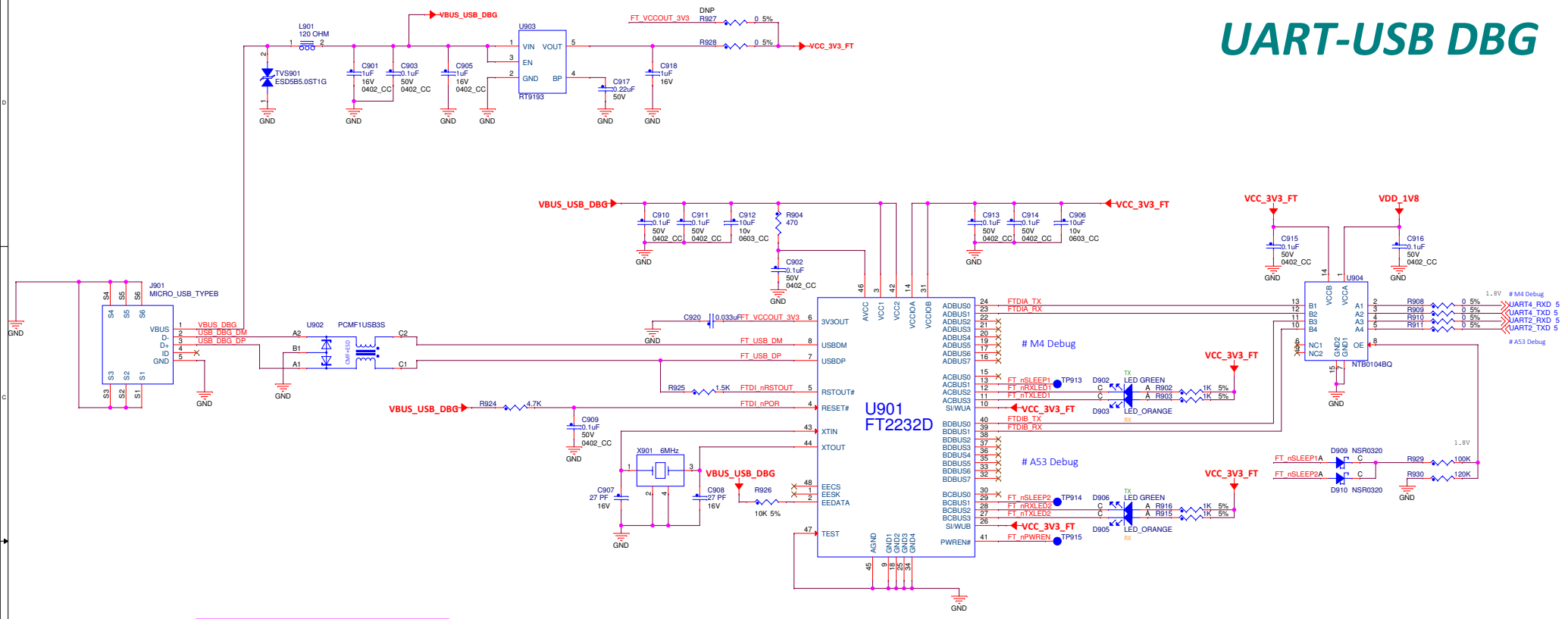
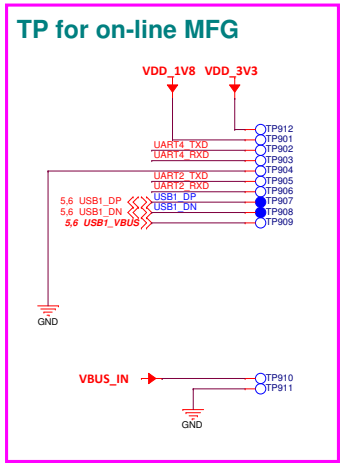
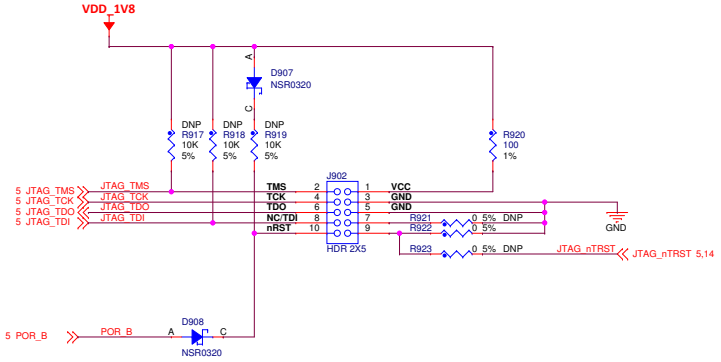
UART-USB DBG



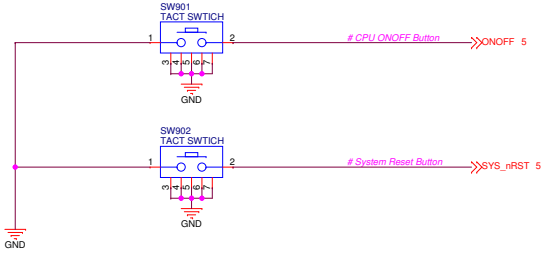
TP for on-line MFG



JTAG Debug



Buttons



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Ext CN

Caution:
IO internal pull up/down is not supported in 3.3V mode, must disable the internal pull up/down via software and use external pull up/down resistors instead.
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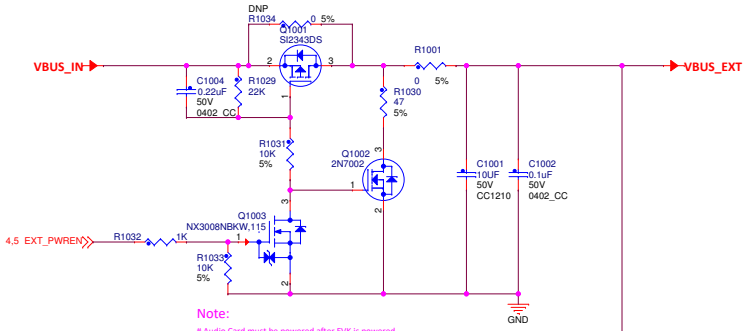
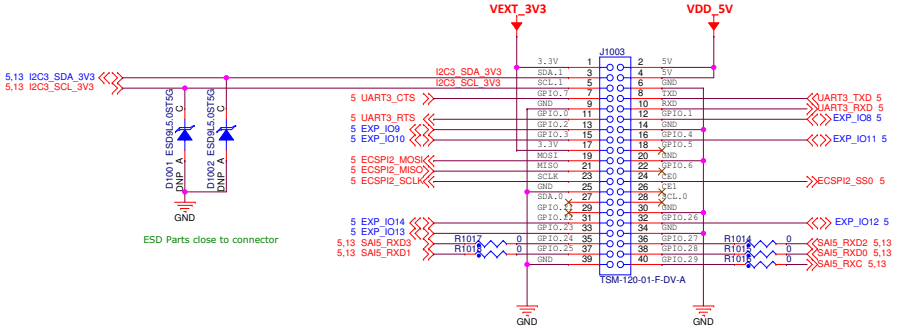
See Errata e50080 for detailed information.

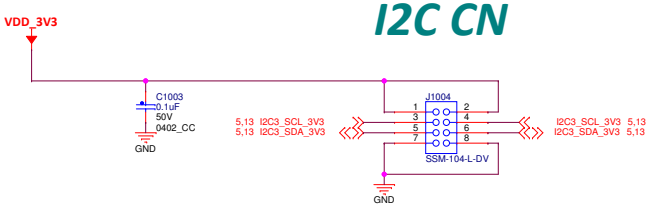


Audio Card CN

EXP CN



I2C CN



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Boot Mode and CFG Switch

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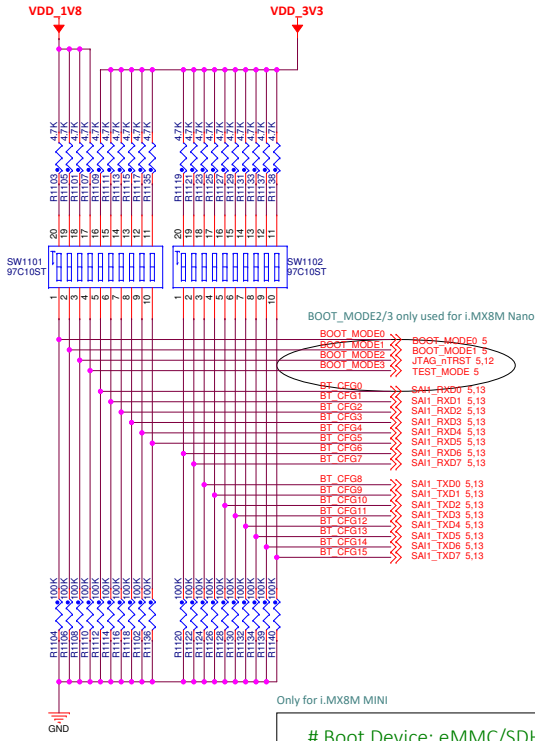
IO internal pull up/down is not supported in 3.3V mode, must disable the internal pull up/down via software and use external pull up/down resistors instead.
All IO pin groups are impacted except for XTAL, DDR, PCI, USB and MIPI PHY IO's.
See Errata e50080 for detailed information.

i.MX8M MINI ROM Fuse

	Address	7	6	5	4	3	2	1	0
	0x470[15:8]	**BOOT_CFG[15]**	**BOOT_CFG[14]**	**BOOT_CFG[13]**	**BOOT_CFG[12]**	**BOOT_CFG[11]**	**BOOT_CFG[10]**	**BOOT_CFG[9]**	**BOOT_CFG[8]**
	0x470[15:8]	Infinit-Loop (Debug USE only) 0 - Disable 1 - Enable	001 - SD/eSD			Port Select: 00 - uSDHC1 01 - uSDHC2 10 - uSDHC3		Power Cycle Enable '0' - No power cycle '1' - Enabled via	SD Loopback Clock Source Sel (for SDR50 and SDR104 only) '0' - through SD pad '1' - direct
	0x470[15:8]		010 - MMC/eMMC						
	0x470[15:8]		011 - NAND			Pages In Block: 00 - 128 01 - 64 10 - 32 11 - 256		Nand_Row_address_bytes: 00 - 3 01 - 2 10 - 4 11 - 5	
	0x470[15:8]		100 - QSPI			Flash Auto Probe	FLASH_TYPE 000-Device supports 3B read by default 001-Device supports 4B read by default 010-HyperFlash 1V8 011-HyperFlash 3V3 100-MXIC Octal DDR		
	0x470[15:8]		110 - SPI NOR			Port Select: 000 - eCSPI1 001 - eCSPI2 010 - eCSPI3			SPI Addressing: 0 - 3-bytes (24-bit) 1 - 2-bytes (16-bit)
	0x470[15:8]	Others - Reserved for future use							
		BOOT_CFG[7]	**BOOT_CFG[6]**	**BOOT_CFG[5]**	**BOOT_CFG[4]**	**BOOT_CFG[3]**	**BOOT_CFG[2]**	**BOOT_CFG[1]**	**BOOT_CFG[0]**
SD/eSD	0x470[7:0]	Fast Boot: 0 - Regular 1 - Fast Boot	Reserved	Reserved	Bus Width: 0 - 1-bit 1 - 4-bit	Speed 000 - Normal/SDR12 001 - High/SDR25 010 - SDR50 011 - SDR104 101 - Reserved for DDR50 Others - Reserved			Reserved
MMC/eMMC	0x470[7:0]		Bus Width: 000 - 1-bit 001 - 4-bit 010 - 8-bit 101 - 4-bit DDR (MMC 4.4) 110 - 8-bit DDR (MMC 4.4) Else - reserved.			Speed 00 - Normal 01 - High 10 - Reserved for HS200 11 - Reserved		USDHC IO VOLTAGE SELECTION For Normal Boot Mode 0 - 3.3V 1 - 1.8V	USDHC IO VOLTAGE SELECTION For Manufacture Mode 0 - 3.3V 1 - 1.8V
NAND	0x470[7:0]	BT_TOGGLEMODE	BOOT_SEARCH_COUNT: 00 - 2 01 - 2 10 - 4 11 - 8		Toggle Mode 33MHz Preamble Delay, Read Latency: '000' - 16 GPMICLK cycles. '001' - 1 GPMICLK cycles. '010' - 2 GPMICLK cycles. '011' - 3 GPMICLK cycles. '100' - 4 GPMICLK cycles. '101' - 5 GPMICLK cycles. '110' - 6 GPMICLK cycles. '111' - 7 GPMICLK cycles. '1111'- 15 GPMICLK cycles.			Reserved
FlexSPI	0x470[7:0]	HOLD TIME: 00 - 500us 01 - 1ms 10 - 3ms 11 - 10ms		FLASH Auto Probe Type		FlexSPI FLASH Dummy Cycle			
SPINOR	0x470[7:0]	CS select SPI only: 00 - CS#0 default 01 - CS#1 10 - CS#2 11 - CS#3	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved



Only for i.MX8M MINI

BMODE

BOOT_MODE1	BOOT_MODE0
BOOT TYPE:	
00	*Boot From Fuses*
01	*Serial Downloader*
10	***Internal Boot (Development)***
11	*Reserved*

 # Boot Device: eMMC/SDHC3

SW1101 [1-10]: 0110110001
SW1102 [1-10]: 0001010100

 # Boot Device: MicroSD/SDHC2

SW1101 [1-10]: *0110110010*
SW1102 [1-10]: *0001101000*

 # Boot Device: NAND

SW1101 [1-10]: 0110000000
SW1102 [1-10]: 1000111100

 # Download Mode

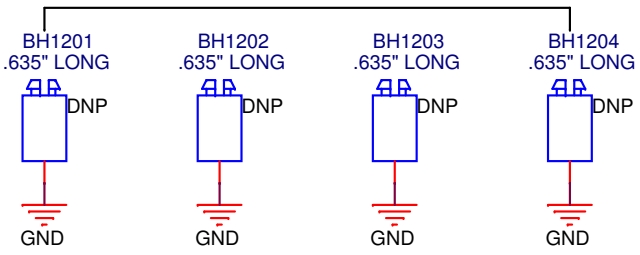
SW1101 [1-10]: 1010xxxxxx
SW1102 [1-10]: xxxxxxxxx0

Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

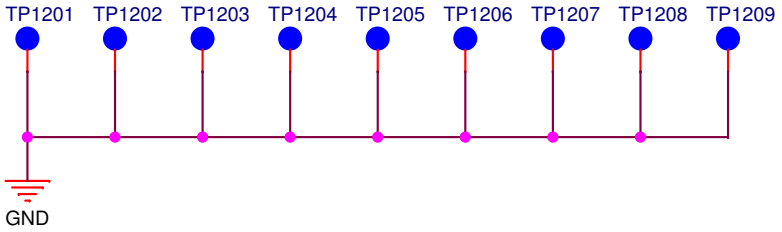
ICAP Classification: CP: IUO: X PUBI:

Designer: <JW>	Drawing Title: 8MMINI-BB	
Drawn by: <JW>	Page Title: BOOT CFG	
Approved: <Approver>	Size C	Document Number SCH-31407 PDF: SPF-31407 Rev C2
	Date: Friday, March 22, 2019	Sheet 14 of 16

Base board positioning holes

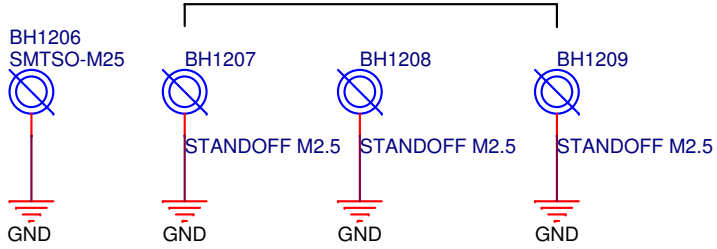


GND Testpoints



Standoff for M.2

Standoff for CPU board TOP



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Designer: <JW>	Drawing Title: **8MMINI-BB**		
Drawn by: <JW>	Page Title: **Mechanical and Testpoints**		
Approved: <Approver>	Size A	Document Number SCH-31407 PDF: SPF-31407	Rev C2
	Date: Friday, March 22, 2019	Sheet 15 of 16	

i.MX8M MINI IOMUX

NAME	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	Alt6 Special EN	ALT7	Alt7 Special EN
TEST_MODE	tcu.TEST_MODE	tcu.TEST_MODE									
BOOT_MODE0	ccmsrcgpcmix.BOOT_MODE[0]	ccmsrcgpcmix.BOOT_MODE[0]									
BOOT_MODE1	ccmsrcgpcmix.BOOT_MODE[1]	ccmsrcgpcmix.BOOT_MODE[1]									
JTAG_MOD	cjtag_wrapper.MOD	cjtag_wrapper.MODE									
JTAG_TRST_B	cjtag_wrapper.TRST_B	cjtag_wrapper.TRST_B									
JTAG_TDI	cjtag_wrapper.TDI	cjtag_wrapper.TDI									
JTAG_TMS	cjtag_wrapper.TMS	cjtag_wrapper.TMS									
JTAG_TCK	cjtag_wrapper.TCK	cjtag_wrapper.TCK									
JTAG_TDO	cjtag_wrapper.TDO	cjtag_wrapper.TDO									
RTC_XTALI	snvsmix.RTC	snvsmix.RTC									
RTC_XTALO											
PMIC_STBY_REQ	ccmsrcgpcmix.PMIC_STBY_REQ	ccmsrcgpcmix.PMIC_STBY_REQ									
PMIC_ON_REQ	snvsmix.PMIC_ON_REQ	snvsmix.PMIC_ON_REQ									
ONOFF	snvsmix.ONOFF	snvsmix.ONOFF									
POR_B	snvsmix.POR_B	snvsmix.POR_B									
RTC_RESET_B	snvsmix.RTC_POR_B	snvsmix.RTC_RESET_B									
GPIO1_IO00	gpio1.IO[0]	gpio1.IO[0]	ccmsrcgpcmix.ENET_PHY_REF_CLK_ROOT				anamix.REF_CLK_32K	ccmsrcgpcmix.EXT_CLK1		sjc.FAIL	
GPIO1_IO01	gpio1.IO[1]	gpio1.IO[1]	pwm1.OUT				anamix.REF_CLK_24M	ccmsrcgpcmix.EXT_CLK2		sjc.ACTIVE	ccmsrcgpcmix.src_system_rst
GPIO1_IO02	gpio1.IO[2]	gpio1.IO[2]	wdog1.WDOG_B				wdog1.WDOG_ANY			sjc.DE_B	sjc.sjc_gpucr1_reg[30]
GPIO1_IO03	gpio1.IO[3]	gpio1.IO[3]	usdhc1.VSELECT				sdma1.EXT_EVENT[0]	anamix.xtal_ok		sjc.DONE	
GPIO1_IO04	gpio1.IO[4]	gpio1.IO[4]	usdhc2.VSELECT				sdma1.EXT_EVENT[1]	anamix.xtal_ok_lv		usdhc1.TEST_TRIG	
GPIO1_IO05	gpio1.IO[5]	gpio1.IO[5]	m4.NMI				ccmsrcgpcmix.PMIC_READY	ccmsrcgpcmix.INT_BOOT	ccmsrcgpcmix.src_system_rst	usdhc2.TEST_TRIG	
GPIO1_IO06	gpio1.IO[6]	gpio1.IO[6]	enet1.MDC				usdhc1.CD_B	ccmsrcgpcmix.EXT_CLK3		ecspi1.TEST_TRIG	
GPIO1_IO07	gpio1.IO[7]	gpio1.IO[7]	enet1.MDIO				usdhc1.WP	ccmsrcgpcmix.EXT_CLK4		ecspi2.TEST_TRIG	
GPIO1_IO08	gpio1.IO[8]	gpio1.IO[8]	enet1.1588_EVENT0_IN				usdhc2.RESET_B	ccmsrcgpcmix.WAIT		qspi.TEST_TRIG	
GPIO1_IO09	gpio1.IO[9]	gpio1.IO[9]	enet1.1588_EVENT0_OUT			usdhc3.RESET_B	sdma2.EXT_EVENT[0]	ccmsrcgpcmix.STOP		rawnand.TEST_TRIG	
GPIO1_IO10	gpio1.IO[10]	gpio1.IO[10]	usb1.OTG_ID							ocotp_ctrl_wrapper.FUSE_LATCHED	sjc.sjc_gpucr3_reg[14]
GPIO1_IO11	gpio1.IO[11]	gpio1.IO[11]	usb2.OTG_ID			usdhc3.VSELECT	ccmsrcgpcmix.PMIC_READY	ccmsrcgpcmix.OUT0		caam_wrapper.RNG_OSC_OBS	
GPIO1_IO12	gpio1.IO[12]	gpio1.IO[12]	usb1.OTG_PWR				sdma2.EXT_EVENT[1]	ccmsrcgpcmix.OUT1		csu.CSU_ALARM_AUT[0]	
GPIO1_IO13	gpio1.IO[13]	gpio1.IO[13]	usb1.OTG_OC				pwm2.OUT	ccmsrcgpcmix.OUT2		csu.CSU_ALARM_AUT[1]	
GPIO1_IO14	gpio1.IO[14]	gpio1.IO[14]	usb2.OTG_PWR			usdhc3.CD_B	pwm3.OUT	ccmsrcgpcmix.CLKO1		csu.CSU_ALARM_AUT[2]	
GPIO1_IO15	gpio1.IO[15]	gpio1.IO[15]	usb2.OTG_OC			usdhc3.WP	pwm4.OUT	ccmsrcgpcmix.CLKO2		csu.CSU_INT_DEB	
ENET_MDC	enet1.MDC						gpio1.IO[16]				
ENET_MDIO	gpio1.IO[17]	enet1.MDIO					gpio1.IO[17]				
ENET_TD3	gpio1.IO[18]	enet1.RGMII_TD3					gpio1.IO[18]				
ENET_TD2	gpio1.IO[19]	enet1.RGMII_TD2	enet1.TX_CLK /ENET_REF_CLK_ROOT				gpio1.IO[19]				
ENET_TD1	gpio1.IO[20]	enet1.RGMII_TD1					gpio1.IO[20]				
ENET_TD0	gpio1.IO[21]	enet1.RGMII_TD0					gpio1.IO[21]				
ENET_TX_CTL	gpio1.IO[22]	enet1.RGMII_TX_CTL					gpio1.IO[22]				
ENET_TXC	gpio1.IO[23]	enet1.RGMII_TXC	enet1.TX_ER				gpio1.IO[23]				
ENET_RX_CTL	gpio1.IO[24]	enet1.RGMII_RX_CTL					gpio1.IO[24]				
ENET_RXC	gpio1.IO[25]	enet1.RGMII_RXC	enet1.RX_ER				gpio1.IO[25]				
ENET_RD0	gpio1.IO[26]	enet1.RGMII_RD0					gpio1.IO[26]				
ENET_RD1	gpio1.IO[27]	enet1.RGMII_RD1					gpio1.IO[27]				
ENET_RD2	gpio1.IO[28]	enet1.RGMII_RD2					gpio1.IO[28]				
ENET_RD3	gpio1.IO[29]	enet1.RGMII_RD3					gpio1.IO[29]				
SD1_CLK	gpio2.IO[0]	usdhc1.CLK					gpio2.IO[0]				
SD1_CMD	gpio2.IO[1]	usdhc1.CMD					gpio2.IO[1]				
SD1_DATA0	gpio2.IO[2]	usdhc1.DATA0					gpio2.IO[2]				
SD1_DATA1	gpio2.IO[3]	usdhc1.DATA1					gpio2.IO[3]				
SD1_DATA2	gpio2.IO[4]	usdhc1.DATA2					gpio2.IO[4]				
SD1_DATA3	gpio2.IO[5]	usdhc1.DATA3					gpio2.IO[5]				
SD1_DATA4	gpio2.IO[6]	usdhc1.DATA4					gpio2.IO[6]				
SD1_DATA5	gpio2.IO[7]	usdhc1.DATA5					gpio2.IO[7]				
SD1_DATA6	gpio2.IO[8]	usdhc1.DATA6					gpio2.IO[8]				
SD1_DATA7	gpio2.IO[9]	usdhc1.DATA7					gpio2.IO[9]				
SD1_RESET_B	gpio2.IO[10]	usdhc1.RESET_B					gpio2.IO[10]				
SD1_STROBE	gpio2.IO[11]	usdhc1.STROBE					gpio2.IO[11]				
SD2_CD_B	gpio2.IO[12]	usdhc2.CD_B					gpio2.IO[12]				
SD2_CLK	gpio2.IO[13]	usdhc2.CLK					gpio2.IO[13]	ccmsrcgpcmix.OBSERVE0		observe_mux.OUT[0]	
SD2_CMD	gpio2.IO[14]	usdhc2.CMD					gpio2.IO[14]	ccmsrcgpcmix.OBSERVE1		observe_mux.OUT[1]	
SD2_DATA0	gpio2.IO[15]	usdhc2.DATA0					gpio2.IO[15]	ccmsrcgpcmix.OBSERVE2		observe_mux.OUT[2]	
SD2_DATA1	gpio2.IO[16]	usdhc2.DATA1					gpio2.IO[16]	ccmsrcgpcmix.WAIT		observe_mux.OUT[3]	
SD2_DATA2	gpio2.IO[17]	usdhc2.DATA2					gpio2.IO[17]	ccmsrcgpcmix.STOP		observe_mux.OUT[4]	
SD2_DATA3	gpio2.IO[18]	usdhc2.DATA3					gpio2.IO[18]	ccmsrcgpcmix.EARLY_RESET	sjc.sjc_gpucr3_reg[14]		
SD2_RESET_B	gpio2.IO[19]	usdhc2.RESET_B					gpio2.IO[19]	ccmsrcgpcmix.SYSTEM_RESET	sjc.sjc_gpucr3_reg[14]		
SD2_WP	gpio2.IO[20]	usdhc2.WP					gpio2.IO[20]				
NAND_ALE	gpio3.IO[0]	rawnand.ALE	qspi.A_SCLK				gpio3.IO[0]			sim_m.HMASTLOCK	sjc.sjc_gpucr1_reg[11]
NAND_CE0_B	gpio3.IO[1]	rawnand.CE0_B	qspi.A_SS0_B				gpio3.IO[1]			sim_m.HPROT[0]	sjc.sjc_gpucr1_reg[11]
NAND_CE1_B	gpio3.IO[2]	rawnand.CE1_B	qspi.A_SS1_B	usdhc3.STROBE			gpio3.IO[2]			sim_m.HPROT[1]	sjc.sjc_gpucr1_reg[11]
NAND_CE2_B	gpio3.IO[3]	rawnand.CE2_B	qspi.B_SS0_B	usdhc3.DATA5			gpio3.IO[3]			sim_m.HPROT[2]	sjc.sjc_gpucr1_reg[11]
NAND_CE3_B	gpio3.IO[4]	rawnand.CE3_B	qspi.B_SS1_B	usdhc3.DATA6			gpio3.IO[4]			sim_m.HPROT[3]	sjc.sjc_gpucr1_reg[11]
NAND_CLE	gpio3.IO[5]	rawnand.CLE	qspi.B_SCLK	usdhc3.DATA7			gpio3.IO[5]			sim_m.HADDR[0]	sjc.sjc_gpucr1_reg[11]
NAND_DATA00	gpio3.IO[6]	rawnand.DATA00	qspi.A_DATA[0]				gpio3.IO[6]			sim_m.HADDR[1]	sjc.sjc_gpucr1_reg[11]
NAND_DATA01	gpio3.IO[7]	rawnand.DATA01	qspi.A_DATA[1]				gpio3.IO[7]			sim_m.HADDR[2]	sjc.sjc_gpucr1_reg[11]
NAND_DATA02	gpio3.IO[8]	rawnand.DATA02	qspi.A_DATA[2]	usdhc3.CD_B			gpio3.IO[8]			sim_m.HADDR[3]	sjc.sjc_gpucr1_reg[11]
NAND_DATA03	gpio3.IO[9]	rawnand.DATA03	qspi.A_DATA[3]	usdhc3.WP			gpio3.IO[9]			sim_m.HADDR[4]	sjc.sjc_gpucr1_reg[11]
NAND_DATA04	gpio3.IO[10]	rawnand.DATA04	qspi.B_DATA[0]	usdhc3.DATA0			gpio3.IO[10]			sim_m.HADDR[5]	sjc.sjc_gpucr1_reg[11]
NAND_DATA05	gpio3.IO[11]	rawnand.DATA05	qspi.B_DATA[1]	usdhc3.DATA1			gpio3.IO[11]			sim_m.HADDR[6]	sjc.sjc_gpucr1_reg[11]
NAND_DATA06	gpio3.IO[12]	rawnand.DATA06	qspi.B_DATA[2]	usdhc3.DATA2			gpio3.IO[12]			sim_m.HADDR[7]	sjc.sjc_gpucr1_reg[11]
NAND_DATA07	gpio3.IO[13]	rawnand.DATA07	qspi.B_DATA[3]	usdhc3.DATA3			gpio3.IO[13]			sim_m.HADDR[8]	sjc.sjc_gpucr1_reg[11]
NAND_DQS	gpio3.IO[14]	rawnand.DQS	qspi.A_DQS				gpio3.IO[14]			sim_m.HADDR[9]	sjc.sjc_gpucr1_reg[11]
NAND_RE_B	gpio3.IO[15]	rawnand.RE_B	qspi.B_DQS	usdhc3.DATA4			gpio3.IO[15]			sim_m.HADDR[10]	sjc.sjc_gpucr1_reg[11]
NAND_READY_B	gpio3.IO[16]	rawnand.READY_B		usdhc3.RESET_B			gpio3.IO[16]			sim_m.HADDR[11]	sjc.sjc_gpucr1_reg[11]
NAND_WE_B	gpio3.IO[17]	rawnand.WE_B		usdhc3.CLK			gpio3.IO[17]			sim_m.HADDR[12]	sjc.sjc_gpucr1_reg[11]
NAND_WP_B	gpio3.IO[18]	rawnand.WP_B		usdhc3.CMD			gpio3.IO[18]			sim_m.HADDR[13]	sjc.sjc_gpucr1_reg[11]
SAI5_RXFS	gpio3.IO[19]	sai5.RX_SYNC	sai1.TX_DATA[0]				gpio3.IO[19]			sim_m.HADDR[14]	sjc.sjc_gpucr1_reg[11]
SAI5_RXC	gpio3.IO[20]	sai5.RX_BCLK	sai1.TX_DATA[1]			pdm.CLK	gpio3.IO[20]			ecspi3.TEST_TRIG	
SAI5_RXD0	gpio3.IO[21]	sai5.RX_DATA[0]	sai1.TX_DATA[2]			pdm.BIT_STREAM[0]	gpio3.IO[21]			usdhc3.TEST_TRIG	
SAI5_RXD1	gpio3.IO[22]	sai5.RX_DATA[1]	sai1.TX_DATA[3]	sai1.TX_SYNC	sai5.TX_SYNC	pdm.BIT_STREAM[1]	gpio3.IO[22]				
SAI5_RXD2	gpio3.IO[23]	sai5.RX_DATA[2]	sai1.TX_DATA[4]	sai1.TX_BCLK	sai5.TX_BCLK	pdm.BIT_STREAM[2]	gpio3.IO[23]				
SAI5_RXD3	gpio3.IO[24]	sai5.RX_DATA[3]	sai1.TX_DATA[5]	sai1.TX_SYNC	sai5.TX_DATA[0]	pdm.BIT_STREAM[3]	gpio3.IO[24]				
SAI5_MCLK	gpio3.IO[25]	sai5.MCLK	sai1.TX_BCLK				gpio3.IO[25]	ccmsrcgpcmix.TESTER_ACK	~ccmsrcgpcmix.src_en_system_clk		
SAI1_RXFS	gpio4.IO[0]	sai1.RX_SYNC	sai5.RX_SYNC			coresight.TRACE_CLK	gpio4.IO[0]			sim_m.HADDR[15]	sjc.sjc_gpucr1_reg[11]
SAI1_RXC	gpio4.IO[1]	sai1.RX_BCLK	sai5.RX_BCLK			coresight.TRACE_CTL	gpio4.IO[1]			sim_m.HADDR[16]	sjc.sjc_gpucr1_reg[11]
SAI1_RXD0	gpio4.IO[2]	sai1.RX_DATA[0]	sai5.RX_DATA[0]	sai1.TX_DATA[1]	pdm.BIT_STREAM[0]	coresight.TRACE[0]	gpio4.IO[2]	ccmsrcgpcmix.BOOT_CFG[0]	ccmsrcgpcmix.src_system_rst	sim_m.HADDR[17]	sjc.sjc_gpucr1_reg[11]
SAI1_RXD1	gpio4.IO[3]	sai1.RX_DATA[1]	sai5.RX_DATA[1]		pdm.BIT_STREAM[1]	coresight.TRACE[1]	gpio4.IO[3]	ccmsrcgpcmix.BOOT_CFG[1]	ccmsrcgpcmix.src_system_rst	sim_m.HADDR[18]	sjc.sjc_gpucr1_reg[11]
SAI1_RXD2	gpio4.IO[4]	sai1.RX_DATA[2]	sai5.RX_DATA[2]		pdm.BIT_STREAM[2]	coresight.TRACE[2]	gpio4.IO[4]	ccmsrcgpcmix.BOOT_CFG[2]	ccmsrcgpcmix.src_system_rst	sim_m.HADDR[19]	sjc.sjc_gpucr1_reg[11]
SAI1_RXD3	gpio4.IO[5]	sai1.RX_DATA[3]	sai5.RX_DATA[3]		pdm.BIT_STREAM[3]	coresight.TRACE[3]	gpio4.IO[5]	ccmsrcgpcmix.BOOT_CFG[3]	ccmsrcgpcmix.src_system_rst	sim_m.HADDR[20]	sjc.sjc_gpucr1_reg[11]
SAI1_RXD4	gpio4.IO[6]	sai1.RX_DATA[4]	sai6.RX_BCLK			coresight.TRACE[4]	gpio4.IO[6]	ccmsrcgpcmix.BOOT_CFG[4]	ccmsrcgpcmix.src_system_rst	sim_m.HADDR[21]	sjc.sjc_gpucr1_reg[11]
SAI1_RXD5	gpio4.IO[7]	sai1.RX_DATA[5]	sai6.RX_DATA[0]	sai1.RX_SYNC		coresight.TRACE[5]	gpio4.IO[7]	ccmsrcgpcmix.BOOT_CFG[5]	ccmsrcgpcmix.src_system_rst	sim_m.HADDR[22]	sjc.sjc_gpucr1_reg[11]
SAI1_RXD6	gpio4.IO[8]	sai1.RX_DATA[6]	sai6.RX_SYNC			coresight.TRACE[6]	gpio4.IO[8]	ccmsrcgpcmix.BOOT_CFG[6]	ccmsrcgpcmix.src_system_rst	sim_m.HADDR[23]	sjc.sjc_gpucr1_reg[11]
SAI1_RXD7	gpio4.IO[9]	sai1.RX_DATA[7]	sai6.MCLK	sai1.TX_DATA[4]		coresight.TRACE[7]	gpio4.IO[9]	ccmsrcgpcmix.BOOT_CFG[7]	ccmsrcgpcmix.src_system_rst	sim_m.HADDR[24]	sjc.sjc_gpucr1_reg[11]
SAI1_TXFS	gpio4.IO[10]	sai1.TX_SYNC	sai5.TX_SYNC			coresight.EVENTO	gpio4.IO[10]			sim_m.HADDR[25]	sjc.sjc_gpucr1_reg[11]
SAI1_TXC	gpio4.IO[11]	sai1.TX_BCLK	sai5.TX_BCLK			coresight.EVENT1	gpio4.IO[11]			sim_m.HADDR[26]	sjc.sjc_gpucr1_reg[11]
SAI1_TXD0	gpio4.IO[12]	sai1.TX_DATA[0]	sai5.TX_DATA[0]			coresight.TRACE[8]	gpio4.IO[12]	ccmsrcgpcmix.BOOT_CFG[8]	ccmsrcgpcmix.src_system_rst	sim_m.HADDR[27]	sjc.sjc_gpucr1_reg[11]
SAI1_TXD1	gpio4.IO[13]	sai1.TX_DATA[1]	sai5.TX_DATA[1]			coresight.TRACE[9]	gpio4.IO[13]	ccmsrcgpcmix.BOOT_CFG[9]	ccmsrcgpcmix.src_system_rst	sim_m.HADDR[28]	sjc.sjc_gpucr1_reg[11]
SAI1_TXD2	gpio4.IO[14]	sai1.TX_DATA[2]	sai5.TX_DATA[2]			coresight.TRACE[10]	gpio4.IO[14]	ccmsrcgpcmix.BOOT_CFG[10]	ccmsrcgpcmix.src_system_rst	sim_m.HADDR[29]	sjc.sjc_gpucr1_reg[11]
SAI1_TXD3	gpio4.IO[15]	sai1.TX_DATA[3]	sai5.TX_DATA[3]			coresight.TRACE[11]	gpio4.IO[15]	ccmsrcgpcmix.BOOT_CFG[11]	ccmsrcgpcmix.src_system_rst	sim_m.HADDR[30]	sjc.sjc_gpucr1_reg[11]
SAI1_TXD4	gpio4.IO[16]	sai1.TX_DATA[4]	sai6.RX_BCLK	sai6.TX_BCLK		coresight.TRACE[12]	gpio4.IO[16]	ccmsrcgpcmix.BOOT_CFG[12]	ccmsrcgpcmix.src_system_rst	sim_m.HADDR[31]	sjc.sjc_gpucr1_reg[11]
SAI1_TXD5	gpio4.IO[17]	sai1.TX_DATA[5]	sai6.RX_DATA[0]	sai6.TX_DATA[0]		coresight.TRACE[13]	gpio4.IO[17]	ccmsrcgpcmix.BOOT_CFG[13]	ccmsrcgpcmix.src_system_rst	sim_m.HBURST[0]	sjc.sjc_gpucr1_reg[11]
SAI1_TXD6	gpio4.IO[18]	sai1.TX_DATA[6]	sai6.RX_SYNC	sai6.TX_SYNC		coresight.TRACE[14]	gpio4.IO[18]	ccmsrcgpcmix.BOOT_CFG[14]	ccmsrcgpcmix.src_system_rst	sim_m.HBURST[1]	sjc.sjc_gpucr1_reg[11]
SAI1_TXD7	gpio4.IO[19]	sai1.TX_DATA[7]	sai6.MCLK	pdm.CLK		coresight.TRACE[15]	gpio4.IO[19]	ccmsrcgpcmix.BOOT_CFG[15]	ccmsrcgpcmix.src_system_rst	sim_m.HBURST[2]	sjc.sjc_gpucr1_reg[11]
SAI1_MCLK	gpio4.IO[20]	sai1.MCLK	sai1.TX_BCLK	pdm.CLK			gpio4.IO[20]			sim_m.HRESP	sjc.sjc_gpucr1_reg[11]
SAI2_RXFS	gpio4.IO[21]	sai2.RX_SYNC	sai5.TX_SYNC	sai2.RX_DATA[1]		uart1.TX	gpio4.IO[21]			sim_m.HSIZE[0]	sjc.sjc_gpucr1_reg[11]
SAI2_RXC	gpio4.IO[22]	sai2.RX_BCLK	sai5.TX_BCLK			uart1.RX	gpio4.IO[22]			sim_m.HSIZE[1]	sjc.sjc_gpucr1_reg[11]
SAI2_RXD0	gpio4.IO[23]	sai2.RX_DATA[0]	sai5.TX_DATA[0]			uart1.RTS_B	gpio4.IO[23]			sim_m.HSIZE[2]	sjc.sjc_gpucr1_reg[11]
SAI2_TXFS	gpio4.IO[24]	sai2.TX_SYNC	sai5.TX_DATA[1]	sai2.TX_DATA[1]		uart1.CTS_B	gpio4.IO[24]			sim_m.HWRITE	sjc.sjc_gpucr1_reg[11]
SAI2_TXC	gpio4.IO[25]	sai2.TX_BCLK	sai5.TX_DATA[2]				gpio4.IO[25]			sim_m.HREADYOUT	sjc.sjc_gpucr1_reg[11]
SAI2_TXD0	gpio4.IO[26]	sai2.TX_DATA[0]	sai5.TX_DATA[3]				gpio4.IO[26]			tpsmp.CLK	sjc.sjc_gpucr1_reg[11]
SAI2_MCLK	gpio4.IO[27]	sai2.MCLK	sai5.MCLK				gpio4.IO[27]			tpsmp.HDATA_DIR	sjc.sjc_gpucr1_reg[11]
SAI3_RXFS	gpio4.IO[28]	sai3.RX_SYNC	gpt1.CAPTURE1	sai3.RX_DATA[1]			gpio4.IO[28]			tpsmp.HTRANS[0]	sjc.sjc_gpucr1_reg[11]
SAI3_RXC	gpio4.IO[29]	sai3.RX_BCLK	gpt1.CAPTURE2	sai5.RX_BCLK		uart2.CTS_B	gpio4.IO[29]			tpsmp.HTRANS[1]	sjc.sjc_gpucr1_reg[11]
SAI3_RXD	gpio4.IO[30]	sai3.RX_DATA[0]	gpt1.COMPARE1	sai5.RX_DATA[0]		uart2.RTS_B	gpio4.IO[30]			tpsmp.HDATA[0]	sjc.sjc_gpucr1_reg[11]
SAI3_TXFS	gpio4.IO[31]	sai3.TX_SYNC	gpt1.CLK	sai5.RX_DATA[1]	sai3.TX_DATA[1]	uart2.RX	gpio4.IO[31]			tpsmp.HDATA[1]	sjc.sjc_gpucr1_reg[11]
SAI3_TXC	gpio5.IO[0]	sai3.TX_BCLK	gpt1.COMPARE2	sai5.RX_DATA[2]		uart2.TX	gpio5.IO[0]			tpsmp.HDATA[2]	sjc.sjc_gpucr1_reg[11]
SAI3_TXD	gpio5.IO[1]	sai3.TX_DATA[0]	gpt1.COMPARE3	sai5.RX_DATA[3]			gpio5.IO[1]			tpsmp.HDATA[3]	sjc.sjc_gpucr1_reg[11]
SAI3_MCLK	gpio5.IO[2]	sai3.MCLK	pwm4.OUT	sai5.MCLK			gpio5.IO[2]			tpsmp.HDATA[4]	sjc.sjc_gpucr1_reg[11]
SPDIF_TX	gpio5.IO[3]	spdif1.OUT	pwm3.OUT				gpio5.IO[3]			tpsmp.HDATA[5]	sjc.sjc_gpucr1_reg[11]
SPDIF_RX	gpio5.IO[4]	spdif1.IN	pwm2.OUT				gpio5.IO[4]			tpsmp.HDATA[6]	sjc.sjc_gpucr1_reg[11]
SPDIF_EXT_CLK	gpio5.IO[5]	spdif1.EXT_CLK	pwm1.OUT				gpio5.IO[5]			tpsmp.HDATA[7]	sjc.sjc_gpucr1_reg[11]
ECSPI1_SCLK	gpio5.IO[6]	ecspi1.SCLK	uart3.RX				gpio5.IO[6]			tpsmp.HDATA[8]	sjc.sjc_gpucr1_reg[11]
ECSPI1_MOSI	gpio5.IO[7]	ecspi1.MOSI	uart3.TX				gpio5.IO[7]			tpsmp.HDATA[9]	sjc.sjc_gpucr1_reg[11]
ECSPI1_MISO	gpio5.IO[8]	ecspi1.MISO	uart3.CTS_B				gpio5.IO[8]			tpsmp.HDATA[10]	sjc.sjc_gpucr1_reg[11]
ECSPI1_SS0	gpio5.IO[9]	ecspi1.SS0	uart3.RTS_B				gpio5.IO[9]			tpsmp.HDATA[11]	sjc.sjc_gpucr1_reg[11]
ECSPI2_SCLK	gpio5.IO[10]	ecspi2.SCLK	uart4.RX				gpio5.IO[10]			tpsmp.HDATA[12]	sjc.sjc_gpucr1_reg[11]
ECSPI2_MOSI	gpio5.IO[11]	ecspi2.MOSI	uart4.TX				gpio5.IO[11]			tpsmp.HDATA[13]	sjc.sjc_gpucr1_reg[11]
ECSPI2_MISO	gpio5.IO[12]	ecspi2.MISO	uart4.CTS_B				gpio5.IO[12]			tpsmp.HDATA[14]	sjc.sjc_gpucr1_reg[11]
ECSPI2_SS0	gpio5.IO[13]	ecspi2.SS0	uart4.RTS_B				gpio5.IO[13]			tpsmp.HDATA[15]	sjc.sjc_gpucr1_reg[11]
I2C1_SCL	gpio5.IO[14]	i2c1.SCL	enet1.MDC				gpio5.IO[14]			tpsmp.HDATA[16]	sjc.sjc_gpucr1_reg[11]
I2C1_SDA	gpio5.IO[15]	i2c1.SDA	enet1.MDIO				gpio5.IO[15]			tpsmp.HDATA[17]	sjc.sjc_gpucr1_reg[11]
I2C2_SCL	gpio5.IO[16]	i2c2.SCL	enet1.1588_EVENT1_IN	usdhc3.CD_B			gpio5.IO[16]			tpsmp.HDATA[18]	sjc.sjc_gpucr1_reg[11]
I2C2_SDA	gpio5.IO[17]	i2c2.SDA	enet1.1588_EVENT1_OUT	usdhc3.WP			gpio5.IO[17]			tpsmp.HDATA[19]	sjc.sjc_gpucr1_reg[11]
I2C3_SCL	gpio5.IO[18]	i2c3.SCL	pwm4.OUT	gpt2.CLK			gpio5.IO[18]			tpsmp.HDATA[20]	sjc.sjc_gpucr1_reg[11]
I2C3_SDA	gpio5.IO[19]	i2c3.SDA	pwm3.OUT	gpt3.CLK			gpio5.IO[19]			tpsmp.HDATA[21]	sjc.sjc_gpucr1_reg[11]
I2C4_SCL	gpio5.IO[20]	i2c4.SCL	pwm2.OUT	pcie1.CLKREQ_B			gpio5.IO[20]			tpsmp.HDATA[22]	sjc.sjc_gpucr1_reg[11]
I2C4_SDA	gpio5.IO[21]	i2c4.SDA	pwm1.OUT				gpio5.IO[21]			tpsmp.HDATA[23]	sjc.sjc_gpucr1_reg[11]
UART1_RXD	gpio5.IO[22]	uart1.RX	ecspi3.SCLK				gpio5.IO[22]			tpsmp.HDATA[24]	sjc.sjc_gpucr1_reg[11]
UART1_TXD	gpio5.IO[23]	uart1.TX	ecspi3.MOSI				gpio5.IO[23]			tpsmp.HDATA[25]	sjc.sjc_gpucr1_reg[11]
UART2_RXD	gpio5.IO[24]	uart2.RX	ecspi3.MISO				gpio5.IO[24]			tpsmp.HDATA[26]	sjc.sjc_gpucr1_reg[11]
UART2_TXD	gpio5.IO[25]	uart2.TX	ecspi3.SS0				gpio5.IO[25]			tpsmp.HDATA[27]	sjc.sjc_gpucr1_reg[11]
UART3_RXD	gpio5.IO[26]	uart3.RX	uart1.CTS_B	usdhc3.RESET_B			gpio5.IO[26]			tpsmp.HDATA[28]	sjc.sjc_gpucr1_reg[11]
UART3_TXD	gpio5.IO[27]	uart3.TX	uart1.RTS_B	usdhc3.VSELECT			gpio5.IO[27]			tpsmp.HDATA[29]	sjc.sjc_gpucr1_reg[11]
UART4_RXD	gpio5.IO[28]	uart4.RX	uart2.CTS_B	pcie1.CLKREQ_B			gpio5.IO[28]			tpsmp.HDATA[30]	sjc.sjc_gpucr1_reg[11]
UART4_TXD	gpio5.IO[29]	uart4.TX	uart2.RTS_B				gpio5.IO[29]			tpsmp.HDATA[31]	sjc.sjc_gpucr1_reg[11]
CLKIN1		anamix.CLKIN1									
CLKIN2		anamix.CLKIN2									
CLKOUT1		anamix.CLKOUT1									
CLKOUT2		anamix.CLKOUT2									
XTALI_24M		anamix.xtal_24M									
XTALO_24M											

PIN LIST

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ICAP Classification: CP: IUO: X PUBI:

Designer: <JW>	Drawing Title: 8MMINI-BB		
Drawn by: <JW>	Page Title: IOMUX		
Approved: <Approver>	Size: Custom	Document Number: SCH-31407 PDF: SPF-31407	Rev: C2
	Date: Friday, March 22, 2019	Sheet 16 of 16	