NXP Semiconductors
User's Guide

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i.MX 8M Mini LPDDR4 EVK Board Hardware User's Guide

1. Introduction

This document is a hardware user's guide for the i.MX 8M Mini LPDDR4 Evaluation Kit (EVK) based on the NXP Semiconductors' i.MX 8M Mini applications Processor. This board is fully supported by NXP Semiconductors. This manual includes system setup and configurations and provides detailed information about the overall design and usage of the EVK board from a hardware system perspective.

1.1. Board overview

The LPDDR4 EVK board is a platform designed to show the most commonly used features of the i.MX 8M Mini applications processor in a small and low-cost package. The i.MX 8M Mini LPDDR4 EVK board is an entry-level development board, which helps you to become familiar with the processor before investing a large amount of resources into more specific designs.

Table 1 lists the features of the i.MX 8M Mini LPDDR4 EVK board.

Contents

Table 1. Board features

Processor	NXP Applications Processor	MIMX8MM6DVTLZAA
DRAM memory	Micron 2 GB LPDDR4	MT53D512M32D2DS-053 WT:D
Mass storage	SanDisk 16 GB eMMC5.1	SDINBDG4-16G-I
	Micron 32 MB QSPI NOR	MT25QU256ABA1EW7-0SIT
	MicroSD card connector	SD3.0 supported
Power	ROHM PMIC BD71847 + Discrete DCDC/LDO	
Camera	CSI interface (Mini-SAS connector)	
Display interface	DSI interface (Mini-SAS connector)	
Ethernet	1 GB Ethernet with RJ45 connector	
USB	2x USB (2.0) type-C connector, only Port2 can be used as the power input	
Wi-Fi/Bluetooth	1x on-board Wi-Fi/Bluetooth module, 802.11b/g/n/ac, BT4.1	
Audio connectors	3.5 mm stereo line output, 2 Vrms	
	FPC connector (SAI ports) for audio card	
Debug connectors	JTAG (10-pin header)	
	MicroUSB for UART debug, two COM ports for A53 and M4	
M.2 connector	1x M.2 slot (KEY-E type), support PCIE2.0, I^2C interfaces	
Expansion connector	40-pin dual-row pin header for I^2S, UART, I^2C, and GPIO expansion	
I^2C connector	8-pin dual-row pin header for I^2C expansion	
Buttons	ON/OFF, RESET	
LED indicators	Power status, UART	
PCB	8MMINILPD4-CPU: 2-inch x 2-inch, 8-layer 8MMINI-BB: 4-inch x 4.2-inch, 8-layer	

1.2. Board contents

The i.MX 8M Mini LPDDR4 EVK contains these items:

- i.MX 8M Mini LPDDR4 EVK board, assembled from two separate boards: 8MMINILPD4-CPU (SOM board) and 8MMINI-BB (base board)
- IMX-MIPI-HDMI accessory card, MIPI-DSI-to-HDMI adapter board
- USB type-C 45-W power delivery supply, 5 V/3 A, 9 V/3 A, 15 V/3 A, 20 V/2.25 A supported
- Mini-SAS cable, 8" mini-SAS cable
- USB type-C cable, cable – assembly, USB 3.0, type-C male to type-A male
- USB micro-B cable, cable – assembly, USB 2.0, type-A male to micro-B male
- USB type-C-to-A adapter, adapter – USB 3.0, type-C male to type-A female
- Quick start guide

2. Specifications

This section provides detailed information about the electrical design and practical considerations on the LPDDR4 EVK board. Figure 1 describes each block in the high-level block diagram of the LPDDR4 EVK board.

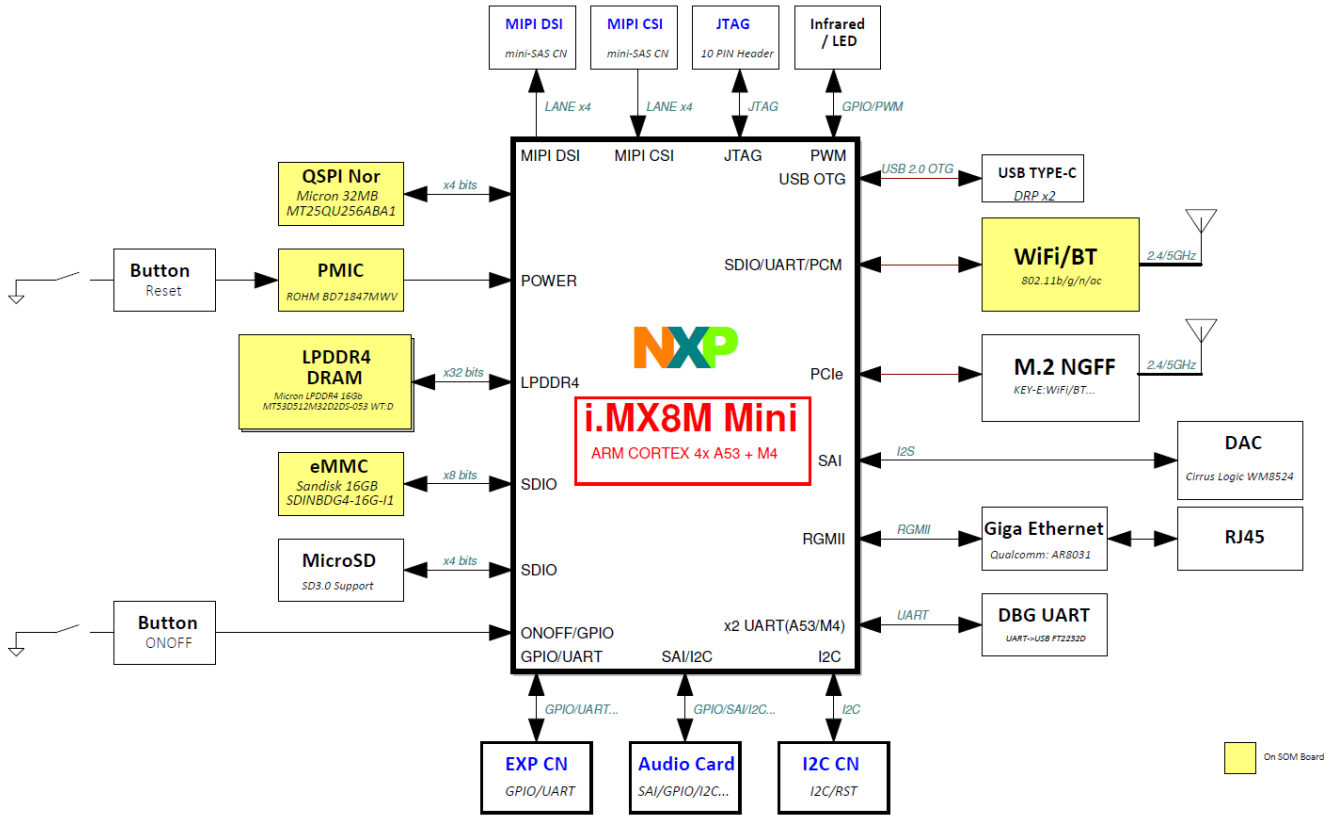

Figure 1. MCIMX8M Mini LPDDR4 EVK block diagram

Figure 2 shows the overview of the i.MX 8M Mini LPDDR4 EVK board.

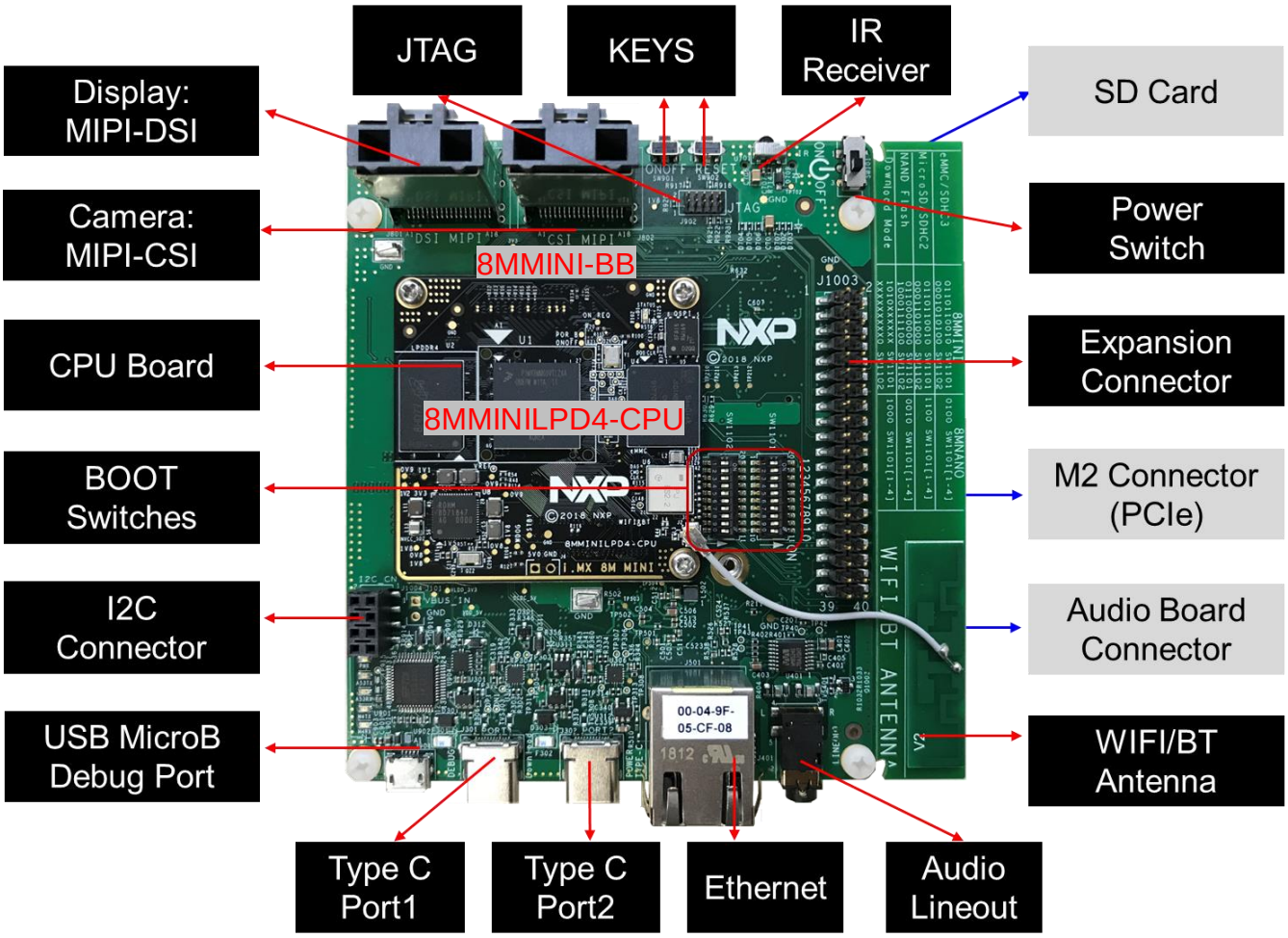

Figure 2. i.MX 8M Mini LPDDR4 EVK board overview

CAUTION

Type-C port 2 is the only power supply port and it must be always supplied for the system to run.

i.MX 8M Mini EVK is not a typical use case of the PD device. It is supplied by the PD charger only, but with a power switch. When the switch is OFF for more than 5.5 seconds after adapting the PD charger, the charger (source) re-powers the EVK (sink) after the system initiates the PD software. See section 6.5.7 in the *Universal Serial Bus Power Delivery Specification Revision 2.0* document. There are two ways to avoid re-powering:

- The power switch must always be in the ON position before attaching the PD charger.
- Change the software to disable the PD function and make it type-C supply only.

2.1. Processor

The i.MX 8M Mini processors represent NXP Semiconductors' latest achievement in the integrated multimedia-focused products offering high-performance processing with a high degree of functional integration, targeted towards the growing market of connected devices. The i.MX 8M Mini processor features NXP's advanced implementation of the quad Arm® Cortex®-A53+ and Arm Cortex-M4 cores, which operate at speeds of up to 1.8 GHz. Each processor provides a 32-bit DDR3L/DDR4/LPDDR4 memory interface and other interfaces for connecting peripherals, such as MIPI LCD, MIPI camera, WLAN, Bluetooth™, Ethernet, digital microphone, GPS, and multi-sensors.

For more information about the processor, see the datasheet and reference manual at www.nxp.com/i.MX8MMINI.

2.2. Boot mode and boot device configurations

The i.MX 8M Mini applications processor can boot from the boot configuration selected on SW1101 or from the boot configuration stored on the internal eFUSE. In addition, the i.MX 8M Mini can download a program image from a USB connection when configured in the serial downloader mode. The method used to determine where the processor finds its boot information is from two dedicated BOOT MODE pins. Table 2 shows the values used in the two methods.

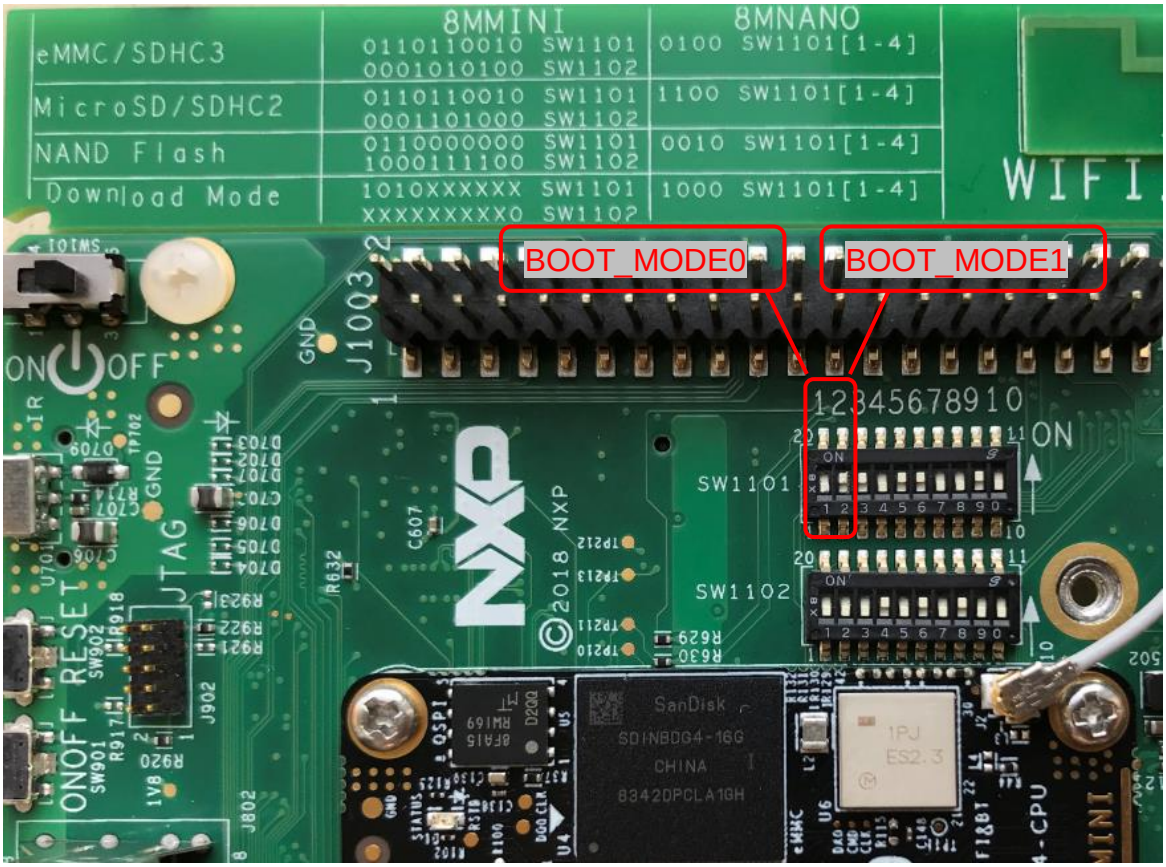

Figure 3. Boot mode selection

Table 2. Boot mode settings

BOOT_MODE0	BOOT_MODE1	Boot mode
0	0	Boot from fuses
1	0	Serial downloader
0	**1**	**Internal boot (default)**
1	1	Reserved

It is important to remember that these two pins are tied to the BOOT modules. To boot the program image from the internal boot mode, which means the processor executes the boot code from the internal boot ROM, the position of switches 1 and 2 must be set to OFF (0) and ON (1). It is the same as choosing the serial downloader mode or booting from the fuse mode to load the boot code into the processor.

If the internal boot mode is selected, you can set switches SW1101 and SW1102 to choose the boot device and related boot configurations according to Table 3 and Figure 4. Figure 5 shows the detailed connection of SW1101 and SW1102.

Table 3. Boot device settings

BOOT device	SW1101	SW1102
eMMC/uSDHC3	0110110001	0001010100
MicroSD/uSDHC2	0110110010	0001101000
NAND Flash	0110000000	1000111100
QSPI NOR Flash	0110xxxxxx	00000x0010
Serial download mode	1010xxxxxx	xxxxxxxxx0

NOTE

The SW1101 bits 3 and 4 are used for designs compatible with i.MX 8M Nano, which must be set to 1 and 0 for i.MX 8M Mini.

The SW1102 bit 10 is used for the infinite loop (debug use only) and must be set to 0.

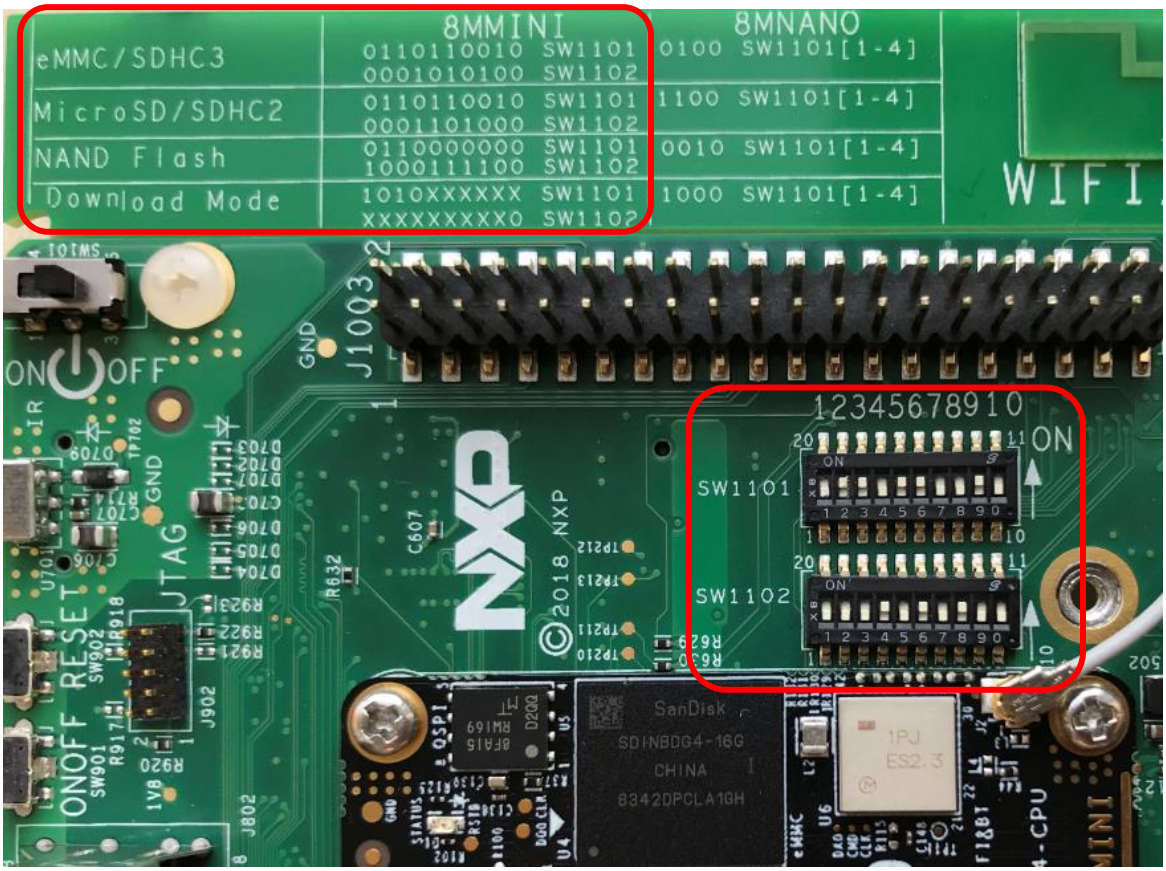

Figure 4. Boot device settings

NOTE

The SW1101 bit[9:10] for the eMMC/SDHC3 boot should be 01 instead of 10 (see Section 4, "Errata" for detailed information).

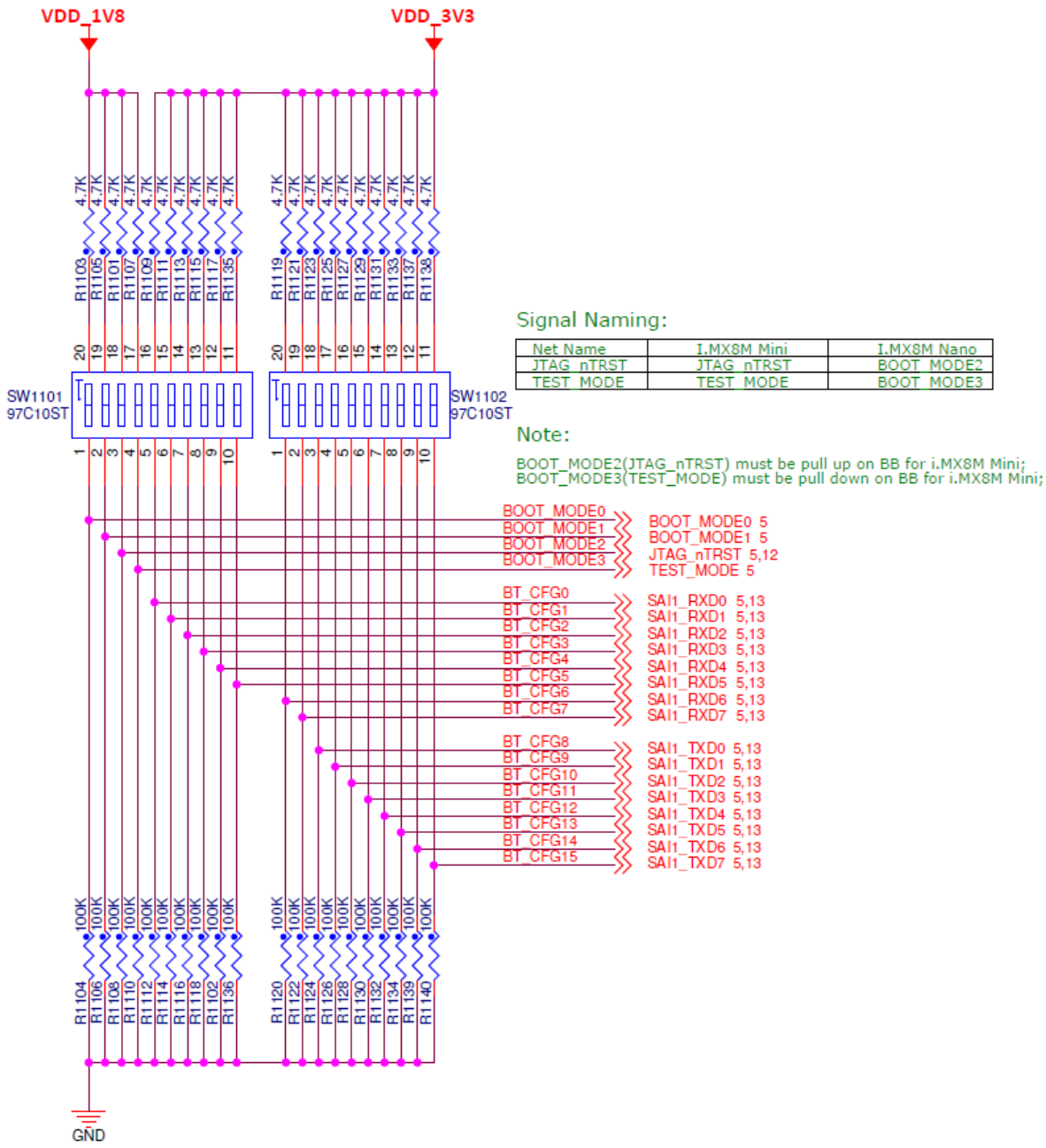

Figure 5. Boot configuration schematic

On the i.MX 8M Mini LPDDR4 EVK board, the default boot mode is from the eMMC device. There are other two boot devices: the first is the QSPI Nor Flash on the CPU board and the second one is the MicroSD connector on the base board. If you set the boot device to QSPI or MicroSD, the board boots from the device accordingly.

NOTE

The NAND boot is not supported on the i.MX 8M Mini LPDDR4 EVK board, but it is supported on the i.MX 8M Mini DDR4 EVK board.

For more information about the boot module (such as the meaning of every bit of the boot switch), see the *i.MX 8M Mini Applications Processor Reference Manual* (document IMX8MMRM).

2.3. Power tree

There is a type-C power supply that must be connected to the i.MX 8M Mini LPDDR4 EVK board using connector J302. The other power sources on the EVK board are generated from the PMIC and discrete devices to supply the whole system. Figure 6 shows the power tree.

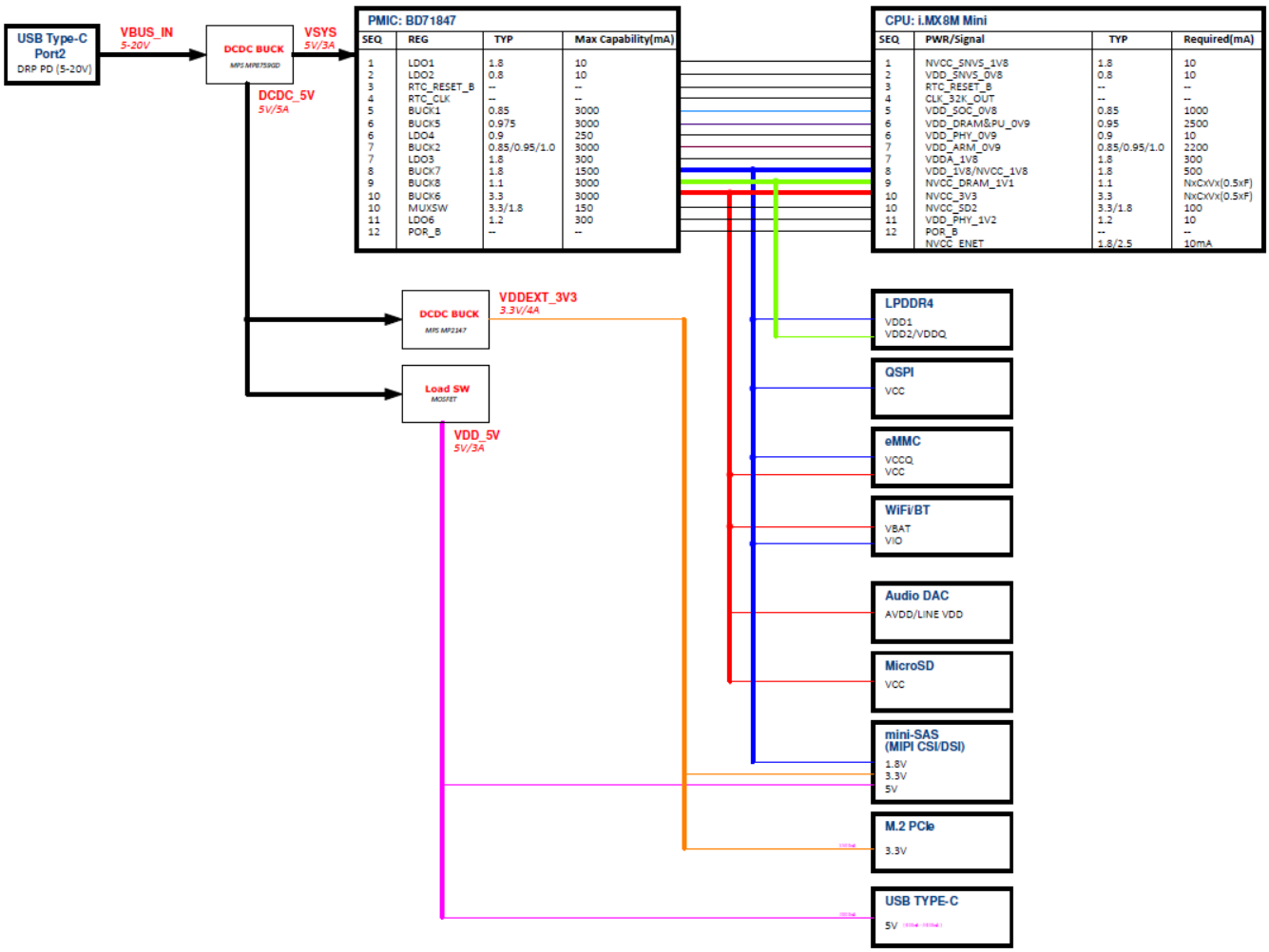

Figure 6. Power tree diagram

In Figure 6, you can find all the power supply rails used on the EVK board. When some modules are not enabled, the power supplies may be shut down by software. Table 4 lists the power rails on the board.

Table 4. Power rails

SEQ	Power rail	Regulator	Value/V
0	DCDC_5V	Discrete	5
1	NVCC_SNVS_1V8	BD71847 LDO1	1.8
2	VDD_SNVS_0V8	BD71847 LDO2	0.8
3	RTC_RESET_B	BD71847	—
4	CLK_32K_OUT	BD71847	—
5	VDD_SOC_0V8	BD71847 BUCK1	0.85[1]
6	VDD_DRAM&PU_0V9	BD71847 BUCK5	0.975[2]
6	VDD_PHY_0V9	BD71847 LDO4	0.9
7	VDD_ARM_0V9	BD71847 BUCK2	0.85/0.95/1.0[3]
7	VDDA_1V8	BD71847 LDO3	1.8
8	VDD_1V8/NVCC_1V8	BD71847 BUCK7	1.8
9	NVCC_DRAM_1V1	BD71847 BUCK8	1.1
10	VDD_3V3/NVCC_3V3	BD71847 BUCK6	3.3
10	NVCC_SD2	BD71847 MUXSW	3.3/1.8
10	VDD_5V	Load switch	5
10	VDDEXT_3V3	Discrete	3.3
11	VDD_PHY_1V2	BD71847 LDO6	1.2
12	POR_B	BD71847	—
13	VSD_3V3	Load switch	3.3

1. BD71847 BUCK1 default output voltage is 0.8 V. The software changes it to 0.85 V in the SPL before the DDR initialization.
2. BD71847 BUCK5 default output voltage is 0.9 V. The software changes it to 0.975 V (BD71847 BUCK5 does not support a 0.95-V output) in the SPL before the DDR initialization.
3. BD71847 BUCK2 default output voltage is 0.9 V. The software changes it to 0.85 V for 1.2 GHz operation, 0.95 V for 1.6 GHz, and 1.0 V for 1.8 GHz.

2.4. LPDDR4 DRAM memory

The i.MX 8M Mini LPDDR4 EVK board has one 512 Meg x 32 (2 channels x 16 I/O) LPDDR4 SDRAM chip (MT53D512M32D2DS-053 WT:D) for a total RAM memory of 2 GB.

In the physical layout, the LPDDR4 chip is placed on the top side and the data traces are not necessarily connected to the LPDDR4 chips in a sequential order. For easier routing, they are connected as determined by the layout and other critical traces.

The DRAM_VREF can be generated by the i.MX 8M Mini internally, so it does not need to use external power-supply and decoupling capacitors. The calibration resistors used by the LPDDR4 chips and processor are 240-Ω 1-% resistors. The differential termination resistor for the DRAM clock is 150-Ω 1-% (on the EVK). You can change this value depending on the simulation and test results.

2.5. eMMC memory (U4)

The eMMC memory is connected to the uSDHC3 interface of the i.MX 8M Mini and supports devices of up to eMMC 5.1. The eMMC memory is on the 8MMINILPD4-CPU board and the part number is SDINBDG4-16G-I. It is the default boot device of the EVK. The boot settings are as shown in Table 3.

2.6. QSPI Nor Flash (U5)

The QSPI memory is connected to the FlexSPI interface of the i.MX 8M Mini and supports up to 166-MHz DDR mode devices. The QSPI memory is on the 8MMINILPD4-CPU board and the part number is MT25QU256ABA1EW7-0SIT. To select it as the boot device of the EVK, see the boot settings shown in Table 3.

2.7. SD card slot (J701)

There is one MicroSD card slot (J701) on the 8MMINI-BB board, connecting to the uSDHC2 interface of the i.MX 8M Mini. This connector supports one 4-bit SD3.0 MicroSD card. To select it as the boot device of the EVK, see the boot settings shown in Table 3.

2.8. MIPI-CSI and MIPI-DSI connectors (J802, J801)

The i.MX 8M Mini processor supports one 4-lane MIPI-CSI and one 4-lane MIPI-DSI. The MiniSAS connectors are designed to support the camera and LCD with a dedicated pin definition. The connectors are shown in Figure 2.

2.9. Ethernet connector (J501)

The Ethernet subsystem of the EVK board is provided by the Qualcomm AR8031 Ethernet transceiver (U501). The Ethernet transceiver (or PHY) receives standard RGMII Ethernet signals from the MAC-NET core of the i.MX 8M Mini. The processor handles all Ethernet protocols at the MAC layer and above. The PHY is only responsible for the link layer formatting. The Ethernet connector (J501) integrates a magnetic transformer inside, so it cannot be connected directly to the AR8031 (U501).

Each EVK board has a unique MAC address, which is printed into the i.MX 8M Mini by a fuse, and the label is glued to the connector.

2.10. USB connectors (J301, J302)

The i.MX 8M Mini applications processors contain two USB 2.0 OTG controllers with two integrated USB PHYs. There are two USB type-C connectors on the EVK board and both support the host and device modes.

- J301 is connected to the USB1 interface of the i.MX 8M Mini, which can act as the download port of the EVK.
- J302 is connected to the USB2 interface of the i.MX 8M Mini, which can act as the power supply port of the EVK.

2.11. Wi-Fi/Bluetooth (U6)

The EVK board has a Wi-Fi/Bluetooth module LBEE5KL1PJ on the 8MMINILPD4-CPU board. The module is based on Qualcomm QCA9377-3, contains the SDIO3.0, UART, and PCM interfaces, and supports 802.11b/g/n/ac, BT4.1. The 2.4G/5G antenna is glued to the edge of the base board with a coaxial cable connected to the CPU board.

2.12. Audio line output (J401)

The EVK board uses a high-quality stereo DAC WM8524 (U401), which supports 24-bit I^2S data and 192-KHz sampling rate. The line output of the WM8524 is 2 Vrms, unlike the common headphone output of 1 Vrms. Be very careful with this interface. The line output connector (J401) is a 3.5-mm 4-pole (or TRRS) phone jack.

CAUTION

The audio line output connector is designed for active speakers with a power amplifier. To connect it to headphones, make sure that the headphones have a volume-control functionality and set the headphones' volume properly before wearing them. Do not plug in non-volume-control headphones directly. The audio output volume may be too high for non-volume-control headphones and may damage them.

2.13. Audio card connector (J1001)

One 60-pin FPC connector (J1001) is provided on the EVK board to support audio card connection and you can use the audio card to perform audio features' development.

2.14. JTAG connector (J902)

The i.MX 8M Mini applications processor has five JATG signals on the dedicated pins and one hardware reset input signal (POR_B). Those signals are directly connected to the 10-pin 1.27-mm JTAG connector J902. The five JTAG signals used by the processor are:

- JTAG_TCK—TAP clock
- JTAG_TMS—TAP machine state
- JTAG_TDI—TAP data in
- JTAG_TDO—TAP data out
- JTAG_nTRST—TAP reset request (active low)

2.15. USB-UART connector (J901)

The i.MX 8M Mini applications processor has four independent UART ports (UART1 – UART4). On the EVK board, UART2 is used for the Cortex-A53 core, and UART4 is used for the Cortex-M4 core. A single-chip USB with the dual-channel UART IC is used for system debugging and the part number is FT2232D. You can download the driver from the FTDI website. After the driver for FT2232D is

installed, the PC enumerates two COM ports when the USB cable is plugged into J901. You can use Putty, Tera Term, Xshell, or other terminal tools. The required settings are listed in Table 5.

Table 5. Terminal setting parameters

Data rate	115,200 baud
Data bits	8
Parity	None
Stop bits	1

2.16. M.2 connector (J601)

One M.2/NGFF connector (J601) is provided on the EVK board to support PCIE2.0, I^2C, and GPIO connections. This port can be used for the Wi-Fi/Bluetooth card or some 3G/4G cards.

2.17. Expansion connector (J1003)

One 40-pin dual-row pin header connector (J1003) is provided on the EVK board to support I^2S, UART, I^2C, and GPIO connection. You can use the port for specific application development.

Table 6. J1003 pin definition

Num	Net name	Description	Num	Net name	Description
1	VEXT_3V3	Power output, 3.3 V	2	VDD_5V	Power output, 5 V
3	I2C3_SDA_3V3	I2C3 data signal	4	VDD_5V	Power output, 5 V
5	I2C3_SCL_3V3	I2C3 clock signal	6	GND	Ground
7	UART3_CTS	UART3 clear to send signal	8	UART3_TXD	UART3 transmit signal
9	GND	Ground	10	UART3_RXD	UART3 transmit signal
11	UART3_RTS	UART3 request to send signal	12	EXP_IO8	Expansion IO signal
13	EXP_IO9	Expansion IO signal	14	GND	Ground
15	EXP_IO10	Expansion IO signal	16	EXP_IO11	Expansion IO signal
17	VEXT_3V3	Power output, 3.3 V	18	—	NC
19	ECSPI2_MOSI	SPI2 data signal, master output slave input	20	GND	Ground
21	ECSPI2_MISO	SPI2 data signal, master input slave output	22	—	NC
23	ECSPI2_SCLK	SPI2 clock signal	24	ECSPI2_SS0	SPI2 chip select signal
25	GND	Ground	26	—	NC
27	—	NC	28	—	NC
29	—	NC	30	GND	Ground
31	EXP_IO14	Expansion IO signal	32	EXP_IO12	Expansion IO signal
33	EXP_IO13	Expansion IO signal	34	GND	Ground
35	SAI5_RXD3	SAI5 receive data signal	36	SAI5_RXD2	SAI5 receive data signal
37	SAI5_RXD1	SAI5 receive data signal	38	SAI5_RXD0	SAI5 receive data signal
39	GND	Ground	40	SAI5_RXC	SAI5 receive clock signal

2.18. I²C connector (J1004)

One 8-pin dual-row pin header connector (J1004) is provided on the EVK board to support I²C connections. You can use the port for specific application development.

Table 7. J1004 pin definition

Num	Net name	Description
1/2	VDD_3V3	Power output, 3.3 V
3/4	I2C3_SCL_3V3	I²C clock signal
5/6	I2C3_SDA_3V3	I²C data signal
7/8	GND	Ground

2.19. User interface buttons

There are two user interface buttons on the EVK board.

2.19.1. Power button (SW901)

The i.MX 8M Mini applications processor supports the use of a button input signal to request main SoC power state changes (ON or OFF) from the PMU.

The ON/OFF button can be used for debounce, OFF-to-ON time, and maximum timeout. Debounce is used to generate a power-off interrupt. In the ON state, if the ON/OFF button is held longer than the debounce time, a power-off interrupt is generated. In the OFF state, if the ON/OFF button is held longer than the OFF-to-ON time, the state transits from OFF to ON. The maximum timeout can also be the time to request a physical power down after the ON/OFF button is held for a defined time.

2.19.2. Reset button (SW902)

The reset button (SW902) is directly connected to PMIC BD71847. Holding the reset button resets the PMIC power outputs, except for the NVCC_SNVS_1V8 and VDD_SNVS_0V8 on the EVK board. The i.MX 8M Mini applications processor is immediately turned off and reinitiates a boot cycle from the OFF state.

2.20. User interface LED indicators

There are four LED indicators on the board. The LEDs have these functions:

- Main power supply (D708):
  - Green—the board is powered on.
  - OFF—the board is powered off.
- System status (D1) on 8MMINILPD4-CPU:
  - Green blinking—the CPU is running well.
  - OFF—the CPU is not running.
- M4 UART (D902/D903):
  - D902 green light flashing—the UART data is transmitted to the PC.

  - D903 orange light flashing—the UART data is received from the PC.
- A53 UART (D906/D905):
  - D906 green light flashing—the UART data is transmitted to the PC.
  - D905 orange light flashing—the UART data is received from the PC.

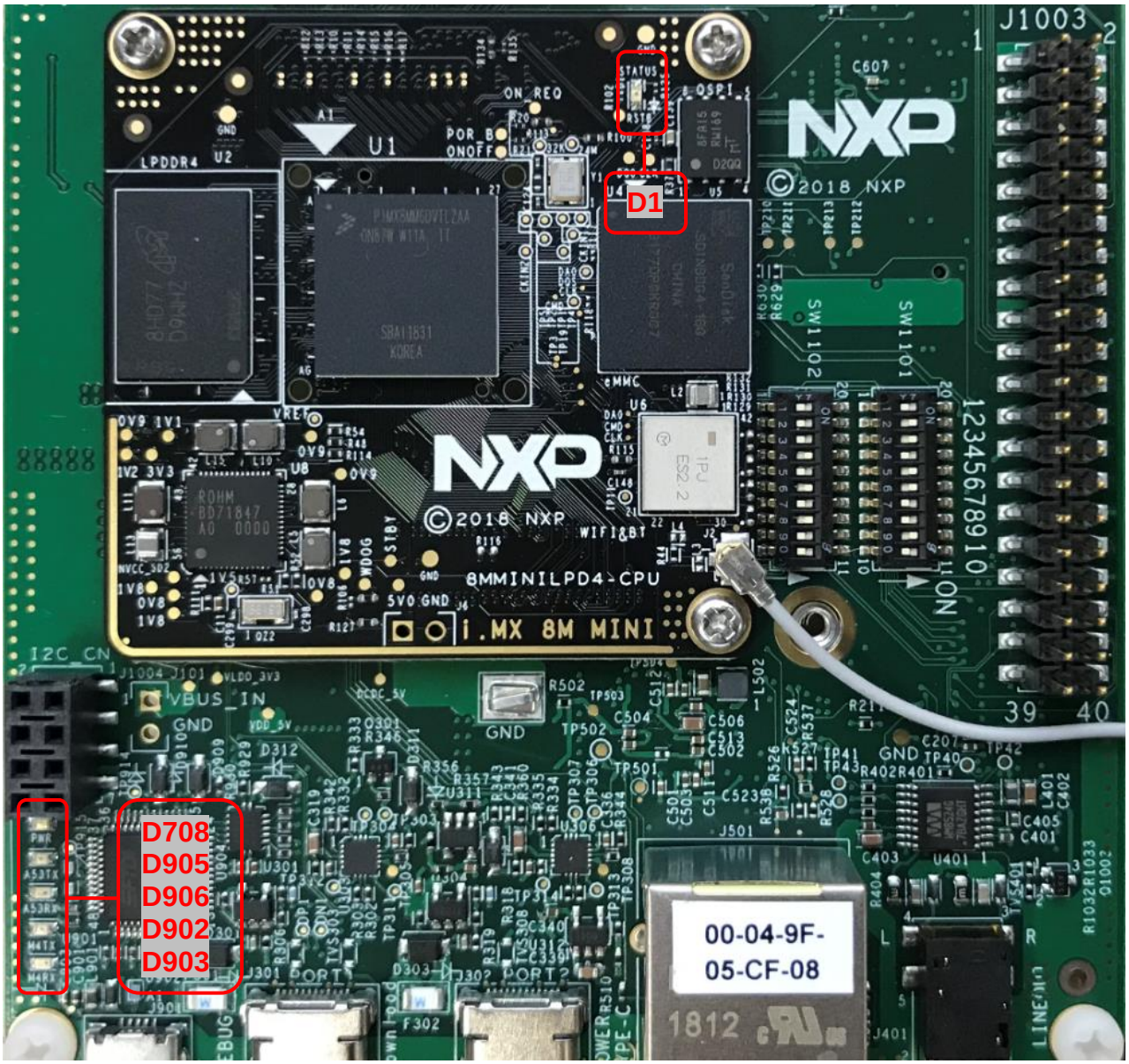

Figure 7. LED indicator

3. PCB information

The i.MX 8M Mini LPDDR4 EVK is composed of 8MMINILPD4-CPU and 8MMINI-BB. Table 1 lists the dimensions of the two boards. Both boards are made using standard 8-layer technology. The material is FR-4, and the PCB stack-up information is shown in Table 8 and Table 9.

Table 8. 8MMINILPD4-CPU board stack-up information

Layer	Description	Copper (Oz.)	Dielectric thickness (mil)
1	Signal	0.333 + plating	
	Dielectric		2.611 mil
2	GND	1	
	Dielectric		3.94 mil
3	Signal	0.5	
	Dielectric		3.7 mil
4	GND	1	
	Dielectric		16.14 mil
5	Power	1	
	Dielectric		3.805 mil
6	Power	0.5	
	Dielectric		3.94 mil
7	GND	1	
	Dielectric		2.611 mil
8	Signal	0.333 + plating	
Finished:	47.244(4.724/-4.724) mil		1.2(+0.12/-0.12) MM
Designed:	43.858 mil		1.114 MM
Material:	TU768		TU768

Table 9. 8MMINI-BB board stack-up information

Layer	Description	Copper (Oz.)	Dielectric thickness (mil)
1	Signal	0.5 + plating	
	Dielectric		2.717 mil
2	GND	1	
	Dielectric		4.33 mil
3	Signal	1	
	Dielectric		11.085 mil
4	Power	1	
	Dielectric		14.170 mil
5	Power	1	
	Dielectric		11.415 mil
6	Signal	1	
	Dielectric		4.33 mil
7	GND	1	
	Dielectric		2.717 mil
8	Signal	0.5 + plating	
Finished:	62.992(6.299/-6.299) mil		1.6(+0.16/-0.16) MM
Designed:	59.173 mil		1.503 MM
Material:	TU768		TU768

3.1. EVK design files

You can download the schematics, layout files, gerber files, and BOM at www.nxp.com/imx8mminievk.

4. Errata

Silkscreen: There is a wrong silkscreen on the board. SW1101 bit[9:10] for the eMMC/SDHC3 boot should be 01 instead of 10.

Description: 01 means 8-bit bus width, while 10 means 4-bit bus width. It only impacts the eMMC bus width during the ROM booting. The U-Boot, kernel, and system functionality are not impacted.

Affected boards: X-8MMINILPD4-EVK (with base board 700-31407 REV X5), 8MMINILPD4-EVK (with base board 700-31407 REV A).

Workaround: Follow the quick start guide or hardware user's guide to correct the SW1101 switch settings for the eMMC/SDHC3 boot.

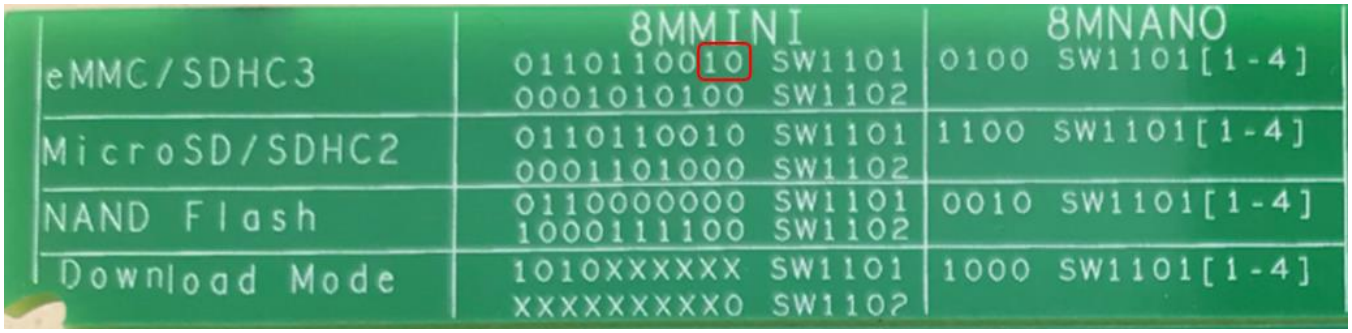

Figure 8. Boot configuration silkscreen

5. Revision history

Table 10. Revision history

Revision number	Date	Substantive changes
0	02/2019	Initial release.
1	05/2019	Corrected Table 1. Corrected Table 6.

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