

Kepad-HDMI Interface

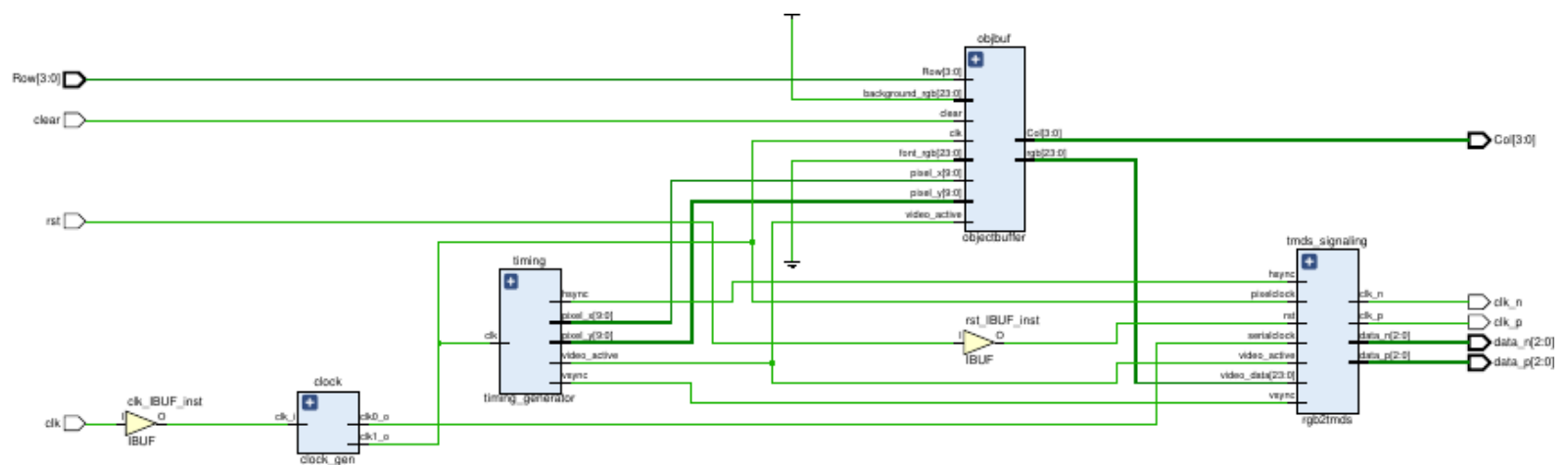
1) Problem Description

This project aims at building a HDMI and keypad interface using Digilent Zybo Board. Keypad input is given using **Pmod Keypad through Pmod port on Zybo**. HDMI Output on the board is connected to a **5 inch 800x480 screen**.

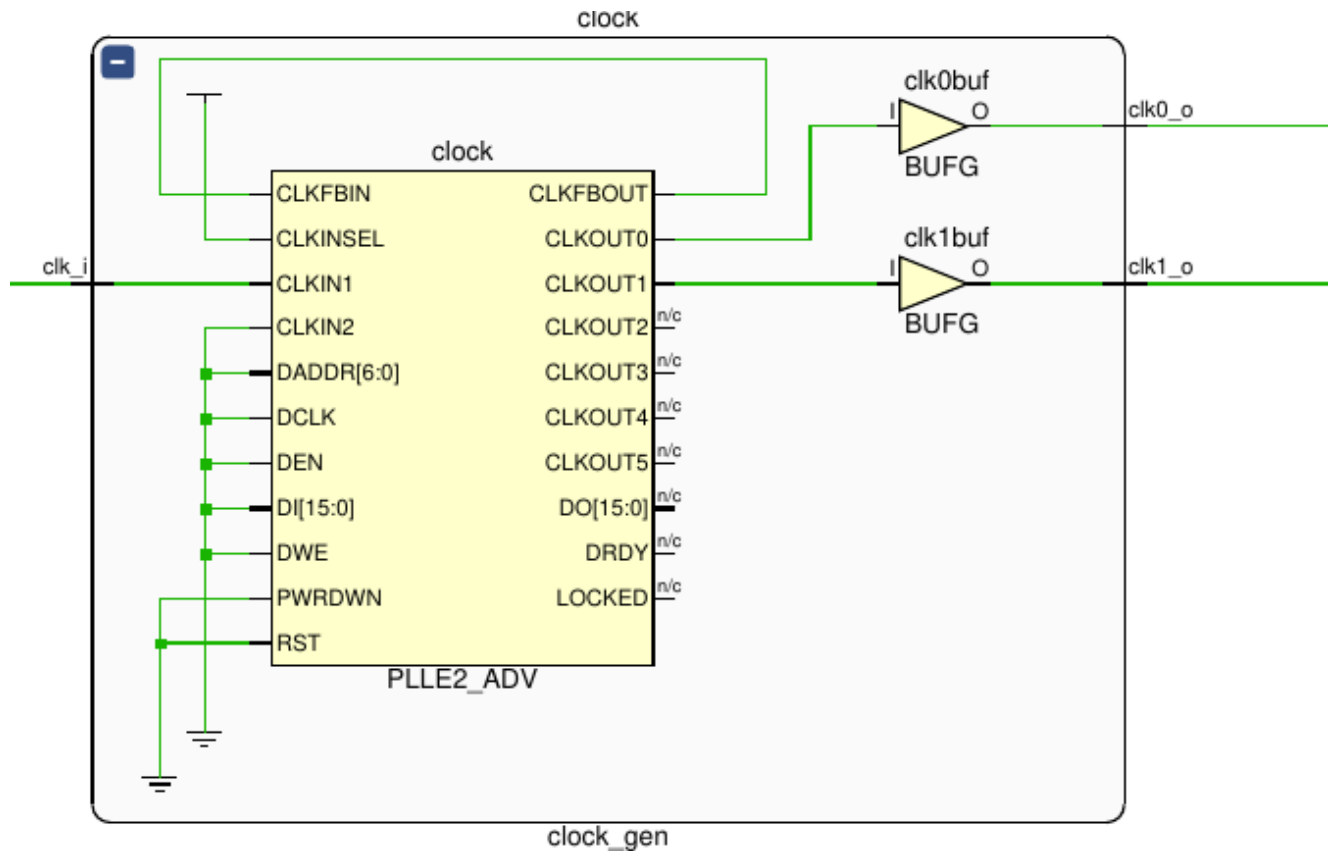
Keypad has 4 rows and 4 columns having 16 keys representing hex characters from **0 to F**. HDMI Display Screen is divided into 20 x 6 display keeping Font Size of 40 x 80 for each character. Initially, screen is blank with white background. On each key press, a character is added to the right of last charcater, Text font color is black.

Reset button resets the screen. Clear button clears the sreen.

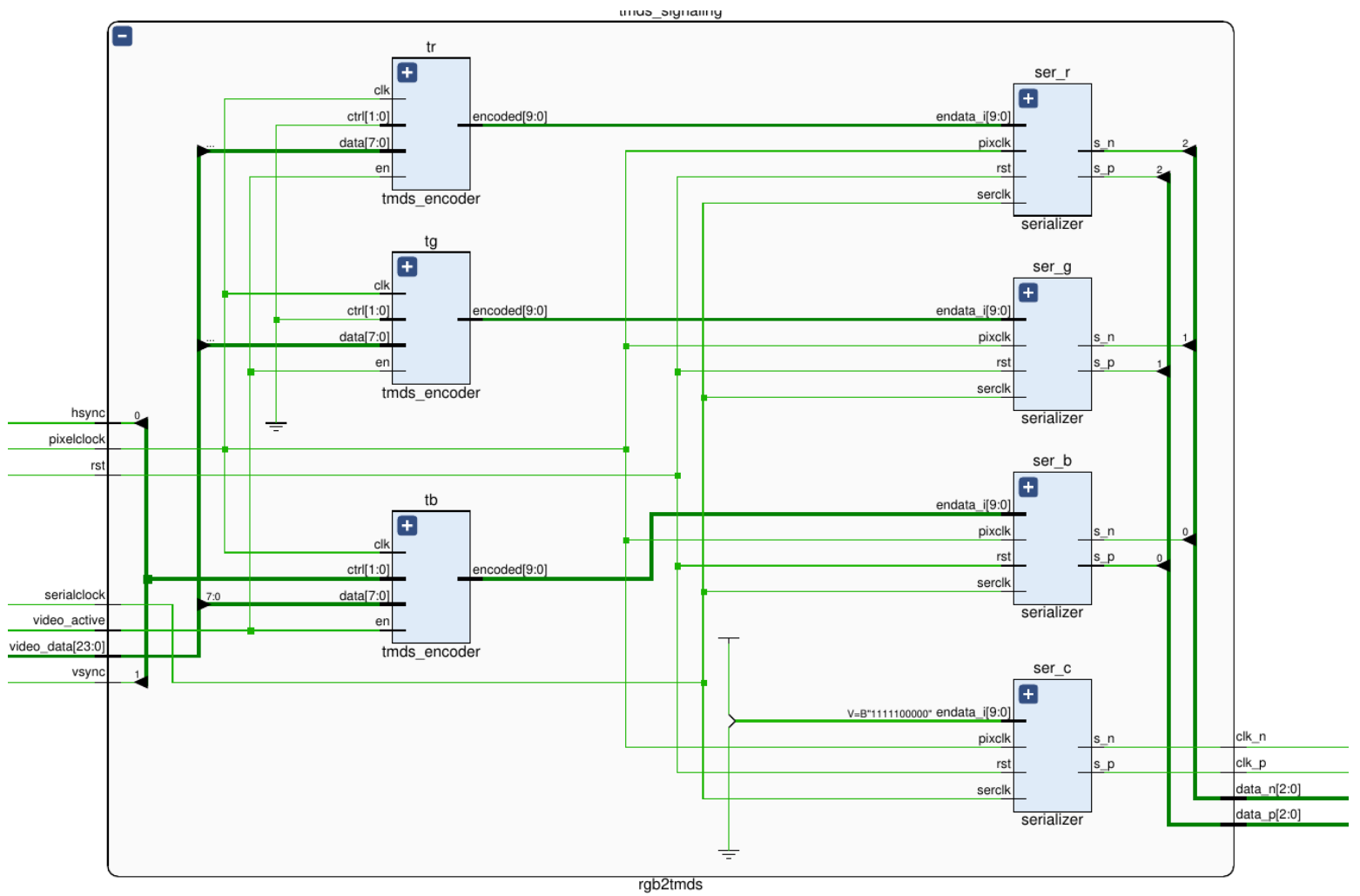
2) Functional Diagram (Architecture)



Clock (Pixel Clock and Serial Clock) Generation using PLL



TMDS Encoder with Serialiser



The schematic diagram illustrates a 10-bit serial-to-parallel converter. It is enclosed in a block labeled 'serializer' with a 'ser_r' input. The circuit consists of two OSERDESE2 blocks, one labeled 'slave' and one labeled 'master'. The 'slave' block has inputs for CLK, CLKDIV, D1-D8, OCE, RST, SHIFTIN1, SHIFTIN2, TBYTEIN, TCE, and T1-T4. Its outputs are OFB (n/c), OQ (n/c), SHIFTOUT1, SHIFTOUT2, TBYTEOUT, TFB (n/c), and TO (n/c). The 'master' block has inputs for CLK, CLKDIV, D1-D8, OCE, RST, SHIFTIN1, SHIFTIN2, TBYTEIN, TCE, and T1-T4. Its outputs are OFB (n/c), OQ, SHIFTOUT1, SHIFTOUT2, TBYTEOUT, TFB (n/c), and TO (n/c). The OQ output of the 'slave' block is connected to the SHIFTIN1 input of the 'master' block. The OQ output of the 'master' block is connected to an OBUFDS block. The OBUFDS block has inputs for O and CB, and outputs for S_n and S_p. The S_n and S_p outputs are connected to the data_n and data_p signals, respectively. The data_n signal is also connected to the data_n input of the 'serializer' block. The data_p signal is connected to the data_p input of the 'serializer' block. The data_n and data_p signals are also connected to the data_n and data_p inputs of the 'serializer' block. The data_n and data_p signals are also connected to the data_n and data_p inputs of the 'serializer' block.

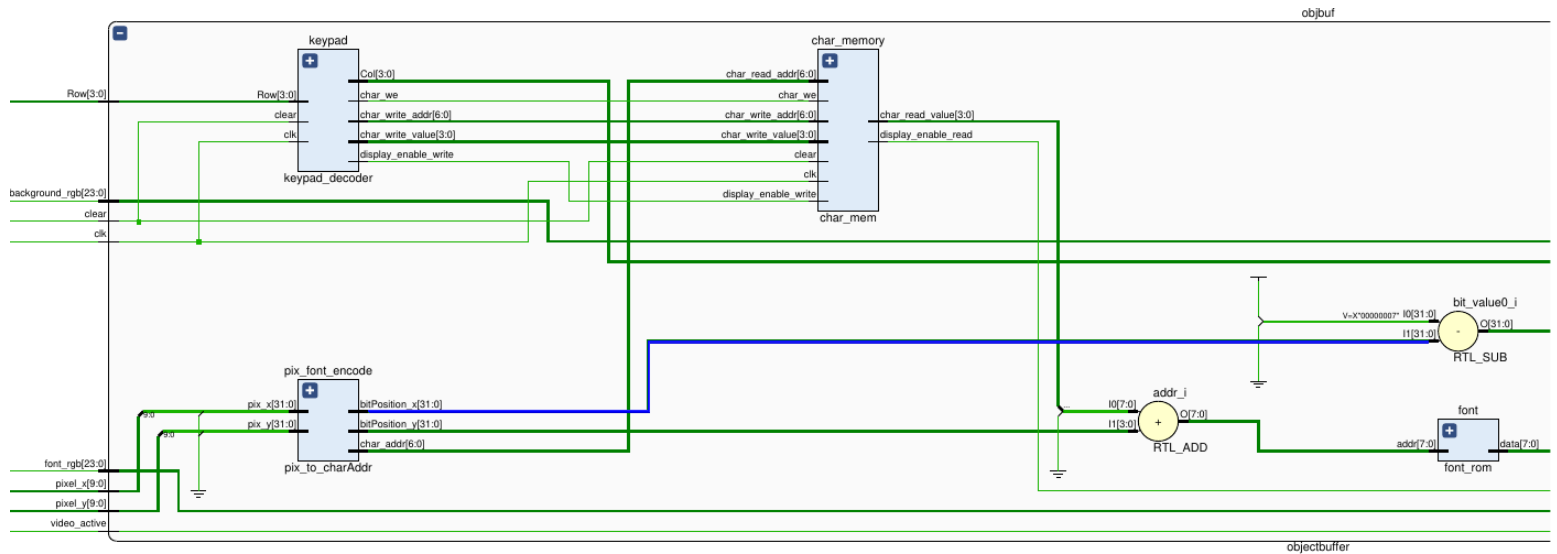
The diagram illustrates the internal connections of the character memory module. It features three main components: a keypad, a display_decoder, and a char_memory block.

- Keypad:** Provides inputs Col[3:0], char_we, char write addr[6:0], char write value[3:0], and display_enable_write.
- display_decoder:** Provides inputs char_read_addr[6:0], char we, char write addr[6:0], char write value[3:0], clear, clk, and display_enable_write.
- char_memory:** A memory block with a '+' symbol, receiving inputs from the keypad and display_decoder, and outputting char read value[3:0] and display_enable_read.

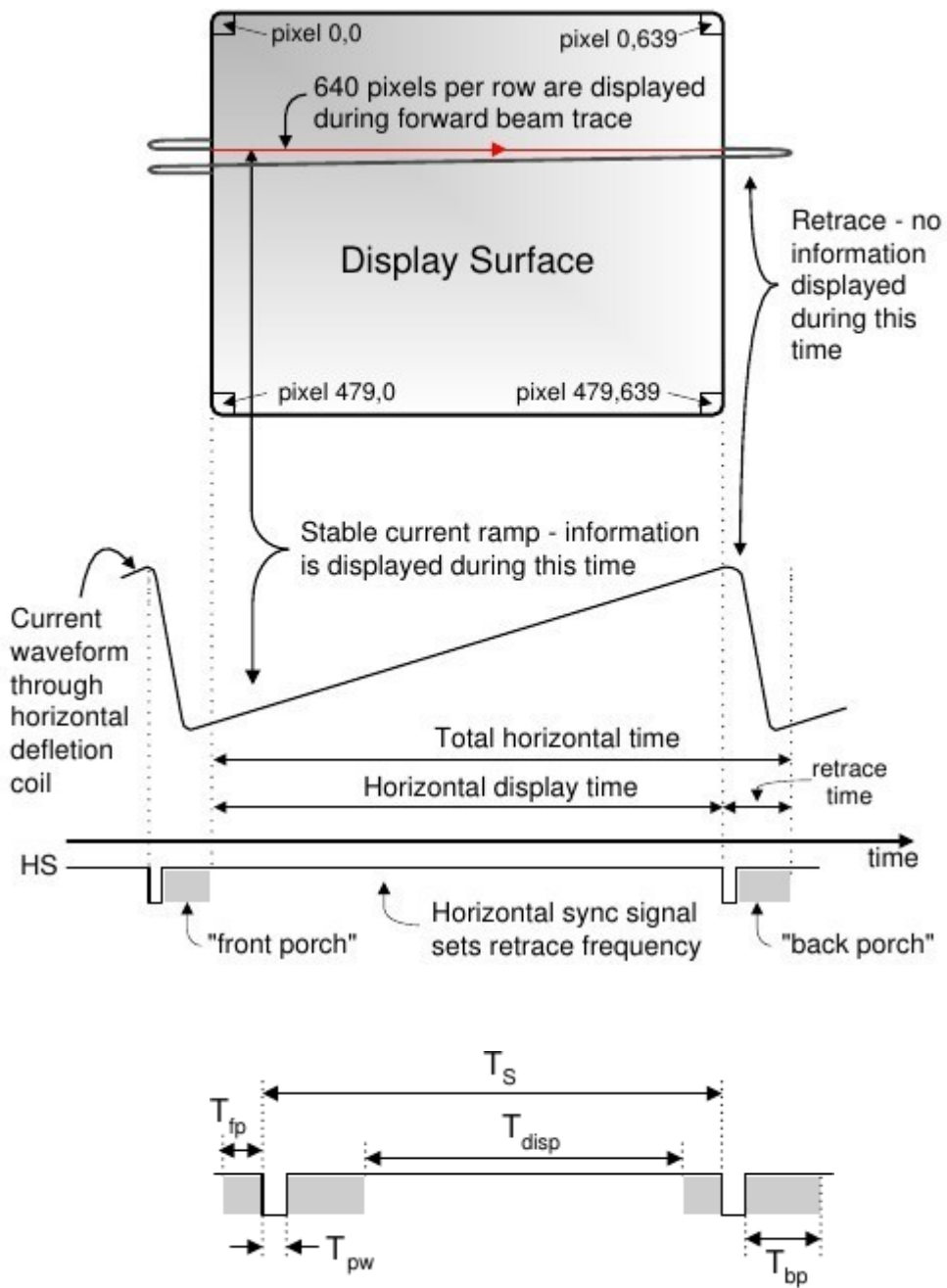
The connections are as follows:

- Keypad Col[3:0] connects to char_read_addr[6:0] of char_memory.
- Keypad char_we connects to char we of char_memory.
- Keypad char write addr[6:0] connects to char write addr[6:0] of char_memory.
- Keypad char write value[3:0] connects to char write value[3:0] of char_memory.
- Keypad display_enable_write connects to display_enable_write of char_memory.
- display_decoder char_read_addr[6:0] connects to char_read_addr[6:0] of char_memory.
- display_decoder char we connects to char we of char_memory.
- display_decoder char write addr[6:0] connects to char write addr[6:0] of char_memory.
- display_decoder char write value[3:0] connects to char write value[3:0] of char_memory.
- display_decoder clear connects to clear of char_memory.
- display_decoder clk connects to clk of char_memory.
- display_decoder display_enable_write connects to display_enable_write of char_memory.
- char_memory char read value[3:0] connects to display_enable_read of char_memory.

Data mapping to each pixel address generated by timing generator at each pixel (after each pixel clock)



3) Timing Diagrams



For 800 x 480 screen,

For **Hsync**,

$T_{fp} = 40$ clock cycles ;

$T_{pw} = 48$ clock cycles ;

$T_s = 928$ clock cycles;
 $T_{disp} = 800$ clock cycles;
 $T_{bp} = 40$ clock cycles;

For Vsync,

$T_{fp} = (13 * 928)$ clock cycles ;
 $T_{pw} = (3 * 928)$ clock cycles ;
 $T_s = (525 * 928)$ clock cycles;
 $T_{disp} = (400 * 928)$ clock cycles;
 $T_{bp} = (29 * 928)$ clock cycles;

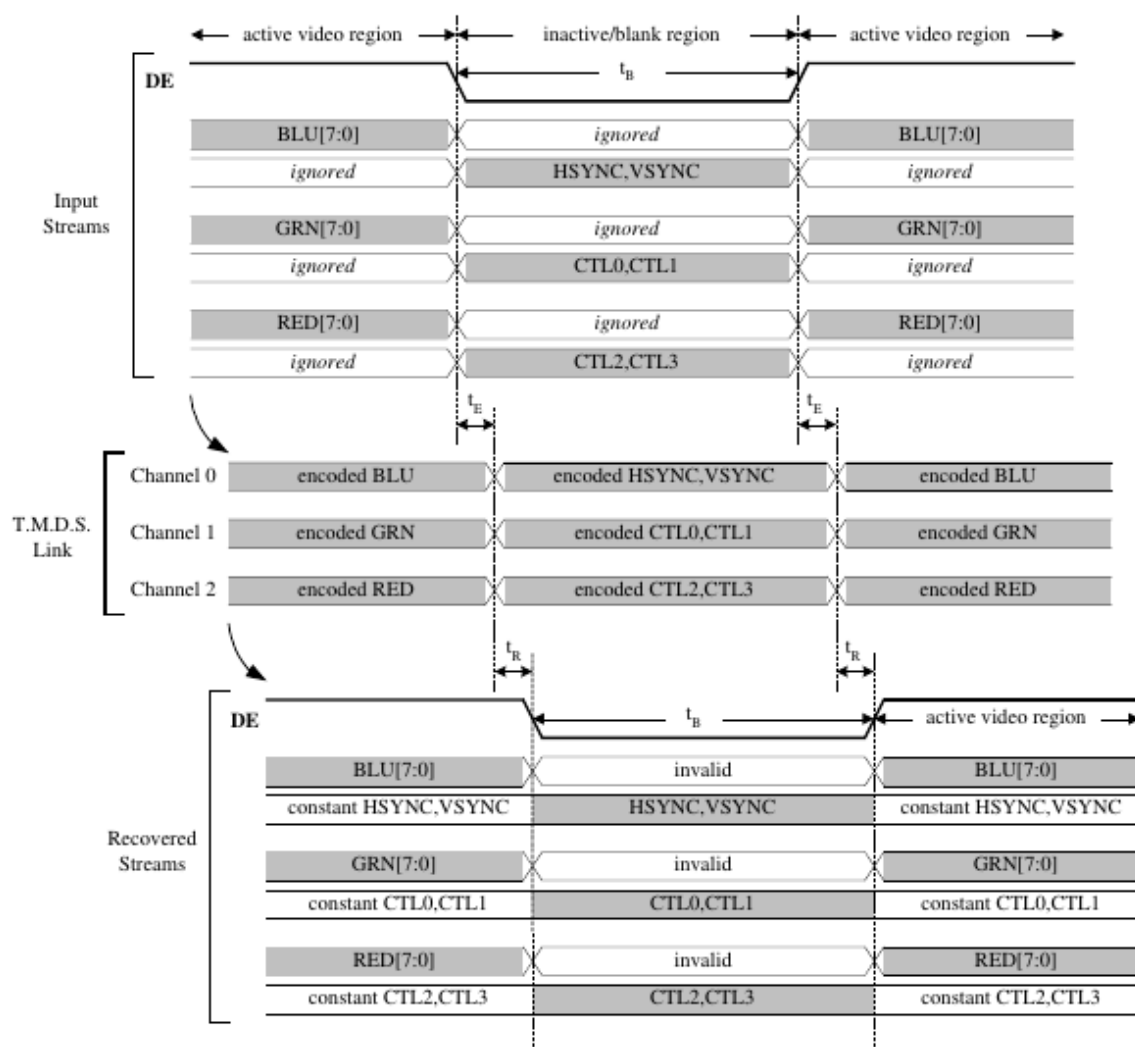
At refresh rate of 60 Hz, clock cycles required is $928 \times 525 \times 60 = 29232000$;

So, pixel clock is set to 30 Mhz.

Each pixel has 24 bits of data which is encoded into 30 bits of data. This is serialised to 3 different channels. So, serial clock should be able to support 10 times data rate and pixel clock. So, 5 times the pixel clock is chosen as serial clock frequency along with DDR (double data rate).

TMDS Link Timing Requirements

The maximum time for encode and serialization and decode is specified in order to bound latency across the interface. Figure 3-7 with Table 3-2 specifies these parameters.



Symbol	Description	Value	Unit
t_B	Minimum duration blanking period required to ensure character boundary recovery at the receiver. Blanking periods of this duration must occur at least once every 50 mS (20 Hz).	128	T_{pixel}
t_E	Maximum encoding/serializer pipeline delay	64	T_{pixel}
t_R	Maximum recovery/de-serializer pipeline delay. Recovery timing includes inter-channel skew, and is measured from the earliest DE transition among the data channels.	64	T_{pixel}

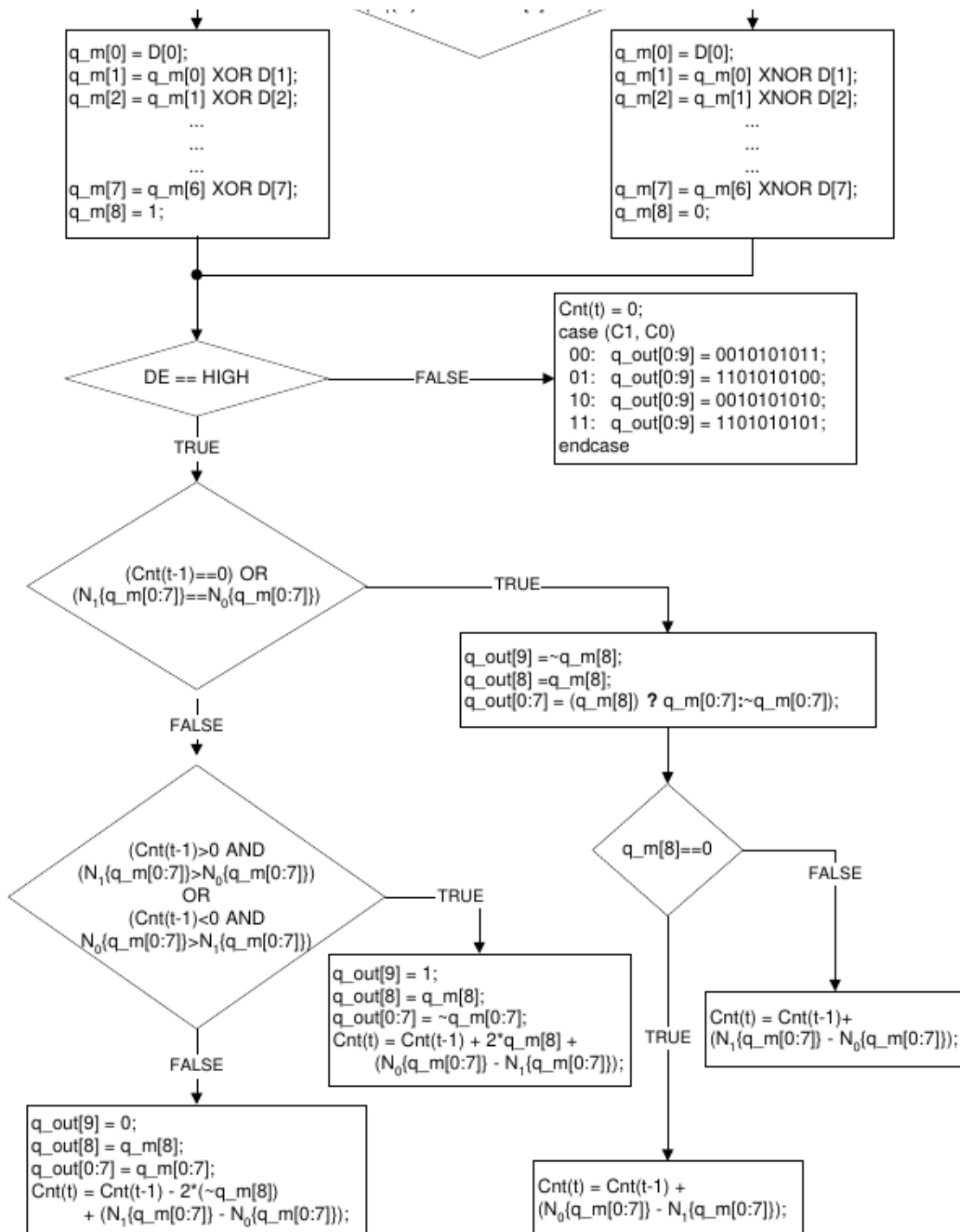
TMD5 Encoding Algorithm

The encoder produces four unique 10-bit characters during blanking and one of 460 unique 10-bit characters during active data. Use of all other 10-bit characters over the link is reserved and must not be generated by the encoder.

D, C0, C1, DE	The encoder input data set. D is eight-bit pixel data, C1 and C0 are the control data for the channel, and DE is data enable
cnt	This is a register used to keep track of the data stream disparity. A positive value represents the excess number of "1"s that have been transmitted. A negative value represents the excess number of "0"s that have been transmitted. The expression $\text{cnt}\{t-1\}$ indicates the previous value of the disparity for the previous set of input data. The expression $\text{cnt}(t)$ indicates the new disparity setting for the current set of input data.
q_out	These 10 bits are the encoded output value.
$N_1\{x\}$	This operator returns the number of "1"s in argument "x"
$N_0\{x\}$	This operator returns the number of "0"s in argument "x"

Table 3-1 Encoding Algorithm Definitions

The stream of T.M.D.S. characters produced by the encoder is serialized for transmission on the T.M.D.S. data channel. The least significant bit of each character ($q_out[0]$) is the first bit to be transmitted.



Font ROM: The appearance of the characters on the screen is determined by a "font ROM". The font ROM contains the pattern of pixels that should be displayed on the screen when a particular character needs to be displayed. The bits within the font ROM indicate which pixels of a 8 x 16 bit tile should be displayed in the 'foreground' and which pixels on the display should be displayed in the background. A '1' in the font ROM indicates the corresponding pixel should be displayed in the foreground (i.e., white

in our case) while a '0' in the font ROM indicates that the corresponding pixel should be blanked or put in the background (black in our case). The text below demonstrates the contents of the font ROM for the upper-case character 'A':

```
"00000000", -- 0
"00000000", -- 1
"00010000", -- 2      *
"00111000", -- 3      ***
"01101100", -- 4      **  **
"11000110", -- 5      **    **
"11000110", -- 6      **    **
"11111110", -- 7      *
"11000110", -- 8      **    **
"11000110", -- 9      **    **
"11000110", -- a      **    **
"11000110", -- b      **    **
"00000000", -- c
"00000000", -- d
"00000000", -- e
"00000000", -- f
```

Character Memory: In addition to the font ROM, we use a "character memory" that stores the character value at each of the 20x6 character locations on the display. The minimum size of this memory is 20x6x4 bits to provide enough room to store characters (one nibble each) for each of the 20 columns and 6 rows.

This memory has two memory ports: a character read port and a character write port. The read port is needed by the character generator to read the character value of the current character location. The write port is used to update the content of the character display.

The **char_read_addr** port is a 7 bit signal used to determine which location in the character memory to read. The result of the read is available on the **char_read_value**. Like the font ROM, this character ROM will provide the character result one clock cycle after the address is provided.

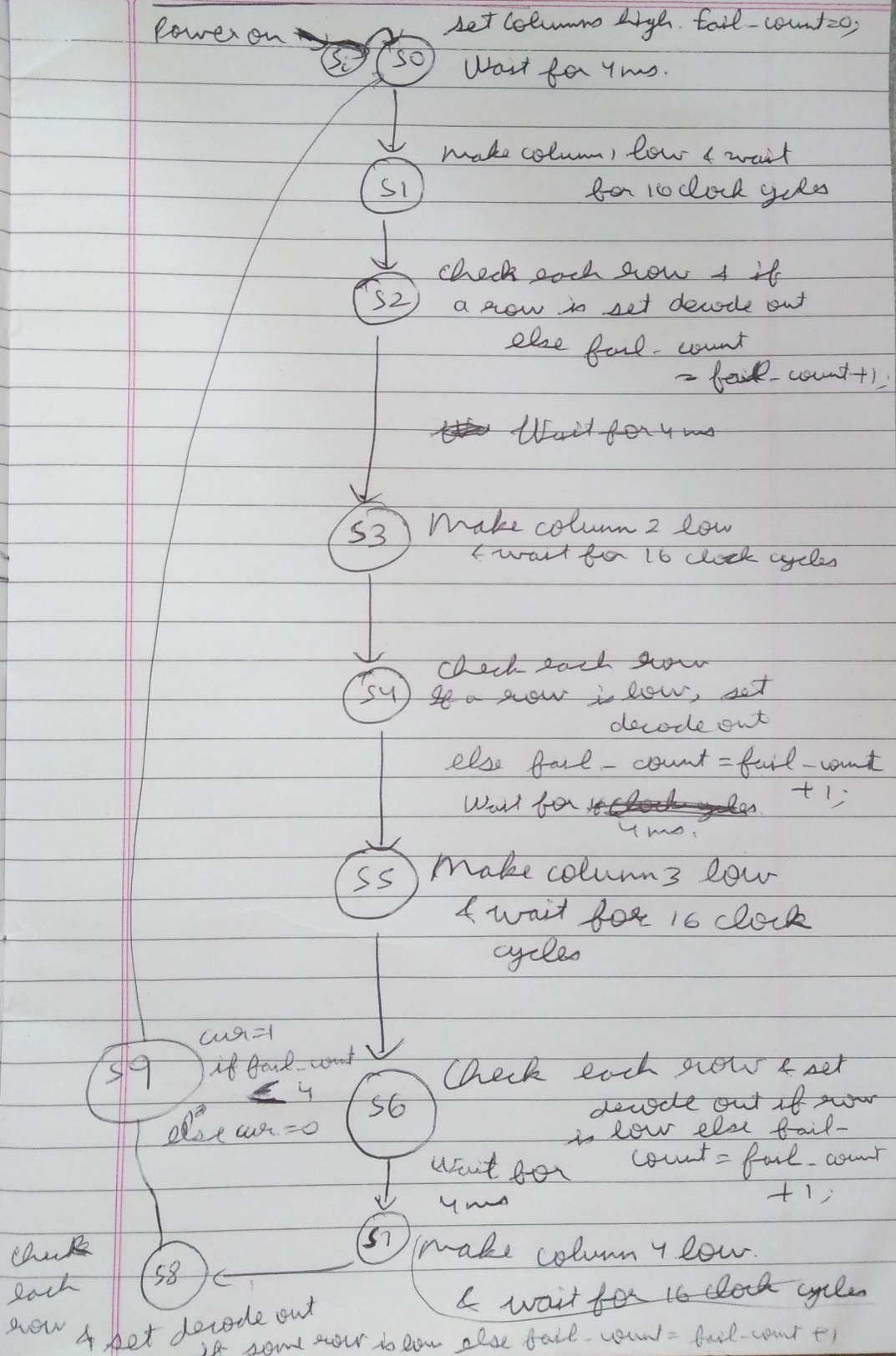
The second memory port is the character write port. This write port is used to update the contents of the character memory so the display can be changed. This port operates simultaneously with the read port so the character display can access characters while the character memory is being updated. Three signals are used for this port. The **char_write_addr** signal is used to indicate the address within the character memory that will be updated. The **char_write_value** is the value that will be written at this address. The **char_we** signal is the control signal to enable a write into the character memory. When the char_we signal is asserted, the value on the char_write_value signal will be written at address char_write_addr at the next clock edge.

Character Memory is used to give video_data to TMDS signal generator.

4) State Diagram for Keyboard Input

Keypad Input State Diagram

Date	
Page	



After each 4 ms, a column is made low. Then, each row is checked for low signal. Corresponding after each 16 ms, it is recorded whether a key was pressed. Then, cur state is recorded. If last state was not key pressed and cur state is key pressed, then keypad writes to character memory.

5)Timing Analysis

System Clock

System Clock (Time Period) = 8 ns;

Worst Negative Slack (Pulse width) = 2 ns

Pixel Clock

Pixel Clock (Time Period= 33.33 ns

Worst Negative Slack (Setup) = 5.44 ns

Worst Negative Slack (Hold) = 0.177 ns

Worst Negative Slack (Pulse width) = 16.167 ns

Serial Clock

Serial Clock (Time Period) = 6.66 ns;

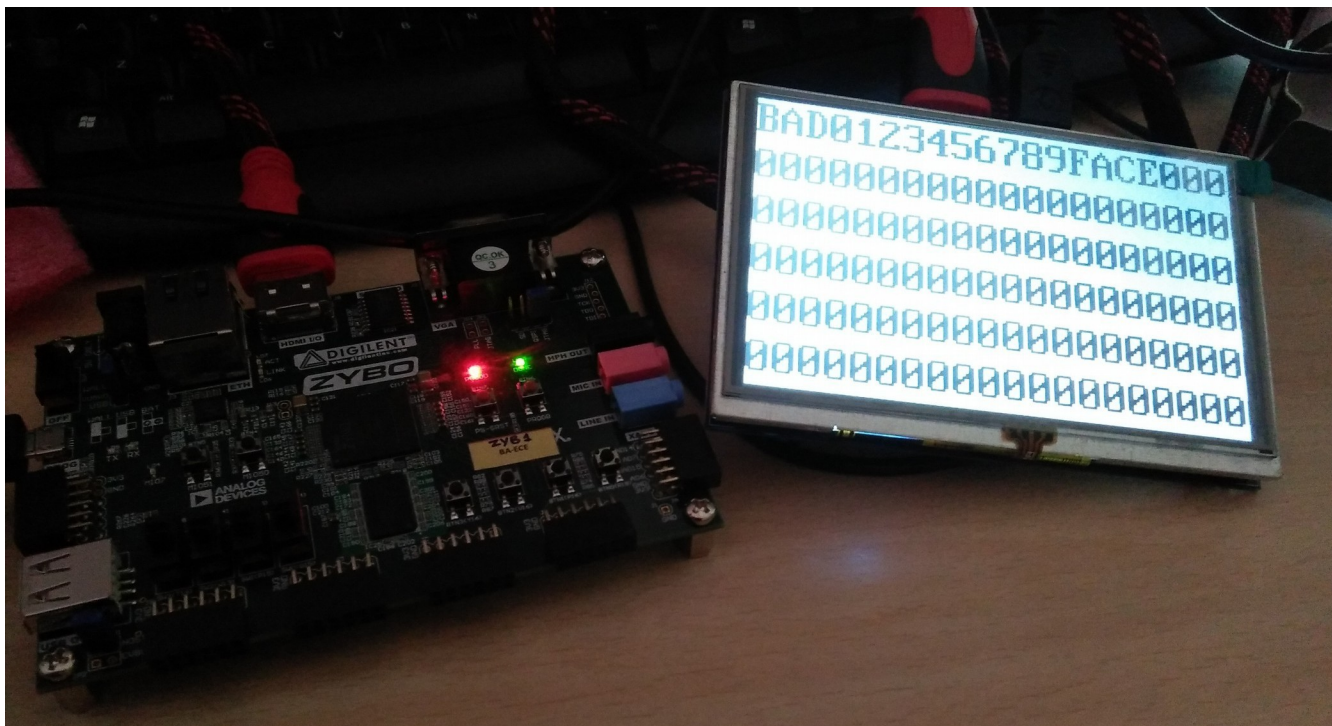
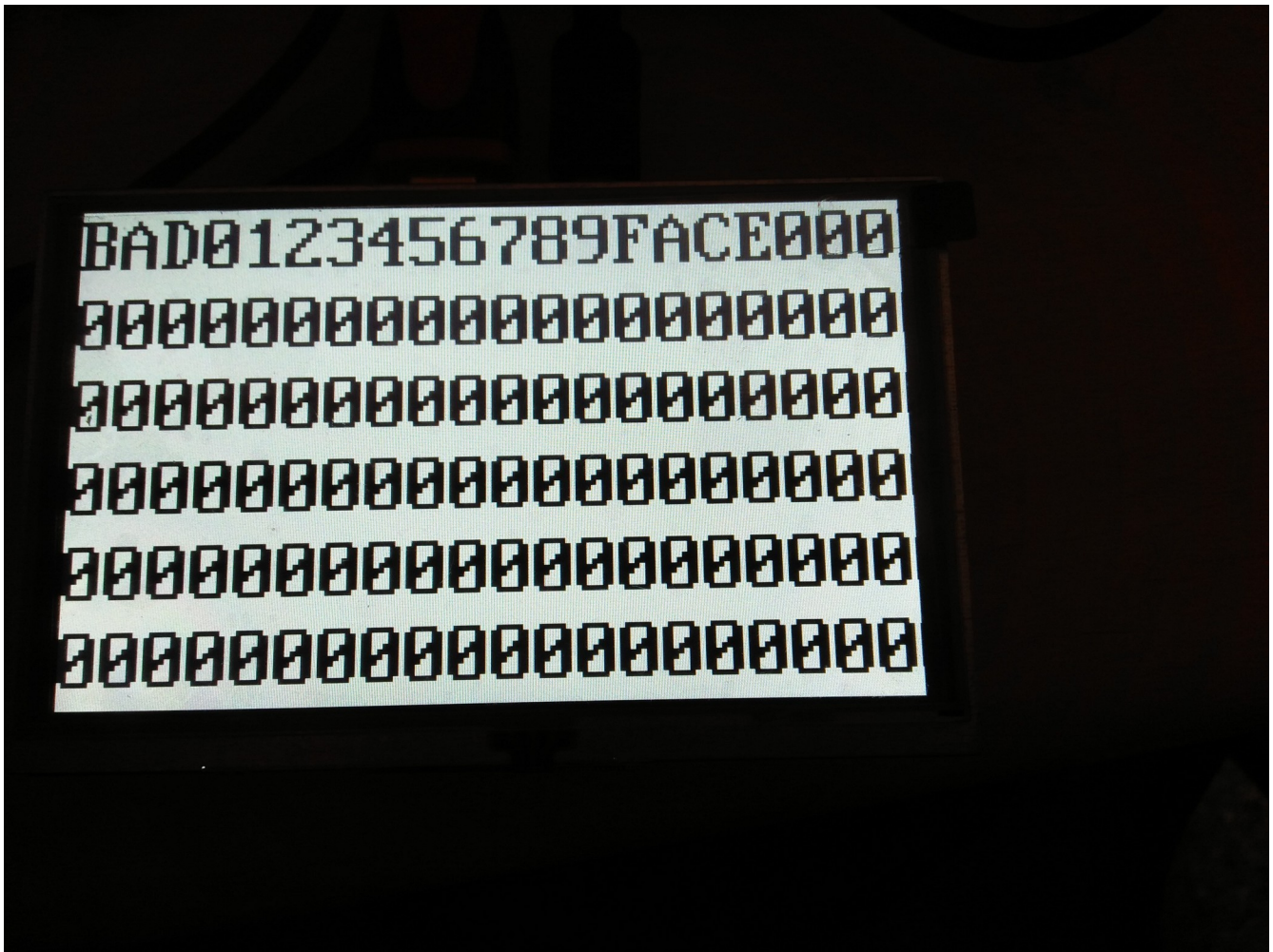
Worst Negative Slack (Pulse width) = 4.511 ns

Resource Utilisation

LUTs = 1189

FFs = 690

6) Results on Board (HDMI Display)



Conclusion

20 x 6 Text Displaying hex characters was implemented using Zybo board HDMI Output printing characters on screen taking input from Pmod Keypad.

References

- 1) Digital Visual Interface – www.ddwg.org
- 2) VGA Text Generator-
https://ece320web.groups.et.byu.net/labs/VGATextGeneration/VGA_Terminal.html