

NE 205: Semiconductor Devices and IC Technology
Indian Institute of Science, Bangalore.
Autumn Semester 2019, Digbijoy N. Nath
Homework V Total points: 40

1. Calculate the shift in the flat band voltage of an MOS capacitor if an oxide charge of $+10^{11} \text{ cm}^{-2}$ is 3x4 = 12

- a) at the Si/SiO₂ interface
- b) uniformly distributed throughout the oxide
- c) at the gate/SiO₂ interface
- d) exactly at the middle of the oxide layer

2. Consider an n-channel MOSFET at room temperature made from p-doped silicon substrate. C-V measurements are done on the MOS capacitor. It is found from the low-frequency measurements that the maximum and the minimum capacitances per unit area are $1.72 \times 10^{-7} \text{ F/cm}^2$ and $2.9 \times 10^{-8} \text{ F/cm}^2$ respectively. The channel mobility is $600 \text{ cm}^2/\text{Vs}$, and the gate length is $1.5 \text{ }\mu\text{m}$ while the gate width is $50 \text{ }\mu\text{m}$. [Assume that the minimum capacitance corresponds to the largest depletion thickness.]

- a) Calculate the oxide thickness
- b) Estimate the p-doping in the channel
- c) Calculate the channel current at saturation when the gate bias is $V_{\text{Th}} + 1.5 \text{ V}$

2 + 4 + 4 = 10

3. The threshold for an n-channel MOSFET was defined when strong inversion occurs, i.e.

$$V_{\text{th}} = \psi_s = 2\psi_b = 2(E_i - E_F)$$

Consider another new criterion in which we say that inversion occurs when the electron density in the channel at the Si/SiO₂ interface becomes 10^{16} cm^{-3} . Calculate the gate threshold voltage needed for an MOS device with the following parameters for the two different criteria: 8

Oxide thickness = 50 nm,

$$\Phi_{\text{ms}} = 1 \text{ V}$$

$$N_A = 10^{13} \text{ cm}^{-3}$$

4. Consider an n-channel MOSFET made from p-doped silicon ($N_A = 10^{16} \text{ cm}^{-3}$) at 300 K. The source and drain contacts are Ohmic (negligible resistance) and are made from n+-doped regions. The other parameters are –

$V_{\text{FB}} = -1 \text{ V}$, electron mobility = 500, hole mobility = 100, gate length = $2 \text{ }\mu\text{m}$, gate width = $20 \text{ }\mu\text{m}$, oxide thickness = 50 nm.

- a) Calculate the channel conductivity near the Si/SiO₂ interface under flat band condition and at inversion. Use $V_{th} = \psi_s = 2\psi_b$ for inversion
- b) Calculate the electron and hole densities at the Si/SiO₂ interface on the source and drain sides of the gate when $V_G = V_{th} + 0.5 \text{ V}$, and $V_{DS} = 1 \text{ V}$.
- c) If the gate bias is such that Si bands are flat, estimate the current density in the channel for a drain bias of 1 V.