UNIVERSITY OF TEHRAN

Electrical and Computer Engineering Department

Digital Logic Design, ECE 367, Fall 1396

Computer Assignment 5

RTL Design Datapath Controller – Complete Design

Name:	**Date:**
Username:	

Complete arithmetic core design: An arithmetic circuit with simple basic handshaking is to be designed here. Design a sequential circuit for calculating *n*-factorial, where *n* is an 8-bit integer, and the result is a 32-bit integer.

The circuit has a 1-bit *start* input, an 8-bit *nBus* input, a 1-bit *done* output, and a 32-bit *nfBus* data output. When a complete positive pulse appears on *start*, the 8-bit data will be read from the *nBus* and factorial calculation begins. When completed, the *done* output becomes 1 indicating that the output bus has a valid factorial value of the input. This signal remains asserted until the next calculation is to start.

Since in many cases, factorial calculations are to be done for consecutive numbers, our factorial calculation device always keeps the information about its most recent calculation, and if the next calculation is for a number above the previous calculation, it can calculate the new factorial in just a few steps without having to start from number 1.

In addition to its data output, the circuit also has an output indicating the number of clock cycles it has taken for a factorial calculation.

Design Phase:

1. Show the schematic diagram of the datapath part of this factorial circuit
2. Show the controller state diagram
3. Implement the datapath in Quartus II using available library components. Use a module with multiplication operator for multiplication, or use a combinational multiplier from Quartus II.
4. Write Controller Verilog description and synthesize it as a component, and generate a symbol for it.
5. Wire the controller symbol with the datapath to build the complete factorial circuit in Quartus II.
6. Produce post-synthesis Verilog file (.vo) and perform post-synthesis simulation in a ModelSim testbench.

Implementation Phase:

1. Build the datapath in Quartus II using predefined Altera components, Verilog modules, or discrete parts.
2. Generate a symbol for the factorial controller from its Verilog description.

3. Generate the complete factorial design by instantiating its datapath and controller.
4. Synthesize the factorial circuit and generate its .vo and .sdo files.
5. In a testbench, test your divider.