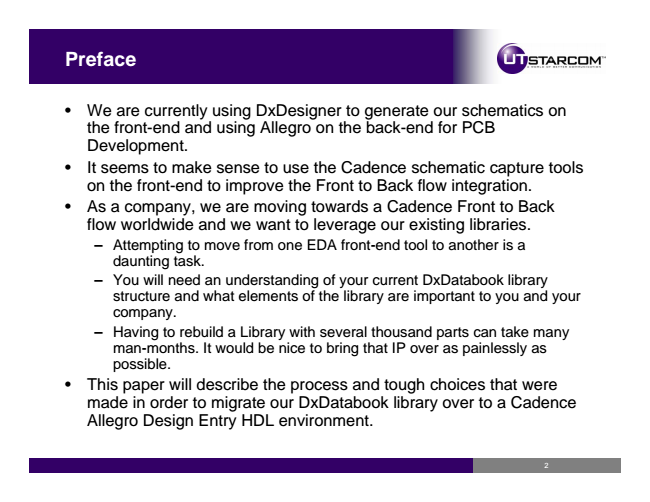


**Silicon Valley 2007 September 10-12, 2007 San Jose, CA**

**Migrating a DxDesigner Library to Allegro Design Entry HDL**

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**Preface**

• We are currently using DxDesigner to generate our schematics on the front-end and using Allegro on the back-end for PCB Development.

• It seems to make sense to use the Cadence schematic capture tools on the front-end to improve the Front to Back flow integration.

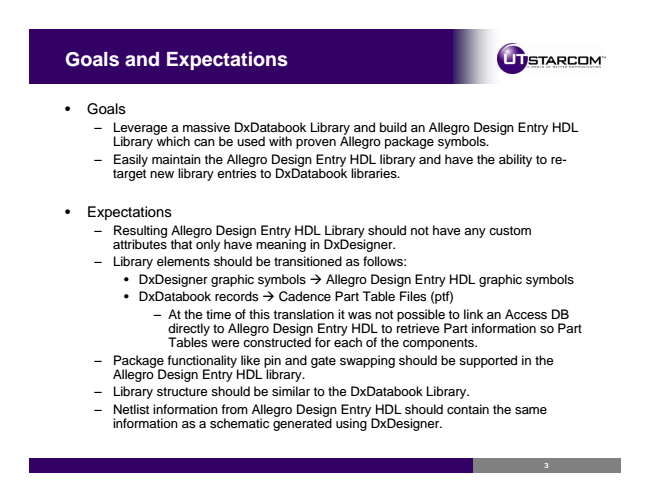
• As a company, we are moving towards a Cadence Front to Back flow worldwide and we want to leverage our existing libraries. – Attempting to move from one EDA front-end tool to another is a

daunting task. – You will need an understanding of your current DxDatabook library

structure and what elements of the library are important to you and your company. – Having to rebuild a Library with several thousand parts can take many man-months. It would be nice to bring that IP over as painlessly as possible.

• This paper will describe the process and tough choices that were made in order to migrate our DxDatabook library over to a Cadence Allegro Design Entry HDL environment.

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**Goals and Expectations**

• Goals

– Leverage a massive DxDatabook Library and build an Allegro Design Entry HDL

Library which can be used with proven Allegro package symbols. – Easily maintain the Allegro Design Entry HDL library and have the ability to re-

target new library entries to DxDatabook libraries.

• Expectations

– Resulting Allegro Design Entry HDL Library should not have any custom

attributes that only have meaning in DxDesigner. – Library elements should be transitioned as follows:

• DxDesigner graphic symbols → Allegro Design Entry HDL graphic symbols

• DxDatabook records → Cadence Part Table Files (ptf)

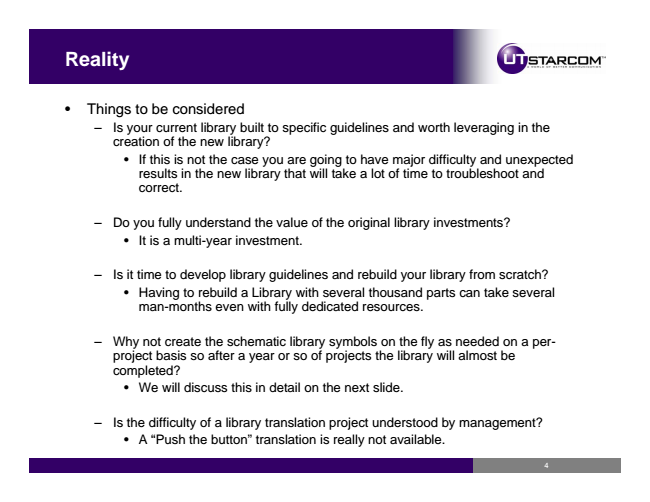
– At the time of this translation it was not possible to link an Access DB

directly to Allegro Design Entry HDL to retrieve Part information so Part Tables were constructed for each of the components. – Package functionality like pin and gate swapping should be supported in the

Allegro Design Entry HDL library. – Library structure should be similar to the DxDatabook Library. – Netlist information from Allegro Design Entry HDL should contain the same

information as a schematic generated using DxDesigner.

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**Reality**

• Things to be considered

– Is your current library built to specific guidelines and worth leveraging in the

creation of the new library?

• If this is not the case you are going to have major difficulty and unexpected results in the new library that will take a lot of time to troubleshoot and correct.

– Do you fully understand the value of the original library investments?

• It is a multi-year investment.

– Is it time to develop library guidelines and rebuild your library from scratch?

• Having to rebuild a Library with several thousand parts can take several man-months even with fully dedicated resources.

– Why not create the schematic library symbols on the fly as needed on a per-

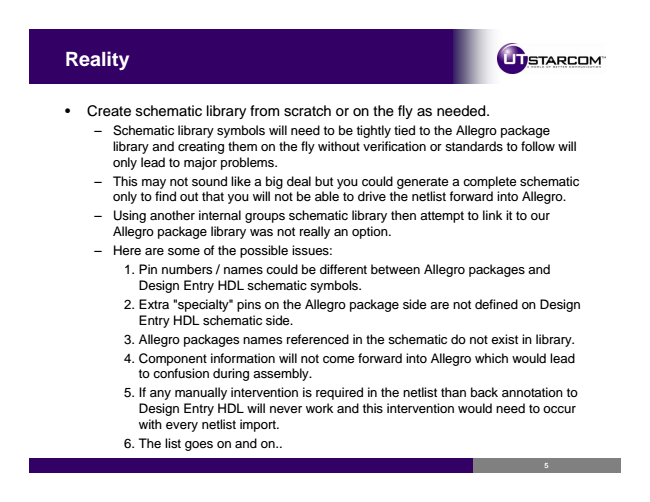
project basis so after a year or so of projects the library will almost be completed?

• We will discuss this in detail on the next slide.

– Is the difficulty of a library translation project understood by management?

• A “Push the button” translation is really not available.

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**Reality**

• Create schematic library from scratch or on the fly as needed.

– Schematic library symbols will need to be tightly tied to the Allegro package

library and creating them on the fly without verification or standards to follow will only lead to major problems. – This may not sound like a big deal but you could generate a complete schematic

only to find out that you will not be able to drive the netlist forward into Allegro. – Using another internal groups schematic library then attempt to link it to our

Allegro package library was not really an option. – Here are some of the possible issues:

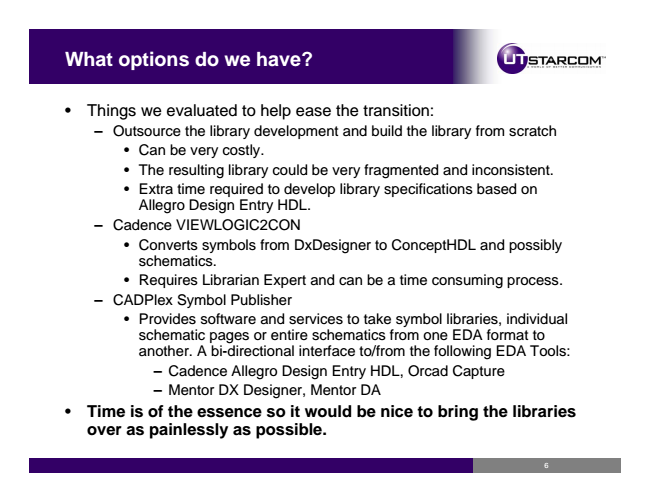
1. Pin numbers / names could be different between Allegro packages and

Design Entry HDL schematic symbols. 2. Extra "specialty" pins on the Allegro package side are not defined on Design

Entry HDL schematic side. 3. Allegro packages names referenced in the schematic do not exist in library. 4. Component information will not come forward into Allegro which would lead

to confusion during assembly. 5. If any manually intervention is required in the netlist than back annotation to Design Entry HDL will never work and this intervention would need to occur with every netlist import. 6. The list goes on and on..

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**What options do we have?**

• Things we evaluated to help ease the transition:

– Outsource the library development and build the library from scratch

• Can be very costly.

• The resulting library could be very fragmented and inconsistent.

• Extra time required to develop library specifications based on Allegro Design Entry HDL. – Cadence VIEWLOGIC2CON

• Converts symbols from DxDesigner to ConceptHDL and possibly schematics.

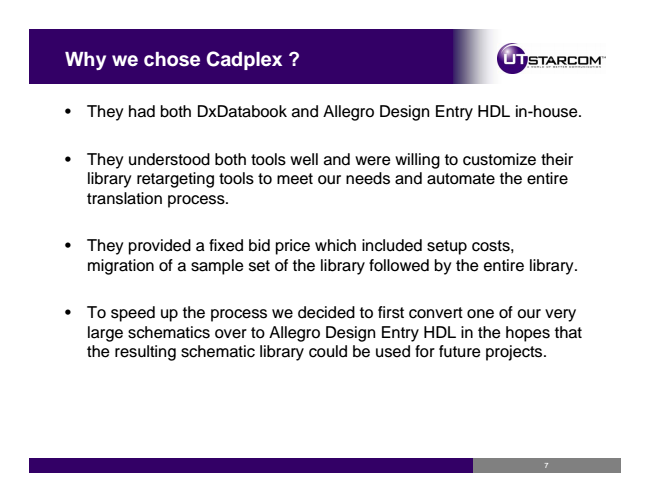
• Requires Librarian Expert and can be a time consuming process. – CADPlex Symbol Publisher

• Provides software and services to take symbol libraries, individual schematic pages or entire schematics from one EDA format to another. A bi-directional interface to/from the following EDA Tools:

– Cadence Allegro Design Entry HDL, Orcad Capture – Mentor DX Designer, Mentor DA

**• Time is of the essence so it would be nice to bring the libraries over as painlessly as possible.**

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**Why we chose Cadplex ?**

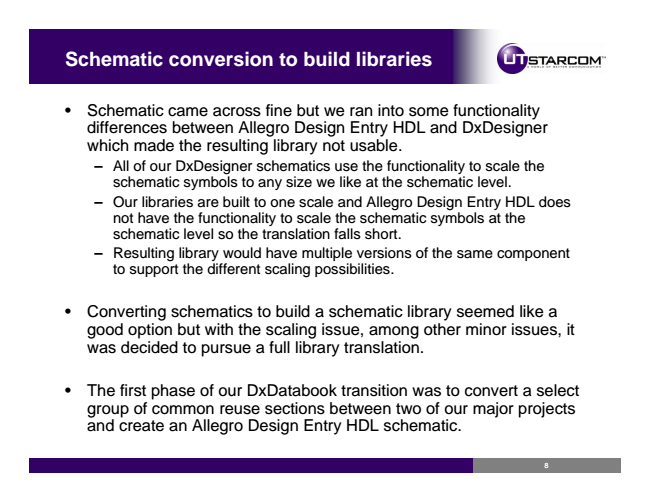
• They had both DxDatabook and Allegro Design Entry HDL in-house.

• They understood both tools well and were willing to customize their library retargeting tools to meet our needs and automate the entire translation process.

• They provided a fixed bid price which included setup costs, migration of a sample set of the library followed by the entire library.

• To speed up the process we decided to first convert one of our very large schematics over to Allegro Design Entry HDL in the hopes that the resulting schematic library could be used for future projects.

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**Schematic conversion to build libraries**

• Schematic came across fine but we ran into some functionality differences between Allegro Design Entry HDL and DxDesigner which made the resulting library not usable.

– All of our DxDesigner schematics use the functionality to scale the

schematic symbols to any size we like at the schematic level. – Our libraries are built to one scale and Allegro Design Entry HDL does

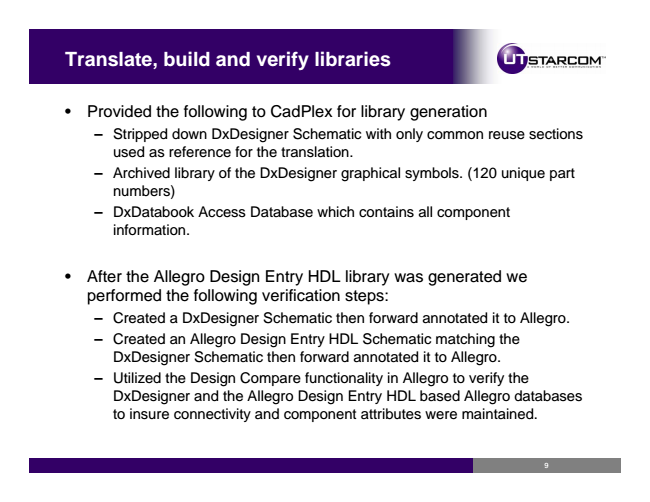
not have the functionality to scale the schematic symbols at the schematic level so the translation falls short. – Resulting library would have multiple versions of the same component

to support the different scaling possibilities.

• Converting schematics to build a schematic library seemed like a good option but with the scaling issue, among other minor issues, it was decided to pursue a full library translation.

• The first phase of our DxDatabook transition was to convert a select group of common reuse sections between two of our major projects and create an Allegro Design Entry HDL schematic.

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**Translate, build and verify libraries**

• Provided the following to CadPlex for library generation

– Stripped down DxDesigner Schematic with only common reuse sections

used as reference for the translation. – Archived library of the DxDesigner graphical symbols. (120 unique part

numbers) – DxDatabook Access Database which contains all component

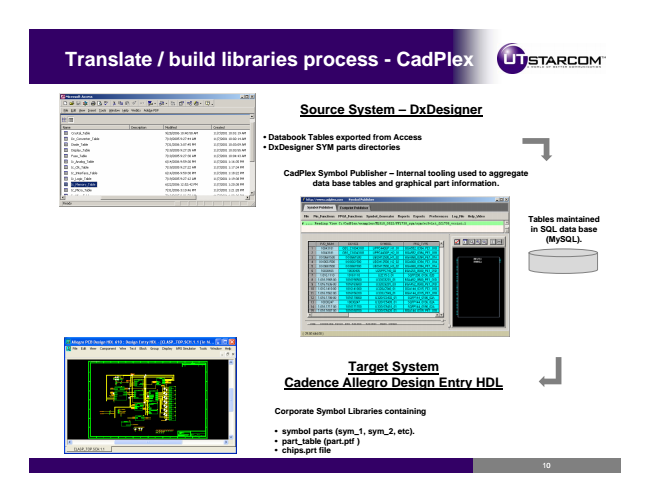
information.

• After the Allegro Design Entry HDL library was generated we performed the following verification steps:

– Created a DxDesigner Schematic then forward annotated it to Allegro. – Created an Allegro Design Entry HDL Schematic matching the DxDesigner Schematic then forward annotated it to Allegro. – Utilized the Design Compare functionality in Allegro to verify the

DxDesigner and the Allegro Design Entry HDL based Allegro databases to insure connectivity and component attributes were maintained.

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**Translate / build libraries process - CadPlex**

**Source System – DxDesigner**

**• Databook Tables exported from Access**

**• DxDesigner SYM parts directories**

**CadPlex Symbol Publisher – Internal tooling used to aggregate data base tables and graphical part information.**

**Tables maintained in SQL data base (MySQL).**

**Target System Cadence Allegro Design Entry HDL**

**Corporate Symbol Libraries containing**

**• symbol parts (sym\_1, sym\_2, etc).**

**• part\_table (part.ptf )**

**• chips.prt file**

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