

Advance Electronic Design

MSE

Matthias Meyer

Exam summary

Switzerland
29. Juni 2023

Inhaltsverzeichnis

1	Intro	4
1.1	Laplace vs Fourier Transform	4
1.2	Thevenin Theorem	4
1.3	Norton equivalent circuit	5
1.4	Bode plot	5
1.4.1	Bode plot of an opamp	6
2	Signal Flow Grapher	8
2.1	Rule of Maison	8
2.1.1	Example	8
3	Noise	11
3.1	Rms Value	11
3.2	Noise figure (NF)	11
3.3	Tangent principle	11
3.4	Measure Noise	11
3.5	Noise at opamps	12
3.5.1	Adding noise	12
3.5.2	Example OP27A	13
3.5.3	Example AD812	14
3.6	Sources of Noise	14
3.6.1	Thermal Noise	14
3.7	Noise Properties	14
3.7.1	Noise Spectra	14
3.7.2	White Noise	15
4	ADC/DAC	16
4.1	DAC	16
4.1.1	binary ADC and DAC	17
4.2	ADC	17
4.2.1	Clock jitter in an ADC	17
4.3	SNR	18
4.3.1	Howland circuit noise	23
5	Analog filters	26
5.1	Second Order	26
5.1.1	low pass filter	26
5.1.2	high pass filter	27
5.1.3	band pass filter	27
5.1.4	KRC filters-or also Sallen-Key filters	27
6	Rectangular filters	28
6.1	Exercises1	30
6.2	Exercises2	30

7 Digital	38
7.1 Calculations of propagation delays on a PCB	38
7.2 Propagation delay calculation with a given dielectric constant ϵ_r	38
7.2.1 Example, what is the t_{PD} in nanoseconds per inch for a given ϵ_r	38
7.2.2 Signal Degradation Effect	38
7.2.3 Signal Degradation Effect	38
7.3 Signalling Methods	41
7.3.1 Isochronous clock free	41
7.3.2 Parallel Signalling vs Serial Signalling	41
7.3.3 Signal encoding	41
7.3.4 Differential Signaling LVDS	41
7.3.5 QAM	41
7.3.6 Shannon Theorem	41
7.4 Questions for the lecture	41
8 Delays	42
9 Clock, Clock skew, clock skitter	44
9.1 Exercises:	44
10 Power consumption	47
10.1 How can I calculate the power dissipation of general-purpose logic ICs	47
10.1.1 Static power dissipation: P_s	47
10.1.2 Dynamic power dissipation	47
10.1.3 Dynamic power dissipation due to load capacitance (C_L) : P_L	47
10.1.4 Dynamic power dissipation due to internal equivalent capacitance (C_{PD}) : P_{PD}	48
10.1.5 Total power dissipation : P_{TTL}	48
10.2 Exercises:	48
11 Clocks and other signals on PCBs	52
12 Monte Carlo simulation	52
13 Stability	52
13.1 Tian's Method	53
13.1.1 Op Amp Circuits	53
13.1.2 Stability Problem	54
14 Special Amplifiers	57
14.1 Differential difference amplifier	57
14.2 Signal flow graph at the exam	57
15 Formulas	62
15.1 Probability	62
15.1.1 Q-funciton	62
15.1.2 Binomialverteilung	62

16 Most important Formulas	65
16.1 Imporant formulas	65
16.2 Definition der Faltung	66
16.3 Defintion der Energie	66
16.4 Defintion der Leistung periodischer Signale	66
16.5 Definition spezieller Signale	66
17 C.2 z-Transformation	66
17.1 Definition	66
17.2 Inverse z -Transformation	66
17.3 Eigenschaften und Rechenregeln	67
17.4 Spezielle Eigenschaften der einseitigen z -Transformation	67
17.5 Rücktransformation durch Partialbruchzerlegung	67
17.6 Korrespondenzen der z -Transformation	68
18 C.3 Laplace-Transformation	68
18.1 Definition	68
18.2 Eigenschaften und Rechenregeln	69
18.3 Spezielle Eigenschaften der einseitigen Laplace-Transformation	69
18.4 Komplexe Umkehrformel der Laplace-Transformation	69
18.5 Rücktransformation durch Partialbruchzerlegung	69
18.6 Korrespondenzen der Laplace-Transformation	70
18.7 Spezielle Korrespondenzen zur Rücktransformation konj. komplexer Polpaare	70
19 C.4 Fourier-Transformation	70
20 Eigenschaften der Fourier-Transformation	71

1 Intro

This summary may contain errors because it has not been proofread by anyone.

Additional materials can be found in the following textbook: Design with operational amplifiers and analog integrated circuits from Sergio Franco.

Videos of the lectures can be downloaded with the following CLI.

Further information with an updated version of the exam summary might be found on my personal website

1.1 Laplace vs Fourier Transform

$$\begin{aligned}\hat{F}(\omega) &= \int_{-\infty}^{\infty} F(t)e^{-i\omega t} dt \\ F(t) &= \frac{1}{2\pi} \int_{-\infty}^{\infty} \hat{F}(\omega)e^{i\omega t} d\omega\end{aligned}\tag{1}$$

$$\begin{aligned}\bar{f}(s) &= \int_0^{\infty} f(t)e^{-(\gamma+i\omega)t} dt = \int_0^{\infty} f(t)e^{-st} dt \\ f(t) &= \frac{1}{2\pi i} \int_{\gamma=-\infty}^{\gamma+i\infty} \bar{f}(s)e^{st} ds \\ s &= \gamma + i\omega\end{aligned}\tag{2}$$

The Fourier transform (Equation 1) is only working for signals that go to zero for plus and minus infinity. Which is quite a restriction. Therefore the Laplace transform generalizes the Fourier transform to a much more important class of functions, by weighting the function $F(t)$ by a factor of $e^{-\gamma t}$ and the Heaviside function $H(T)$.

In the past it turned out the Laplace transform (Equation 2) and Fourier transform (Equation 1) are very useful to draw Bode plots and calculate transfer functions for electronic circuits.

1.2 Thevenin Theorem

The Thevenin's theorem states that „Any linear electrical network containing only voltage sources, current sources and resistances can be replaced at terminals $A - B$ by an equivalent combination of a voltage source V_{th} in a series connection with a resistance R_{th} .“

- The equivalent voltage V_{th} is the voltage obtained at terminals $A - B$ of the network with terminals $A - B$ open circuited.
- The equivalent resistance R_{th} is the resistance that the circuit between terminals A and B would have if all ideal voltage sources in the circuit were replaced by a short circuit and all ideal current sources were replaced by an open circuit.
- If terminals A and B are connected to one another, the current flowing from A and B will be $\frac{V_{th}}{R_{th}}$. This means that R_{th} could alternatively be calculated as V_{th} divided by the short-circuit current between A and B when they are connected together.

In circuit theory terms, the theorem allows any one-port network to be reduced to a single voltage source and a single impedance.

The theorem also applies to frequency domain AC circuits consisting of reactive (inductive and capacitive) and resistive impedances. It means the theorem applies for AC in an exactly same way to DC except that resistances are generalized to impedances.

1.3 Norton equivalent circuit

A Norton equivalent circuit is related to the Thevenin equivalent by the equations:

$$\begin{aligned} R_{\text{th}} &= R_{\text{no}} \\ V_{\text{th}} &= I_{\text{no}} R_{\text{no}} \\ \frac{V_{\text{th}}}{R_{\text{th}}} &= I_{\text{no}} \end{aligned}$$

Example why one normally uses G (conductance) instead of R (resistance)

The output $\frac{V_{\text{out}}}{V_{\text{in}}}$ of Figure 1a can be written as $\frac{G_1}{G_1+G_2} = \frac{R_2}{R_1+R_2}$. So the complexity is about the same but when one would replace G_2 with C_2 a capacitance as it can be seen in Figure 1b, one could simply write the output as $\frac{G_1}{G_1+sC_2}$, whereas with resistors the calculation would be a little bit more difficult. This is one reason to use G instead of R values in the signal flow graphs which will be discussed later on.

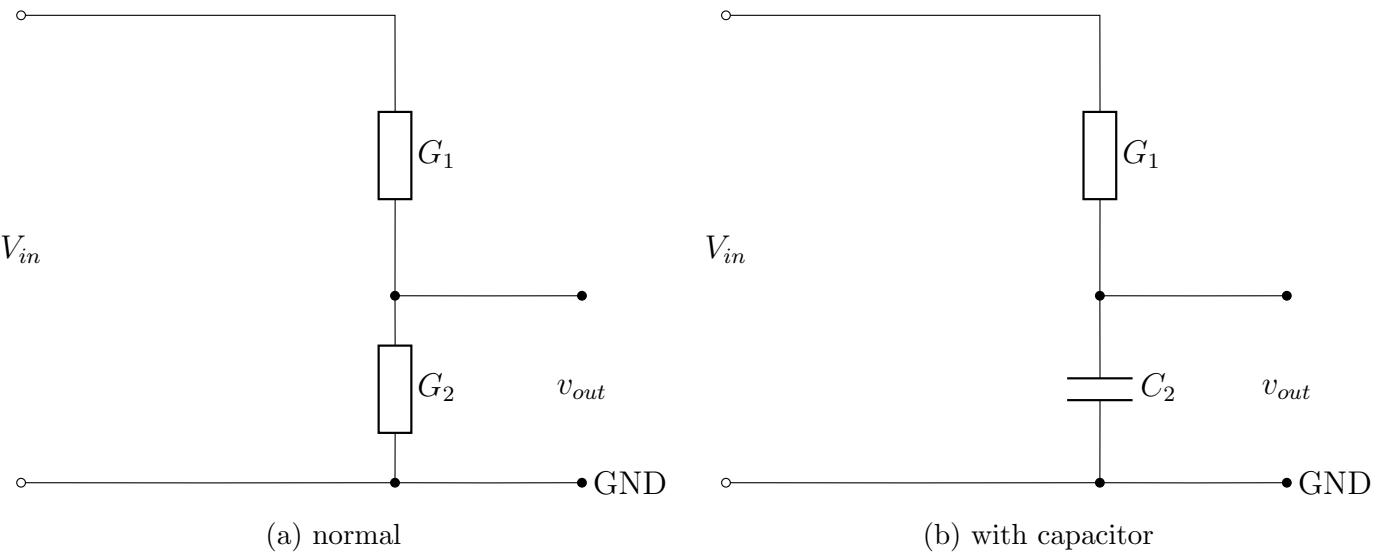


Abbildung 1: Voltage divider

1.4 Bode plot

A bode plot is normally a double logarithmic plot, which is due to the fact that a normal transfer function (the magnitude of it), as the one from Figure 1b, can be represented as $A = k\omega^n$ for large frequencies (Equation 3). When taking from both sides the logarithm one gets again a linear function as it can be seen in Equation 4.

$$\begin{aligned} \frac{G_1}{G_1 + sC_2} &\approx \frac{G_1}{sC_2} \quad (\text{for large frequencies}) \\ |H(j\omega)| &\rightarrow \frac{G_1}{\omega C_2} \end{aligned} \tag{3}$$

$$\begin{aligned} A &= k\omega^n \quad \frac{G_1}{\omega C_2} = \frac{G_1}{C_2} \cdot \omega^{-1} \\ \log A &= \log(k\omega^n) \\ \log A &= \log k + n \cdot \log \omega \\ y &= b + mx \end{aligned} \tag{4}$$

Another benefit of using the bode plot in the Laplace or Fourier domain is shown in Equation 5, where one sees that when one has two linear systems in series, one can just add the magnitude of them in the log scale and the same for the phase in the normal scale. Since, a multiplication in the normal scale is an addition in the logarithmic scale.

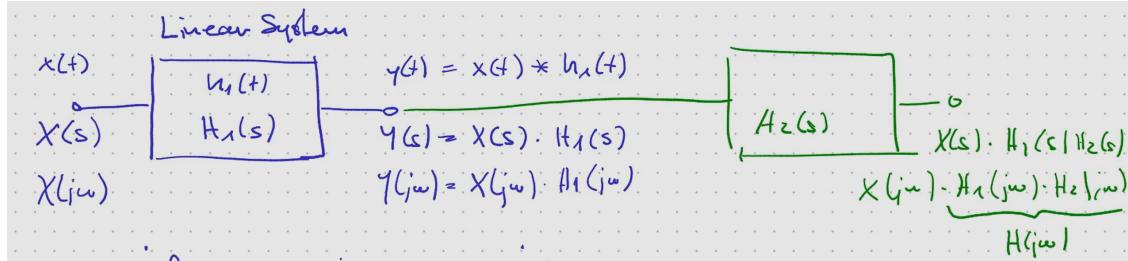


Abbildung 2: Linear Systems

$$\begin{aligned} Ae^{j\varphi} &= A_1 e^{j\varphi_1} A_2^{-1} e^{j\varphi_2} \\ &= A_1 A_2 e^{(\varphi_1 + \varphi_2)} \end{aligned} \quad (5)$$

1.4.1 Bode plot of an opamp

When one has a look at a bode plot like the one in Figure 3 one always has to look for straight lines. Note that the phase margin is $\angle A(jw) + 180^\circ$. And A_0 represents the gain at the frequency zero. Therefore, Figure 3 corresponds to Equation 6

$$\begin{aligned} A(s) &= \frac{\omega_1}{s + \frac{\omega_1}{A_0}} \\ \angle A(jw) &= \frac{\omega_1}{jw} \\ &= -90^\circ \end{aligned} \quad (6)$$

Furthermore, it is important to remember that $\frac{1}{s}$ as it can be observed in an opamp (Figure 3) is an integrator in the Laplace domain.

To draw a bode plot calculate all the poles and zeros as it is shown in the example below. Also have a look at Figure 27, Figure 28, Figure 29 and Figure 30 to get an idea how the plot looks like with different transfer functions.

Example 1.1 With all these tricks, we now succeed in sketching a Bode plot of a larger transfer function. Let the following transfer function be given:

$$T(s) = \frac{10000s^2 + 1010000s + 1000000}{s^3 + 250s^2 + 1000000s}.$$

To draw this transfer function, one needs to find poles and zeros. The zeros (numerator/above the fraction bar) are in this example at -1 and -100 `zeros(10000s^2+1010000s+1000000,s)`. For the poles one gets real pole at 0 and one conjugate complex pole pair with $\omega_p = 1000$ and $q_p = 4$. We now decompose the function into products, each containing only one pole or zero frequency:

$$T(s) = \frac{1}{s} \cdot \frac{s+1}{1} \cdot \frac{s+100}{100} \cdot \frac{1000000}{s^2 + 250s + 1000000}$$

The special thing about this decomposition is that each factor after the first one is normalized such that it goes towards one for small frequencies.

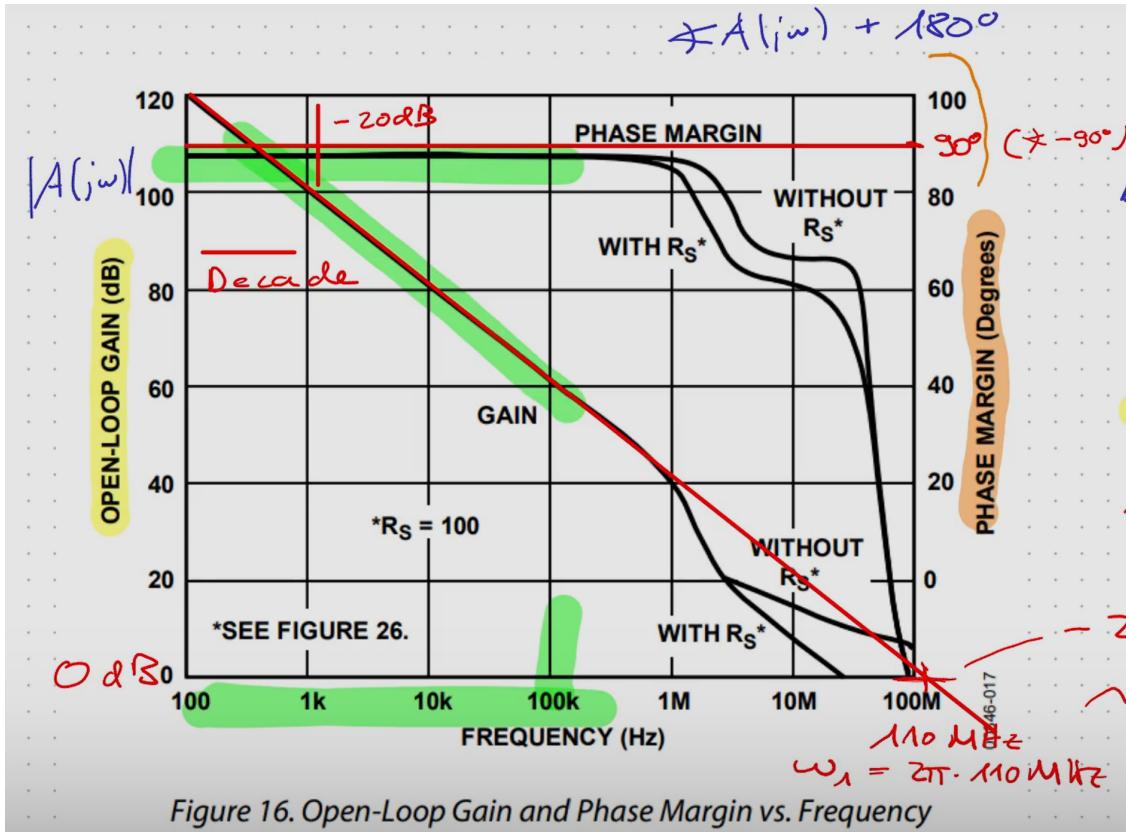
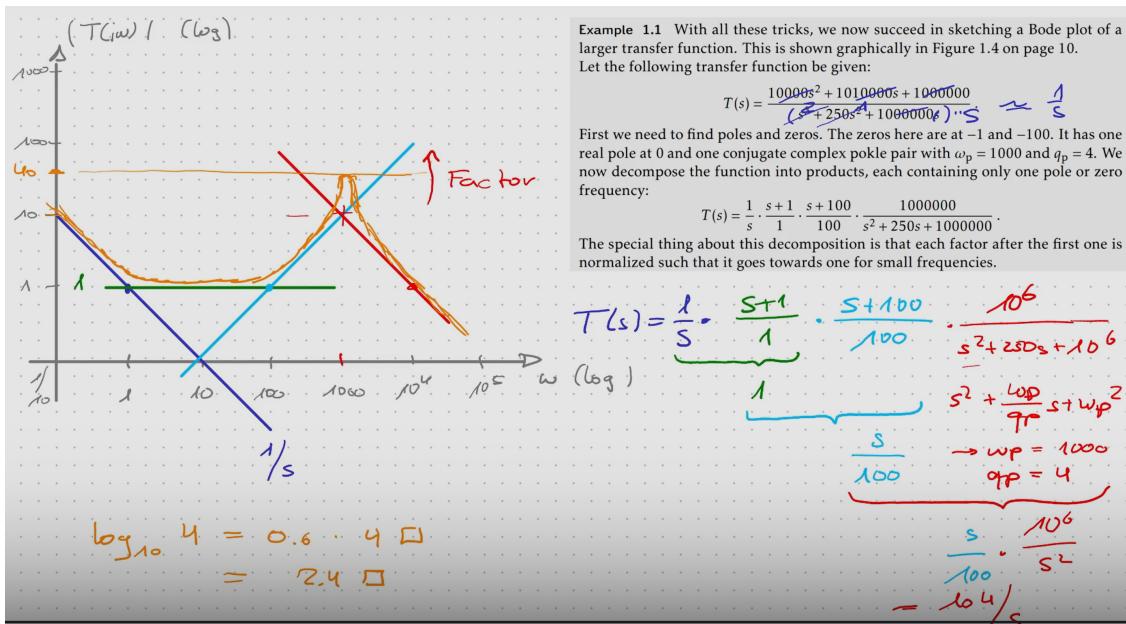


Figure 16. Open-Loop Gain and Phase Margin vs. Frequency

Abbildung 3: open loop gain bode plot



2 Signal Flow Grapher

A signal flow graph is a very powerful tool to analyse a circuit, instead of calculating matrices (German way) one draws graphs and solves the graph (American way).

2.1 Rule of Maison

Given an SFG with n loops L_1, \dots, L_n and m forward paths P_1, \dots, P_m from the source x_s to any node x_a , the transfer function from x_s to x_a is given by Mason's gain rule:

$$T = \frac{x_a}{x_s} = \frac{\sum_{i=1}^m P_i \Delta_i}{\Delta} \quad (7)$$

where Δ is the graph determinant, and the Δ_i are the subdeterminants associated with the paths. The graph determinant is calculated as follows: it is

One

minus the sum of the loop gains of all loops

plus the sum of the products of the loop gains of two loops that have no nodes in common

minus the sum of the products of the loop gains of three loops that have no nodes in common

plus the sum of the products of the loop gains of four loops that have no nodes in common

and so on.

The subdeterminants Δ_i of the forward paths P_i are also calculated in this way, except that here only those loops are considered which have **no nodes** in common with the associated forward path.

2.1.1 Example

In the circuit of Figure 4a the potentiometer is used to control gain magnitude as well as polarity. (a) Letting k denote the fraction of R_3 between the wiper and ground, show that varying the wiper from bottom to top varies the gain over the range $-R_2/R_1 \leq A \leq 1 \text{ V/V}$, so that making $R_1 = R_2$ yields $-1 \text{ V/V} \leq A \leq +1 \text{ V/V}$. (b) To accommodate gains greater than unity, connect an additional resistance R_4 from the op amp's inverting-input pin to ground. Derive an expression for A in terms of R_1, R_2, R_4 , and k . (c) Specify resistance values suitable for achieving $-5 \text{ V/V} \leq A \leq +5 \text{ V/V}$.

1. Analyze the circuit, replace R with G, see Figure 4b
2. Draw the voltage sources, see Figure 4c
3. Draw the current sources everywhere where no voltage source is, see Figure 4d
4. Draw the graph, see Figure 50
5. Use the rule of maison from Equation 7

- $P_1 = G_1 \cdot \frac{1}{G_1+G_2} \cdot (-1) = \frac{-G_1}{G_1+G_2}$
- $P_2 = \frac{G_3}{1-k} \cdot \frac{1}{\frac{G_3}{1-k} + \frac{G_3}{k}} \cdot 1$
- $L_1 = G_2 \cdot \frac{1}{G_1+G_2} \cdot (-1)$
- $L_2 = 1$
- $\Delta_1 = 1$
- $\Delta_2 = 1$

- $\Delta = 1 - (L_1 + L_2) = 1 + \frac{G_2}{G_1+G_2} - 1 = \frac{G_2}{G_1+G_2}$

- $T = \frac{\frac{-G_1}{G_1+G_2} \cdot 1 + \frac{G_3}{1-k} \cdot \frac{1}{\frac{G_3}{1-k} + \frac{G_3}{k}} \cdot 1}{\frac{G_2}{G_1+G_2}} = \frac{k \cdot (G_1 + G_2)}{G_2} - \frac{G_1}{G_2}$

Therefore when $k=1$ the output is one and when $k=0$ the output is $-\frac{G_1}{G_2} = -\frac{R_2}{R_1}$
With an additional Reistor P_1, L_1, Δ_1 and Δ would change as it can be also seen in Figure 4f

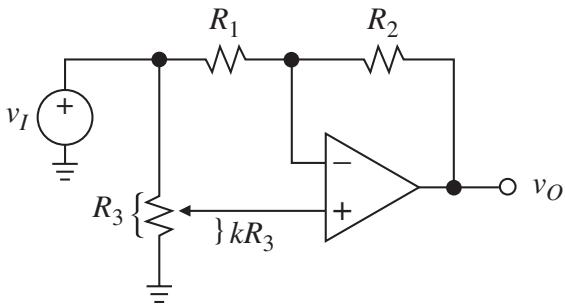
$$T = \frac{\frac{-G_1}{G_1+G_2+G_4} \cdot 1 + \frac{G_3}{1-k} \cdot \frac{1}{\frac{G_3}{1-k} + \frac{G_3}{k}} \cdot 1}{\frac{G_2}{G_1+G_2+G_4}} = \frac{k \cdot (G_1 + G_2 + G_4)}{G_2} - \frac{G_1}{G_2}$$

c) for achieving $-5V$ to $5V$ $-\frac{G_1}{G_2} = -\frac{R_2}{R_1}$ must be -5 . Then let's assume $R_1 = 10\text{ k}\Omega$

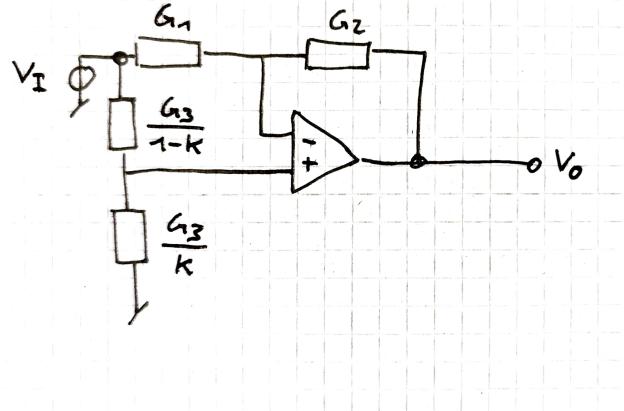
$$\begin{aligned} \frac{k \cdot (G_1 + G_2 + G_4)}{G_2} - \frac{G_1}{G_2} &= \frac{1 \cdot (0.0001 + 0.00002 + G_4)}{0.00002} - 5 = 5 \Rightarrow \\ 10 &= \frac{(0.0001 + 0.00002 + G_4)}{0.00002} \Rightarrow G_4 = 0.00008 \Rightarrow R_4 = 12.5\text{ k}\Omega \end{aligned}$$

With the signalflowgrapher tool one would have the following steps:

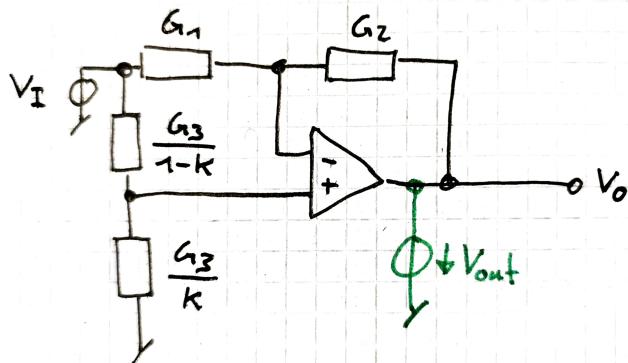
1. Start signal flow grapher with the following command `python .\src\main\python\main.py` in the 'signalflowgrapher' folder (make also sure the right environment is activated `conda activate sfg`)
2. Draw the graph in the signal flow grapher:
3. Copy maison, see below



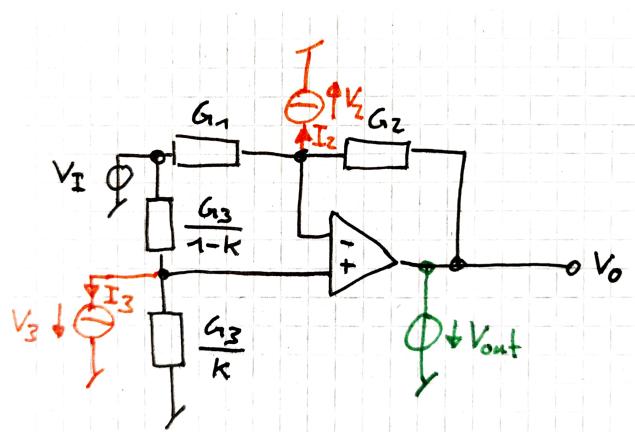
(a) Opamp circuit



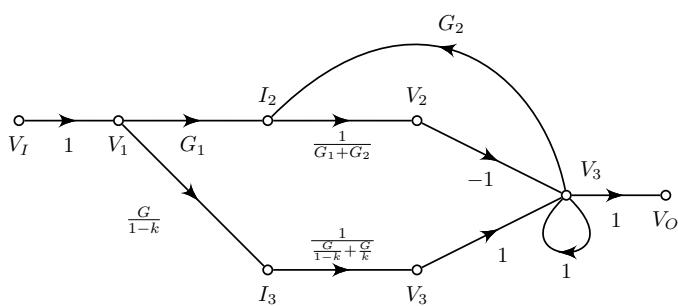
(b) Opamp circuit redrawn



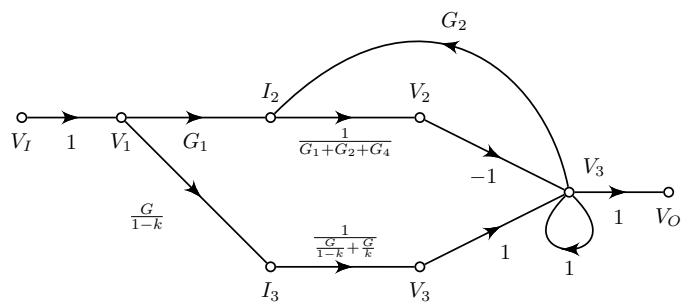
(c) Opamp circuit voltage source



(d) Opamp circuit voltage and current sources



(e) Opamp circuit signal flow graph



(f) Opamp circuit signal flow graph, with additional resistor

3 Noise

The signal in the presence of noise is specified by means of the signal-to-noise ratio (SNR) as it can be seen in Equation 8. Where X_s is the rms value of the signal, and X_n is that of its noise component. The poorer the SNR, the more difficult it is to rescue the useful signal from noise.

$$\text{SNR} = 10 \log_{10} \frac{X_s^2}{X_n^2} \quad (8)$$

3.1 Rms Value

Using subscript n to denote noise quantities, we define the root-mean-square (rms) value X_n of a noise voltage or current $x_n(t)$ as

$$X_n = \left(\frac{1}{T} \int_0^T x_n^2(t) dt \right)^{1/2}$$

where T is a suitable averaging time interval. The square of the rms value, or X_n^2 , is called the mean square value. Physically, X_n^2 represents the average **power dissipated** by $x_n(t)$ in a $1 - \Omega$ resistor.

In voltage-comparator applications, such as A-D converters and precision multivibrators, accuracy and resolution are affected by the instantaneous rather than the rms value of noise. In these situations, expected peak values of noise are of more concern.

3.2 Noise figure (NF)

The noise figure is the SNR at the input minus the SNR at the output. So if $NF = 2dB$ the SNR gets reduced by 2dB.

$$NF = SNR_1 - SNR_2 \quad (9)$$

3.3 Tangent principle

A bode plot is normally in a double logarithmic scale, therefore the noise density on the right is much more weighted than the one on the left. The tangent principle says that one can take the pink-noise tangent as in Figure 5 to approximate the noise. So in the example below the noise would be

$$V_{n,rms}^2 = \left(200 \text{ nV}/\sqrt{\text{Hz}} \right)^2 \cdot 10 \times 10^5 \text{ Hz} \cdot \frac{\pi}{2}$$

even tough, it seems like there is a lot missing on the left side. The factor $\frac{\pi}{2}$ comes from the noise equivalent bandwidth (NEB), which is $NEB_{MF} = 1.57 \cdot f_0$ for $n = 1$, $1.11 \cdot f_0$ for $n = 2$, $1.05 \cdot f_0$ for $n = 3$, and $1.025 \cdot f_0$ for $n = 4$, indicating that NEB_{MF} rapidly approaches f_0 as n is increased.

3.4 Measure Noise

It is not possible to read the SNR from a power spectrum density What you should do is to input a signal (sine wave) with a signal generator into your circuit, sample the output with a high frequency, and calculate the power spectrum density, integrate the power spectrum density around your expected signal plus some tolerance, integrate the rest. Then divide the integrated power spectrum density around your expected signal by the rest. This gives you the SNR. This

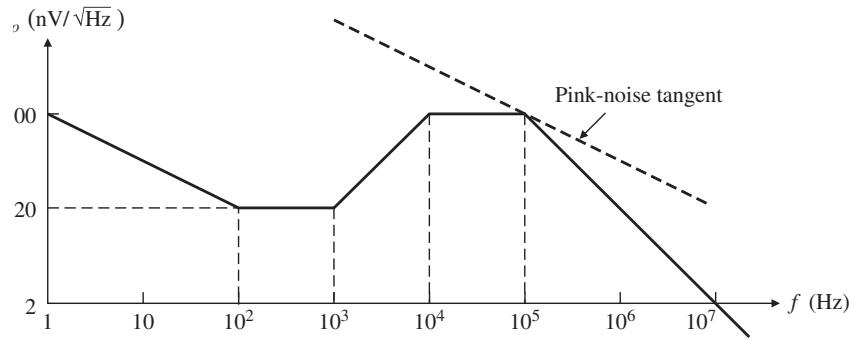


Abbildung 5: Pink noise tangent example

3.5 Noise at opamps

When the opamp noise is given as V_n^2 it is not recommended to add the source at one of the inputs, but it is much better with doing it like in Figure 6, where it is just an additional input in the signal flow graph. Furthermore, the inputs of the opamp are also not ideal, they have like some input protection circuits and so one therefore one has to add on both inputs also an current noise source.

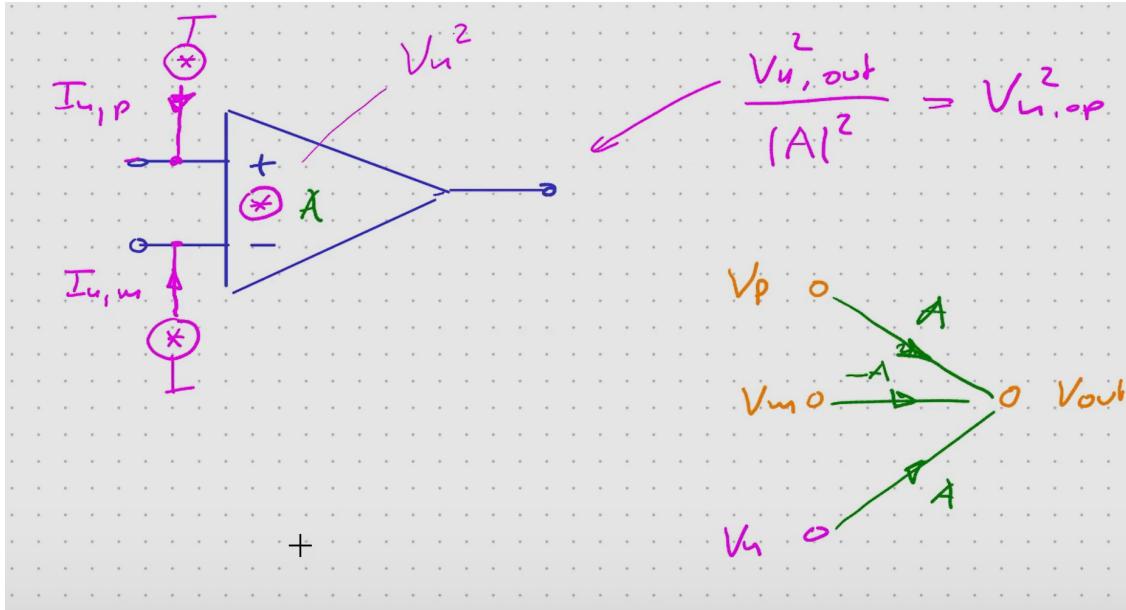


Abbildung 6: Opamp noise sfg

3.5.1 Adding noise

$$P_x = \frac{1}{T} \int_0^T x(t)^2 dt [V_{\text{rms}}^2]$$

$$\sqrt{\underbrace{\frac{1}{T} \int_0^T \underbrace{x(t)^2 dt}_{\text{Square}}}_{\text{Mean}}} [V_{\text{rms}}]$$

$$\begin{aligned}
P_t &= \frac{1}{T} \int_0^T \overbrace{(x+y)^2}^{x^2+2xy} dt \\
&= \underbrace{\frac{1}{T} \int_0^T x^2 dt}_{P_x} + \underbrace{\frac{1}{T} \int_0^T y^2 dt}_{P_y} + \underbrace{\frac{1}{T} \int_0^T 2x(t)y(t)dt}_{=0}
\end{aligned}$$

3.5.2 Example OP27A

The input noise density is for $f_0 = 1000 \text{ kHz}$:

- $V_{n,op} = 3.0 \text{ nV}/\sqrt{\text{Hz}}$
- $I_{n,p} = I_{n,m} = 0.4 \text{ nA}/\sqrt{\text{Hz}}$

What is the noise When the circuit like in Figure 7 is given one can draw its signal flow graph accordingly. With Mason one then gets

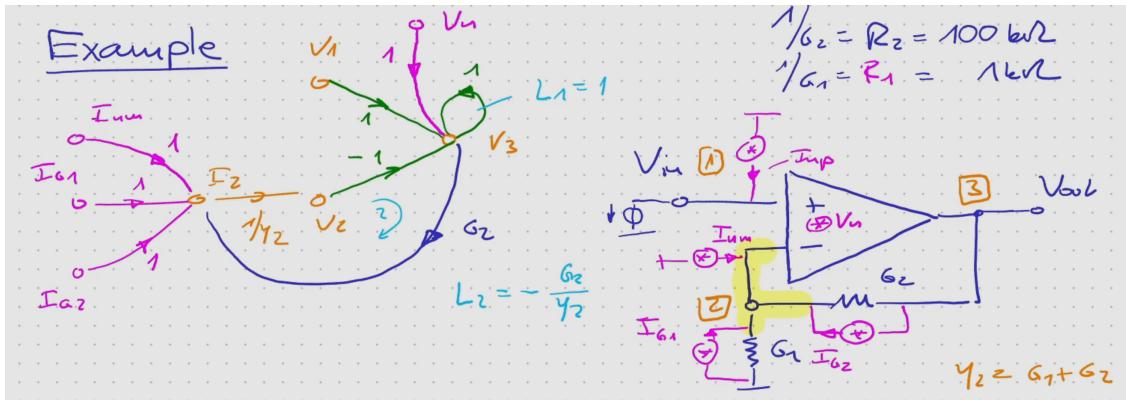


Abbildung 7: Opamp noise circuit signalflow graph

$$L_1 = 1$$

$$L_2 = -\frac{G_2}{G_1 + G_2}$$

$$\Delta = 1 - L_1 - L_2 = \frac{G_2}{G_1 + G_2}$$

For $V_1, V_n \rightarrow V_3$ one gets the following

$$P_1 = 1$$

$$\Delta_1 = 1 - 0$$

$$T_{n,v} = \frac{G_1 + G_2}{G_2}$$

and for $I_{n,m} \rightarrow V_3$ one gets

$$P_1 = -\frac{1}{G_1 + G_2}$$

$$\Delta_1 = 1 - 0$$

$$T_{n,i} = -\frac{1}{G_2}$$

$$V_{n,out}^2 = \underbrace{\frac{V_n^2 |T_{n,v}|^2}{(3 \text{nV}/\sqrt{\text{Hz}})^2 \cdot (101)^2}} + \underbrace{\frac{I_{n,m}^2 |T_{n,i}|^2}{(0.4 \text{pA}/\sqrt{\text{Hz}})^2 \cdot (100 \text{k}\Omega)^2}} + \underbrace{\frac{I_{n,G_1}^2 |T_{n,i}|^2}{4kTR_2 \frac{G_1}{G_2^2}}}_{(40 \text{nV}/\sqrt{\text{Hz}})^2 \cdot (100)} + \underbrace{\frac{I_{n,G_2}^2 |T_{n,i}|^2}{(40 \text{nV}/\sqrt{\text{Hz}})^2}} = \left(500 \text{nV}/\sqrt{\text{Hz}}\right)^2$$

3.5.3 Example AD812

Note for current feedback opamps you have two different noise levels at the two inputs.

- $V_{n,op} = 3.5 \text{nV}/\sqrt{\text{Hz}}$
- $I_{n,p} = 1.5 \text{pA}/\sqrt{\text{Hz}}$
- $I_{n,p} = I_{n,m} = 18 \text{pA}/\sqrt{\text{Hz}}$

3.6 Sources of Noise

3.6.1 Thermal Noise

Thermal noise, also called Johnson noise, is present in all passive resistive elements, including the stray series resistances of practical inductors and capacitors. Thermal noise is due to the random thermal motion of electrons (or holes, in the case of *p*-type semiconductor resistors). It is unaffected by dc current, so a resistor generates thermal noise even when sitting in a drawer.

Thermal noise is modeled by a noise voltage of spectral density e_R in series with an otherwise noiseless resistor. Its power density is

$$e_R^2 = 4kTR$$

where $k = 1.38 \times 10^{-23} \text{ J/K}$ is Boltzmann's constant, and T is absolute temperature, in kelvins. At 25°C , $4kT = 1.65 \times 10^{-20} \text{ W/Hz}$. An easy figure to remember is that at 25°C , $e_R \cong 4\sqrt{R}\text{nV}/\sqrt{\text{Hz}}$, **R in kilo-ohms**. For instance, $e_{100\Omega} = 4\sqrt{0.1} = 1.26 \text{nV}/\sqrt{\text{Hz}}$, and $e_{10\text{k}\Omega} = 12.6 \text{nV}/\sqrt{\text{Hz}}$.

Converting from Thevenin to Norton, we can model thermal noise also with a noise current i_R in parallel with an otherwise noiseless resistor, as shown in Fig. 7.6b. We have $i_R^2 = e_R^2/R^2$, or

$$i_R^2 = 4kT/R$$

The preceding equations indicate that thermal noise is of the white type. Purely reactive elements are free from thermal noise.

EXAMPLE . Consider a $10\text{-k }\Omega$ resistor at room temperature. Find (a) its voltage and (b) current spectral densities, and (c) its rms noise voltage over the audio range. Solution. (a) $e_R = \sqrt{4kTR} = \sqrt{1.65 \times 10^{-20} \times 10^4} = 12.8 \text{nV}/\sqrt{\text{Hz}}$ (b) $i_R = e_R/R = 1.28 \text{pA}/\sqrt{\text{Hz}}$ (c) $E_R = e_R\sqrt{f_H - f_L} = 12.8 \times 10^{-9} \times \sqrt{20 \times 10^3 - 20} = 1.81 \mu\text{V}$

3.7 Noise Properties

3.7.1 Noise Spectra

Since X_n^2 represents the average power dissipated by $x_n(t)$ in a $1 - \Omega$ resistor, the physical meaning of mean square value is the same as for ordinary ac signals. However, unlike an ac signal, whose power is concentrated at just one frequency, noise power is usually spread all over the frequency spectrum

because of the random nature of noise. Thus, when referring to rms noise, we must always specify the frequency band over which we are making our observations, measurements, or calculations.

In general, noise power depends on both the width of the frequency band and the band's location within the frequency spectrum. The rate of change of noise power with frequency is called the **noise power density**, and is denoted as $e_n^2(f)$ in the case of voltage noise, and $i_n^2(f)$ in the case of current noise. We have

$$e_n^2(f) = \frac{dE_n^2}{df} \quad i_n^2(f) = \frac{dI_n^2}{df} \quad (10)$$

where E_n^2 and I_n^2 are the mean square values of voltage noise and current noise. Note that the units of $e_n^2(f)$ and $i_n^2(f)$ are volts squared per hertz (V^2/Hz) and amperes squared per hertz (A^2/Hz). Physically, noise power density represents the average noise power over a 1-Hz bandwidth as a function of frequency. When plotted versus frequency, it provides a visual indication of how power is distributed over the frequency spectrum. In integrated circuits, the two most common forms of power density distribution are white noise and $1/f$ noise.

The quantities $e_n(f)$ and $i_n(f)$ are called the **spectral noise densities**, and are expressed in volts per square root of hertz ($V/\sqrt{\text{Hz}}$) and amperes per square root of hertz ($A/\sqrt{\text{Hz}}$). Some manufacturers specify noise in terms of noise power densities, others in terms of spectral noise densities. Conversion between the two is accomplished by squaring or by extracting the square root.

Multiplying both sides in Equation 10 by df and integrating from f_L to f_H , the lower and upper limits of the frequency band of interest, allows us to find the rms values in terms of the power densities,

$$E_n = \left(\int_{f_L}^{f_H} e_n^2(f) df \right)^{1/2} \quad I_n = \left(\int_{f_L}^{f_H} i_n^2(f) df \right)^{1/2} \quad (11)$$

Once again it is stressed that the concept of rms cannot be separated from that of frequency band: in order to find the rms value, we need to know the lower and upper limits of the band as well as the density within the band.

3.7.2 White Noise

White noise is characterized by a uniform spectral density, or $e_n = e_{nw}$ and $i_n = i_{nw}$, where e_{nw} and i_{nw} are suitable constants. It is so called by analogy with white light, which consists of all visible frequencies in equal amounts. When played through a loudspeaker, it produces a waterfall sound. Applying Equation 11 we get

$$E_n = e_{nw} \sqrt{f_H - f_L} \quad I_n = i_{nw} \sqrt{f_H - f_L} \quad (12)$$

indicating that the rms value of white noise increases with the square root of the frequency band. For $f_H \geq 10f_L$ we can approximate as $E_n \cong e_{nw}\sqrt{f_H}$ and $I_n \cong i_{nw}\sqrt{f_H}$ at the risk of an error of about 5% or less.

Squaring both sides in Equation 12 yields $E_n^2 = e_{nw}^2 (f_H - f_L)$ and $I_n^2 = i_{nw}^2 (f_H - f_L)$, indicating that white-noise power is proportional to the bandwidth, regardless of the band's location within the frequency spectrum. Thus, the noise power within the 10 – Hz band between 20 Hz and 30 Hz is the same as that within the band between 990 Hz and 1kHz.

4 ADC/DAC

To get an idea of the quantization error or error voltage $V_e = \epsilon = V_{out} - V_{in}$ it is always a good idea to think that one has an ADC and DAC connected in series. So the input is a voltage and the output is a voltage.

4.1 DAC

Important to remember when speaking about DACs is that they normally start at zero but do not go up to V_{ref} . When it would go up to V_{ref} to voltage division factor would be very strange ($0, \frac{1}{7}, \frac{1}{7}, \dots, \frac{7}{7}$). So it makes it much easier when one just divides by 8.

The error of a DAC can be divided into offset error, gain error and nonlinearity error, as it can be seen in Figure 8. Note FS stands for full scale, which is in the case of Figure 8 $V_{ref} \cdot \frac{7}{8}$. When something

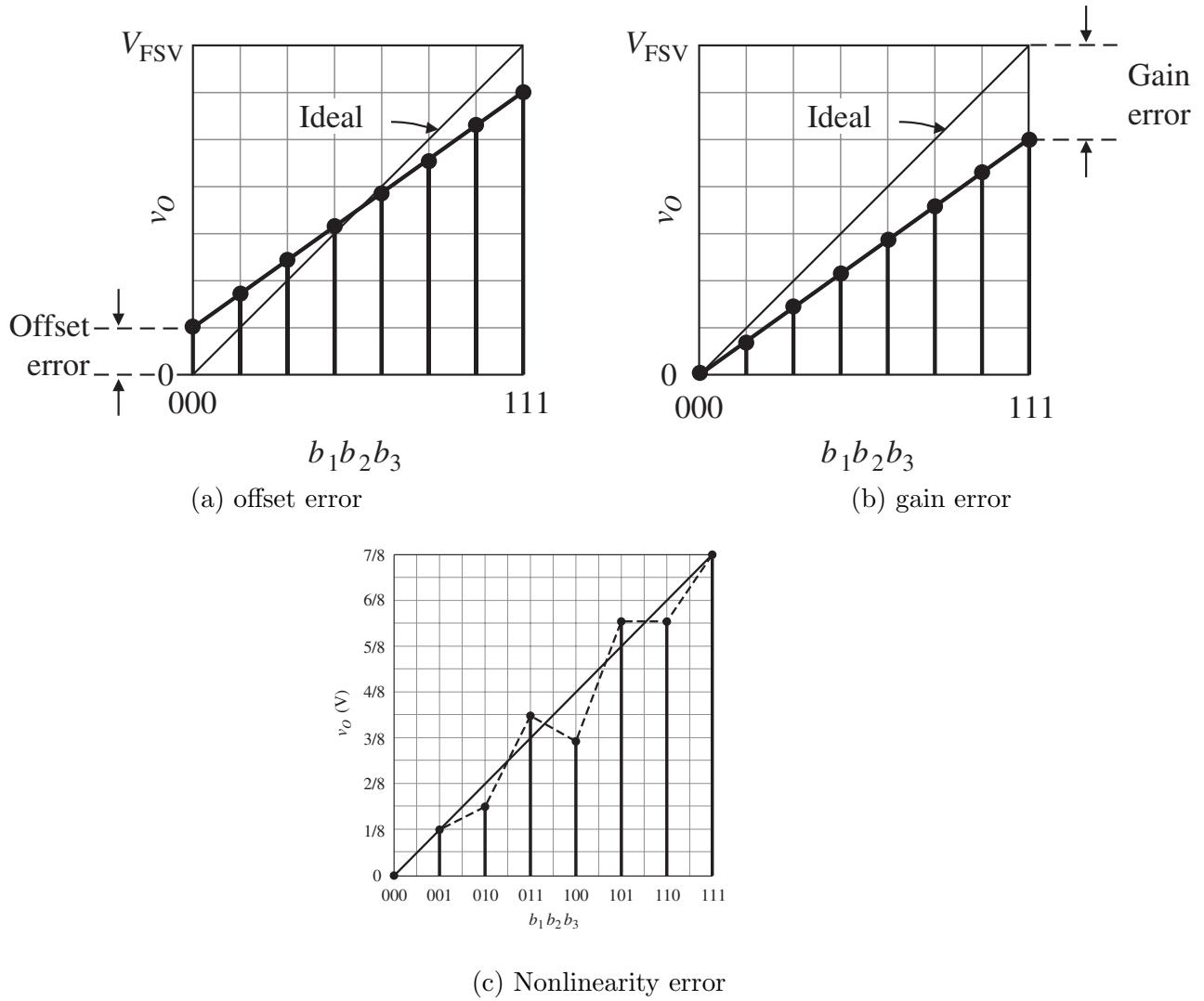


Abbildung 8: DAC offset and gain error

happens like in Figure 8c from 011 to 100 then the DAC is called non-monotonic. This is very bad for a control system. To check if one does not have missing codes one should have a look at the INL (Integral nonlinearity), when it is inside ± 1 then it is ok (monotonic), otherwise it is non-monotonic and has missing codes.

EXAMPLE 12.1. Find the INL and DNL of the 3-bit DAC of Figure 8c. Comment on your results.

Solution. By inspection, the individual-code integral and differential nonlinearities, in fractions of 1LSB, are found to be

$$\begin{array}{llllllll} k : & 000 & 001 & 010 & 011 & 100 & 101 & 110 & 111 \\ \text{INL}_k : & 0 & 0 & -1/2 & 1/2 & -1 & 1/2 & -1/2 & 0 \\ \text{DNL}_k : & 0 & 0 & -1/2 & 1 & -3/2 & 3/2 & -1 & 1/2 \end{array}$$

The maxima of INL_k and DNL_k are, respectively, $\text{INL} = 1\text{LSB}$ and $\text{DNL} = 1\frac{1}{2}\text{LSB}$. We observe a nonmonotonicity as the code changes from 011 to 100, where the step size is $-\frac{1}{2}\text{LSB}$ instead of $+1\text{LSB}$; hence, $\text{DNL}_{100} = -\frac{1}{2} - (+1) = -\frac{3}{2}\text{LSB} < -1\text{LSB}$. The fact that $\text{DNL}_{101} = \frac{3}{2}\text{LSB} > 1\text{LSB}$, though undesirable, does not cause nonmonotonicity.

4.1.1 binary ADC and DAC

An example of an binary DAC can be found in Figure 9. One can recognize them when one sees that there is a big jump in the middle of the DNL plots.

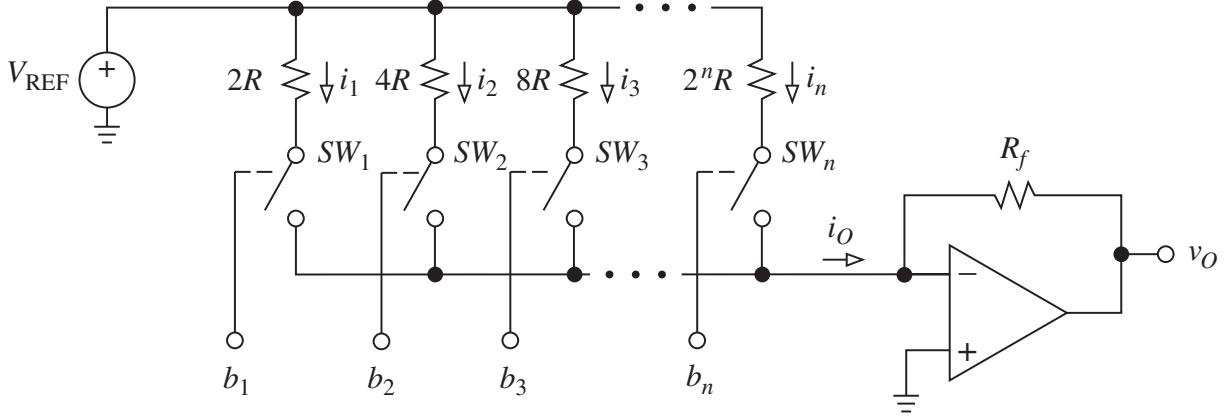


Abbildung 9: Weighted-Resistor DAC

4.2 ADC

An example ADC characteristic can be found in Figure 10, which shows that there is a missing code at the value 100.

4.2.1 Clock jitter in an ADC

Let's say we have clock jitter of $\sigma_j = 5\text{ps}$ on a sinus signal like $x(t) = A \cdot \sin(2\pi ft)$. To get the amplitude difference one can look at the place where the slope of the signal is the steepest which can be approximated like the following $x(t) = A \cdot 2\pi ft$. Therefore $x_{\text{rms}} = A \cdot 2\pi f \sigma_j$ and since $\text{Sig}_{\text{rms}} = \frac{A}{\sqrt{2}}$ one gets Equation 13.

$$\begin{aligned} SNR &= \frac{\text{Sig}_{\text{rms}}^2}{x_{\text{rms}}^2} = \frac{A^2}{2} \cdot \frac{1}{A^2 \cdot (2\pi f)^2 \cdot \sigma_j^2} \\ SNR &= \frac{1}{8\pi^2 f^2 \cdot \sigma_j^2} \end{aligned} \tag{13}$$

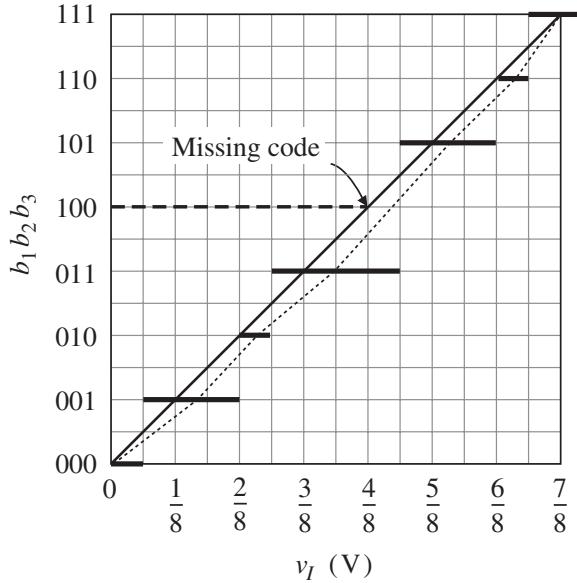


Abbildung 10: Example ADC characteristic

4.3 SNR

The signal-to-noise ratio of an ADC is normally given with a sine wave as a reference, when one would use a triangle or something else the signal to noise ratio would be different. The Error of an ideal ADC can be calculated according to Equation 14

$$\begin{aligned}
 V_{e,\text{rms}}^2 &= \int_0^1 \left(-t \cdot \frac{V_{LSB}}{2} \right)^2 dt \\
 &= \left(\frac{V_{LSB}}{2} \right)^2 \underbrace{\int_0^1 t^2 dt}_{\rightarrow \frac{1}{3}} = \frac{V_{LSB}^2}{12}
 \end{aligned} \tag{14}$$

When one calculates the $V_{e,\text{rms}}$ from Equation 14 one gets the result which can be seen in Equation 15, where $V_{LSB} = \frac{V_{ref}}{2^N}$. The max amplitude a signal (sine wave) can have is $\frac{V_{ref}}{2}$ therefore the signal to noise ratio can be calculated according to Equation 16

$$V_{e,\text{rms}} = \frac{V_{ref}/2^N}{\sqrt{12}} = \frac{V_{ref}}{2^N \cdot \sqrt{12}} \tag{15}$$

$$V_{\text{sig, max}} = \frac{V_{ref}}{2} \Rightarrow V_{\text{sig, rms}} = \frac{V_{ref}}{\underbrace{2 \cdot \sqrt{2}}_{\sqrt{8}}} \tag{16}$$

$$SNR = \frac{V_{\text{sig, rms}}}{V_{e,\text{rms}}} = \frac{V_{ref}}{\sqrt{8}} \frac{2^N \sqrt{12}}{V_{ref}} = 2^N \cdot \sqrt{\frac{3}{2}} = \underline{6.02n + 1.76dB}$$

Note Equation 16 you can only use when you look at the rms values.

When you sample twice as fast you get one bit more resolution. When we sample faster we can filter out the noise (unneeded signal) in the digital domain and through away the quantization noise of the ADC. A lock in amplifier uses this property. Important to remember is the $V_{e,\text{rms}}$ signal is total independent of the sampling frequency. So just oversample and you get a much better result. So it is

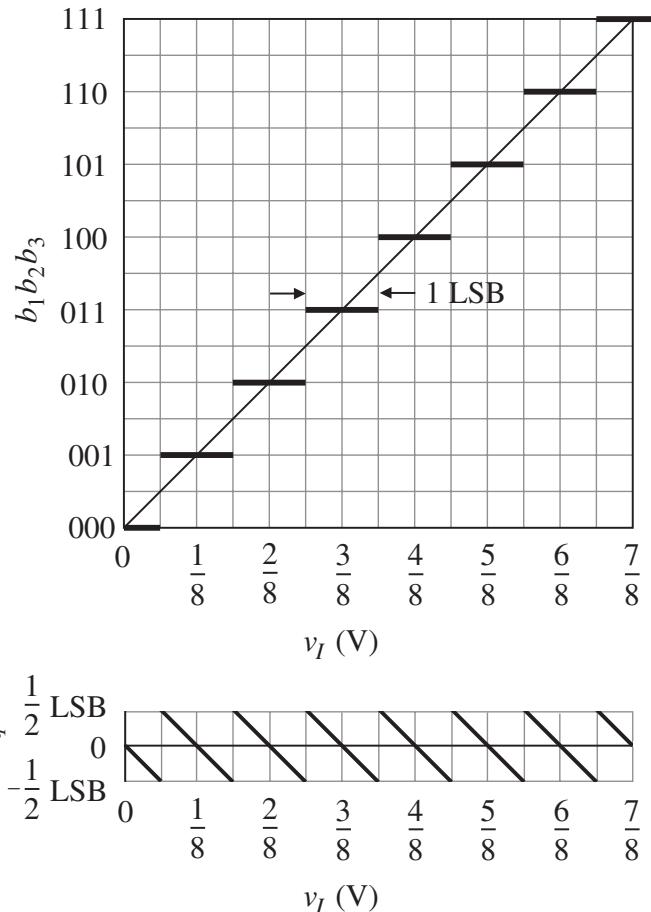


Abbildung 11: ADC diagram, and ideal transfer characteristic and quantization noise for $n = 3$ and VFSR = 1 V

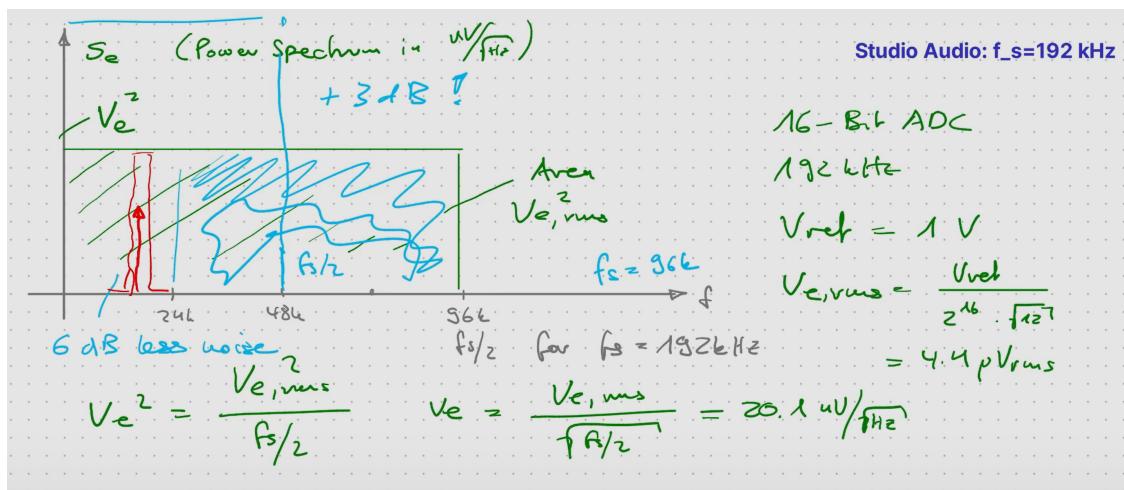


Abbildung 12: Calculations

possible to achieve a 18 bit resolution with a 16 bit adc when you oversample, because you have the information in the high frequencies.

Let's assume one has a 24-Bit ADC with 108.5dB dynamic range typical. This means the number of effective bits (ENOB) is $ENOB = \frac{SNR - 1.76dB}{6.02dB} = 17.73\text{bits}$. **SINAD** signal to noise and distortion.

Is the value from the signal to the distortion as it can be seen in Figure 13. In the graph the adc was connected with a input signal $V_{in} = \frac{V_{ref}}{2} \cdot 10^{-\frac{0.25}{20}} \cdot \sin \omega_0 \cdot t$. The ADC produces a third order distortion which causes the SINAD to be -120dB.

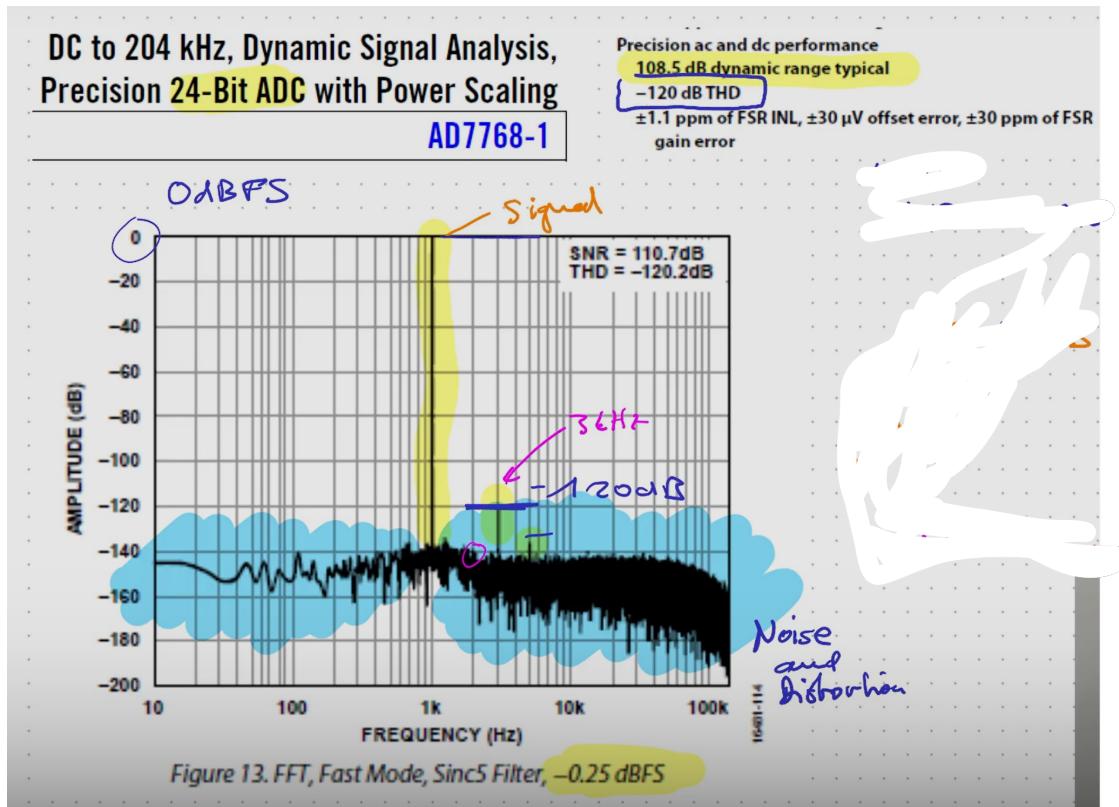


Abbildung 13: SNR and THD (THD = SINAD)

Exercise

- Go to <https://www.adafruit.com/product/1063>, where the datasheets of the components in the Adafruit Electret Microphone Amplifier can be found. That page says you can connect that device to an Arduino board,
 - Look at the microphone datasheet. Assuming the microphone has white noise and the noise is integrated, use the data on the datasheet to calculate the output voltage noise density when the supply is 3.3 V

To answer this question one must first know what sound power is, see the following link for further information. In a medium, the sound power is given by

$$P = \frac{Ap^2}{\rho c} \cos \theta$$

where

- A is the area of the surface;
- ρ is the mass density;
- c is the sound velocity;

- θ is the angle between the direction of propagation of the sound and the normal to the surface.
- p is the sound pressure.
- $P_0 = 1\text{pW}$ commonly used reference sound power in air.
- $p_0 = 2 \times 10^{-5} \text{ N m}^{-2} = 2 \times 10^{-5} \text{ Pa}$ reference sound pressure for SPL calculation

For example, a sound at $\text{SPL} = 85 \text{ dB}$ or $p = 0.356 \text{ Pa} = 10^{\frac{85}{20} \cdot 2 \times 10^{-5} \text{ Pa}}$ in air ($\rho = 1.2 \text{ kg} \cdot \text{m}^{-3}$ and $c = 343 \text{ m} \cdot \text{s}^{-1}$) through a surface of area $A = 1 \text{ m}^2$ normal to the direction of propagation ($\theta = 0^\circ$) has a sound energy flux $P = 0.3 \text{ mW}$.

Now for the exercise, the datasheet says the following: The SNR is given as 60dBA and

SPECIFICATIONS

directivity	omnidirectional
sensitivity (S)	$-44 \pm 2 \text{ dB}$
	$f = 1\text{KHz}, 1\text{Pa} \quad 0\text{dB} = 1\text{V/Pa}$
sensitivity reduction (ΔS -Vs)	-3 dB
	$f = 1\text{KHz}, 1\text{Pa} \quad Vs = 3.0 \sim 2.0 \text{ V dc}$
operating voltage	3 V dc (standard), 10 V dc (max.)
output impedance (Z_{out})	2.2 K Ω
	$f = 1\text{KHz}, 1\text{Pa}$
operating frequency (f)	20 ~ 20,000 Hz
current consumption ($Idss$)	0.5 mA max.
	$Vs = 3.0 \text{ V dc} \quad RL = 2.2\text{K}\Omega$
signal to noise ratio (S/N)	60 dBA
	$f = 1\text{KHz}, 1\text{Pa} \quad \text{A-weighted}$
operating temperature	-20 ~ +70° C
storage temperature	-20 ~ +70° C
dimensions	$\varnothing 9.7 \times 4.5 \text{ mm}$
weight	0.80 g max.
material	Al
terminal	pin type (hand soldering only)
RoHS	yes

Abbildung 14: Section from the datasheet of CMA-4544PF-W

the sensitivity as $-44 \pm 2\text{dB}$ with a reference of 1V Pa^{-1} . Therefore lets say the sensitivity is -42dB . Which gives us $10^{\frac{-42}{20}} = 7.94 \text{ mV Pa}^{-1}$. Since the SNR is 60dB our noise is $V_{n,w,rms} = 10^{\frac{-60}{20}} \cdot 7.94 \text{ mV Pa}^{-1} = 7.94 \mu\text{V Pa}^{-1}$. Furthermore lets assume that our bandwidth is 20 kHz This results in the following:

$$V_{n,w}^2 = V_{n,w,rms}^2 \cdot \frac{1}{20 \times 10^3 \text{ Hz}} = \left(56 \text{nV}/\sqrt{\text{Hz}} \right)^2 \quad (17)$$

- (b) Look at the MAX 4466 datasheet linked on the same page. Estimate the total input referred noise density. What is the noise figure of this amplifier compared to the microphone?

In the datasheet of the amplifier (opamp circuit) one can read that the input noise voltage density is $80 \text{nV}/\sqrt{\text{Hz}}$. Also important to note is that there are also resistors in the circuit, but since a $1\text{k}\Omega$ resistor gives $4 \text{nV}/\sqrt{\text{Hz}}$ at room temperature $80 \text{nV}/\sqrt{\text{Hz}}$ corresponds to $400 \text{k}\Omega$. So the resistors can be made small enough such that the opamp dominates noise. So, using this amplifier reduces the effective resolution by 0.8 bit. (NF can be calculated according to Equation 9)

$$NF = 1 + \frac{V_{n,op}^2}{V_{n,w}^2} = 1 + \frac{80^2}{56^2} = 3.04$$

$$10 \cdot \log 3.04 = 4.83 \text{ dB} = \underbrace{60}_{\text{input}} - 20 \cdot \log \left(\underbrace{\sqrt{\left(\left(80 \text{ nV}/\sqrt{\text{Hz}} \right)^2 + \left(56 \text{ nV}/\sqrt{\text{Hz}} \right)^2 \right) \cdot 20 \text{ kHz}}}_{\text{output}} \right)$$

$$0.8\text{bit} = \frac{60dB - 1.76dB}{6.02dB} - \frac{55.2dB - 1.76dB}{6.02dB}$$

- (c) Assume that you have an Arduino Mega 2560 to sample and process the data. Find out from <https://store.arduino.cc/mega-2560-r3> which contains an ATmega2560 microcontroller. Estimate from the microcontroller datasheet what the input-referred voltage noise of the ADC on that microcontroller would be if you sample at full speed (15kSPS). Then refer it to the input of the MAX 4466 when the gain setting is 125.³ What is the noise figure of the ADC?

The microcontroller has a reference voltage of 2.56V, 15kSPS and 10bit resolution. Therefore one gets with Equation 15

$$V_e^2 = \frac{V_{e, \text{rms}}^2}{\sqrt{\frac{f_s}{2}}} = \frac{\left(\frac{2.56 \text{ V}}{2^{10} \cdot \sqrt{12}} \right)^2}{\frac{f_s}{2}} = \frac{2.56 \text{ V}}{2^{20} \cdot f_s \cdot \frac{12}{2}} = \left(8.33 \mu\text{V}/\sqrt{\text{Hz}} \right)^2$$

Which can also be written as below:

$$\begin{aligned} V_{n,ADC}^2 &= \frac{V_{ref}^2}{6f_s \cdot 2^{2ENOB}} = \frac{(2.56 \text{ V})^2}{6 \cdot 15 \text{ kHz} \cdot 2^{20}} \\ &= \left(8.33 \mu\text{V}/\sqrt{\text{Hz}} \right)^2 \end{aligned} \quad (18)$$

Referenced to the input of the ADC one gets:

$$\begin{aligned} V_{n,ADC,a}^2 &= \frac{V_{n,ADC}^2}{125^2} = 67 \text{ nV}/\sqrt{\text{Hz}} \\ NF &= 1 + \frac{V_{n,ADC,a}^2}{V_{n,w}^2 + V_{n,op}^2} = 1.47 \\ &\quad (1.67\text{dB}) \\ &\quad (0.28\text{bit}) \end{aligned} \quad (19)$$

- (d) What will the effective number of bits of the whole signal processing chain be?

At the microphone, we have SNR=60dB

$$ENOB_{in} = \frac{60dB - 1.76dB}{6.02dB} = 9.67\text{bit}$$

We lose 0.8bit through the amplifier and another 0.28 bit through the ADC so $ENOB_{in} = 9.67 - 0.8 - 0.28 = \underline{8.59\text{bit}}$

- (b) This does not seem so nice, so using an external ADC and providing the sampling clock signal with the Arduino seems attractive. Now a guy on the Arduino forum programmed something and wrote: I just ran a test adding a timestamp to the analog output value. [...] At 20kHz, the *RMS* timing jitter is about 0.4 microseconds. If he uses this to sample audio up to 10kHz, what SJNR and ENOB will he get? And what timing jitter must he reach if he wants 16-bit resolution?

From Equation 13 one knows that $SNR = \frac{1}{8\pi^2 f^2 \sigma_j^2}$, therefore the SNR is $\frac{1}{8\cdot\pi^2\cdot(10\text{kHz})^2\cdot(0.4\text{ }\mu\text{s})^2} = 791.572 = 10 \cdot \log(791.572) = 28.98\text{dB} \Rightarrow ENOB = \frac{29.98\text{dB}-1.76\text{dB}}{6.02\text{dB}} = \underline{\underline{4.5\text{bit}}}$.

For a 16 bit resolution, one needs $16 \cdot 6.02 + 1.76 = 98.08\text{dB}$. Therefore $\sigma_j^2 = \frac{1}{8\cdot\pi^2\cdot(10\text{kHz})^2\cdot10^{\frac{98.08}{10}}} = \underline{\underline{(140\text{ps})^2}}$

4.3.1 Howland circuit noise

For the calculation have a look at Equation 7 and Figure 4f. From $V_i \Rightarrow I_y$

- $L_1 = \frac{-A \cdot G_2}{G_1 + G_2}$
- $L_2 = \frac{A \cdot G_3}{G_x + G_y + G_3}$
- $\Delta = 1 - L_1 - L_2 = 1 + \frac{A \cdot G_2}{G_1 + G_2} - \frac{A \cdot G_3}{G_x + G_y + G_3}$
- $\Delta_1 = 1 + \frac{A \cdot G_2}{G_1 + G_2}$
- $P_1 = \frac{G_x \cdot G_y}{G_x + G_y + G_3}$
- $T_{V_i \Rightarrow I_y} = \frac{V_{in}}{I_4} = \frac{\frac{G_x \cdot G_y}{G_x + G_y + G_3} \cdot \left(1 + \frac{A \cdot G_2}{G_1 + G_2}\right)}{1 + \frac{A \cdot G_2}{G_1 + G_2} - \frac{A \cdot G_3}{G_x + G_y + G_3}}$
 $T_{V_i \Rightarrow I_y}(G_1 = G_2 = G_3 = G) = \frac{\left(\frac{G_x \cdot G_y}{G_x + G_y + G_x}\right) \cdot \left(1 + \frac{A}{2}\right)}{1 + \frac{A}{2} - A \cdot G \cdot \frac{1}{G + G_x + G_y}} \cdot \frac{(G + G_y + G_x)}{(G + G_y + G_x)} = \frac{G_x \cdot G_y \cdot \left(1 + \frac{A}{2}\right)}{\left(1 + \frac{A}{2}\right)(G + G_x + G_y) - A \cdot G}$

From $I_{n_1} \Rightarrow I_y$ (influence of resistor noise R_1, R_2)

- $L_1 = \frac{-A \cdot G_2}{G_1 + G_2}$
- $L_2 = \frac{A \cdot G_3}{G_x + G_y + G_3}$
- $\Delta = 1 - L_1 - L_2 = 1 + \frac{A \cdot G_2}{G_1 + G_2} - \frac{A \cdot G_3}{G_x + G_y + G_3}$
- $\Delta_1 = 1$
- $P_1 = \frac{-A \cdot G_3 \cdot G_y}{(G_1 + G_2) \cdot (G_x + G_y + G_3)}$
- $T_{I_{n_1} \Rightarrow I_y} = \frac{V_{in}}{I_4} = \frac{\frac{-A \cdot G_3 \cdot G_y}{(G_1 + G_2) \cdot (G_x + G_y + G_3)} \cdot (1)}{1 + \frac{A \cdot G_2}{G_1 + G_2} - \frac{A \cdot G_3}{G_x + G_y + G_3}}$

Note when $G_x = G$ the current does not depend on G_y anymore, therefore we set in the equation below $G_1 = G_2 = G_3 = G_x = G$.

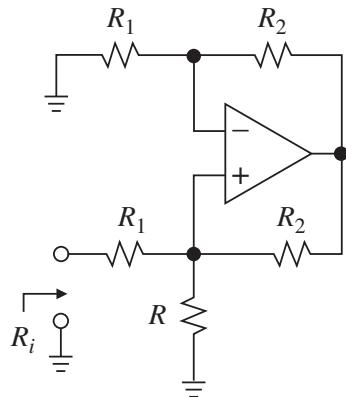
$$\frac{T_{I_{n_1} \Rightarrow I_y}}{T_{V_i \Rightarrow I_y}} = -\frac{A \cdot G_3}{(A \cdot G_2 + G_2 + G_1) \cdot G_x} \underset{G_1=G_2=G_3=G_x=G}{\overbrace{\Rightarrow}} -\frac{A}{A \cdot G + 2 \cdot G}$$

The same can be done for $T_{I_{nx} \Rightarrow I_y}$ (noise of resistor x and resistor 3) and $T_{V_n \Rightarrow I_y}$ (noise of opamp), which results in the following:

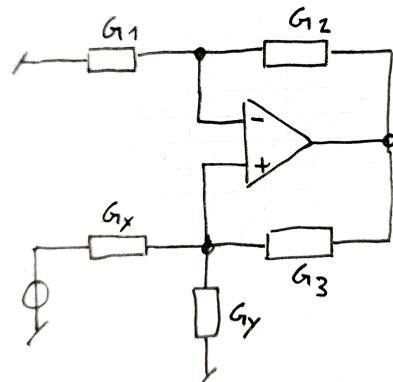
$$\frac{T_{I_{nx} \Rightarrow I_y}}{T_{V_i \Rightarrow I_y}} = \frac{1}{G}$$

$$\frac{T_{V_n \Rightarrow I_y}}{T_{V_i \Rightarrow I_y}} = \frac{2AG}{AG + 2G}$$

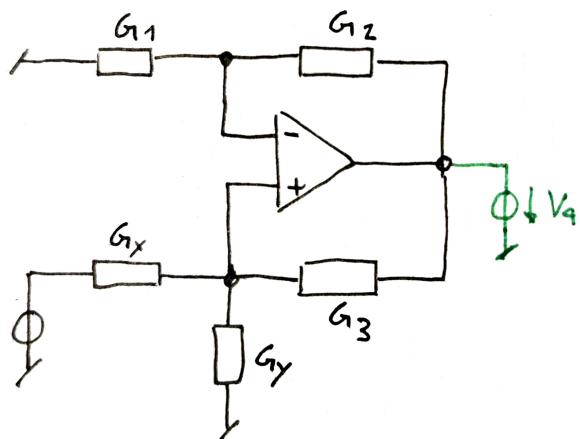
Therefore, the noise of the opamp has twice the influence as the noise of the input. And all resistors have the same influence on the noise, since both contribute in terms of absolute value $\frac{1}{G}$ times the input value.



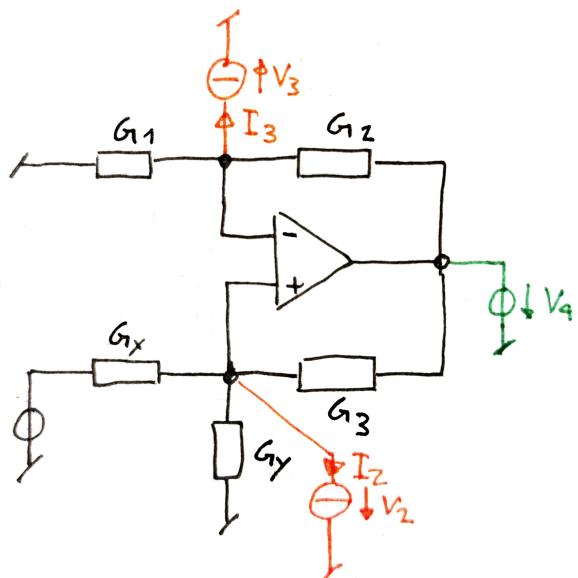
(a) Opamp circuit



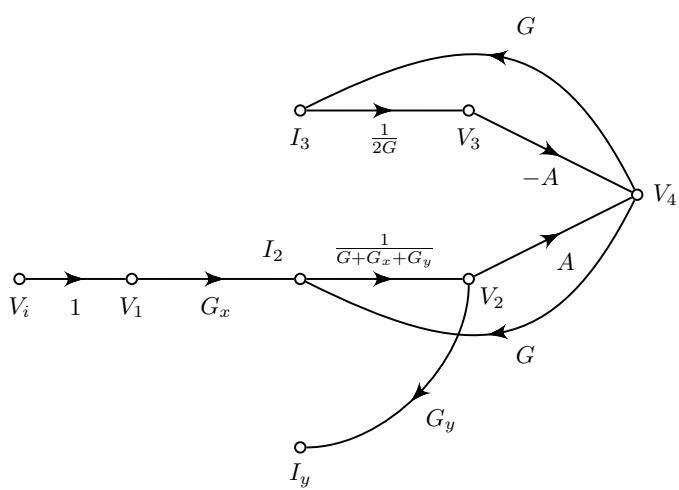
(b) Opamp circuit redrawn



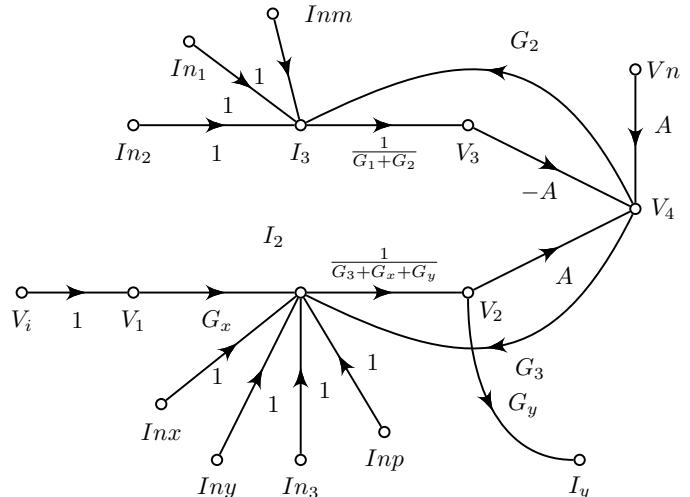
(c) Opamp circuit voltage source



(d) Opamp circuit voltage and current sources



(e) Opamp circuit signal flow graph



(f) Opamp circuit signal flow graph, with noise sources

5 Analog filters

5.1 Second Order

- Low Pass
- Band Pass
- High Pass

$$H(s) = \frac{\omega_p^2 \omega_p s s^2}{s^2 + \frac{w_p}{q_p} s + w_p^2} \cdot k \quad (20)$$

5.1.1 low pass filter

$$\begin{aligned} H(s) &= \frac{\omega_p^2 \cdot k}{s^2 + \frac{w_p}{q_p} s + w_p^2} \\ H(s) &= \frac{\omega_p^2 \cdot k}{s^2 + \frac{w_p}{q_p} s + w_p^2} \cdot \frac{\frac{1}{s^2}}{\frac{1}{s^2}} \\ &= \frac{b_p^2 / s^2}{1 + \underbrace{\frac{w_p}{q_p} \frac{1}{s} + \frac{\omega_p^2}{s^2}}_{\Delta = 1 - L_1 - L_2}} \end{aligned} \quad (21)$$

With the equation above, one could now take the rule of Mason and draw a signal flow graph as the one in Figure 16. This signal flow graph can then be translated in a circuit like the one from Figure 17.

$$\begin{aligned} L_1 &= -\frac{\omega_p}{q_p} \frac{1}{s} \\ L_2 &= -\frac{\omega_p^2}{s} \end{aligned}$$

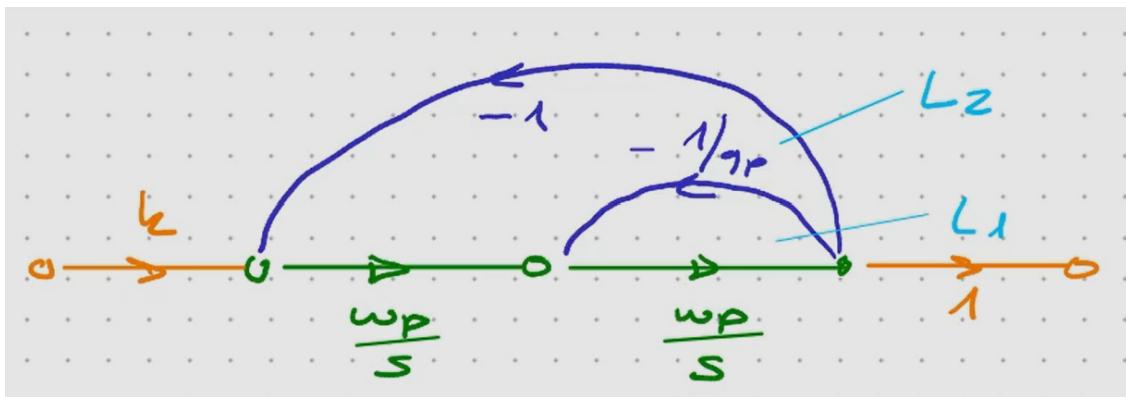


Abbildung 16: Signal flow graph low pass

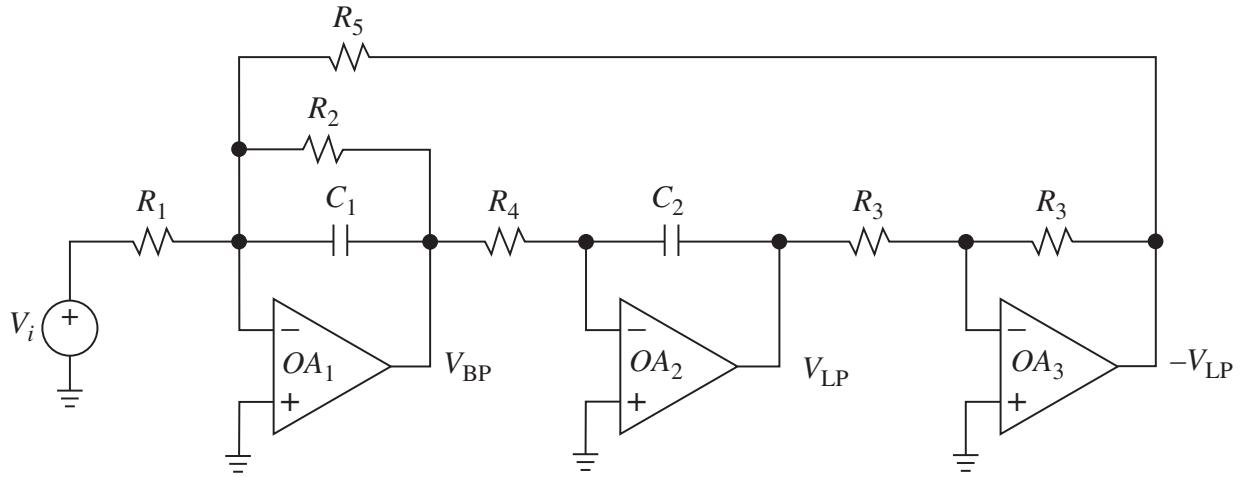


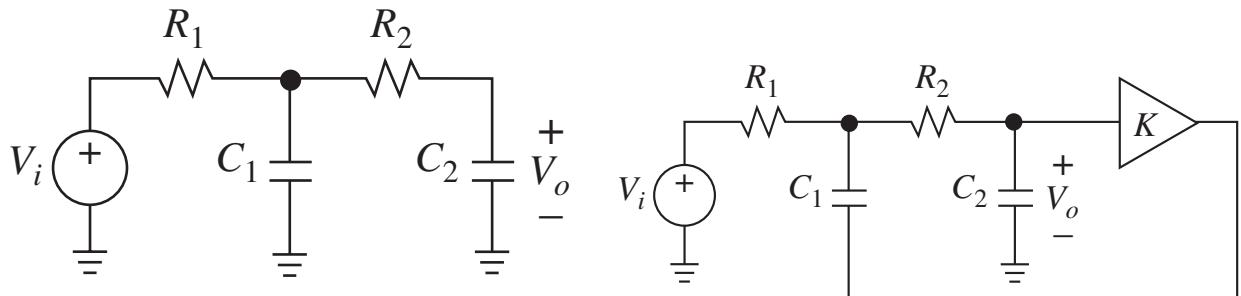
Abbildung 17: Tow-Thomas Filter/Biquad filter

5.1.2 high pass filter

5.1.3 band pass filter

5.1.4 KRC filters-or also Sallen-Key filters

With a passive low pass filter as it can be seen in Figure 18a it is only possible to achieve a Q-factor of 0.5 or less. One way to achieve a higher factor is by providing a controlled amount of positive feedback. In Figure 18b the output of the $R_2 - C_2$ stage is magnified by an amplifier with gain K , and then is fed back to the interstage node via C_1 , whose bottom terminal has been lifted off ground to create the positive feedback path. This feedback must be effective only in the vicinity of $\omega = \omega_0$, where bolstering is specifically needed. We can use physical insight to verify the band-pass nature of the feedback: for $\frac{\omega}{\omega_0} \ll 1$ the impedance of C_1 is simply too large to feed back much signal, whereas for $\frac{\omega}{\omega_0} \gg 1$, the shunting action by C_2 makes V_o too small to do much good. However, near $\frac{\omega}{\omega_0} = 1$ there will be feedback, which we can adjust for the desired amount of peaking by acting on K . Filters of the type of Fig. Figure 18b are aptly called **KRC** filters-or also Sallen-Key filters, for their inventors. When using

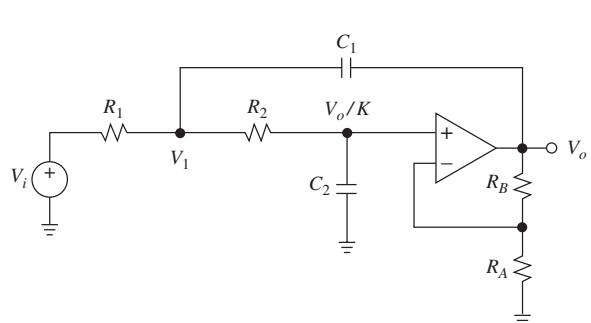


(a) Passive second-order low-pass filter

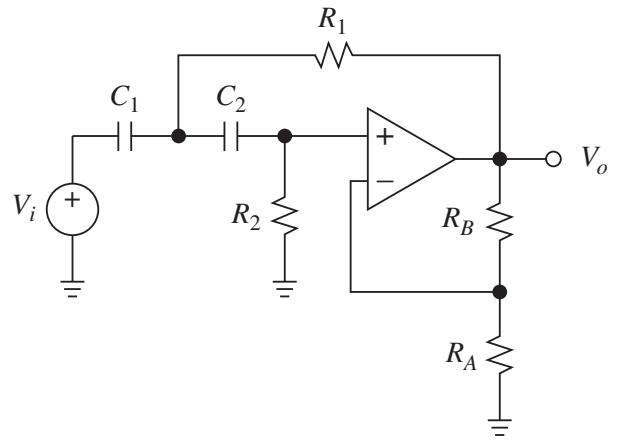
(b) Active realization of a second-order low-pass filter

a real opamp like in Figure 19a the gain can be configured with R_B and R_A , as it can be seen in Equation 22

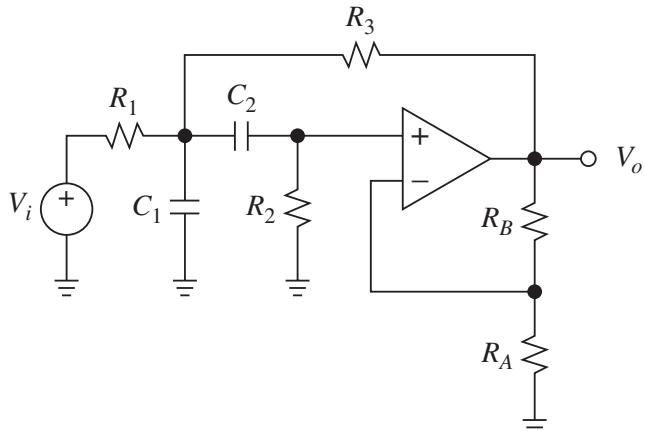
$$K = 1 + \frac{R_B}{R_A} \quad (22)$$



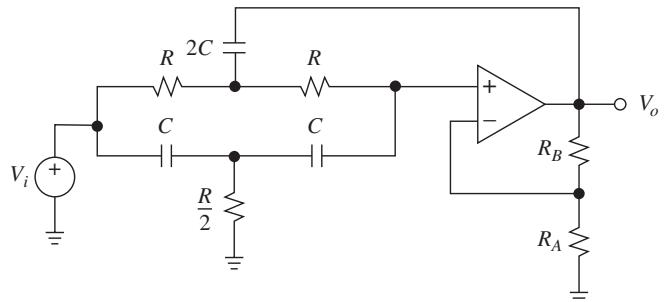
(a) Low-pass KRC filter



(b) High-pass KRC filter



(c) Band-pass KRC filter



(d) Band-reject KRC filter

6 Rectangular filters

When one wants to build a very rectangular filter, one uses normally a Bessel filter, which has the property that it is linear in the passband. Furthermore, the best filter we can build is an LC filter as one can see in Figure 20, because there it has been shown that signal that goes through the filter have a nearly unchanged shape. But the problem is that we hate inductors, since they are really large. Due to that one often simulates an inductor instead of using one. One way of doing that is by using a generalized impedance converter, as it can be seen in Figure 21a. The corresponding signal flow graph can be seen in Figure 21b. The idea behind it is that when we multiply every component by a factor, the transferfunction stays the same, which means when we multiply everything by s . A resistor becomes a capacitor and a inductor becomes a resistor and the inductor becomes a frequency dependent negative

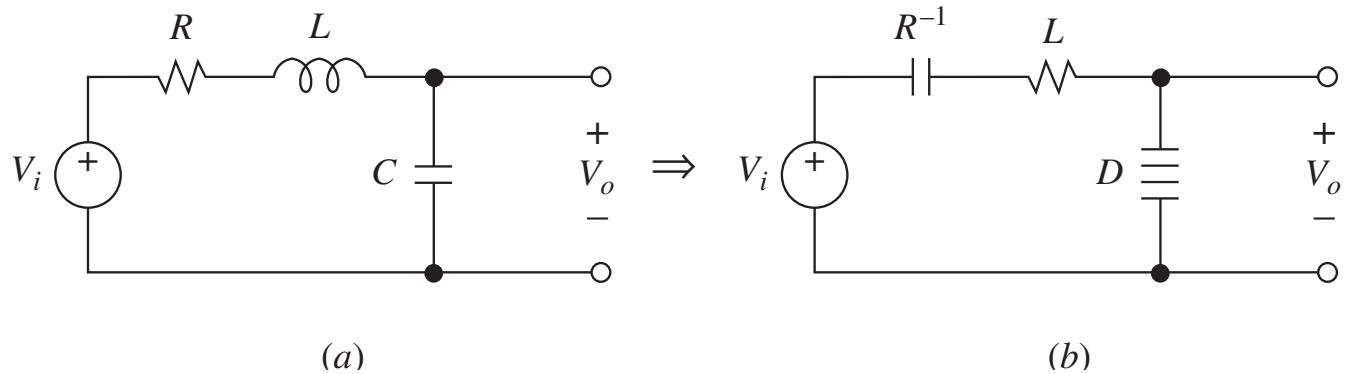
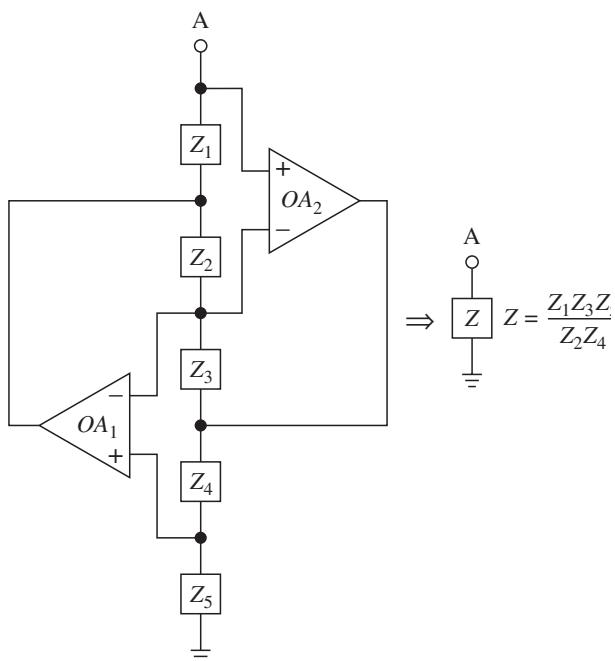


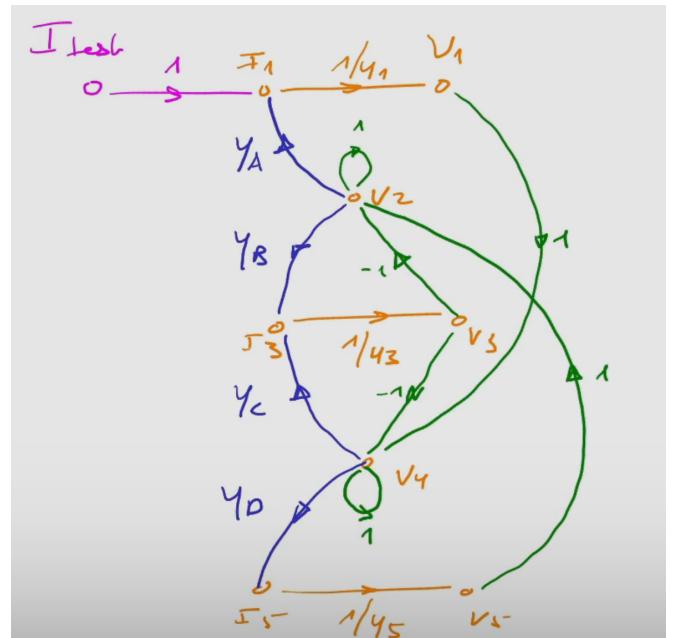
Abbildung 20: Low-pass RLC filter prototype and its CRD equivalent

resistor.

$$\begin{aligned} R &\rightarrow \frac{Rw_1}{s} \\ sL &\rightarrow \frac{sLw_1}{s} = Lw_1 \\ \frac{1}{sC} &\rightarrow \frac{1}{sC} \cdot \frac{w_1}{s} = \frac{1 \cdot w_1}{s^2 C} \end{aligned}$$



(a) Generalized impedance converter (GIC)



(b) GIC signal flow graph

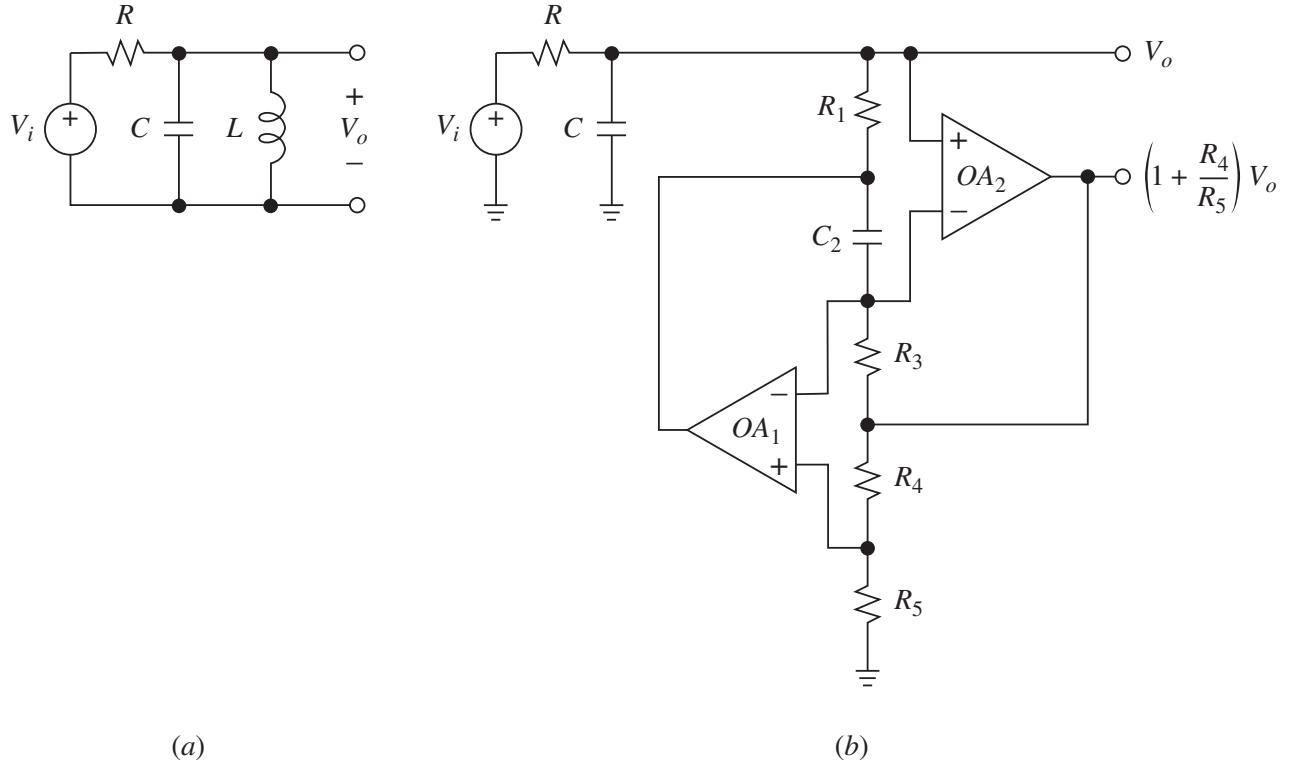


Abbildung 22: Passive band-pass filter prototype and (b) active realization using an inductance simulator.

6.1 Exercises1

Make a double-log drawing of the standard second-order band-pass filter,

$$T(s) = \frac{k\omega_p s}{s^2 + \frac{\omega_p}{q_p} s + \omega_p^2}$$

Repeat the same for the low-pass and high-pass filters,

$$T(s) = \frac{k\omega_p^2}{s^2 + \frac{\omega_p}{q_p} s + \omega_p^2}, \quad T(s) = \frac{ks^2}{s^2 + \frac{\omega_p}{q_p} s + \omega_p^2}$$

Solution From Figure 29 one knows that the numerator is a straight line which goes through the amplitude 0dB at the point $\frac{1}{k\cdot\omega_p}$. Furthermore, one knows from Figure 28 that the denominator causes a gain of $\frac{1}{\omega_p^2}$ for $\omega \ll \omega_p$. For $\omega \gg \omega_p$ it decreases with -40dB/Dec. Furthermore, its peak has a height of $20 \cdot \log(q_p)$. Therefore one would get the green graph in Figure 24. Also the other solutions can be found there.

6.2 Exercises2

Analyse the circuit visible in Figure 25.

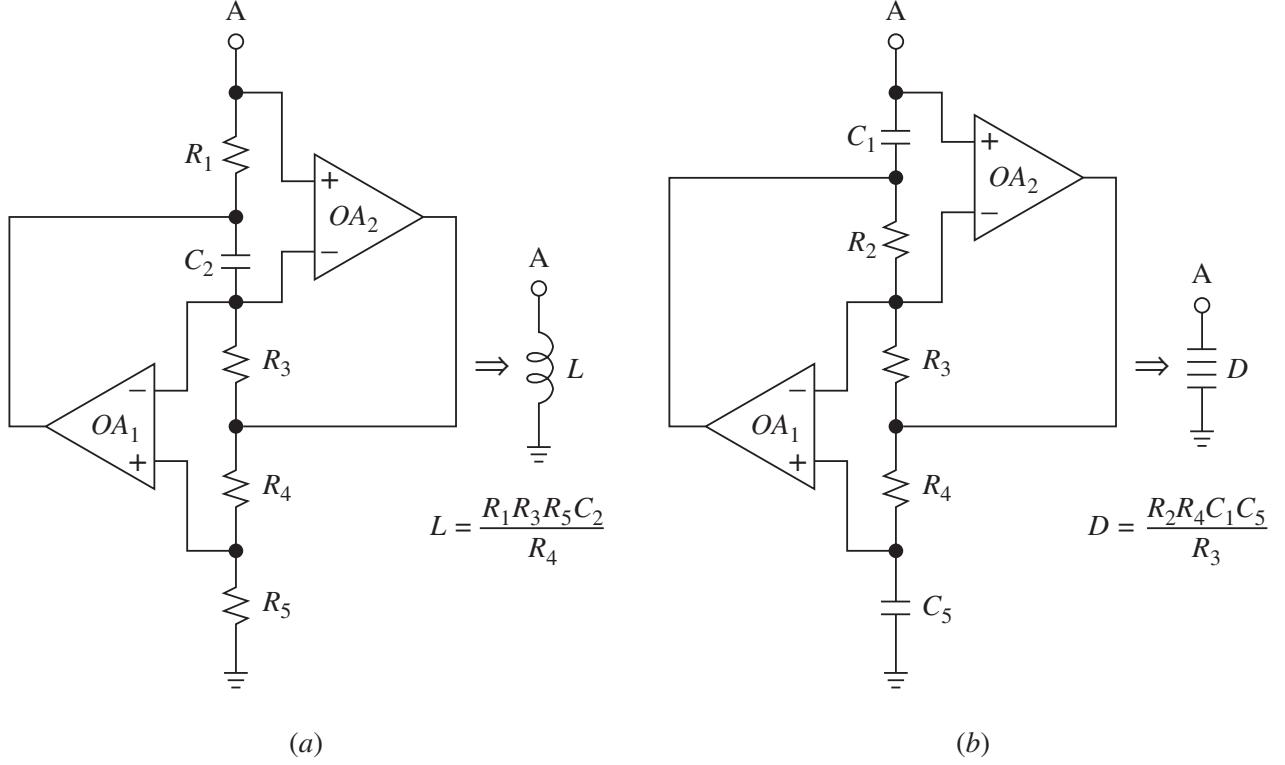


Abbildung 23: (a) Inductance simulator and (b) D-element realization.

Solution When one draws the Signal flow graph one gets Figure 26: When one now analyses the circuit one gets the following:

$$\begin{aligned}
 L_1 &= \frac{s \cdot C}{G + \frac{G}{m} + s \cdot C} \\
 L_2 &= \frac{G}{n \cdot \left(\frac{G}{n} + s \cdot C \right)} \\
 L_3 &= \frac{s \cdot C}{\frac{G}{n} + s \cdot C} \\
 L_4 &= 1 \\
 L_5 &= 1 \\
 P_1 &= G \cdot \frac{1}{G + \frac{G}{m} + s \cdot C} \cdot (-1) \cdot \frac{G}{n} \cdot \frac{1}{\frac{G}{n} + s \cdot C} \cdot (-1) \\
 \Delta &= 1 - L_1 - L_2 - L_3 - 1 - 1 + L_1 \cdot L_3 + L_1 + L_3 + 1 \\
 T &= \frac{P_1}{\Delta} = -\frac{G^2}{-C^2 n s^2 - C G s - \frac{G^2(m+1)}{m}}
 \end{aligned}$$

Now we have to normalize the numerator and denominator: For the denominator one gets the following:

$$s^2 + \frac{Gs}{Cn} + \frac{G^2}{C^2 n} + \frac{G^2}{C^2 m n}$$

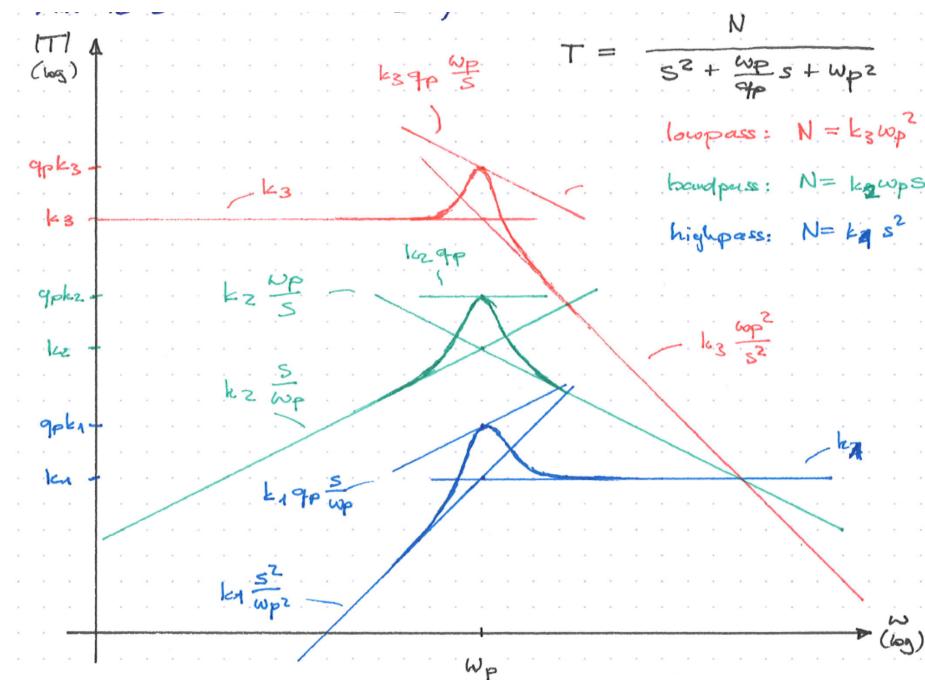


Abbildung 24: Solution of bode plot exercise

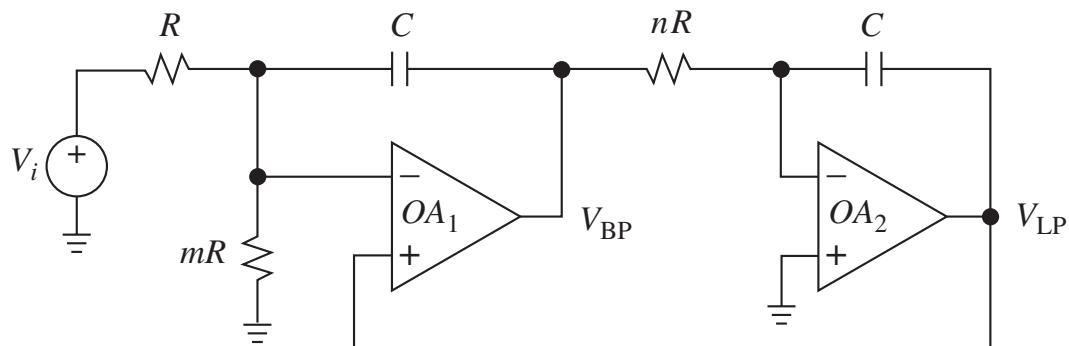


Abbildung 25: Tow-Thomas biquad

and therefore for the numerator

$$\frac{G^2}{C^2 n}$$

Due to that one gets a low pass filter:

$$T(s) = \frac{k\omega_p^2}{s^2 + \frac{\omega_p}{q_p} s + \omega_p^2}$$

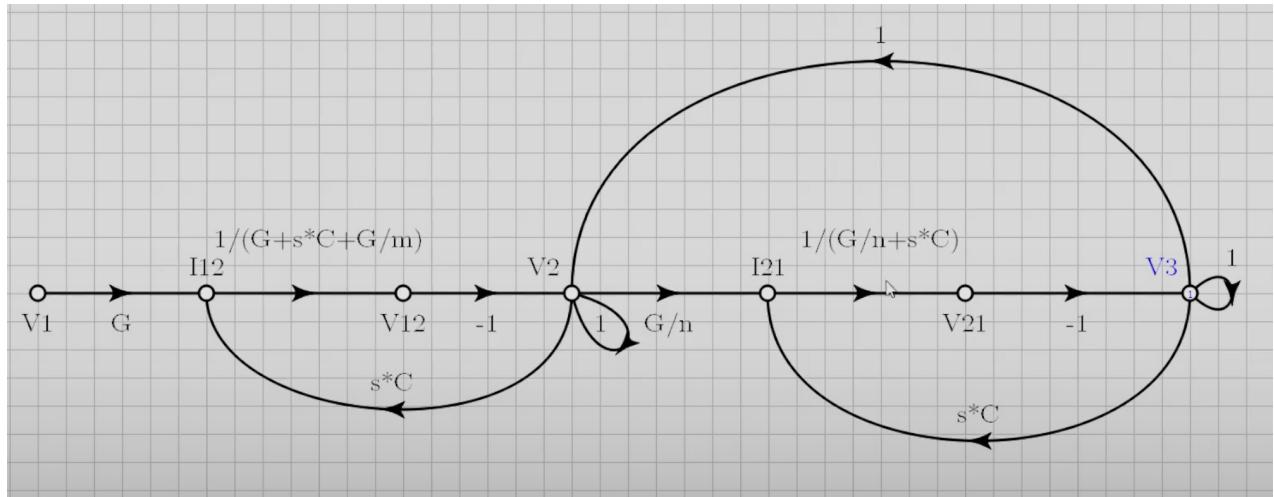


Abbildung 26: Signal Flow graph Tow-Thompson

with

$$\omega_p^2 = \frac{G^2(m+1)}{C^2mn}$$

$$\frac{\omega_p}{q_p} = \frac{G}{Cn}$$

$$k\omega_p^2 = \frac{G^2}{C^2n}$$

$$G = \frac{1}{s + a}$$

$a = -1$ $a = 0$ $a = +1$

$$\omega_g = |a| \Rightarrow$$

$$\angle G(j\omega_g) = -45^\circ / -135^\circ$$

$$|G(j\omega_g)| = \frac{1}{\sqrt{2}} \approx -3 \text{ dB}$$

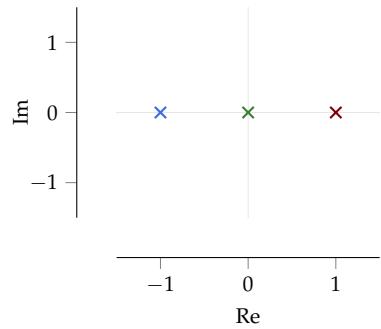
$$\omega \ll \omega_g :$$

$$|G| \approx \frac{1}{|a|}$$

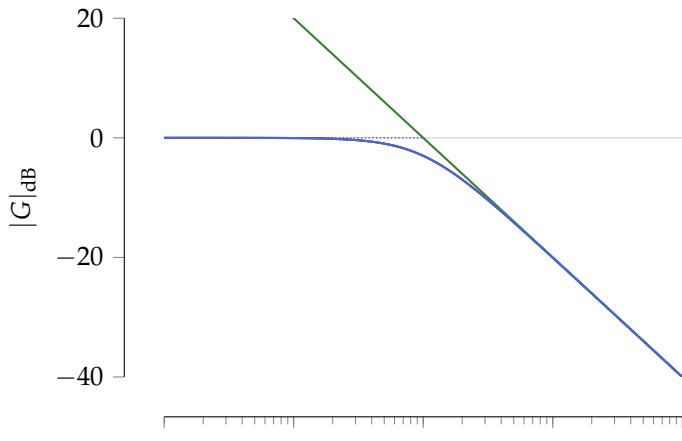
$$\omega_g \ll \omega :$$

$$|G| \propto -20 \text{ dB/Dek.}$$

Pol-Nullstellenplan



Bodediagramm



Sprungantwort

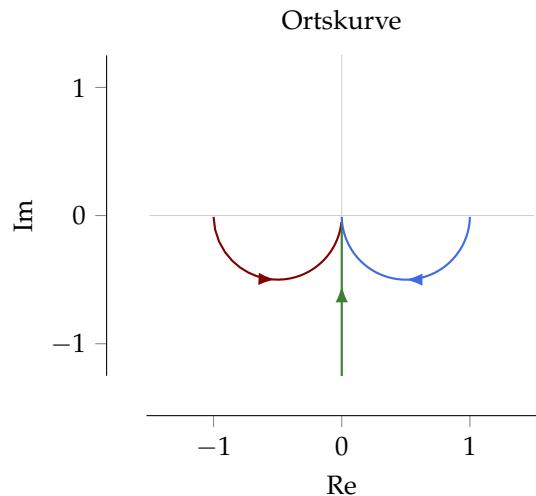
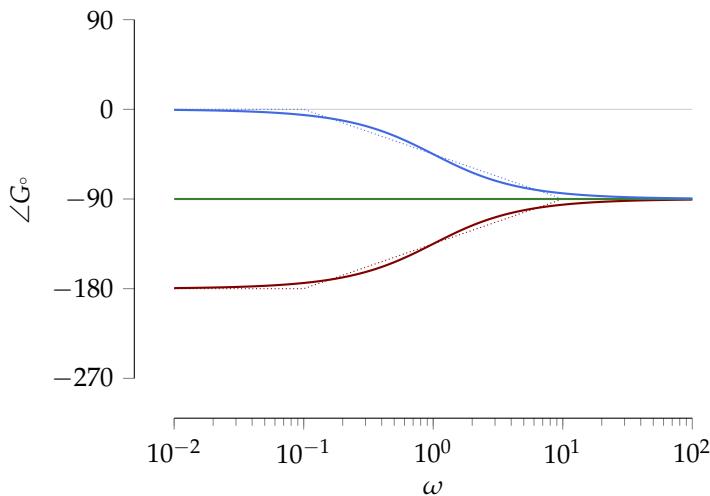
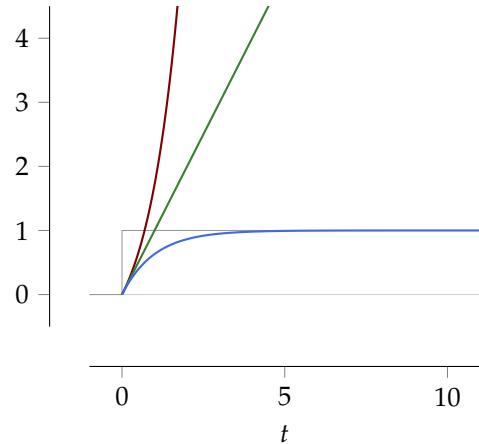


Abbildung 27: real pole: $\dot{y} + ay = u$

$$\frac{1}{s^2 + 2\zeta\omega_0 s + \omega_0^2}$$

$\omega_0 = 1$ $\zeta = 1$ $\zeta = 0.5$ $\zeta = 0.1$
 $\angle G(j\omega_0) = -90^\circ$
 $\omega \ll \omega_0 :$ $|G| \approx 1/\omega_0^2$
 $\omega_0 \ll \omega :$ $|G| \propto -40 \text{ dB/Dek.}$
 $M_p = e^{-\pi\zeta/\sqrt{1-\zeta^2}}$ relatives Überschiessen

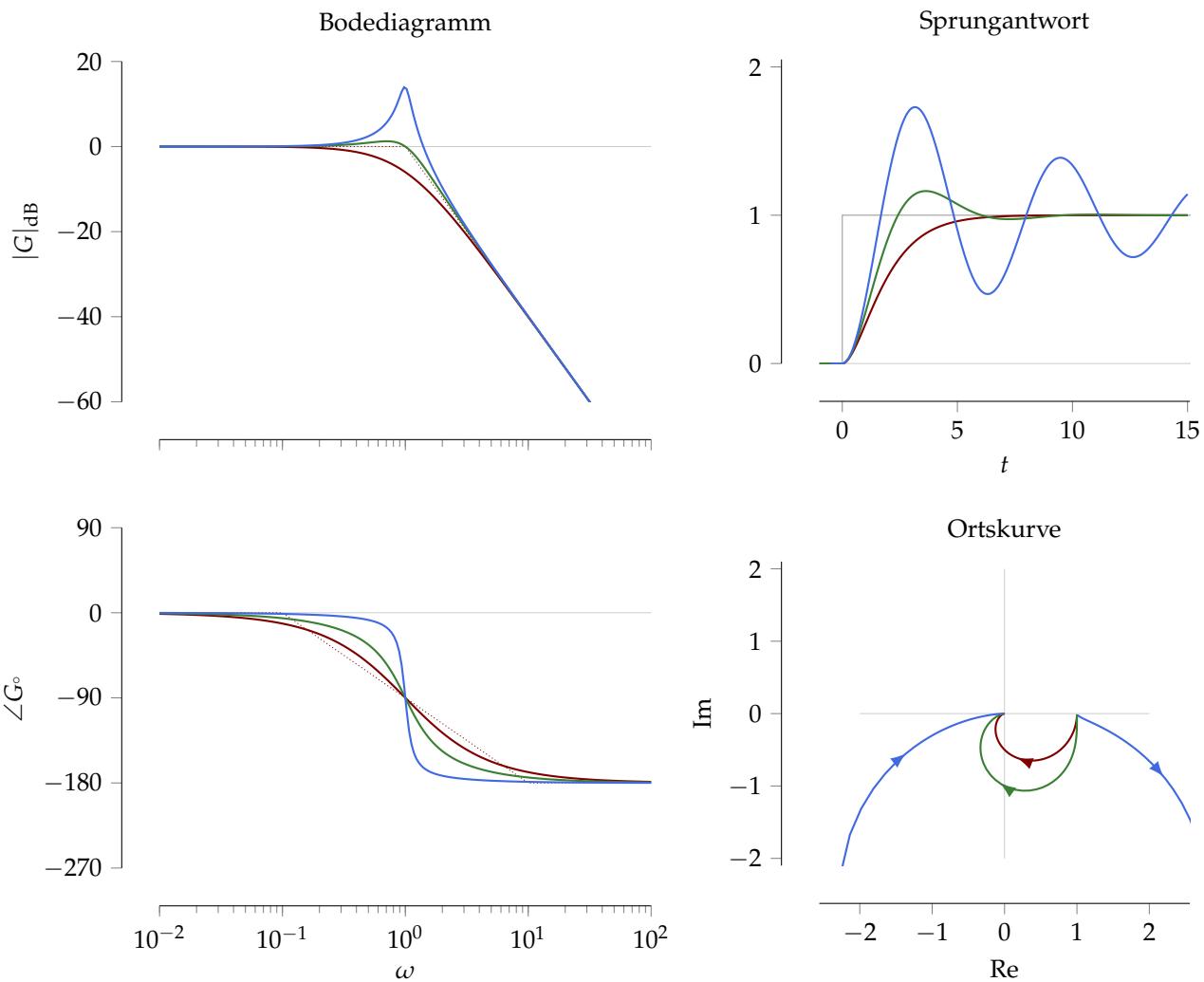
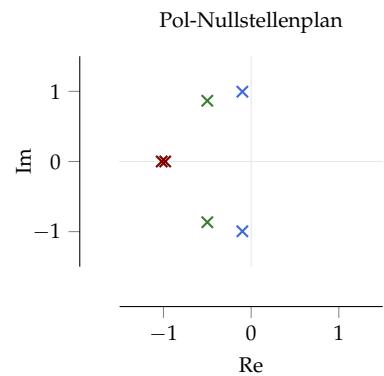


Abbildung 28: conjugate complex Pole pair : $\ddot{y} + 2a\dot{y} + by = u$.

$$\begin{aligned}
G &= s + a & a = -1 \quad a = 0 \quad a = +1 \\
\omega_g &= |a| \quad \Rightarrow \quad & \angle G(j\omega_g) = +45^\circ / +135^\circ \\
\omega &\ll \omega_g : & |G(j\omega_g)| = \sqrt{2} \approx +3 \text{ dB} \\
\omega_g &\ll \omega : & |G| \approx |a| \\
&& |G| \propto +20 \text{ dB/Dek.}
\end{aligned}$$

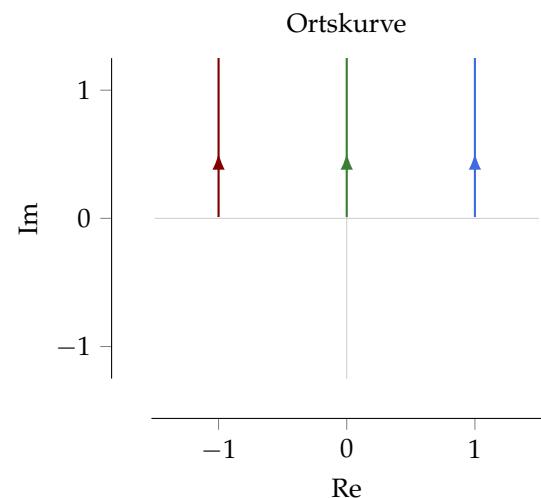
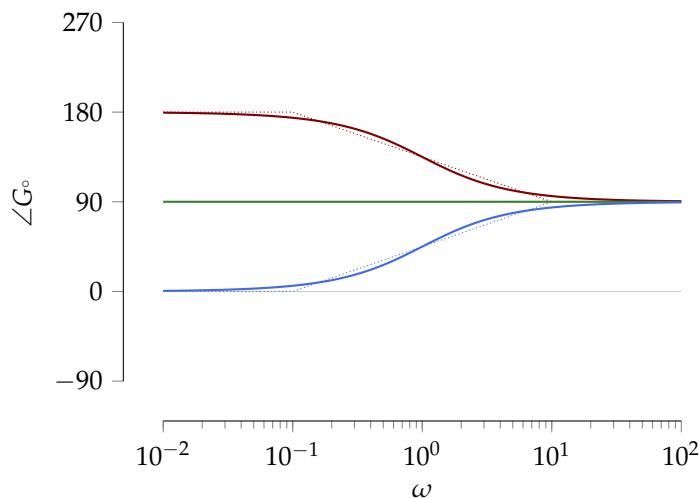
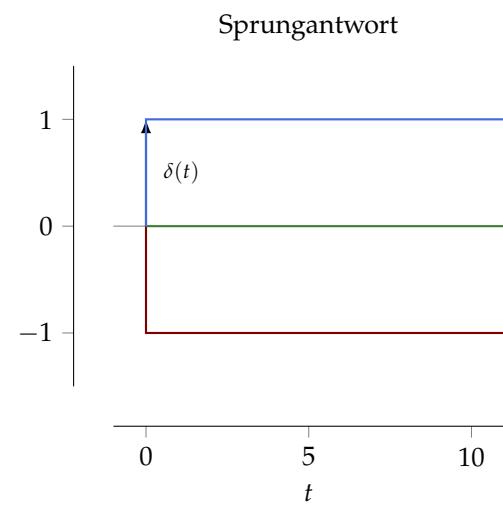
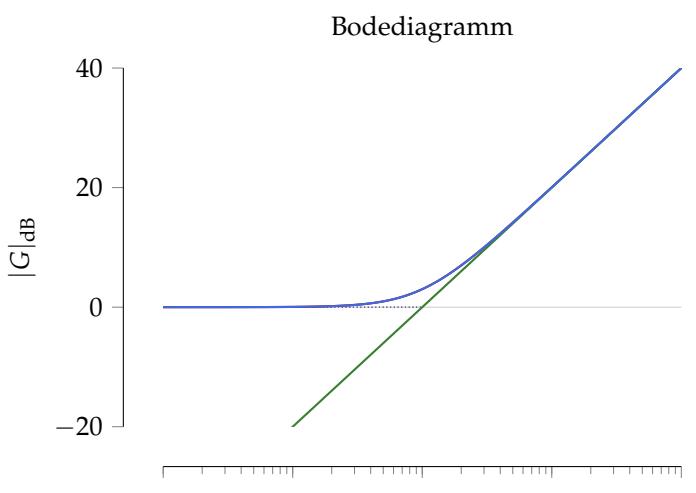
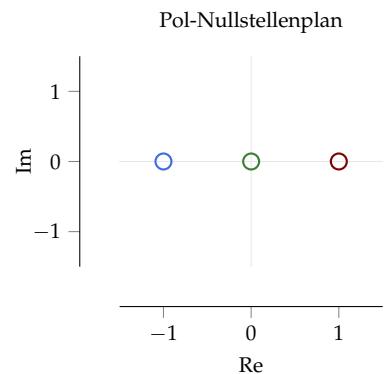
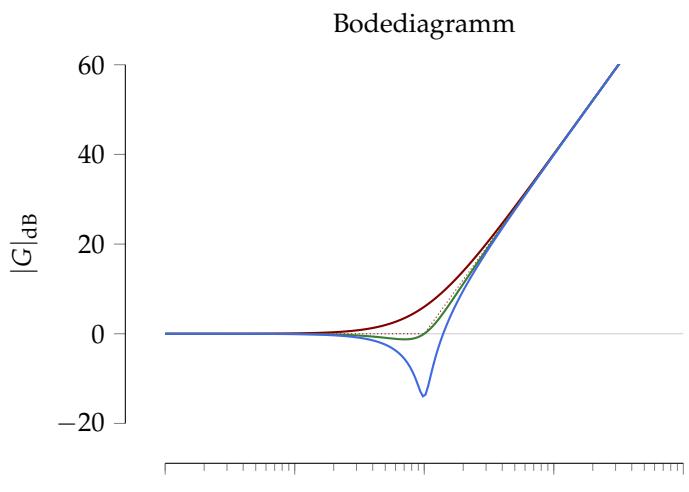
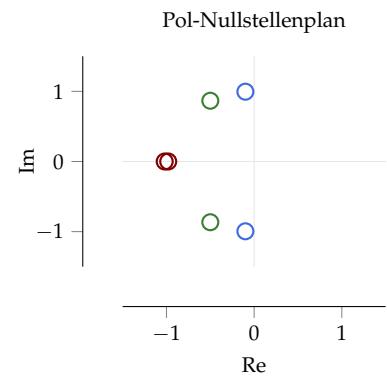


Abbildung 29: real zero : $y = \dot{u} + au$

$$\begin{aligned}
& s^2 + 2\zeta\omega_0 s + \omega_0^2 \\
& \omega_0 = 1 \quad \zeta = 1 \quad \zeta = 0.5 \quad \zeta = 0.1 \\
& \angle G(j\omega_0) = +90^\circ \\
\omega \ll \omega_0 : & \quad |G| \approx \omega_0^2 \\
\omega_0 \ll \omega : & \quad |G| \propto +40 \text{ dB/Dek.}
\end{aligned}$$



Sprungantwort

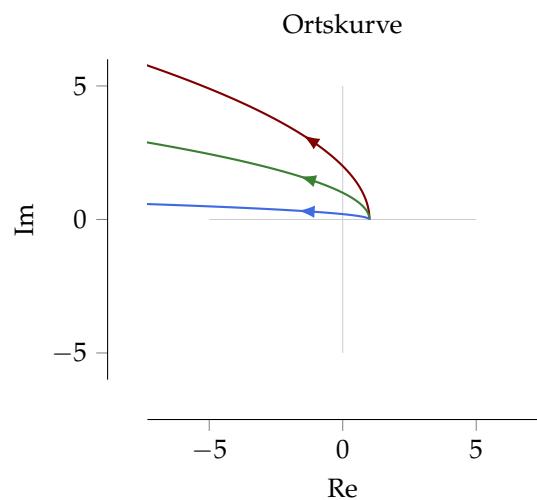
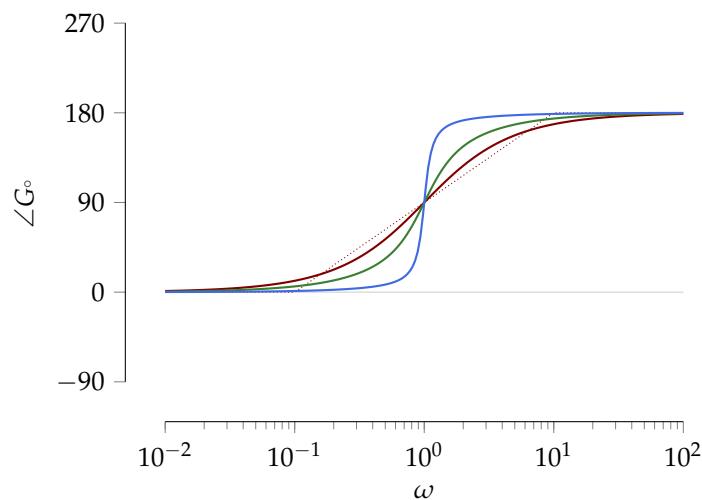
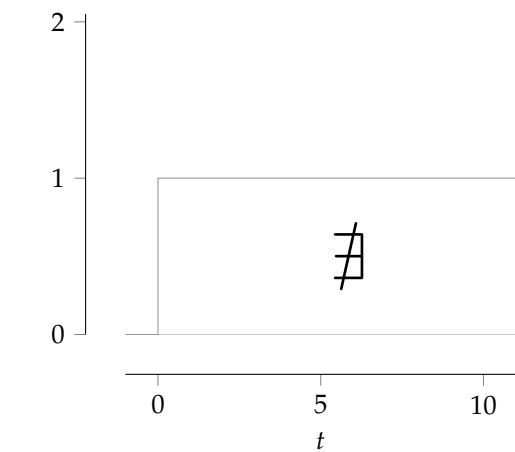


Abbildung 30: conjugate complex zero pair : $y = \ddot{u} + 2a\dot{u} + bu$.

7 Digital

7.1 Calculations of propagation delays on a PCB

symbol naming

1. t_{rf} Rise fall time of a system
2. t_{PD} propagation speed [$\frac{ps}{inch}$] or [$\frac{s}{meter}$] for FR4 $\epsilon_r = 4 \rightarrow \frac{\sqrt{4}}{3 \times 10^8 \text{ m s}^{-1}} = 6.66 \text{ ns m}^{-1}$ (which is about 170 ps m^{-1})
3. L Length of rising edge

Propagation Delay of ideal (lossless) Transmission Line:

$$t_{PD} = \sqrt{L_{\Delta x} \cdot C_{\Delta x}}$$

7.2 Propagation delay calculation with a given dielectric constant ϵ_r

$$t_{PD} = \frac{\sqrt{\epsilon_r}}{c}$$

$$1 \text{ ns m}^{-1} \approx 0.0254 \frac{\text{ns}}{\text{inch}}$$

7.2.1 Example, what is the t_{PD} in nanoseconds per inch for a given ϵ_r

Given is the following:

- $\epsilon_r = 4.5$

$$t_{PD} = \frac{\sqrt{4.5}}{3 \times 10^8 \text{ m s}^{-1}} = 7.08 \times 10^{-9} \text{ s m}^{-1} = 0.18 \frac{\text{ns}}{\text{inch}}$$

With TI nspire type in the following $\frac{\sqrt{4.5}}{c} \blacktriangleright \frac{\text{ns}}{\text{in}} \Rightarrow 0.18 \frac{\text{ns}}{\text{in}}$

7.2.2 Signal Degradation Effect

The wire line is a low pass filter, attenuation rises by 1 dB/m per decade.

7.2.3 Signal Degradation Effect

pre emphasize output signal to compensate low pass filter effects. Does one not add even higher frequencies and they get even more compensated?

We have traces laid out on a PCB using copper wires on FR4 material. What is the wire delay for a trace of 100 mm length

$$6.66 \text{ ns m}^{-1} \cdot 0.1 \text{ m} = \underline{\underline{0.67 \text{ ns}}}$$

Understanding signaling methods

- What is the difference between bit rate and symbol rate? What are the units for the two rates?
Bit Rate: (digital information) Bits per Second
Symbol Rate: Signal changes per second (Baud - NOT "Baud-per-second"). e.g. in QAM256 there are 256 values transmitted in one symbol, i.e. 8 bits in one symbol
- Suppose a QAM-256 System in DVB-C (=today's HDTV over cable) on a 8MHz channel. Forward error correction is done with Reed-Solomon RS (204,188) code (which means that 188 used bytes are coded into 204 transmitted bytes) and (due to SNR) a ratio of 1.15 between bandwidth and symbol rate. What is the resulting maximal bit rate?

Channel Width: 8 MHz

Bandwidth / Symbol Rate: 1.15

Reed-Solomon 204/188 = 1.085106

Bits per Symbol = 8

Max. Bit Rate = $8 \text{ MHz} \cdot 8 \cdot \frac{1}{1.15} \cdot \frac{188}{204} = 51.2873 \text{ Mbit s}^{-1}$

Bandwidth examples:

- MPEG-2 coded SDTV Signal: around 3.5 Mbit/s
- MPEG-4 for HDTV 8..15 Mbit/s
- 4K TV: Amazon recommends at least 15 megabits per second, Netflix advises 25 Mbps
- BlueRay Disc has max. 40Mbit/s

Compare data rates

- What are max. data rates of parallel systems (such as SCSI etc.) and serial systems? data rates of parallel interfaces (such as Centronics[old printing connection] etc.) are typically much lower than serial channels, because classic parallel interfaces use an asynchronous signalling requiring 2 - 3 clock cycles for one transfer. serial interfaces can also be multiplied in parallel, but since they are synchronous they can transport up to 2 bits per clock cycle (DDR interfaces).

Note: USB and SATA are serial interfaces

Why are we using serial instead of parallel today:

- In parallel connection all data of the lines should arrive at the same time at very high frequencies this is difficult to achieve
- crosstalk: signal gets from one line to the others, which should not happen.
- lots of pins, easy to break one

Note a graphic card also has a lot of PCI lines but each of these has its own clock, they are independent of each other, not as in parallel connection

- Which type of communication system (parallel data or serial data) allows for a higher data rate at similar power consumption?

the power consumption is lower in LVDS (Low Voltage Differential Signaling) interfaces due to the lower voltage swing. besides that the power consumption is basically linked to the frequency - i.e. independent of "parallelör serial". But a good signal coding can reduce the number of transitions (e.g. Gray Code instead of standard binary coding)

- **Why?**

see above

Differential signaling

- **What is the reason for differential signaling?**

remove need for a ground line (note: grounding is still a good choice just for bonding reasons!), remove common mode noise, allow for AC coupling avoiding ground coupling problems

- **Give examples of differential signaling methods**

LVDS, PCI Express

- **Explain the function of the SGMII / QSGMII interface and the usage of SERDES**

The MII (Media Independent Interface) is the interface between MAC and PHY. For the fastest protocols, a serial interface is used (SGMII with 1.25 Gbps dual-data-rate path and QSGMII for four lines with a 5 Gbps dual-datarate path). Modern FPGA can directly interface by using their SERDES interfaces - see application notes from Altera/Intel and Xilinx.

CDR

- **What is the reason to use clock data recovery?**

clock data recovery is necessary whenever there is no clock transported - and by that one (high power) signal line is removed.

- **What is the reason for the use of n-th-rate phase detector?**

When the data rate is so high that the design of a VCO with the frequency of that data rate becomes too complex. Then the design of the VCO can be simplified by reducing its frequency by a factor of 2^n and using a n -th-rate phase detector

- **What are the characteristic differences between the CDR methods?**

The different methods characterize by

- Proportional or "bang-bang" phase detectors
- VCO (or low speed NCO) or full digital solution by re-timing
- Computing requirement / precision
- Phase Detector / Timing Error Detector are functionally the same

Converting Meters

1 metre	\approx	1.0936	yard
1 metre	\approx	39.370	inches
1 centimetre	\approx	0.39370	inch
1 millimetre	\approx	0.039370	inch

7.3 Signalling Methods

7.3.1 Isochronous clock free

You recover the clock out of the data.

7.3.2 Parallel Signalling vs Serial Signalling

7.3.3 Signal encoding

7.3.4 Differential Signaling LVDS

7.3.5 QAM

7.3.6 Shannon Theorem

What are max. data rates of parallel systems (such as SCSI etc.) and serial systems? HD TV has 10 to 12 Mbit/s

Why do we still see active value to zero: This comes from the TTL transistors, one had like nmos transistors only, so the nmos is connected to a pull up resistor. When it is normally low always a certain current will flow, therefore it is normally one. Today with CMOS it does not matter anymore.

An edge detector can be manufactured with an delay element (like d-flipflop) and an xor.

A flipflop is two latches behind each other.

One mux with feedback is a transparent latch.

Powerconsumption can be reduced when used with double edge triggered flipflop (DET FF), since the clock network consumes quite some power.

Digital oscillators have high frequency jitter.

analog oscillators have low frequency jitter.

7.4 Questions for the lecture

- What do we need to know about clock data recovery, different topologies?
-

8 Delays

- t_{DQSCK} describes the allowed range for a rising data strobe relative to CK, CK# (Spec: -400ps .. +400ps)
- t_{PCQ} max clock-to-output delay of flip-flop
- t_{Setup} max. data setup time to clock (time the signal must be signal)
- t_{NET} max. data path between flip-flops (time signal has to propagate)
- t_{CLK} the two different clocks are not exactly at the same time

Static simulation, calculates the theoretical worst possible delay (it is maybe too pessimistic, only works in the same clock region) in dynamic timing analysis might be too optimistic
 receiving flip flop: stable time
 sending flip flop time delay from clock to the output

When the slack is positive we have some margin, otherwise we have issues (clock period is smaller than the path delay)

In the FPGA one has to define a multi clock cycle path. (Define slow elements)

Estimate the clock behaviour e.g. in a 74AC technology from Texas Instruments: (see Figure 31)

Example 1: Counter

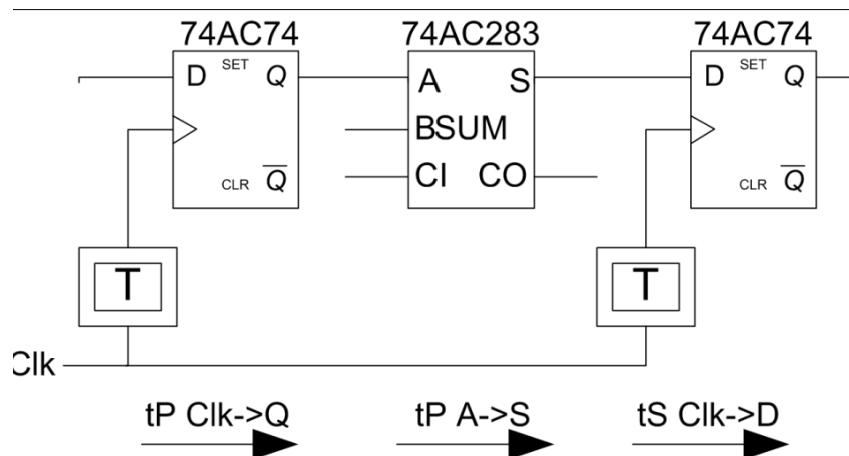


Abbildung 31: Circuit

- What is the delay of a circuit in AC technology, e.g. 4 bit full adder (74283) at 1.5V / 3.3V / 5V

From the datasheet one knows that the propagation delay for An or Bn to Sn is (note the timing for rising and falling edge is the same $t_{PLH} = t_{PHL}$):

- 1.5V: 207ns
- 3.3V: 23.2ns
- 5V: 16.5ns

- What are setup- and propagation times of a D-Flip-Flop in AC technology (7474)

From the datasheet one knows that:

- t_{SU} (Setup time): 3.1ns
 - t_{PLH} (Propagation time high): 9.1ns
 - t_{PLL} (Propagation time low): 9.1ns
- What is the resulting maximal clock frequency of a "4 bit counter" built out of the two circuits? (Q-output of the DFF connected to B-input of the adder, S output of the adder connected to the D-input of the DFF)
When we assume to operate it at 5V. One gets a total delay of $9.1\text{ ns} + 16.5\text{ ns} + 3.1\text{ ns} = 34.7\text{ ns} \Rightarrow 25.8\text{ MHz}$. Which is the time the rising edge needs to propagate through 74AC734 then through 74AC283 and finally the setup time, the time the output must be stable on the next flip flop input.
 - What is the maximal clock frequency if the clock has a skew of 10 ns
When the clock has an additional skew one just adds the skew to the propagation time and gets: $9.1\text{ ns} + 16.5\text{ ns} + 3.1\text{ ns} + 10\text{ ns} = 38.7\text{ ns} \Rightarrow 25.8\text{ MHz}$

Example 2: Shift Register

- What are the most important specifications for timing, when implementing a shift register with the 74AC components from before?
 - Propagation delays through gates / flipflops, setup times, hold times (typically not important), wire delays and their dependency from voltage and temperature
 - Worst case (longest delay / lowest frequency) is with highest temperature and lowest voltage from specification!
- What is the maximal clock frequency for a "shift register" (Q-output of a DFF connected to the D-input of the next DFF)
Connect Q of flipflop directly with D of next flipflop. Path delay is CLK \Rightarrow Q propagation delay of first flipflop + wire delay (can normally be neglected) + setup time of next flipflop. In this case: $9.1\text{ ns} + 3.1\text{ ns} = 12.2\text{ ns} \Rightarrow 81.97\text{ MHz}$
- What is the effect if the clock has a skew of 10 ns?
 $9.1\text{ ns} + 3.1\text{ ns} + 10\text{ ns} = 22.2\text{ ns} \Rightarrow 45.045\text{ MHz}$

Timing Behaviour

- How does a gate delay behave if
 - The temperature rises **delay is increased**
 - the process gets better **delay is decreases**
 - the supply voltage is decreased **delay is increased**
- How does a wiring delay behave if
 - the device is cooled down **no major influence**
 - the IC process gets worse **no major influence**
 - the supply voltage is increased **no major influence**

9 Clock, Clock skew, clock skitter

The clock and the asynchronous reset are the only signal which are triggered on the edge.

Clock skew changes over the position measured

race condition is when the data path is faster than the clock path

Clock jitter is not stable over time.

9.1 Exercises:

If it happens that cooling spray was overused on INV2 which is now cooled down to -40°C , what would be the maximum allowed clock skew between the clock inputs of the two D-flip-flops DFF1 and DFF2?

Consider the following information:

- assume the circuit from Figure 32 and the datasheet from Figure 33
- The circuit is operated at 5V (if no data is available for 5V take the closest specification).
- The signal "Clk" has a frequency of 40 MHz with a 50% duty cycle
- All devices are operated at 85°C (if not mentioned differently below)
- Every wire is expected to have a capacity of 40 pF and 0Ω resistance.
- The devices are from the family SN74ACxx by Texas Instruments. Excerpts of the data sheets of SN74AC04 and SN74AC74 are found in Figure 33.

From Figure 33 one knows that the inverter has a max propagation delay of $t_{PLH} = 7.5 \text{ ns}$ in the temperature range of -40°C to 85°C . Furthermore, the clock period is $\frac{1}{40 \text{ MHz}} = 25 \text{ ns}$. The propagation delay of the d-flipflop is maximal 10.5 ns and the setup time 3 ns. Therefore, the slack is $25 \text{ ns} - 10.5 \text{ ns} - 7.5 \text{ ns} - 3 \text{ ns} = 4 \text{ ns} \Rightarrow \frac{1}{21 \text{ ns}} = 47.619 \text{ MHz}$

Furthermore, one is not able to say how the delay of the inverter behaves when the temperature is -40°C . The two inverters could also have at normal temperature a completely different delay, see datasheet $T_A = 25^{\circ}\text{C}$. But what one could say is that in the worst case the INV2 is much faster than INV1 and would have the minimal delay of 1 ns, which would reduce the slack by a value of 6.5 ns, which would result in a total slack of $-2.5 \text{ ns} \Rightarrow \frac{1}{27.5 \text{ ns}} = 36.3636 \text{ MHz}$

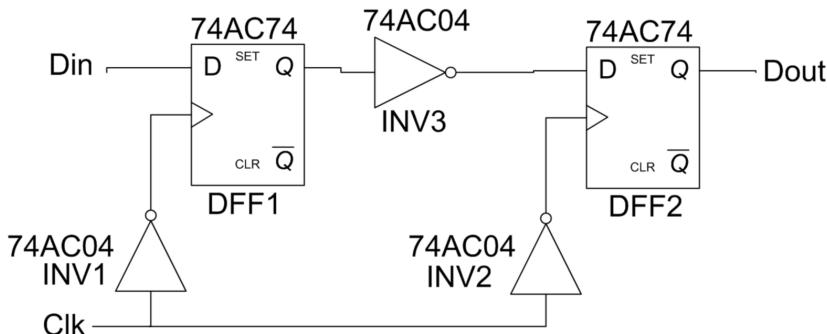


Abbildung 32: Circuit

– SN74AC04:

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			SN54AC04		SN74AC04		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.5	4	7	1	8.5	1	7.5	ns
t_{PHL}			1.5	3.5	6.5	1	7.5	1	7	

– SN74AC74:

timing requirements over recommended operating free-air temperature range,
 $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (unless otherwise noted) (see Figure 1)

			$T_A = 25^\circ\text{C}$		SN54AC74		SN74AC74		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			140		95		125	MHz
t_w	Pulse duration		PRE or $\overline{\text{CLR}}$ low	4.5		5.5		5	ns
			CLK	4.5		5.5		5	
t_{SU}	Setup time, data before CLK^\uparrow		Data	3		4		3	ns
			PRE or $\overline{\text{CLR}}$ inactive	0		0.5		0	
t_h	Hold time, data after CLK^\uparrow			0.5		0.5		0.5	ns

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			SN54AC74		SN74AC74		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			140	160		95		125		MHz
t_{PLH}	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or \overline{Q}	2.5	6	9	1	9.5	2	10	ns
			3	8	9.5	1	10.5	2.5	10.5	
t_{PLH}	CLK	Q or \overline{Q}	3.5	6	10	1	12	3	10.5	ns
			2.5	6	10	1	10	2.5	10.5	

Abbildung 33: Datasheet

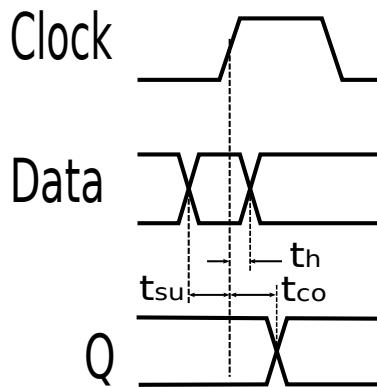


Abbildung 34: Setup and hold time ($t_{SU} =$ setup time, $t_H =$ hold time, $t_{SU} + T_h =$ aperture (time in which the input must be stable), $t_{CO} = t_P =$ Clock to output time (when there are two different times there is t_{PLH} (low to high) and t_{PHL} (high to low) mentioned in the datasheet))

How does this circuit (Figure 35) behave in terms of Hold Time violation?

Consider the following information:

- The circuit is operated at 5V (if no data is available for 5V take the closest specification).

- The signal "Clk" has a frequency of 40 MHz with a 50% duty cycle
- All devices are operated 85 °C (if not mentioned differently below)
- Every wire is expected to have a capacity of 40 pF and 0 Ω resistance.
- The devices are from the family SN74ACxx by Texas Instruments. Excerpts of the data sheets of SN74AC04 and SN74AC74 are included after the questions

The signal off the first flip flop arrives at the second one after a delay of 10.5 ns, which is before the clock propagated through the two inverters which have a delay of 7.5 ns each. This means from the signal arrival to the clock edge one has a time of difference of $2 \cdot (7.5 \text{ ns}) - 10.5 \text{ ns} = 4.5 \text{ ns}$. From the datasheet one knows that $t_H = 0.5 \text{ ns}$, therefore with the longest delay of the inverters everything is ok, but when one has a closer look at the clock skew one sees that it can largely vary 2 ns to 15 ns.

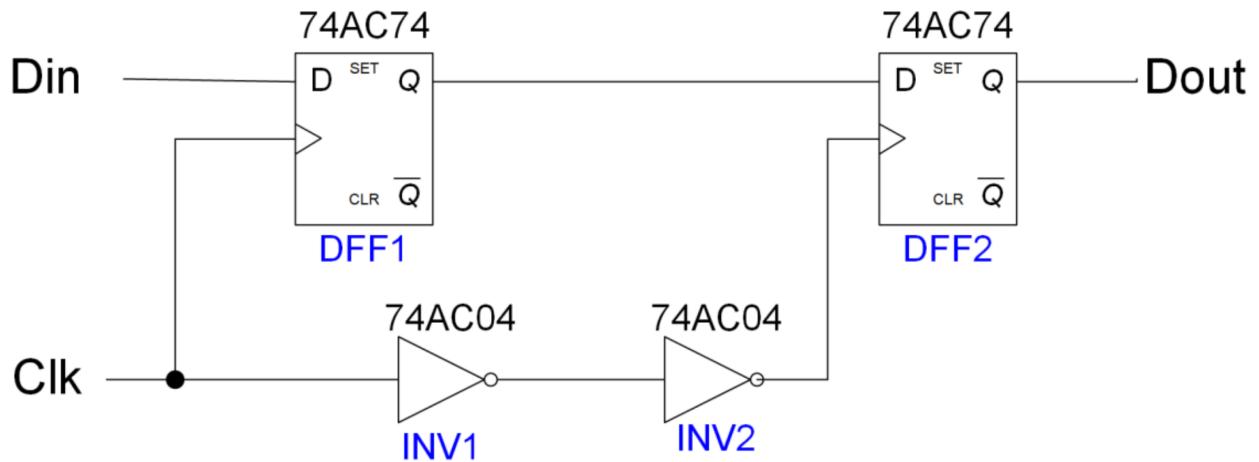


Abbildung 35: Circuit

what are the advantages of LVDS over single clock lines?

- LVDS has lower voltage swing ⇒ shorter transition time (with same slope)
- LVDS is differential ⇒ no influence of ground variation and switch level variation since only difference of two signals counts
- LVDS sees less influence of (common mode) noise and thus noise on switch level / switch time

10 Power consumption

10.1 How can I calculate the power dissipation of general-purpose logic ICs

Power dissipation should be calculated from both of the following (source):

- Static supply current
- Dynamic supply current

Power dissipation can be obtained by multiplying the above current by the voltage applied to an IC.

10.1.1 Static power dissipation: P_s

While CMOS logic ICs are in a static state (i.e., while its input signal remains unchanged), little current flows in it except tiny leakage current that flows across the internal reverse-biased pn junction (known as static supply current, I_{CC}). Static power dissipation is I_{CC} multiplied by the supply voltage.

$$P_s = V_{CC} \cdot I_{CC} \quad (23)$$

V_{CC} : Voltage applied to a logic IC

I_{CC} : Static supply current shown in the datasheet

10.1.2 Dynamic power dissipation

Dynamic supply current is the current that flows in CMOS logic while its input transitions between High and Low. This current flows during the charging and discharging of capacitance. It is necessary to consider both parasitic capacitance (internal equivalent capacitance) and load capacitance. Dynamic power dissipation is obtained by multiplying this current by the voltage applied to the P-channel or N-channel MOSFET. Here, for the sake of simplicity, the V_{CC} value at which the maximum current flows is used for power calculation.

10.1.3 Dynamic power dissipation due to load capacitance (C_L) : P_L

P_L is dissipated when an external load is charged and discharged as shown by the right-hand figure. The amount of charge (Q) stored on the load capacitance is calculated as follows:

$$Q_L = C_L \cdot V_{CC}$$

C_L : Load capacitance

Let the output signal frequency be f_{OUT} ($=1/T_{OUT}$). Then, the average current (I_L) is expressed as follows:

$$I_L = \frac{Q_L}{T} = C_L \cdot V_{CC} \cdot f_{OUT}$$

Hence, dynamic power dissipation (P_L) is:

$$P_L = V_{CC} \cdot I_L = C_L \cdot V_{CC}^2 \cdot f_{OUT}$$

If an IC has multiple outputs, its dynamic power dissipation can be calculated as follows:

$$P_L = V_{CC}^2 \cdot \Sigma (C_{Ln} \cdot f_{OUTn}) \quad (24)$$

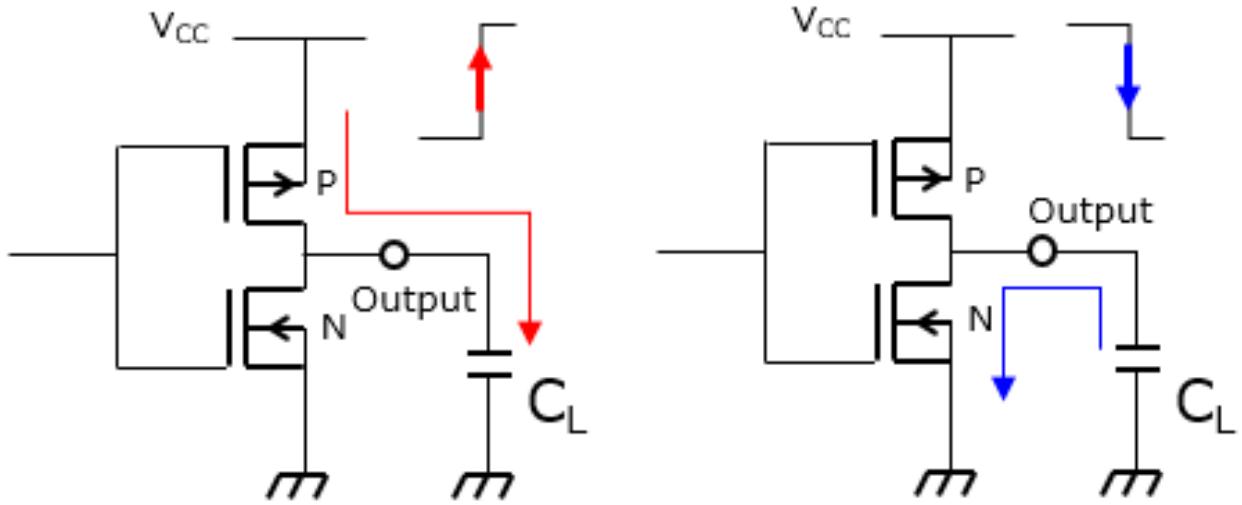


Abbildung 36: Power Consumption 1

10.1.4 Dynamic power dissipation due to internal equivalent capacitance (C_{PD}) : P_{PD}

CMOS logic ICs have various parasitic capacitances as shown by the below figure. These capacitances are equivalently expressed as C_{PD} . (Actually, C_{PD} is calculated from power dissipation at relatively high frequency (1 MHz) under a zero-load condition.)

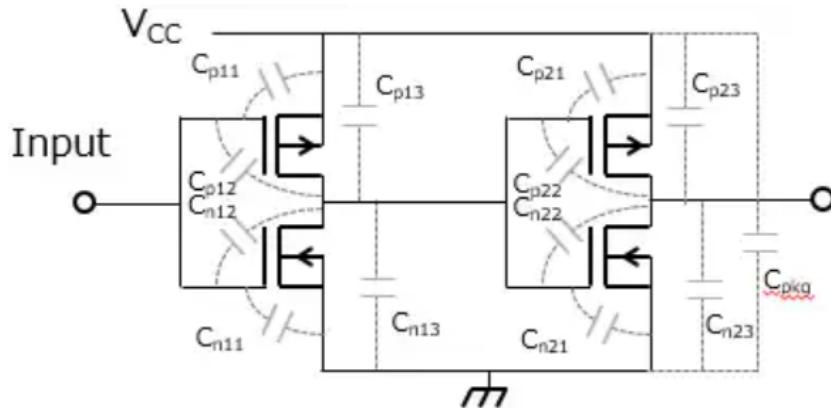


Abbildung 37: Power Consumption 2

P_{PD} is the power dissipated by the equivalent capacitance of an IC and can be considered in the same manner as P_L . Note, however, that P_{PD} is calculated at input frequency (f_{IN}) :

$$P_T = P_{PD} = V_{CC} \cdot I_L = C_{PD} \cdot V_{CC}^2 \cdot f_{IN} \quad (25)$$

10.1.5 Total power dissipation : P_{TTL}

Total power dissipation (P_{TTL}) can be obtained as the sum of static power dissipation (P_S) and dynamic power dissipation ($P_L + P_{PD}$) :

$$P_{TTL} = P_S + P_L + P_{PD} \quad (26)$$

10.2 Exercises:

Answer the following questions for the circuit given in Figure 32:

Consider the following information:

- Supply voltage (core and pin): 5V (take the closest specification value)
- Signals: "Clk": 10 MHz, 50% duty cycle; "D": 5 MHz 50% duty cycle
- Operating Temp 85 °C
- Every wire is expected to have a capacity of 40 pF and 0 Ω resistance.
- To simplify the calculation you may neglect the static input (leakage) current through the input pins of the devices.
- Assume that Dout has the same load as the Q output of DFF1.
- The devices are from the family SN74ACxx by Texas Instruments

Questions:

- What is the total power consumption of DFF1?

Item	Find on page	Value
C _{PD}	Page 5 bottom	45 pF
V _{CC}	Spec	5 V
f _i	Spec ('Clk')	10 MHz
N _{SW}	Page 2 ('Q', 'QN')	2
C _L	Spec ('load 40 pF') and datasheet 74AC04, page 3 'Ci'	40 pF + 2.8 pF = 42.8 pF
f _o	Spec ('D'), Function of DFF	5 MHz
I _{CC}	Page 4 ~ center	20 μA

When using Equation 25 one gets the following for P_{PD} :

$$P_{PD} = C_{PD} \cdot V_{CC}^2 \cdot f_{IN} = \underbrace{2}_{\text{since we have two outputs}} \cdot (45 \text{ pF} \cdot (5 \text{ V})^2 \cdot 10 \text{ MHz}) = 22.5 \text{ mW}$$

with Equation 24 one gets P_L

$$P_L = V_{CC}^2 \cdot \Sigma (C_{Ln} \cdot f_{OUTn}) = \underbrace{1}_{\text{only one output is connected to a load}} \cdot (42.8 \text{ pF} \cdot (5 \text{ V})^2 \cdot 5 \text{ MHz}) = 5.35 \text{ mW}$$

with Equation 23 one gets P_S

$$P_S = V_{CC} \cdot I_{CC} = 5 \text{ V} \cdot 20 \mu\text{A} = 20 \mu\text{W}$$

Therefore with Equation 26 one gets for P_{TTL} :

$$P_{TTL} = P_S + P_L + P_{PD} = 27.95 \text{ mW}$$

- What is the total power consumption of INV2?

$$P_{TOT} = P_T + P_L + P_S = 22.1 \text{ mW}$$

$$P_T = C_{PD} \cdot V_{CC}^2 \cdot f_i \cdot N_{SW} = 45 \text{ pF} \cdot 5^2 \cdot 10 \text{ MHz} \cdot 1 = 11.25 \text{ mW}$$

$$P_L = C_L \cdot f_o \cdot V_{CC}^2 = 43 \text{ pF} \cdot 10 \text{ MHz} \cdot 5^2 = 10.75 \text{ mW}$$

$$P_S = I_{CC} \cdot V_{CC} = 20 \mu\text{A} \cdot 5 = 0.1 \text{ mW}$$

- What is the total power consumption of INV3?

$$P_{\text{TOT}} = P_T + P_L + P_S = 11.1 \text{ mW}$$

$$P_T = C_{\text{PD}} \cdot V_{\text{CC}} \cdot f_i \cdot N_{\text{SW}} = 45 \text{ pF} \cdot 5^2 \cdot 5 \text{ MHz} \cdot 1 = 5.625 \text{ mW}$$

$$P_L = C_L \cdot f_o \cdot V_{\text{CC}2} = 43 \text{ pF} \cdot 5 \text{ MHz} \cdot 5^2 = 5.375 \text{ mW}$$

$$P_S = I_{\text{CC}} \cdot V_{\text{CC}} = 20 \mu\text{A} \cdot 5 = 0.1 \text{ mW}$$

- What is the total power consumption of this complete circuit?

$$P_{\text{circuit}} = 2 \cdot P_{\text{DFF}} + 2 \cdot P_{\text{INV2}} + P_{\text{INV3}} = 111.2 \text{ mW}$$

Answer the following questions for the circuit given in Figure 38:

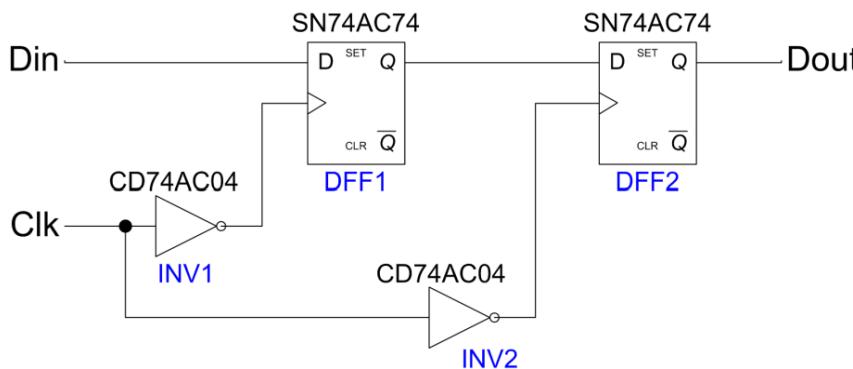


Abbildung 38: Circuit

**switching characteristics over recommended operating free-air temperature range,
 $V_{\text{CC}} = 5 \text{ V} \pm 0.5 \text{ V}$, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	-40°C TO 85°C		-55°C TO 125°C		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.7	5.9	1.6	6.5	ns
t_{PHL}			1.7	5.9	1.6	6.5	

Abbildung 39: CD74AC04

- Consider a circuit like the following one: all devices are in Texas Instruments AC technology (see data sheets in datasheet1 and datasheet2)
- Assume that INV2 is running at 'Worst Case Industrial' condition, INV1 and all DFF at 'Best Case Industrial' condition. Assume that all wiring delays are neglected and $V_{\text{CC}} = 5\text{V}$.

In this case INV2 has a delay of $t_{PD} = 5.9 \text{ ns}$ and INV1 a delay of $t_{PD} = 1.7 \text{ ns}$

- Calculate the clock skew at the two flip-flops

The clock skew is $t_{Skew} = 5.9 \text{ ns} - 1.7 \text{ ns} = 4.2 \text{ ns}$

- Calculate the data path delay from DFF1 to DFF2

In the best case it is 2.5 ns

- What is the slack? Does it work? What is the problem?

The following $t_{PHL} + t_h = 3 \text{ ns}$ must be longer than the clock skew.

**timing requirements over recommended operating free-air temperature range,
 $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (unless otherwise noted) (see Figure 1)**

			$T_A = 25^\circ\text{C}$			SN54AC74		SN74AC74		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	
f_{clock}	Clock frequency		140		95		125		MHz	
t_w	Pulse duration	PRE or CLR low	4.5		5.5		5			ns
		CLK	4.5		5.5		5			
t_{su}	Setup time, data before CLK↑	Data	3		4		3			ns
		PRE or CLR inactive	0		0.5		0			
t_h	Hold time, data after CLK↑		0.5		0.5		0.5		ns	

**switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			SN54AC74		SN74AC74		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			100	125		70		95		MHz
t_{PLH}	PRE or CLR	Q or \bar{Q}	3.5	8	12	1	13	2.5	13	ns
			4	10.5	12	1	14	3.5	13.5	
t_{PHL}	CLK	Q or \bar{Q}	4.5	8	13.5	1	17.5	4	16	ns
			3.5	8	14	1	13.5	3.5	14.5	

**switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			SN54AC74		SN74AC74		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			140	160		95		125		MHz
t_{PLH}	PRE or CLR	Q or \bar{Q}	2.5	6	9	1	9.5	2	10	ns
			3	8	9.5	1	10.5	2.5	10.5	
t_{PHL}	CLK	Q or \bar{Q}	3.5	6	10	1	12	3	10.5	ns
			2.5	6	10	1	10	2.5	10.5	

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS			TYP	UNIT
	$C_L = 50 \text{ pF}$	$f = 1 \text{ MHz}$			
C_{pd}	Power dissipation capacitance			45	pF

Abbildung 40: SN74AC74

11 Clocks and other signals on PCBs

Normally one has a flat line on the amplitude frequency plot at low frequencies and then -20db and -40dB. The first cut off-frequency is at $\frac{T}{2}$ and the second cut off-frequency at T_r (Rise, fall time).

In a microchip you normally have a slow clock and a lot of PLL which provide the fast clock in the different region.

Sometimes one has a resistor before the chip to break the highest frequency. This is very bad for an ADC because the slope is lower and therefore the clock skew on the ADC gets higher.

Never split a ground plain unless you have a clear reason.

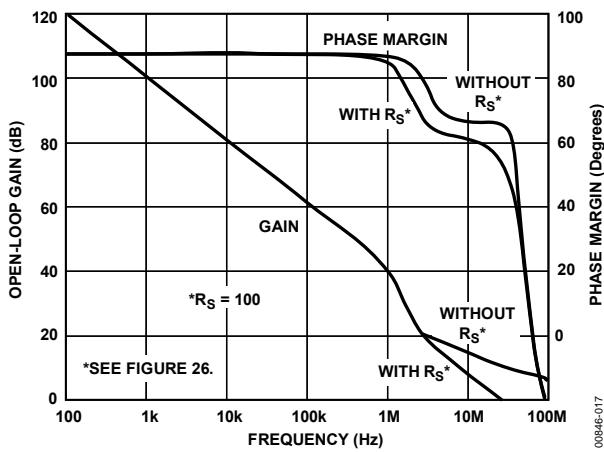
12 Monte Carlo simulation

Current opamp has an influence on the bandwidth.

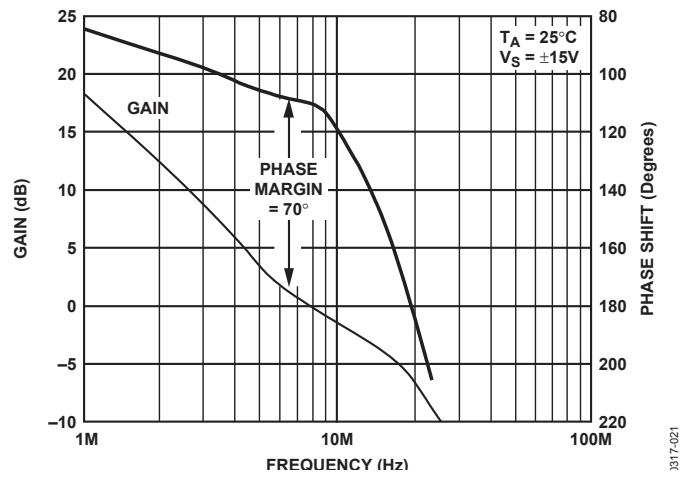
When I oversample, I get a higher effective number of bits. A 12 bit oscilloscope with ENOB=9.7 makes sense, since this number would further reduce when on only uses a 10bit oscilloscope.

13 Stability

The most important to remember is that an op amp circuit with a high gain has normally a higher phase margin than an op amp with low gain. Furthermore very low noise opamps are not designed for very low gains as can be seen in Figure 41a. There the phase margin for a loop gain of one is negative (at the frequency of 110MHz the phase margin is less than zero degree). When one would make a loop gain of $10 \Rightarrow 20 \cdot \log_{10}(10) = 20$ so one would move the zero dB line to 20db, one sees that the crossing is not anymore at 110MHz but at 3MHz or so and there the phase margin is about 70° which is actually good. Furthermore, one can also read the gain margin which is with a gain loop of 10 about 12db (difference between intersect of phase plot and 20dB line and gain at intersection point). Some manufacturers also plot only the interesting part of the phase margin plot as it can be seen in Figure 41b (with a loop gain of one the phase margin is 70° and the gain margin about 7dB) To make an opamp circuit with a



(a) Open-Loop Gain and Phase Margin vs. Frequency of AD797



(b) Gain, Phase Shift vs. Frequency of OP27

loop gain of one stable when one uses for example the opamp from Figure 41a one could add additional components to the circuit to achieve something like in Figure 47 (β_6), which shows that the phase margin

is 4.5 times the difference between the slope of $\frac{1}{\beta}$ and the one of the opamp. Note β_6 can be achieved by adding a parallel cap to the feedback resistor of the op amp circuit.

A very low noise opamp is not built for a very low gain. When the phase margin gets below, 0° the circuit gets instable.

To see what happens when we have an amplifier with gain of 10 one can move the Gain line in the plot 20db down or the zero dB open-loop gain 20db up.

(see rate of closure in the book)

13.1 Tian's Method

It does not matter where you cut your loop open.

13.1.1 Op Amp Circuits

Figure 42 shows the basic structure of a negative-feedback circuit. The arrows indicate signal flow, and the generic symbol x stands for either a voltage or a current signal. Besides the source and load, we identify the following basic blocks:

1. An amplifier called the error amplifier, which accepts a signal x_ε called the error signal, and yields the output signal

$$x_O = a_\varepsilon x_\varepsilon \quad (27)$$

where a_ε is called the open-loop gain.

2. A feedback network, which samples x_o and produces the feedback signal

$$x_f = bx_o \quad (28)$$

where b is the gain of the feedback network and is called the feedback factor.

3. A summing network, denoted as Σ , which sums the negative of x_f to the input signal x_i to yield the difference

$$x_\varepsilon = x_i - x_f \quad (29)$$

The designation negative feedback stems from the fact that we are in effect feeding a portion b of x_o back to the error amplifier's input, where it is subtracted from x_i to yield a reduced signal x_ε . Were it added instead, feedback would be positive. For reasons that will become clearer as we move along, negative feedback is also said to be degenerative, and positive feedback regenerative.

Substituting Equation 28 into Equation 29, and then into Equation 27, we get

$$A = \frac{x_o}{x_i} = \frac{a_\varepsilon}{1 + a_\varepsilon b} \quad (30)$$

where A is called the closed-loop gain (not to be confused with the open-loop gain $a_\varepsilon = x_o/x_\varepsilon$). Note that for feedback to be negative we must have $a_\varepsilon b > 0$. Consequently, A will be smaller than a_ε by the amount $1 + a_\varepsilon b$, which is called the amount of feedback. (Should there be no feedback, we would have $b = 0$ and $A \rightarrow a$, a situation referred to as open-loop operation.)

As a signal propagates around the loop consisting of the error amplifier, feedback network, and summer, it experiences an overall gain of $a_\varepsilon \times b \times (-1)$, or $-a_\varepsilon b$. Its negative shall be denoted as the loop gain L ,

$$L = a_\varepsilon b$$

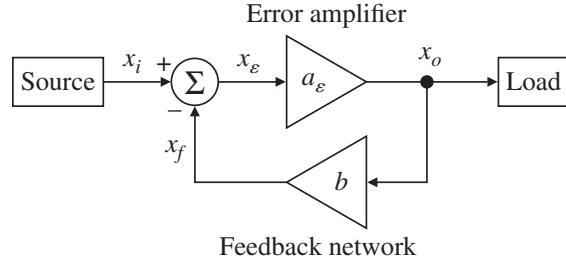


Abbildung 42: Block diagram of a negative-feedback system

This gain allows us to express Equation 30 in the more insightful form $A = (1/b) \times L/(1 + L) = (1/b)/(1 + 1/L)$. Letting $L \rightarrow \infty$ yields the ideal situation

$$A_{\text{ideal}} = \lim_{L \rightarrow \infty} A = \frac{1}{b}$$

that is, A becomes independent of a_e and is set exclusively by the feedback network, regardless of the error amplifier in use. By proper choice of the topology and components of the feedback network, we can tailor the circuit to a variety of different applications. For instance, specifying $b < 1$ so that $1/b > 1$, will cause x_o to be a magnified replica of x_i . Or, implementing the feedback network with reactive elements such as capacitors will yield a frequency-dependent circuit with the transfer function $H(s) = 1/b(s)$, where s is the complex frequency. Filters and oscillators are two popular examples.

Henceforth we shall express the closed-loop gain in the insightful form

$$A = A_{\text{ideal}} \frac{1}{1 + 1/L}$$

Rearranging as

$$A = A_{\text{ideal}} \left(1 - \frac{1}{1 + L} \right)$$

indicates that the fractional departure of the actual gain A from the ideal gain A_{ideal} is inversely proportional to the amount of feedback $1 + L$. This departure is more commonly expressed via the gain error

$$\text{GE}(\%) = 100 \frac{A - A_{\text{ideal}}}{A_{\text{ideal}}} = \frac{1}{1 + L}$$

13.1.2 Stability Problem

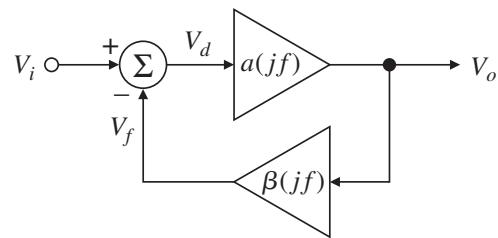


Abbildung 43: Negative-feedback system with unilateral amplifier and unilateral feedback network

The strategy is to represent an op amp feedback circuit always in the form as it can be seen in Equation 31, whereby a_ε is the gain and b the feedback factor.

$$x_O = a_\varepsilon (x_I - bx_O) \quad (31)$$

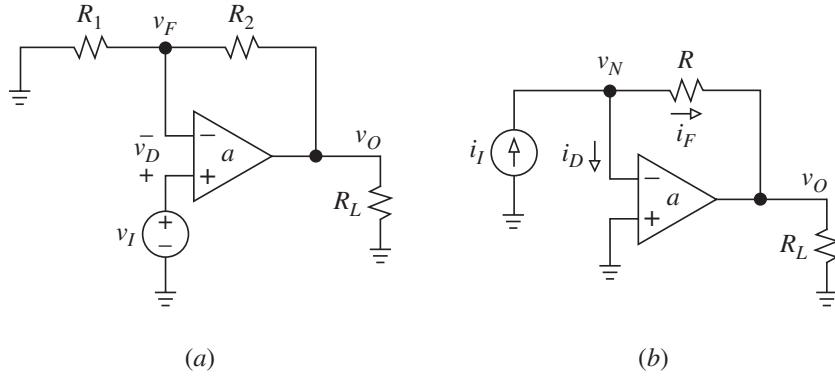


Abbildung 44: The (a) series-shunt and (b) shunt-shunt topologies.

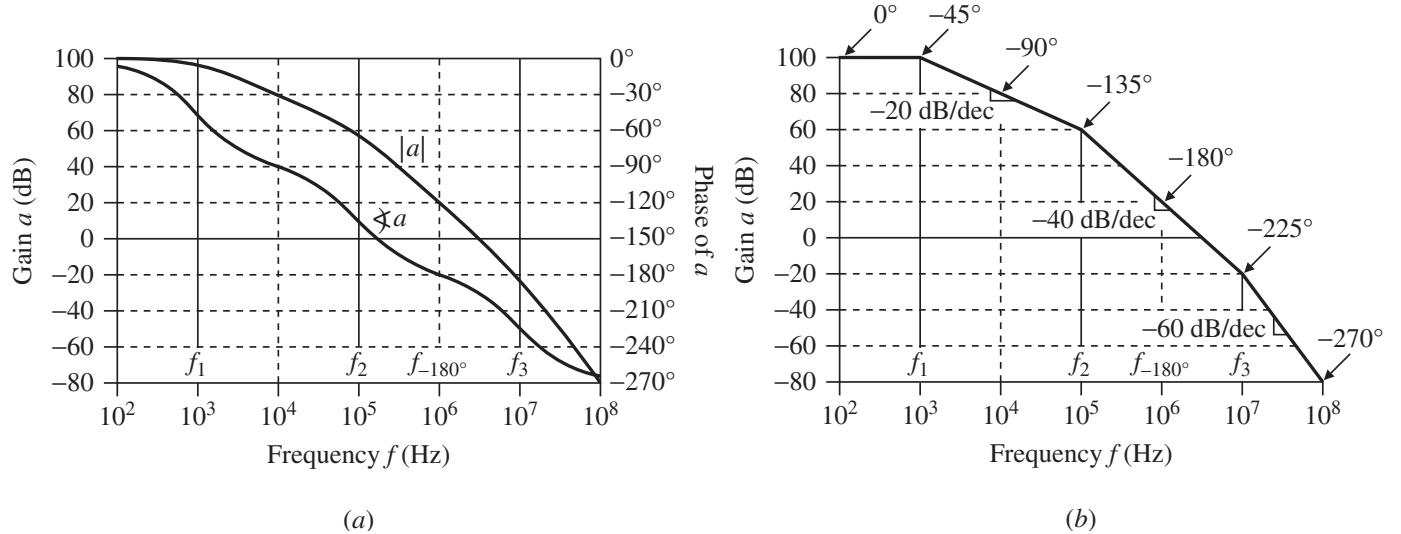


Abbildung 45: Open-loop magnitude and phase plots for the op amp, Linearized magnitude plot associating phase with slope

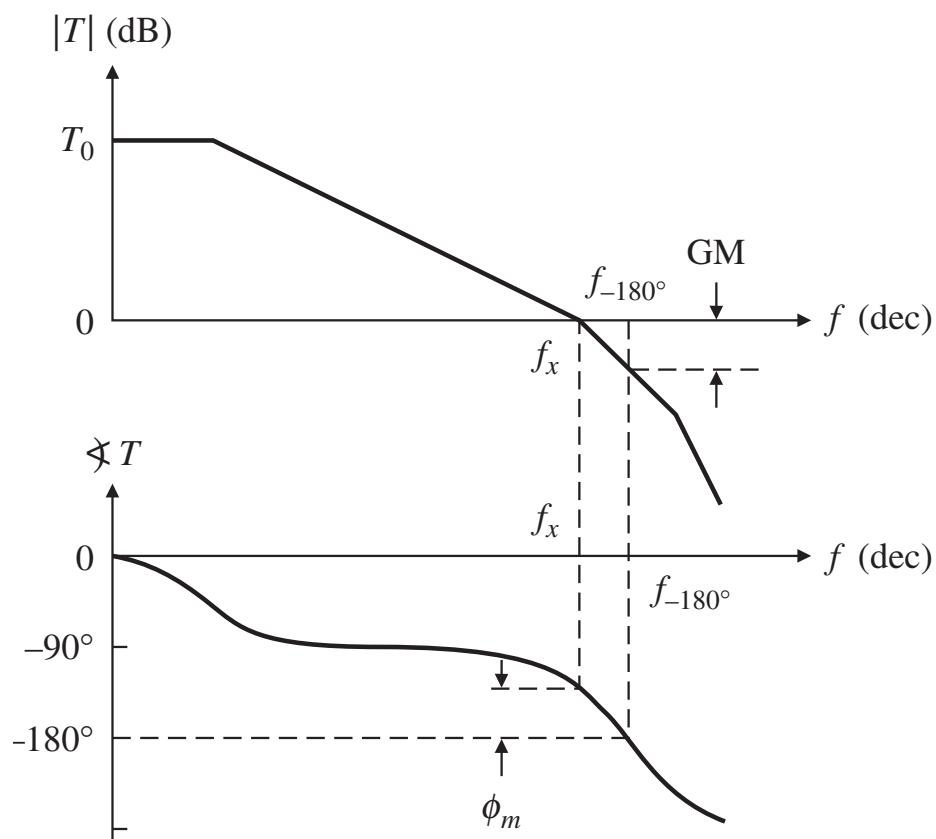


Abbildung 46: Visualizing gain margin GM and phase margin Φ_m .

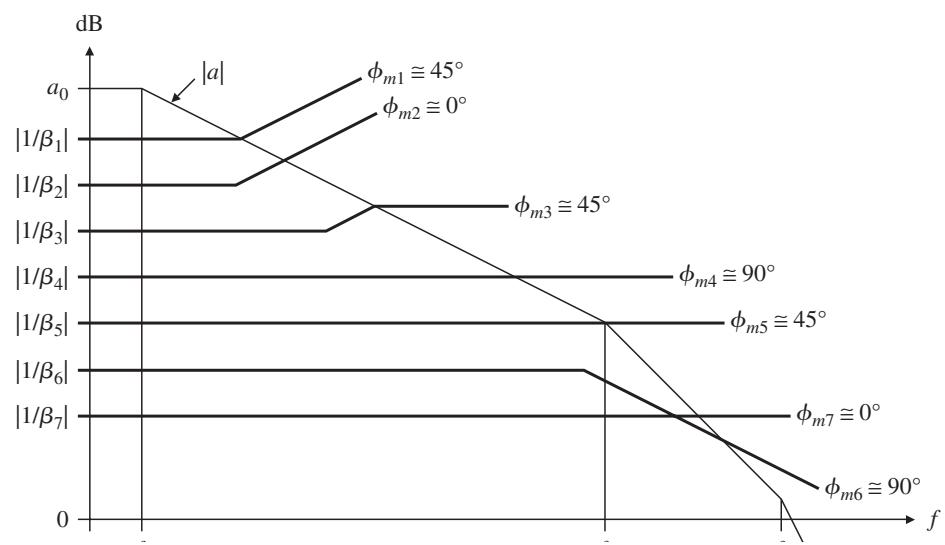


Abbildung 47: Rate of closure (ROC) for different feedback-factor types.

14 Special Amplifiers

14.1 Differential difference amplifier

A Swiss guy invented this amplifier which has four inputs and can handle two differential inputs. An application would be for example an ECG(electrocardiogram) measurement.

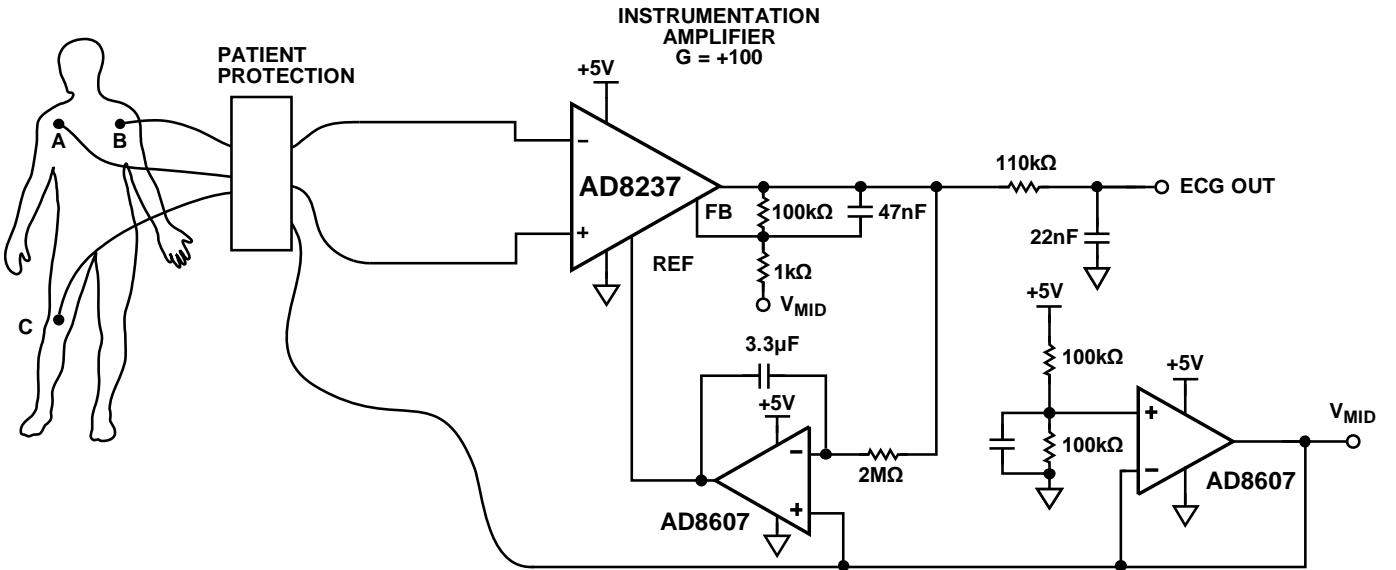
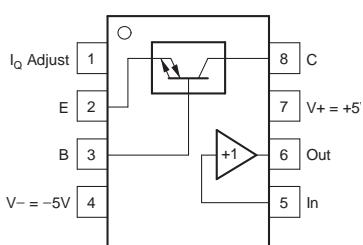
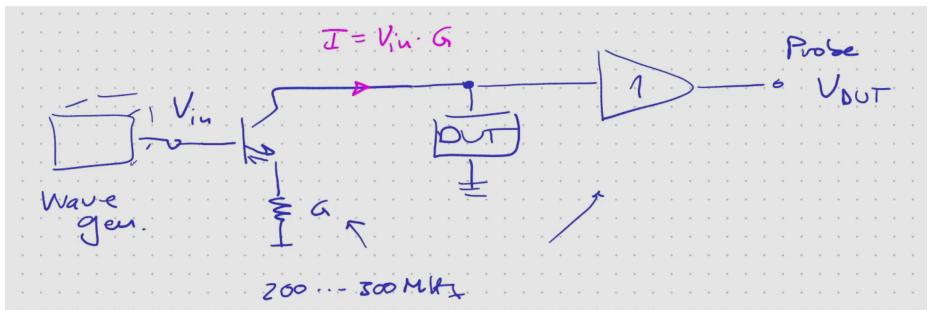


Abbildung 48: Differential opamp circuit (AD8237 in ECG)

The impedance of a circuit could be measured with a circuit like the one in Figure 49b. Which contains a dyiamond opamp. Note that a dyiamond opamp makes sure that the voltage on the base and the emitter are always the same and the current on the emitter and the collector are also the same, but in opposite direction. In this way one can control with the Resistor G what current is flowing with a specific input voltage. The OPA860 furthermore has a integrated voltage buffer, to which one can afterwards connect the oscilloscope probe.



(a) OPA860 overview



(b) Voltage to current transformer (impedance analyser)

14.2 Signal flow graph at the exam

1. open terminal and type in `conda activate sfg`

2. go to the right folder :

```
cd C:\Users\matth\Documents\Matthias_Meyer\Schule\Master\2. Semester\AdvElDes\signalflo
```

3. start the signal flow grapher with: `python .\src\main\python\main.py`

4. draw graph:

- double click to **add new point** and give it a name
- ctrl select point, ctrl select next point \Rightarrow **add connection between points**
- select point, shift select point \Rightarrow **generate signal flow graph from first to second point**

5. copy signal flow graph:

```
1 %matplotlib notebook
2 %matplotlib inline
3 from sympy import *
4 import sympy as sp
5 import numpy as np
6 import matplotlib.pyplot as plt
7 import hanspitoools as ht
8 def niceT(T,s):
9     return ht.mani.numden(lambda p: ht.mani.nicepoly(p,s),T)
10 def di(x):
11     display(x)
12     # print(latex(x))
13 def sigdig(expr, num_digits):
14     return expr.xreplace({n.evalf() : n if type(n)==int else Float(n, num_digits) for n in expr})
15 def eseries(v, E):
16     return 10**((log(v, 10)*E).round()/E)
```

```
1 import sympy as sp
2 Delta = sp.symbols('Delta')
3 L1,L2,L3,L4,L5,L6,L7 = sp.symbols('L1,L2,L3,L4,L5,L6,L7')
4 T_num = sp.symbols('T_num')
5 T_den = sp.symbols('T_den')
6 T_io = sp.symbols('T_io')
7 s,G,C = sp.symbols('s,G,C')
8
9 loops = [(L1, -1/2), (L2, -1/2), (L3, -1/2), (L4, -1/2*G/(C*s + G)), (L5, 1), (L6, 1), (L7, G/(C*s + G))]
10 determinant = [(Delta, -L1 + L2*L5 - L2 + L3*L6 - L3 - L4 + L5*L6 - L5 - L6 - L7 + 1)]
11 denominator = [(T_den, Delta)]
12
13 P1,D1 = sp.symbols('P1,D1')
14 paths = [(P1, 1/(C*s)), (D1, L2*L5 - L2 + L3*L6 - L3 - L4 + L5*L6 - L5 - L6 + 1)]
15 numerator = [(T_num, D1*P1)]
16
17 transfer_function = [(T_io, T_num/T_den)]
```

```

18 T=T_io.subs(transfer_function).subs(numerator).subs(denominator).subs(determinant).subs(paths).
19 print('Transferfunction =')
20 display(T)

```

```

1 def find_first_larger_index(arr, threshold):
2     for i, element in enumerate(arr):
3         if element > threshold:
4             return i
5     return None # If no element is larger than the threshold
6
7 # Generate values for fn (frequency in Hz) and wn (frequency in rad/s)
8 fn = 10.0**np.arange(-4,1,0.025)
9 wn = 2*np.pi*fn
10
11 # Create a figure and axes for plotting
12 fig, ax1 = plt.subplots(figsize=(6.4,4.8))
13
14 # Set labels for the plot axes
15 ax1.set_xlabel('$f$ in Hz')
16 ax1.set_ylabel('$|T(j\omega)|$')
17
18 # Define substitution variables
19 numvals = [(G, 1/(1)), (C, 1e-6)]
20
21 # Define T (transfer function), substitute values, and Convert a SymPy expression into a function that
22 T = (G + s)
23 Tn = T.subs(numvals)
24 Tl = lambdify(s, Tn, 'numpy')
25
26 # Calculate Ta (absolute value of transfer function) by evaluating Tl for complex values
27 Ta = np.abs(Tl(1j*wn))
28
29 # Plot fn vs. Ta using a logarithmic scale, color the line blue
30 ax1.loglog(fn, Ta, color='tab:blue')
31
32 # Find the index of the first element in Ta that is larger than Ta[0] multiplied by the square root of
33 index = find_first_larger_index(Ta, Ta[0]*sqrt(2))
34
35 # Plot the corresponding point as a red circle
36 ax1.plot(fn[index], Ta[index], 'o', color='tab:red')
37
38 # Enable gridlines for both major and minor ticks
39 ax1.grid(True, which='both')
40
41 # Get the y-axis limits for better layout
42 ax1_lim = ax1.get_ylimits()
43

```

```

44 # Adjust the spacing of subplots to prevent clipping of labels
45 fig.tight_layout()

```

```

1 %matplotlib notebook
2 %matplotlib inline
3 from sympy import *
4 import numpy as np
5 import scipy
6 from scipy import integrate
7 import hanspitoools as ht
8 import matplotlib.pyplot as plt
9
10 def find_first_larger_index(arr, threshold):
11     for i, element in enumerate(arr):
12         if element > threshold:
13             return i
14     return None # If no element is larger than the threshold
15
16 def find_first_smaller_index(arr, threshold):
17     for i, element in enumerate(arr):
18         if element < threshold:
19             return i
20     return None # If no element is larger than the threshold
21
22 fn = 10.0*np.arange(-4,5,0.01)
23 wn = fn*2*np.pi
24
25
26 # Define substitution variables
27 numvals = [(G, 1/(1)), (C, 1e-6)]
28
29 # Define T (transfer function), substitute values, and Convert a SymPy expression into a function that
30 T = (10000*10000/((1+s)*(100+s)**2))
31 Tn = T.subs(numvals)
32
33 v1 = np.ones(len(wn))
34 T1_a = ht.freq.amplitude(Tn,s,wn,[])
35 T1_p = ht.freq.phase(Tn,s,wn,[])
36 fig, ax1 = plt.subplots(figsize=(6.4,3.6))
37
38 color = 'tab:blue'
39 ax1.set_xlabel('$f$ in Hz')
40 ax1.set_ylabel('$|T|$', color=color)
41 ax1.loglog(fn, T1_a, color=color)
42 ax1.loglog(fn, v1, ':', color=color)
43 ax1.tick_params(axis='y', labelcolor=color)
44 ax1_lim = ax1.get_ylim()

```

```

45 index = find_first_smaller_index(T1_a, 1)
46 print(f"frequency {fn[index]:.2f}Hz= {fn[index]*2*np.pi:.2f}rad, {T1_a[index]:.2f}")
47 # Plot the corresponding point as a red circle
48 ax1.plot(fn[index], T1_a[index], 'o', color='tab:red')
49
50 ax2 = ax1.twinx() # instantiate a second axes that shares the same x-axis
51
52 color = 'tab:red'
53 ax2.set_ylabel('$\phi_T$ in degrees', color=color) # we already handled the x-label with ax1
54 ax2.plot(fn, T1_p, color=color)
55 ax2.tick_params(axis='y', labelcolor=color)
56 ax2_lim = ax2.get_ylim()
57 # ax2.set_yticks([0,-45,-90,-135,-180,-270,-360,-450,-540])
58 ax2.set_ylim(ax2_lim)
59
60 fig.tight_layout() # otherwise the right y-label is slightly clipped

```

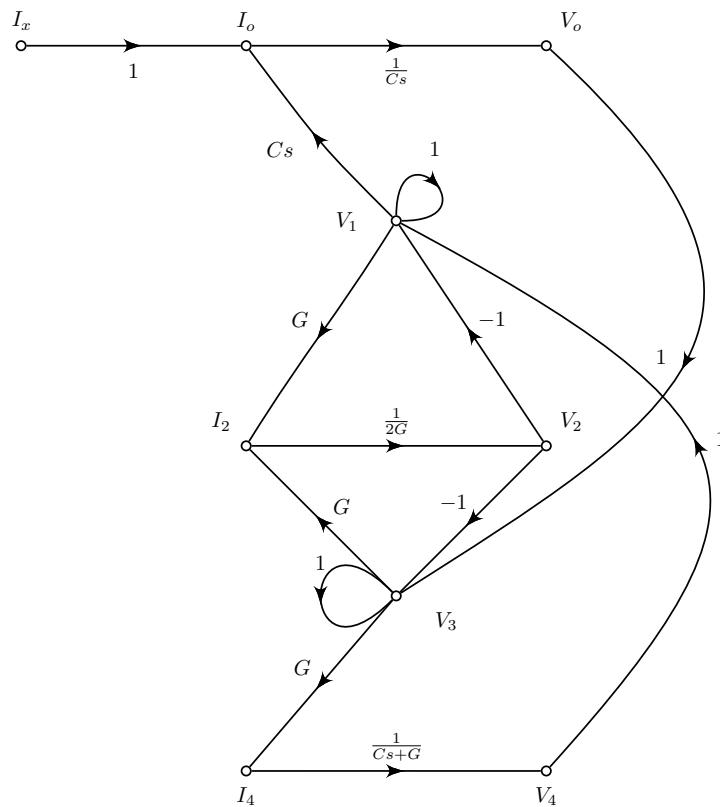


Abbildung 50: Signal flow graph example

15 Formulas

15.1 Probability

15.1.1 Q-funciton

$$Q(x) = \frac{1}{\sqrt{2\pi}} \int_x^\infty \exp\left(-\frac{u^2}{2}\right) du \quad (32)$$

15.1.2 Binomialverteilung

Ein Bernoulli-Experiment mit den beiden sich gegenseitig ausschliessenden Ergebnissen (Ereignissen) A und \bar{A} werde n -mal nacheinander ausgefuehrt (sog. mehrstufiges Bernoulli-Experiment vom Umfang n). Dann genuegt die diskrete Zufallsvariable

$X = \text{Anzahl der Versuche, in denen das Ereignis } A \text{ eintritt}$

der sog. Binomialverteilung mit der Wahrscheinlichkeitsfunktion

$$f(x) = P(X = x) = \binom{n}{x} p^x \cdot q^{n-x} \quad (x = 0, 1, 2, \dots, n) \quad (33)$$

und der zugehoerigen Verteilungsfunktion

$$F(x) = P(X \leq x) = \sum_{k \leq x} \binom{n}{k} p^k \cdot q^{n-k} \quad (x \geq 0)$$

(fuer $x < 0$ ist $F(x) = 0$). n und p sind dabei die Parameter der Verteilung. Die Kennwerte oder Masszahlen der Binomialverteilung lauten:

- Mittelwert: $\mu = np$
- Varianz: $\sigma^2 = npq = np(1 - p)$
- Standardabweichung: $\sigma = \sqrt{npq} = \sqrt{np(1 - p)}$

Dabei bedeuten:

- p : Konstante Wahrscheinlichkeit fÃ¼r das Eintreten des Ereignisses A beim Einzelversuch ($0 < p < 1$)
- q : Konstante Wahrscheinlichkeit fÃ¼r das Eintreten des zu A komplementÃ¤ren Ereignisses \bar{A} beim Einzelversuch ($q = 1 - p$)
- n : Anzahl der AusfÃ¼hrungen des Bernoulli-Experiments (Umfang des mehrstufigen Bernoulli-Experiments)

Common angles

Degrees	0°	30°	45°	60°	90°
Radians	0	$\frac{\pi}{6}$	$\frac{\pi}{4}$	$\frac{\pi}{3}$	$\frac{\pi}{2}$
$\sin \theta$	0	$\frac{1}{2}$	$\frac{\sqrt{2}}{2}$	$\frac{\sqrt{3}}{2}$	1
$\cos \theta$	1	$\frac{\sqrt{3}}{2}$	$\frac{\sqrt{2}}{2}$	$\frac{1}{2}$	0
$\tan \theta$	0	$\frac{\sqrt{3}}{3}$	1	$\sqrt{3}$	

Reciprocal functions

$$\cot x = \frac{1}{\tan x}$$

$$\csc x = \frac{1}{\sin x}$$

$$\sec x = \frac{1}{\cos x}$$

Even/odd

$$\sin(-x) = -\sin x$$

$$\cos(-x) = \cos x$$

$$\tan(-x) = -\tan x$$

Pythagorean identities

$$\sin^2 x + \cos^2 x = 1$$

$$1 + \tan^2 x = \sec^2 x$$

$$1 + \cot^2 x = \csc^2 x$$

Cofunction identities

$$\sin\left(\frac{\pi}{2} - x\right) = \cos x$$

$$\cos\left(\frac{\pi}{2} - x\right) = \sin x$$

$$\tan\left(\frac{\pi}{2} - x\right) = \cot x$$

$$\cot\left(\frac{\pi}{2} - x\right) = \tan x$$

$$\sec\left(\frac{\pi}{2} - x\right) = \csc x$$

$$\csc\left(\frac{\pi}{2} - x\right) = \sec x$$

Sum and difference of angles

$$\sin(x + y) = \sin x \cos y + \cos x \sin y$$

$$\sin(x - y) = \sin x \cos y - \cos x \sin y$$

$$\cos(x + y) = \cos x \cos y - \sin x \sin y$$

$$\cos(x - y) = \cos x \cos y + \sin x \sin y$$

$$\tan(x + y) = \frac{\tan x + \tan y}{1 - \tan x \tan y}$$

$$\tan(x - y) = \frac{\tan x - \tan y}{1 + \tan x \tan y}$$

Double angles

$$\sin(2x) = 2 \sin x \cos x$$

$$\cos(2x) = \cos^2 x - \sin^2 x$$

$$= 2 \cos^2 x - 1$$

$$= 1 - 2 \sin^2 x$$

$$\tan(2x) = \frac{2 \tan x}{1 - \tan^2 x}$$

Half angles

$$\sin \frac{x}{2} = \pm \sqrt{\frac{1 - \cos x}{2}}$$

$$\cos \frac{x}{2} = \pm \sqrt{\frac{1 + \cos x}{2}}$$

$$\begin{aligned}\tan \frac{x}{2} &= \frac{1 - \cos x}{\sin x} \\ &= \frac{\sin x}{1 + \cos x}\end{aligned}$$

Power reducing formulas

$$\begin{aligned}\sin^2 x &= \frac{1 - \cos 2x}{2} \\ \cos^2 x &= \frac{1 + \cos 2x}{2} \\ \tan^2 x &= \frac{1 - \cos 2x}{1 + \cos 2x}\end{aligned}$$

Product to sum

$$\begin{aligned}\sin x \sin y &= \frac{1}{2} [\cos(x - y) - \cos(x + y)] \\ \cos x \cos y &= \frac{1}{2} [\cos(x - y) + \cos(x + y)] \\ \sin x \cos y &= \frac{1}{2} [\sin(x + y) + \sin(x - y)] \\ \tan x \tan y &= \frac{\tan x + \tan y}{\cot x + \cot y} \\ \tan x \cot y &= \frac{\tan x + \cot y}{\cot x + \tan y}\end{aligned}$$

Sum to product

$$\begin{aligned}\sin x + \sin y &= 2 \sin\left(\frac{x+y}{2}\right) \cos\left(\frac{x-y}{2}\right) \\ \sin x - \sin y &= 2 \cos\left(\frac{x+y}{2}\right) \sin\left(\frac{x-y}{2}\right) \\ \cos x + \cos y &= 2 \cos\left(\frac{x+y}{2}\right) \cos\left(\frac{x-y}{2}\right) \\ \cos x - \cos y &= -2 \sin\left(\frac{x+y}{2}\right) \sin\left(\frac{x-y}{2}\right) \\ \tan x + \tan y &= \frac{\sin(x+y)}{\cos x \cos y} \\ \tan x - \tan y &= \frac{\sin(x-y)}{\cos x \cos y}\end{aligned}$$

Why $\frac{1}{N-1}$ see the following video

16 Most important Formulas

16.1 Imporant formulas

Real-/Imaginary part:	$\operatorname{Re}\{x\} = x_R = \frac{1}{2}[x + x^*]$	$\operatorname{Im}\{x\} = x_I = \frac{1}{2j}[x - x^*]$
even/odd part:	$x_g(t) = \frac{1}{2}[x(t) + x(-t)]$	$x_u(t) = \frac{1}{2}[x(t) - x(-t)]$
conj. even/odd part:	$x_{g^*}(t) = \frac{1}{2}[x(t) + x^*(-t)]$	$x_{u^*}(t) = \frac{1}{2}[x(t) - x^*(-t)]$

16.2 Definition der Faltung

	aperiodisch	periodisch
diskret:	$x[n] * y[n] = \sum_{i=-\infty}^{\infty} x[i] \cdot y[n-i]$	$x[n] \circledast y[n] = \sum_{i=n_0}^{n_0+N_p-1} x[i] \cdot y[n-i]$
kontinuierlich:	$x(t) * y(t) = \int_{-\infty}^{\infty} x(\tau) \cdot y(t-\tau) d\tau$	$x(t) \circledast y(t) = \int_{t_0}^{t_0+T_p} x(\tau) \cdot y(t-\tau) d\tau$

16.3 Defintion der Energie

diskret:	$E_x^{(d)} = \sum_{k=-\infty}^{\infty} x[k] ^2 = T \int_{-1/2T}^{1/2T} X(f) ^2 df = \frac{1}{2\pi} \int_{-\pi}^{\pi} X(\Omega) ^2 d\Omega$
kontinuierlich:	$E_x^{(k)} = \int_{-\infty}^{\infty} x(t) ^2 dt = \int_{-\infty}^{\infty} X(f) ^2 df = \frac{1}{2\pi} \int_{-\infty}^{\infty} X(j\omega) ^2 d\omega = T \cdot E_x^{(d)}$

16.4 Defintion der Leistung periodischer Signale

diskret:	$P_x^{(d)} = \frac{1}{N_p} \sum_{k=0}^{N_p-1} x[k] ^2 = \sum_{n=0}^{N_p-1} X_n ^2 = \frac{1}{N^2} \sum_{n=0}^{N_p-1} X[n] ^2$
kontinuierlich:	$P_x^{(k)} = \frac{1}{T_p} \int_{-T_p/2}^{T_p/2} x(t) ^2 dt = \sum_{n=-\infty}^{\infty} X_n ^2 = P_x^{(d)}$

16.5 Definition spezieller Signale

Impulskamm:	$W_T(t) = \sum_{n=-\infty}^{\infty} \delta(t - nT) = \frac{1}{ T } W\left(\frac{t}{T}\right)$
periodische Impulsfolge:	$U_N[k] = \sum_{n=-\infty}^{\infty} \delta[k - nN]$

17 C.2 z-Transformation

17.1 Definition

zweiseitig:	einseitig:
$X(z) = \sum_{k=-\infty}^{\infty} x[k]z^{-k}$	$X(z) = \sum_{k=0}^{\infty} x[k]z^{-k}$
Konvergenzgebiet \mathcal{K} : $a < z < b$	Konvergenzgebiet \mathcal{K} : $ z > a$

17.2 Inverse z-Transformation

$$x[k] = \frac{1}{2\pi j} \oint_{\mathcal{C}} X(z) z^{k-1} dz = \sum_{\alpha_i \in \mathcal{A}} \operatorname{Res} \{ X(z) \cdot z^{k-1}; \alpha_i \}$$

\mathcal{C} : pos. orientierte Kurve in \mathcal{K} . \mathcal{A} : Menge aller von \mathcal{C} umschlossenen Pole.

17.3 Eigenschaften und Rechenregeln

	Zeitbereich	Bildbereich	Konvergenz
Linearität	$c_1x_1[k] + c_2x_2[k]$	$c_1X_1(z) + c_2X_2(z)$	$\mathcal{K}_{x_1} \cap \mathcal{K}_{x_2}$
Faltung	$x[k] * y[k]$	$X(z) \cdot Y(z)$	$\mathcal{K}_x \cap \mathcal{K}_y$
Verschiebung	$x[k - k_0]$	$z^{-k_0}X(z)$	\mathcal{K}_x
Dämpfung	$a^k \cdot x[k]$	$X\left(\frac{z}{a}\right)$	$ a \cdot \mathcal{K}_x$
lineare Gewichtung	$k \cdot x[k]$	$-z \cdot \frac{d}{dz}X(z)$	\mathcal{K}_x
konj. komplexes Signal	$x^*[k]$	$X^*(z^*)$	\mathcal{K}_x
Zeitinversion	$x[-k]$	$X\left(\frac{1}{z}\right)$	$1/\mathcal{K}_x$
diskrete Ableitung	$x[k] - x[k - 1]$	$X(z) \cdot \frac{z-1}{z}$	\mathcal{K}_x
diskrete Integration	$\sum_{i=0}^k x[i]$	$X(z) \cdot \frac{z}{z-1}$	$\mathcal{K}_x \cap \{ z > 1\}$
periodische Fortsetzung	$\sum_{i=0}^{\infty} x[k - iN_p]$	$X(z) \cdot \frac{1}{1-z^{-N_p}}$	$\mathcal{K}_x \cap \{ z > 1\}$
Upsampling	$x\left[\frac{k}{N}\right]$	$X(z^N)$	$\sqrt[N]{\mathcal{K}_x}$

17.4 Spezielle Eigenschaften der einseitigen z -Transformation

Verschiebung links	$x[k + k_0], k_0 > 0$	$z^{k_0}X(z) - \sum_{i=0}^{k_0-1} x[i]z^{k_0-i}$
Verschiebung rechts	$x[k - k_0], k_0 > 0$	$z^{-k_0}X(z) + \sum_{i=-k_0}^{-1} x[i]z^{-k_0-i}$
Anfangswertsatz	$x[0] = \lim_{z \rightarrow \infty} X(z), \quad \text{falls Grenzwert existiert}$	
Endwertsatz	$\lim_{k \rightarrow \infty} x[k] = \lim_{z \rightarrow 1}(z - 1)X(z), \quad \text{falls } X(z) \text{ nur Pole mit } z < 1 \text{ oder bei } z = 1$	

17.5 Rücktransformation durch Partialbruchzerlegung

Die Partialbruchzerlegung von $\tilde{X}(z) = \frac{X(z)}{z}$ führt auf die Form:

$$X(z) = \sum_{i \geq 1} g_i \cdot z^i + \sum_i \frac{z \cdot r_i}{z - \alpha_i} + \sum_i \sum_{l=1}^{m_i} \frac{z \cdot \tilde{r}_{i,l}}{(z - \tilde{\alpha}_i)^l}, \quad g_i, \alpha_i, \tilde{\alpha}_i, r_i, \tilde{r}_{i,l} \in \mathbb{C},$$

welche für $\mathcal{K} : |z| > r_0$ mit den Korrespondenzen 2, 5, 6 und 12 gliedweise zur Rücktransformation werden kann.

17.6 Korrespondenzen der z -Transformation

Nr.	$x[k]$	$X(z)$	\mathcal{K}
1	$\delta[k]$	1	$z \in \mathbb{C}$
2	$\delta[k - k_0]$	z^{-k_0}	$0 < z < \infty$
3	$\varepsilon[k]$	$\frac{z}{z-1}$	$ z > 1$
4	$k \cdot \varepsilon[k]$	$\frac{z}{(z-1)^2}$	$ z > 1$
5	$a^k \cdot \varepsilon[k]$	$\frac{z}{z-a}$	$ z > a $
6	$\binom{k}{m} a^{k-m} \cdot \varepsilon[k]$	$\frac{z}{(z-a)^{m+1}}$	$ z > a $
7	$\sin(\Omega_0 k) \cdot \varepsilon[k]$	$\frac{z \cdot \sin(\Omega_0)}{z^2 - 2z \cdot \cos(\Omega_0) + 1}$	$ z > 1$
8	$\cos(\Omega_0 k) \cdot \varepsilon[k]$	$\frac{z \cdot [z - \cos(\Omega_0)]}{z^2 - 2z \cdot \cos(\Omega_0) + 1}$	$ z > 1$
9	$a^k \cdot \varepsilon[-k - 1]$	$-\frac{z}{z-a}$	$ a < z < a $
10	$a^{ k }, a < 1$	$\frac{2}{ c \cdot (a - \frac{1}{a}) }$	
11	$\frac{1}{k!} \cdot \varepsilon[k]$	$e^{\frac{1}{z}}$	$ z < \frac{1}{a} $

Spezielle Korrespondenzen zur Rücktransformation konj. komplexer Polpaare

12	$2 r \alpha^k \cos(\varphi\alpha \cdot k + \varphi r) \cdot \varepsilon[k]$	$\frac{z \cdot r}{z - \alpha} + \frac{z \cdot r^*}{z - \alpha^*}$	$ z > \alpha$
13	$a^k \cdot \frac{\cos(\Omega_0 k + \varphi_0)}{\cos(\varphi_0)} \cdot \varepsilon[k]$ $a = \sqrt{c}, \Omega_0 = \arccos\left(\frac{b}{2\sqrt{c}}\right), \varphi_0 = \arctan\left(\frac{2d-b}{\sqrt{4c-b^2}}\right)$	$\frac{z(z-d)}{z^2 - bz + c}, c > \frac{b^2}{4}$	$ z > \sqrt{c}$

18 C.3 Laplace-Transformation

18.1 Definition

zweiseitig:	einseitig:
$X(s) = \int_{-\infty}^{\infty} x(t)e^{-st}dt$	$X(s) = \int_{0^-}^{\infty} x(t)e^{-st}dt$
Konvergenzgebiet \mathcal{K} : $a < \operatorname{Re}\{s\} < b$	Konvergenzgebiet \mathcal{K} : $\operatorname{Re}\{s\} > a$

18.2 Eigenschaften und Rechenregeln

	Zeitbereich	Bildbereich	Konvergenz
Linearität	$c_1 x_1(t) + c_2 x_2(t)$	$c_1 X_1(s) + c_2 X_2(s)$	$\mathcal{K}_{x_1} \cap \mathcal{K}_{x_2}$
Faltung	$x(t) * y(t)$	$X(s) \cdot Y(s)$	$\mathcal{K}_x \cap \mathcal{K}_y$
Verschiebung	$x(t - t_0)$	$e^{-st_0} \cdot X(s)$	\mathcal{K}_x
Dämpfung	$e^{at} \cdot x(t)$	$X(s - a)$	$\mathcal{K}_x + \text{Re}\{a\}$
lineare Gewichtung	$t \cdot x(t)$	$-\frac{d}{ds} X(s)$	\mathcal{K}_x
Differentiation	$\frac{d}{dt} x(t)$	$s \cdot X(s)$	\mathcal{K}_x
Integration	$\int_{-\infty}^t x(\tau) d\tau$	$\frac{1}{s} \cdot X(s)$	$\mathcal{K}_x \cap \{\text{Re}\{s\} > 0\}$
Skalierung	$x(at)$	$\frac{1}{ a } \cdot X\left(\frac{s}{a}\right)$	$a \cdot \mathcal{K}_x$
konj. komplexes Signal	$x^*(t)$	$X^*(s*)$	\mathcal{K}_x

18.3 Spezielle Eigenschaften der einseitigen Laplace-Transformation

Verschiebung links	$x(t + t_0), t_0 > 0$	$e^{st_0} [X(s) - \int_{0^-}^{t_0} x(t) \cdot e^{-st} dt]$
Verschiebung rechts	$x(t - t_0), t_0 > 0$	$e^{-st_0} [X(s) + \int_{-t_0}^{0^-} x(t) \cdot e^{-st} dt]$
Differentiation	$\frac{d}{dt} x(t)$	$s \cdot X(s) - x(0^-)$
Anfangswertsatz	$x(0^+) = \lim_{s \rightarrow \infty} s \cdot X(s)$, falls $x(0^+)$ existiert	
Endwertsatz	$\lim_{t \rightarrow \infty} x(t) = \lim_{s \rightarrow 0} s \cdot X(s)$, falls $\lim_{t \rightarrow \infty} x(t)$ existiert	

18.4 Komplexe Umkehrformel der Laplace-Transformation

$$x(t) = \frac{1}{2\pi j} \int_{\sigma-j\infty}^{\sigma+j\infty} X(s) \cdot e^{st} ds, \quad \sigma \in \mathcal{K}$$

18.5 Rücktransformation durch Partialbruchzerlegung

$$X(s) = g_0 + \sum_i \frac{r_i}{s - \alpha_i} + \sum_i \sum_{l=1}^{m_i} \frac{\tilde{r}_{i,l}}{(s - \tilde{\alpha}_i)^l}, \quad g_i, \alpha_i, \tilde{\alpha}_i, r_i, \tilde{r}_{i,l} \in \mathbb{C}$$

kann für $\mathcal{K} : \text{Re}\{s\} > a_0$ mit den Korrespondenzen 1, 4, 5 und 10 gliedweise zur Rücktransformiert werden.

18.6 Korrespondenzen der Laplace-Transformation

Nr.	$x(t)$	$X(s)$	\mathcal{K}
1	$\delta(t)$	1	$s \in \mathbb{C}$
2	$\varepsilon(t)$	$\frac{1}{s}$	$\operatorname{Re}\{s\} > 0$
3	$\rho(t) = t \cdot \varepsilon(t)$	$\frac{1}{s^2}$	$\operatorname{Re}\{s\} > 0$
4	$e^{at} \cdot \varepsilon(t)$	$\frac{1}{s-a}$	$\operatorname{Re}\{s\} > \operatorname{Re}\{a\}$
5	$\frac{t^m}{m!} e^{at} \cdot \varepsilon(t)$	$\frac{1}{(s-a)^{m+1}}$	$\operatorname{Re}\{s\} > \operatorname{Re}\{a\}$
6	$\sin(\omega_0 t) \cdot \varepsilon(t)$	$\frac{\omega_0}{s^2 + \omega_0^2}$	$\operatorname{Re}\{s\} > 0$
7	$\cos(\omega_0 t) \cdot \varepsilon(t)$	$\frac{s}{s^2 + \omega_0^2}$	$\operatorname{Re}\{s\} > 0$
8	$\sin(\omega_0 t + \varphi_0) \cdot \varepsilon(t)$	$\frac{s \cdot \sin(\varphi_0) + \omega_0 \cdot \cos(\varphi_0)}{s^2 + \omega_0^2}$	$\operatorname{Re}\{s\} > 0$
9	$\delta(t - t_0)$	e^{-st_0}	$s \in \mathbb{C}$

18.7 Spezielle Korrespondenzen zur Rücktransformation konj. komplexer Polpaare

10	$2 r e^{\operatorname{Re}\{\alpha\}t} \cos(\operatorname{Im}\{\alpha\}t + \arg r)\varepsilon(t)$	$\frac{r}{s-\alpha} + \frac{r^*}{s-\alpha^*}$	$\operatorname{Re}\{s\} > \operatorname{Re}\{\alpha\}$
11	$e^{at} \cdot \frac{\cos(\omega_0 t + \varphi_0)}{\cos(\varphi_0)} \cdot \varepsilon(t)$ $a = \frac{b}{2}, \omega_0 = \sqrt{c - \frac{b^2}{4}}, \varphi_0 = \arctan\left(\frac{2d-b}{\sqrt{4c-b^2}}\right)$	$\frac{s-d}{s^2 - bs + c}, c > \frac{b^2}{4}$	$\operatorname{Re}\{s\} > \frac{b}{2}$

19 C.4 Fourier-Transformation

Definition:	Rücktransformation:
$X(f) = \int_{-\infty}^{\infty} x(t) \cdot e^{-j2\pi ft} dt$	$x(t) = \int_{-\infty}^{\infty} X(f) \cdot e^{j2\pi ft} df$

Definition über die Kreisfrequenz $\omega = 2\pi f$:

$$X(j\omega) = \int_{-\infty}^{\infty} x(t) \cdot e^{-j\omega t} dt \quad x(t) = \frac{1}{2\pi} \int_{-\infty}^{\infty} X(j\omega) \cdot e^{j\omega t} d\omega$$

20 Eigenschaften der Fourier-Transformation

	Zeitbereich	Frequenzbereich	
Linearity	$c_1x_1(t) + c_2x_2(t)$	$c_1X_1(f) + c_2X_2(f)$	$c_1X_1(j\omega) + c_2X_2(j\omega)$
Faltung	$x(t) * y(t)$	$X(f) \cdot Y(f)$	$X(j\omega) \cdot Y(j\omega)$
Multiplikation	$x(t) \cdot y(t)$	$X(f) * Y(f)$	$\frac{1}{2\pi}X(j\omega) * Y(j\omega)$
Verschiebung	$x(t - t_0)$	$X(f) \cdot e^{-j2\pi f t_0}$	$X(j\omega) \cdot e^{-j\omega t_0}$
Modulation	$e^{j2\pi f_0 t} \cdot x(t)$	$X(f - f_0)$	$X(j[\omega - \omega_0])$
lineare Gewichtung	$t \cdot x(t)$	$-\frac{1}{j2\pi} \frac{d}{df} X(f)$	$-\frac{d}{d(j\omega)} X(j\omega)$
Differentiation	$\frac{d}{dt} x(t)$	$j2\pi f \cdot X(f)$	$j\omega \cdot X(j\omega)$
Integration	$\int_{-\infty}^t x(\tau) d\tau$	$\frac{1}{j2\pi f} X(f) + \frac{1}{2} X(0) \delta(f)$	$\frac{1}{j\omega} X(j\omega) + \pi X(0) \delta(f)$
Skalierung	$x(at)$	$\frac{1}{ a } \cdot X\left(\frac{f}{a}\right)$	$\frac{1}{ a } \cdot X\left(\frac{j\omega}{a}\right) \delta(\omega)$
Zeitinversion	$x(-t)$	$X(-f)$	$X(-j\omega)$
konj. komplex	$x^*(t)$	$X^*(-f)$	$X^*(-j\omega)$
Real part	$x_R(t)$	$X_{g^*}(f)$	$X_{g^*}(j\omega)$
Imaginary part	$jx_I(t)$	$X_{u^*}(f)$	$X_{u^*}(j\omega)$
duality	$X(t)[X(jt)]$	$x(-f)$	$2\pi x(-\omega)$
Parsevalsches Theorem	$\int_{-\infty}^{\infty} x(t) \cdot y^*(t) dt = \int_{-\infty}^{\infty} X(f) \cdot Y^*(f) df = \frac{1}{2\pi} \int_{-\infty}^{\infty} X(j\omega) \cdot Y^*(j\omega) d\omega$		

Nr.	$x(t)$	$X(f)$	$X(j\omega)$
1	$\delta(t)$	1	1
2	1	$\delta(f)$	$2\pi\delta(\omega)$
3	$U_T(t)$	$\frac{1}{ T } \text{IH}_{\frac{1}{T}}(f)$	$\frac{2\pi}{ T } U_{\frac{2\pi}{T}}(\omega)$
4	$\varepsilon(t)$	$\frac{1}{2}\delta(f) + \frac{1}{j2\pi f}$	$\pi\delta(\omega) + \frac{1}{j\omega}$
5	$\text{sgn}(t)$	$\frac{1}{j\pi f}$	$\frac{2}{j\omega}$
6	$\frac{1}{\pi t}$	$-j \text{sgn}(f)$	$-j \text{sgn}(\omega)$
7	$\text{rect}\left(\frac{t}{T}\right)$ ($T = \text{width}$)	$ T \cdot \text{si}(\pi T f)$	$ T \cdot \text{si}\left(\frac{T}{2}\omega\right)$
8	$\text{si}\left(\pi\frac{t}{T}\right)$	$ T \cdot \text{rect}(T f)$	$ T \cdot \text{rect}\left(\frac{T}{2\pi}\omega\right)$
9	$\Lambda\left(\frac{t}{T}\right)$	$ T \cdot \text{si}^2(\pi T f)$	$ T \cdot \text{si}^2\left(\frac{T}{2}\omega\right)$
10	$\text{si}^2\left(\pi\frac{t}{T}\right)$	$ T \cdot \Lambda(T f)$	$ T \cdot \Lambda\left(\frac{T}{2\pi}\omega\right)$
11	$e^{j2\pi f_0 t}$	$\delta(f - f_0)$	$2\pi\delta(\omega - \omega_0)$
12	$\cos(2\pi f_0 t)$	$\frac{1}{2} [\delta(f + f_0) + \delta(f - f_0)]$	$\pi [\delta(\omega + \omega_0) + \delta(\omega - \omega_0)]$
13	$\sin(2\pi f_0 t)$	$\frac{1}{2}j [\delta(f + f_0) - \delta(f - f_0)]$	$\pi j [\delta(\omega + \omega_0) - \delta(\omega - \omega_0)]$
14	$e^{-a^2 t^2}$	$\frac{\sqrt{\pi}}{a} e^{-\frac{\pi^2 f^2}{a^2}}$	$\frac{\sqrt{\pi}}{a} e^{-\frac{\omega^2}{4a^2}}$
15	$e^{-\frac{ t }{T}}$	$\frac{2T}{1+(2\pi T f)^2}$	$\frac{2T}{1+(T\omega)^2}$

Where

$$\text{sinc}(x) = \frac{\sin \pi x}{\pi x}$$

$$\text{si}(x) = \frac{\sin x}{x}$$