A Bootstrapped Switch with Accelerated Rising Speed and Reduced On-Resistance

Haoyu Zhuang, Qifu Cao, Xizhu Peng, and He Tang
School of Electronic Science and Engineering
University of Electronic Science and Technology of China
tanghe@uestc.edu.cn

2021 IEEE International Symposium on Circuits and Systems (ISCAS) | 978-1-7281-9201-7/20/$31.00 ©2021 IEEE | DOI: 10.1109/ISCAS51556.2021.9401785

***Abstract*—This paper presents a bootstrapped switch with an accelerated gate-voltage rising speed and a reduced on-resistance for high-speed ADCs. Compared to the classic bootstrapped switch, this design accelerates the rising speed of gate voltage through four novel techniques. First, an extra NMOS transistor is added to pull up the gate voltage by injecting extra charges into the gate node. Second, the parasitic capacitance at the gate node is reduced by simplifying the circuit structure, leading to a faster speed. Third, transmission gates are used to reduce the two delays to one delay. Fourth, the voltage stored on the capacitor is increased to slightly larger than V_{DD}, which leads to a faster gate-voltage rising speed as well as a larger value of gate voltage (about V_{in}+1.05V_{DD}). The larger gate voltage also helps reduce the on-resistance of the bootstrapped switch, which is helpful for the high-speed sampling of ADCs. In a 40 nm CMOS process, post-layout simulation results show that the rising speed of gate voltage is increased by 3.3 times compared to the classic thin-oxide bootstrapped switch circuit. And the on-resistance of the bootstrapped switch is reduced by 2.2 times compared to the classic structure, due to the larger gate voltage value.**

Keywords—Bootstrapped Switch; High-Speed; Reduced On-Resistance; Rising Speed Acceleration.

I. Introduction

Due to the development of communication industry, high-speed analog-to-digital converter (ADC) is of great interest over the past decade. In such ADCs, the sample-and-hold circuit is indispensable and has a significant influence on the ADC performance, such as the sampling rate and resolution. To improve resolution, bootstrapped switches, instead of CMOS switches, are widely used, thanks to the low and constant on-resistance.

In recent years, there are many techniques reported to enhance the performance of bootstrapped switches, such as [1]-[14]. These works mainly focus on the sampling accuracy, rather than the sampling rate, of bootstrapped switch circuits. However, in high-speed medium-resolution ADCs (6~8 bits, several GHz), such as [15]-[18], the sampling rate is the top priority, while the sampling accuracy is secondary. Thus, the goal of this paper is to increase the sampling rate.

The sampling rate of a bootstrapped switch depends on three factors: the size of sampling capacitor, the on-resistance of the bootstrapped switch, and the gate-voltage rising speed of bootstrapped switch (rises from 0 to V_{in}+V_{DD}). Among them, the first factor can hardly be improved for faster sampling rate, because this factor is already determined by the allowed maximum kT/C noise and capacitance mismatch due to the target ADC resolution. By contrast, the last two factors can be easily improved for faster sampling rate. For example, we can increase the gate voltage value to slightly larger than V_{in}+V_{DD} (for example V_{in}+1.05V_{DD}), rather than slightly smaller than V_{in}+V_{DD} (for example V_{in}+0.8V_{DD}) as in a conventional structure (due to the coupling of parasitic capacitance). This helps reduce the on-resistance of the bootstrapped switch. Note that the slightly larger gate voltage value will not cause the aging effect of transistor, because the voltage across transistor is at most 1.05V_{DD} and thus it is still much smaller than the upper limit of valid bias range, according to the PDK. In sum, this paper focuses on how to improve the last two factors for a faster sampling rate.

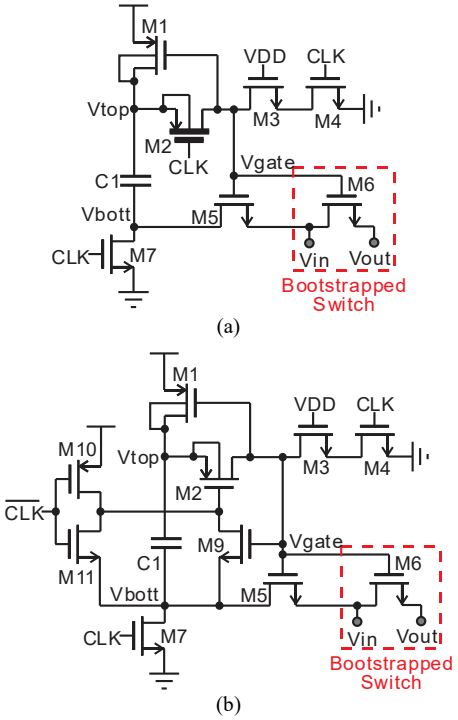

Fig. 1. Classic bootstrapped switch circuits (a) with a thick-oxide MOS transistor and (b) with thin-oxide MOS transistors only.

Fig. 1 shows two classic bootstrapped switch circuits, where Fig. 1(a) [2] shows the bootstrapped switch with a thick-oxide MOSFET M2, and Fig. 1(b) [3] shows the bootstrapped switch with thin-oxide MOSFETs only. In Fig. 1(a), the thick oxide of M2 is used to prevent M2 from being broken down, because the voltage across M2 can be as large as 2V_{DD}, and a thick-oxide MOSFET has a larger breakdown voltage of 4V_{DD}. By contrast, in Fig. 1(b), a more complicated structure is used to prevent the voltage across M2 from being as large as 2V_{DD}, thus the thick oxide is no longer needed for M2. The principle of Fig. 1(a) and Fig. 1(b) are similar. During the reset phase (CLK=1), the voltage across the capacitor C1 is reset to V_{DD}, and the gate voltage V_{gate} of the bootstrapped switch is reset to 0V. During the bootstrap phase (CLK=0), M5 is turned on to connect the bottom plate of capacitor C1 to V_{in}, so that the top plate of capacitor C1 is V_{in}+V_{DD}. And then, M2 is turned on to transmit V_{in}+V_{DD} to the gate voltage V_{gate} of the switch. Since the on-resistance of a thin-oxide MOSFET is much smaller (3.7 times) than a thick-oxide MOSFET, the gate-voltage rising speed of Fig. 1(b) is much faster than Fig. 1(a). Simulation results in 40 nm CMOS show

that the gate-voltage rising speed of Fig. 1(b) is 2.1 times faster than Fig. 1(a). Thus, the proposed structure in this paper is based on the thin-oxide version of Fig. 1(b).

For a faster sampling rate, this paper proposes four novel techniques. Firstly, an additional NMOS transistor is added to pull up the gate voltage of the bootstrapped switch, by injecting extra charges into the gate node. Secondly, the parasitic capacitance at the gate node is reduced by simplifying the circuit structure, thus leading to a faster speed. Thirdly, transmission gates are used to further reduce the delay. Fourthly, the voltage stored on the capacitor is increased to slightly larger than V_{DD}, which helps increase the gate-voltage rising speed as well as reduce the on-resistance of the bootstrapped switch. Designed in a 40nm CMOS process, the proposed bootstrapped switch circuit increases the gate voltage value to V_{in}+1.05V_{DD}. Compared to the conventional structure of Fig. 1(b), the gate-voltage rising speed is increased by 3.3 times, and the on-resistance of bootstrapped switch is decreased by 2.2 times.

This paper is organized as follows. Section II discusses the proposed bootstrapped switch and analyses the circuit principle. Section III shows the post-layout simulation results and compares with the state-of-the-art work. Section IV concludes the paper.

II. The Proposed Bootstrapped Switch

A. First Version of the Proposed Bootstrapped Switch

For a faster sampling rate, Fig. 2 shows the first version of the proposed bootstrapped switch. Compared to the classic structure of Fig. 1(b), the only difference is the addition of M8 in Fig. 2 for accelerating the gate-voltage rising speed of V_{gate}. To understand the reason of adding M8, let us first review the operation of Fig. 1(b) as well as its drawbacks.

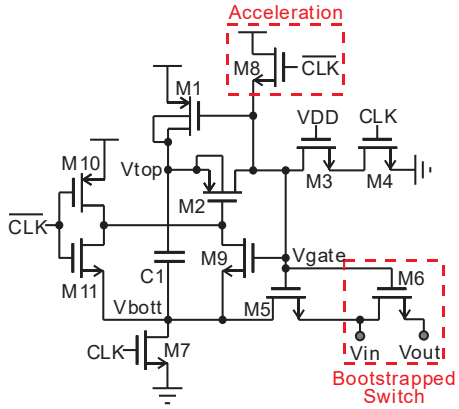

Fig. 2. First version of the proposed bootstrapped switch.

In the bootstrap phase of Fig. 1(b), $\overline{CLK}$ rises and turns on M11, which pulls down the gate V_{g2} of M2 to the bottom plate V_{bott} of capacitor C1. At this moment, the voltage across capacitor C1 (equal to V_{DD}) is applied onto the source-gate of M2, which turns on M2 for pulling up the gate voltage V_{gate}. This process, from the rising of $\overline{CLK}$ to the rising of V_{gate}, can be divided into two delays: the delay from the rising of $\overline{CLK}$ to the falling of V_{g2} (pulled down by M11), and the delay from the falling of V_{g2} to the rising of V_{gate} (pulled up by M2). More seriously, before the rising of V_{gate}, M5 cannot be turned on to pull up V_{bott} to V_{in}, which means more delay required before the bootstrap process finishes.

To reduce delay, an additional transistor M8 is added into Fig. 2. Thus, at the rising edge of $\overline{CLK}$, M8 is turned on to pull up V_{gate} immediately. This means that, from the rising of $\overline{CLK}$ to the rising of V_{gate}, there is only one transistor delay left. This is how M8 accelerates the V_{gate} rising speed. After that, when V_{gate} rises to above V_{DD}, M8 is turned off automatically, and no longer affects the bootstrap process. And finally, V_{gate} will rise to approximately V_{in}+V_{DD}. Another advantage of M8 is that, M8 is an NMOS transistor, and the NMOS electron mobility is 2 to 3 times larger than the PMOS hole mobility. Thus, compared to the case where only PMOS M2 is used to pull up V_{gate} as in Fig. 1(b), an additional NMOS M8 can effectively accelerate the V_{gate} rising speed. The only cost is that, M8 injects additional charges into the V_{gate} node, causing V_{gate} to slightly deviate from the desired value. And this deviation is dependent on V_{in}, which will slightly influence the ADC sampling accuracy. Nevertheless, for high-speed medium-resolution ADCs (6~8 bits, several GHz) [15]-[18], the sampling speed is the top priority, while the sampling accuracy is secondary, thus this cost can be neglected.

Under a 40nm CMOS process, simulation results show that the gate-voltage rising speed is increased by 1.1 times compared to Fig. 1(b). (see Section III for more details)

B. Second Version of the Proposed Bootstrapped Switch

For an even faster sampling rate, Fig. 3 shows the second version of the proposed bootstrapped switch. Compared to the first version in Fig. 2, the difference is the three modifications below.

Firstly, transistors M3, M4, and M8 in Fig. 2 are combined into one transistor M3 in Fig. 3, which realizes the same function as M3, M4, and M8. This modification helps simplify the circuit structure and reduce the parasitic capacitance at the V_{gate} node, thus accelerating the gate-voltage rising speed. The principle of this M3 in Fig. 3 is as follows. During the reset phase ($\overline{CLK}$=0), M3 is turned on for resetting V_{gate} to 0. During the bootstrap phase ($\overline{CLK}$=1), M3 is turned on for pulling up V_{gate}. After V_{gate} rises to above V_{DD}, M3 is turned off automatically, and no longer affects the bootstrap process. Finally, V_{gate} rises to approximately V_{in}+V_{DD}.

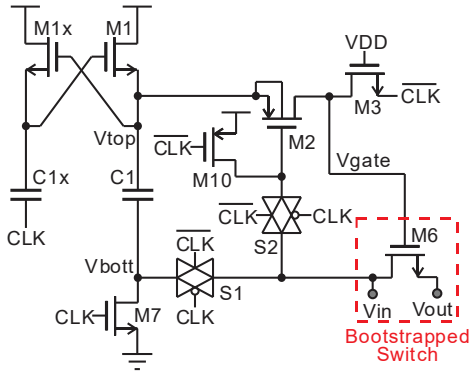

Fig. 3. Second version of the proposed bootstrapped switch.

Secondly, M5, M9, and M11 in Fig. 2 are replaced by the transmission gates S1 and S2 in Fig. 3. This modification accelerates the connection of both V_{g2} and V_{bott} to V_{in}, which further increases the gate-voltage rising speed. For easy understanding, let us first review the operation of Fig. 2. In Fig. 2, after $\overline{CLK}$ rises, M8 is turned on to pull up V_{gate}. The rising of V_{gate} turns on M5 to pull up V_{bott} to V_{in}. This process can be divided into two delays: the delay from the rising of

$\overline{CLK}$ to the rising of V_{gate} (pulled up by M8), and the delay from the rising of V_{gate} to the rising of V_{bott} (pulled up by M5). By contrast, in Fig. 3, after $\overline{CLK}$ rises, the transmission gate S1 is turned on immediately to pull up V_{bott} to V_{in}, which means only one transistor delay. This helps accelerate the gate-voltage rising speed. Furthermore, in Fig. 2, after V_{gate} rises, both M5 and M9 are turned on to connect V_{g2} to V_{in}. By contrast, in Fig. 3, after $\overline{CLK}$ rises, the transmission gate S2 is turned on immediately to connect V_{g2} to V_{in}. This realizes the same operation, while simplifying the circuit structure.

Thirdly, the PMOS M1 in Fig. 2 is replaced by an NMOS M1 in Fig. 3, whose gate voltage is generated by additional M1x and C1x. The reason for this modification is as follows. If Fig. 3 still uses a PMOS for M1, and if the gate of M1 in Fig. 3 is still connected to V_{gate} as Fig. 2 does, then M1 in Fig. 3 will be unexpectedly turned on during the bootstrap phase ($\overline{CLK}$=1). This is because, after $\overline{CLK}$ rises, the switch S1 in Fig. 3 is immediately turned on to pull up V_{bott} to V_{in}, and pull up V_{top} to V_{in}+V_{DD} though capacitor C1. Meanwhile, V_{gate} is also pulled up to V_{DD}-V_{th} by M3. This means that, M1 is turned on unexpectedly at this moment, because its drain voltage (V_{in}+V_{DD}) is much larger than the gate voltage (V_{DD}-V_{th}). This unexpected state of M1 will pull down V_{top}, destroying the voltage stored on the capacitor C1. To solve this problem in Fig. 3, we replace the PMOS of M1 with an NMOS. Because the gate voltage of NMOS M1 is V_{DD} at this moment, M1 is turned off, preventing the above problem from happening again.

Under a 40nm CMOS process, simulation results show that the gate-voltage rising speed is increased by 2.6 times compared to Fig. 1(b). Furthermore, compared to Fig. 1(b) where V_{gate} only rises to V_{in}+0.71V_{DD} due to the parasitic capacitance, V_{gate} in Fig. 3 rises to V_{in}+0.81V_{DD} due to the reduced parasitic capacitance at the nodes V_{gate} and V_{top}. (see Section III for more details)

C. *Final Version of the Proposed Bootstrapped Switch*

To further increase the sampling rate, Fig. 4 shows the final version of the proposed bootstrapped switch. Compared to the second version of Fig. 3, the difference is the two modifications as discussed below.

Firstly, the drain of M1 is no longer connected to V_{DD}. Instead, it is connected to VY which is larger than V_{DD}. This is to reset the top plate V_{top} of capacitor C1 to slightly larger than V_{DD} in the reset phase. As a result, during the bootstrap phase, V_{gate} can rise to slightly larger than V_{in}+V_{DD}, rather than slightly smaller than V_{in}+V_{DD} as in a conventional structure. This can effectively reduce the on-resistance of the bootstrapped switch M6.

Secondly, the source of M10 is no longer connected to V_{DD}. Instead, it is connected to V_{top} through M12. To understand the reason for this modification, let us first review Fig. 3 again. In the reset phase ($\overline{CLK}$=0) of Fig. 3, M10 is turned on to pull up V_{g2} to V_{DD}. This makes M2 turned off, because both the gate and source of M2 are at V_{DD} at this moment. However, in Fig. 4, the case is different, where the source of M2 (node V_{top}) is slightly larger than V_{DD}, rather than equal to V_{DD}, making M2 fail to be turned off. To address this issue, we connect the gate of M2 to V_{top} through M10 and M12 (M10 and M12 are turned on at this moment). This ensures that M2 is turned off.

The operation of Fig. 4 is as follows. During the reset phase (CLK=1, $\overline{CLK}$=0), VY raises to 2V_{DD} to charge V_{top} through M1. This makes V_{top} raise to larger than V_{DD}. Note that, V_{top} can only be charged to slightly larger than V_{DD}, rather than equal to 2V_{DD}. This is because VY will decrease after the charge sharing, and the voltage across M1 is as large as V_{th}≈0.45V. During the bootstrap phase (CLK=0, $\overline{CLK}$=1), V_{top} rises to slightly larger than V_{in}+V_{DD}, while V_{g2} is connected to V_{in}. This makes the source-gate voltage of M2 slightly larger than V_{DD} so that M2 can pull up V_{gate} at a higher speed than Fig. 3. This is another advantage of this circuit.

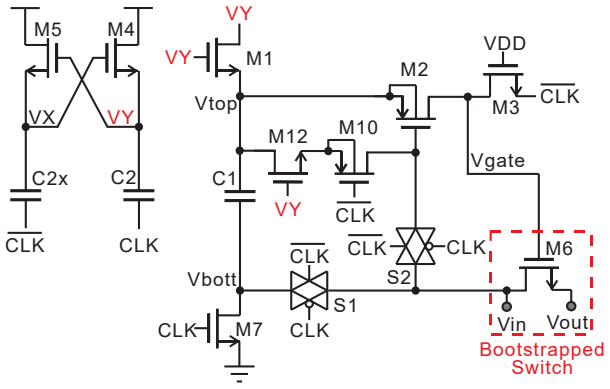

Fig. 4. Final version of the proposed bootstrapped switch.

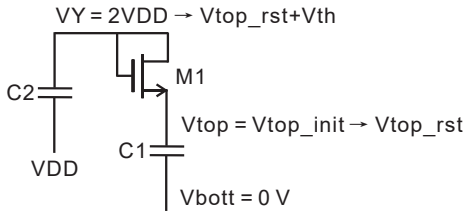

Fig. 5. Voltage values at the beginning and the end of reset phase.

For easy understanding, we derive formulas to quantitatively discuss the circuit in detail, as follows.

Ideally, for a conventional bootstrapped switch circuit, the gate voltage should rise to V_{in}+V_{DD}. However, in reality, the gate voltage can only rise to a smaller value V_{in}+ΔV (ΔV<V_{DD}), due to the parasitic capacitances in the conventional circuit. Here, ΔV can be calculated as follows:

$$\Delta V = V_{top\_rst}\frac{C1 + C_{p\_top}}{C1 + C_{p\_top} + C_{p\_gate}} - V_{in}\frac{C_{p\_top} + C_{p\_gate}}{C1 + C_{p\_top} + C_{p\_gate}} \quad (1)$$

where V_{top_rst} is the V_{top} value at the end of reset phase, C_{p_top} is the parasitic capacitance at node V_{top}, and C_{p_gate} is the parasitic capacitance at node V_{gate}. For the conventional structure of Fig. 1(b), V_{top_rst} is equal to V_{DD}. For the proposed circuit of Fig. 4, V_{top_rst} is slightly larger than V_{DD}. Thus, according to Eq. (1), if the parasitic capacitances are 0, then ΔV of Fig. 1(b) will be V_{DD}, and ΔV of Fig. 4 will be slightly larger than V_{DD}. Simulation results show that ΔV of Fig. 1(b) is 0.71V_{DD} due to the parasitic capacitances, and ΔV of Fig. 4 is 1.05V_{DD}.

To calculate V_{top_rst} for Fig. 4, Fig. 5 shows the voltage values at the beginning and the end of reset phase (CLK=1). At the beginning of reset phase, VY rises to about 2V_{DD}, while V_{top} is at its initial value V_{top_init}. This makes M1 turned on which transfers charges from C2 to C1. As a result, at the end of reset phase, V_{top} rises to V_{top_rst}, while VY falls to V_{top_rst}+V_{th}, where V_{th} is the threshold voltage of M1. Thus, according to

the law of conservation of charges, V_{top_rst} can be calculated as follows:

$$V_{top\_rst} = \frac{2 \cdot V_{DD} \cdot C2 + V_{top\_init} \cdot C1 - V_{th} \cdot C2}{C1 + C2} \quad (2)$$

With a proper ratio between C1 and C2, the V_{top_rst} can be set to slightly larger than V_{DD}.

As mentioned before, one advantage of this circuit is the increased driving ability of M2 and thus a faster rising speed of V_{gate}, because the source-gate voltage of M2 is increased to slightly larger than V_{DD} in the bootstrap phase. Due to the squared relationship in *I-V* of MOSFET in saturation region, the increased source-gate voltage of M2 leads to an increase in its current I_2. Simulation results show that the current I_2 of Fig. 4 is increased by 2.1 times compared to Fig. 3.

Besides, as mentioned before, the V_{gate} slightly larger than V_{in}+V_{DD} leads to a reduced on-resistance of the bootstrapped switch M6. Simulation results show that the on-resistance of M6 is reduced by 2.2 times compared to the classic structure of Fig. 1(b), and 1.6 times compared to Fig. 3.

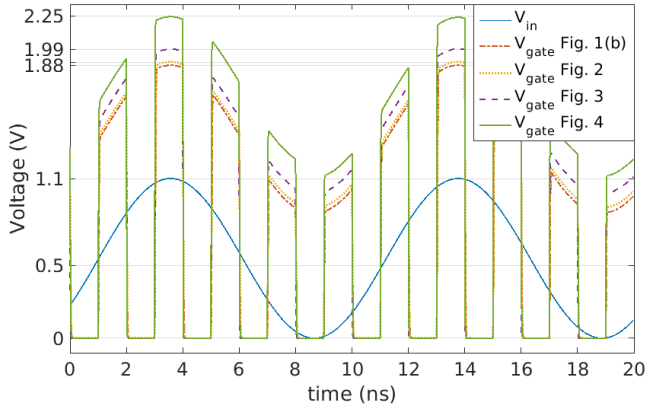

Fig. 6. The curve of V_{gate} and V_{in}.

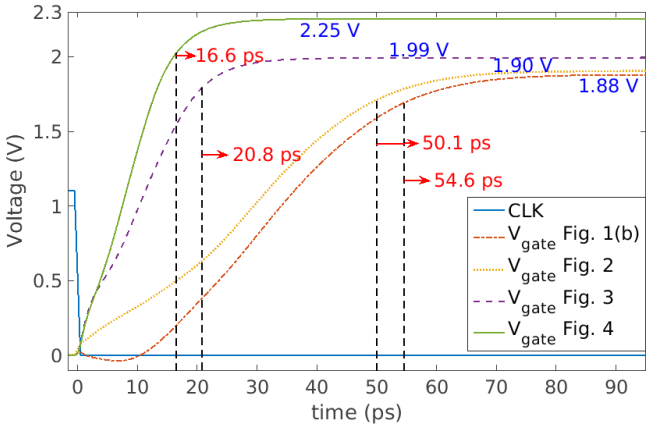

Fig. 7. The rising time of V_{gate} when V_{in}=V_{DD}.

III. Post-Layout Simulation Results

All the above bootstrapped switch circuits of Fig. 1 to Fig. 4 are designed in the same 40nm CMOS process. To make a fair comparison, all the circuits use the same MOSFET sizes and the same capacitor sizes.

With a 1.1V V_{DD}, a 500MHz CLK, and a 1.1V_{pp} 100MHz sinusoidal V_{in}, Fig. 6 shows the curve of V_{gate} and V_{in}. As can be seen, ΔV of Fig. 1(b) is only 0.71V_{DD}, while that of Fig. 4 is 1.05V_{DD}.

Fig. 7 shows the rise time of V_{gate} when V_{in}=V_{DD}. This rise time is calculated at the 90% settling of V_{gate}. As can be seen, the rise time of the classic structure of Fig. 1(b) is 54.6ps, and its ΔV is only 0.71V_{DD}. Its slow rising is because of the two delays discussed before and the small current I_2, while the small ΔV is due to the large parasitic capacitance. By contrast, Fig. 2 reduces the rise time by 4.5ps using an additional transistor to inject extra charges. Fig. 3 has a small rise time of 20.8ps and a large ΔV of 0.81V_{DD}. Fig. 4 has a rise time of only 16.6ps and a large ΔV of 1.05V_{DD}. Note that, Fig. 4 only needs 13.4ps to rise to the same voltage as Fig. 3. This means that, the rising speed of Fig. 4 is 1.55 times faster than Fig. 3.

Table I summarizes the performance of each bootstrapped switch circuit. The key highlight of the proposed circuit of Fig. 4 is the smallest rise time of V_{gate} as well as the smallest R_{on}. Compared to Fig. 1(b), it reduces V_{gate} rise time by 3.3 times, and reduces R_{on} by 2.2 times.

Table II compares the dynamic performance of sampling-hold (S/H) circuits constituted by the bootstrapped switch circuits, respectively. The S/H circuit using Fig. 4 as the sampling switch achieves the highest ENOB, due to the smallest on-resistance R_{on} than other structures.

TABLE I
PERFORMANCE OF DIFFERENT STRUCTURES

	Fig. 1(b)	Fig. 2	Fig. 3	Fig. 4
ΔV	0.71V_{DD}	0.73V_{DD}	0.81V_{DD}	1.05V_{DD}
I_2 normalized to Fig. 1(b)	1	1	1	2.1
rise time of V_{gate}	54.6ps	50.1ps	20.8ps	16.6ps
R_{on} normalized to Fig. 1(b)	1	0.93	0.74	0.46

TABLE II
DYNAMIC PERFORMANCE OF THE S/H CIRCUIT

	Fig. 1(b)	Fig. 2	Fig. 3	Fig. 4
ENOB	11.79	11.74	11.46	12.15
SNDR	72.77	72.60	72.31	75.1

IV. Conclusion

This paper presents a novel bootstrapped switch circuit with an accelerated gate-voltage rising speed and a reduced on-resistance of switch. Several techniques are proposed to realize this improved performance. Designed in a 40nm CMOS process, simulation results show that the gate-voltage rising speed is increased by 3.3 times, and the on-resistance is reduced by 2.2 times.

V. Acknowledgment

This work is supported by NSFC under Grant 62004023, Department of Science and Technology of Sichuan Province under Grant 2018GZDZX0003 / 2020YFG0285, and National Key R&D Program of China under Grant 2018YFB2100100.

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