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A Compact 20GHz Dynamic Latch Comparator in 65nm CMOS Process

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***Abstract* —This work reports techniques for designing an ultra-high speed dynamic latch comparator. The effective transconductance of the cross-coupled devices consisting the latch mechanism has been improved using a compact architecture, then reducing mismatch and parasitic, increasing therefore the regeneration speed. The pre-charge step of the preamplifier has been speeded-up using an enhanced differential pair amplifier based active NMOS load. Monte-Carlo analysis of the proposed circuit implemented in 65nm CMOS process, proved that the device can achieve 20GHz sampling frequency while consuming only 78µW of power from 1V supply voltage. The high-speed behavior of the circuit was guaranteed with 14.28ps time delay and 4.45mV offset voltage. The compact circuit layout occupied only 133.15μm^2 of active area.**

Keywords —propagation delay, latch systems, kickback noise power dissipation.

I. INTRODUCTION

High-speed analog to digital converters (ADCs) are frequently used to handle data conversion and signal transmission in communication systems, microprocessors, microcontrollers and FPGA devices. The strap between analog and digital processing methods requires the usage of accurate and low-power ADCs. Variety of communications systems such as Ethernet, wireless communication still need miniaturized and power-efficient mixed signal circuits [1] – [4].

Mixed-mode signal circuits are greatly affected by mismatch and process variations [1], [3], [4]. High frequency (> 1GHz) operations, exacerbate the situation. The main mixed-mode parts circuits of the ADC greatly affected by this concern is the comparator. For high-speed and low-power purpose, latch type comparators are preferred to static counterpart, since their positive feedback enhances the comparison process and the decision making of the latch [5] – [9]. As illustrated on Fig.1, the important role of a latch type comparator is exhibited in the block diagram of a sigma-delta analog to digital converter (ADC).

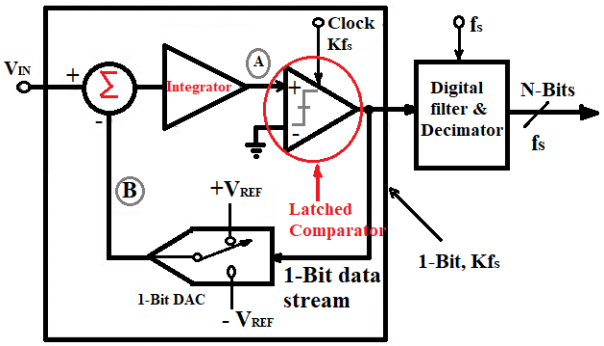

Figure.1. Block diagram of a sigma-delta ADC

The main inconvenient in latch type voltage sense amplifier is the static power dissipation which worsen with scaling down of technology [9]. Besides, input common mode voltage [10] – [12] strongly influences, the operation's speed and offset of the circuit. Reducing offset involves enlarging the devices, increasing the parasitic capacitance, which in turns slows the regeneration process, increases power dissipation therefore and occupies more space [11], [10]. These are the most challenges while implementing high-speed dynamic latched comparator (DLC).

In this research, a compact two stages latch type comparator is designed for ultra-high speed ADCs. The proposed circuit was implemented in 65nm CMOS process using LTSpice and Electric VLSI tools.

II. DESIGN METHODOLOGY

A. The proposed latch type comparator

A custom differential pair amplifier is used as preamplifier stage. The circuit works based on active NMOS load resistor as illustrated in Fig.2 (dotted rectangle). This allows driving a maximum output voltage of V_{DD} - V_{THN} when the drain and gate of the NMOS load devices are settled to V_{DD}. The output terminals of the differential pair should be pre-charged from 0 to V_{DD} - V_{THN} therefore; ensuring a fast comparison speed at this stage. The threshold voltage shifting was minimized thanks to custom transistor design that reduced the body effect which affects the comparison process in the preamplifier module. The proposed compact dynamic latch comparator works in two main steps: the pre-charge step and the regeneration one.

1. *The pre-charge step*

When the clock is low; no current flows through the tail transistor of the sense amplifier (M1), since the device is off. No static power is therefore consumed by the circuit in this state. Transistors M5 and M4 are switched ON, driving therefore nodes F1 and F2 to V_{DD} -V_{THN}; which in turn helps in switching M6 and M7 ON. In addition transistors M8 and M9 behave as an open circuit, then M6 and M7 are turned ON; involving terminals D1 and D2 to be discharged to ground state. Then, the latch outputs are pre-charged to V_{DD} due to the action of the pull-up transistors (M15 and M14) which are switched ON.

2. *The regeneration step*

During the regeneration process, transistors M5, M4, M15, M14, M17 and M16 are switched Off; giving therefore the possibility to transistors M10 and M11 to drive their drain-source current respectively. Currents I_{F1} and I_{F2} flow from V_{DD} to ground; enabling therefore current Icm to flow which helps in turning ON the tail transistor of the sense amplifier. Thanks to the highest transconductance of M2 comparing to M3, the drain's potential of M2 decreases at a faster speed than the drain of M3 when *Vinp>Vinm*. The cross-coupled mechanism of M13/M10 exhibits a positive feedback that kicks in, enabling therefore terminal D1 to drop faster and pulling Voutm to low logic; in the same time M12 is switched ON and pulls Voutp to high logic, the decision is therefore made. Ones the decision made, M10 and M11 are turned off, that avoid static power dissipation [2]. When *Vinp<Vinm,* the opposite phenomena is produced, allowing Voutp to settle low logic and Voutm to high logic. The design of M1 should be therefore of high interest to minimize Icm and prevent dynamic power dissipation of the circuit. The transient induced kickback noise at the regeneration nodes D1 and D2 is reduced thanks to switches M6 and M7 which in turn isolate the drains of the differential input transistors from D1 and D2 during the regeneration phase [2]. The outputs swing of the circuit when its inputs are very close to the latch's trip point is presented in Fig.3. The circuit works slowly and inters in a metastable state, since the differential input voltage of only 5mV is very close to the comparator's input-referred offset. Accordingly, the comparator would not settle a valid level. That phenomenon known as meta-stability, occurs in latch type comparator when the input is near the comparator's decision point. [2], [4]-[8].

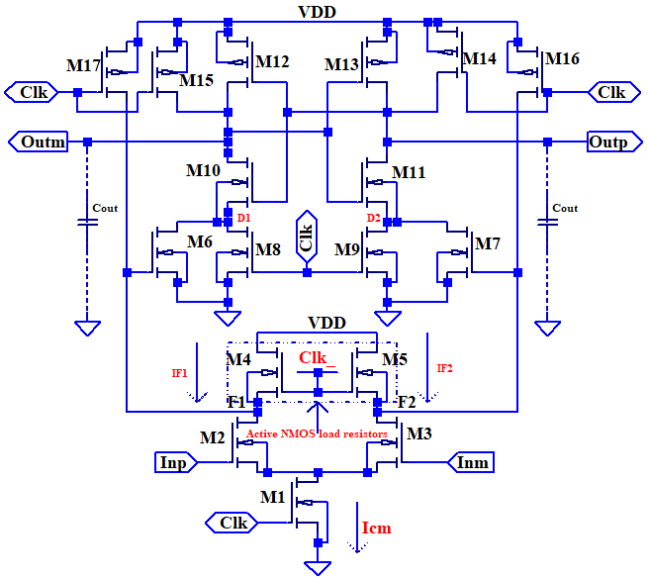

Figure.2. Block diagram of our DLC.

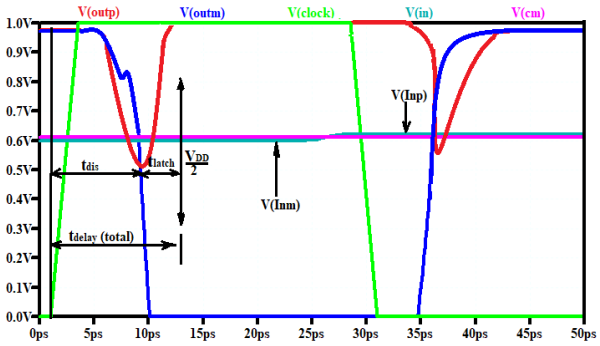

Figure.3.Transient simulation of the proposed dynamic latch comparator (VDD =1V, Vcm= 0.5V, ΔVin = 5mV, clk= 20GHz).

III. RESULTS AND DISCUSSION

A. *Simulation outcomes*

The circuit has been designed and simulated with respect to the 65nm CMOS technology. Fig.4 shows the simulated power-delay product (PDP) of the proposed comparator versus common mode voltage for different differential input voltages. As shwon in Figure.4, when the common mode voltage is larger than 0.6V, the circuit achieved the optimal

design parameters in term of power consumption and time delay. In Fig.5, the average power conmsumption of the proposed circuit is simulated along with the comparator output voltages (Voutp and Voutm). From 1V supply voltage, the circuit consumes only 78 µW of power while operating at 20GHz sampling frequency; the differential input voltage being set to 20mV and the common-mode voltage to 0.5V.

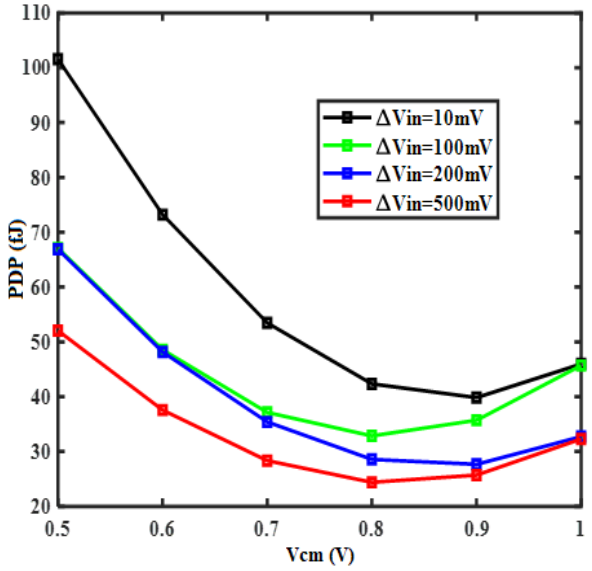

Figure.4. Power delay product of our DLC versus differential input voltage

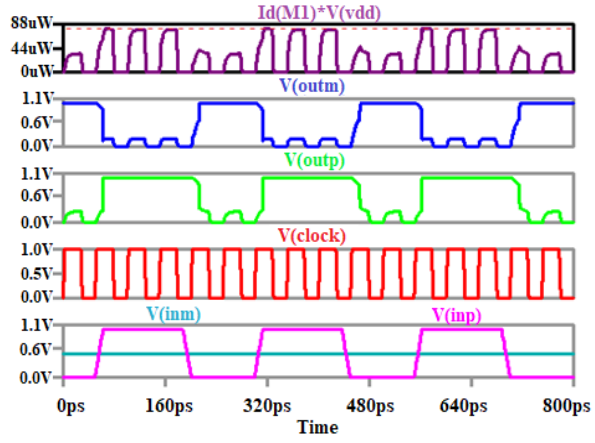

Figure.5.Power consumption of our DLC (VDD =1V, Vcm= 0.5V, ΔVin = 20mV, clk= 20GHz)

B. *Monte-Carlo Simulation*

The transient simulation provided by Monte-Carlo analysis is presented in Fig.6; it clearly reveals that at 20GS/s sampling rate, the proposed DLC's outputs swing do not vary significantly for 500runs. The stability of our circuit has been verified through Monte-Carlo simulation for 500 runs. The latch outputs voltages vary from 0 to $V_{DD} - 62.08mV > \frac{V_{DD}}{2}$ (for Outp) and from 0 to $V_{DD} - 71.13mV > \frac{V_{DD}}{2}$ (for Outm) respectively for 500 runs. As depicted on Fig.6, error due to process variation on Voutp and Voutm is 62.08mV and 71.13mV respectively.

These little variations do not affect the decision of the latch system; confirming therefore the 20GHz clock frequency for ultra-high speed operations respectively when ΔVin = 0.5V, Vcm = 0.5V and the sampling rate being set to 20GHz while using 1V supply voltage. From this statistical analysis, the comparator's offset voltage was reduced to 4.45mV with 3.74mV standard deviation as illustrated on Fig.7. In addition, an average delay time of only 14.28ps with 1.82ps standard deviation was controlled as shown on Fig.8.

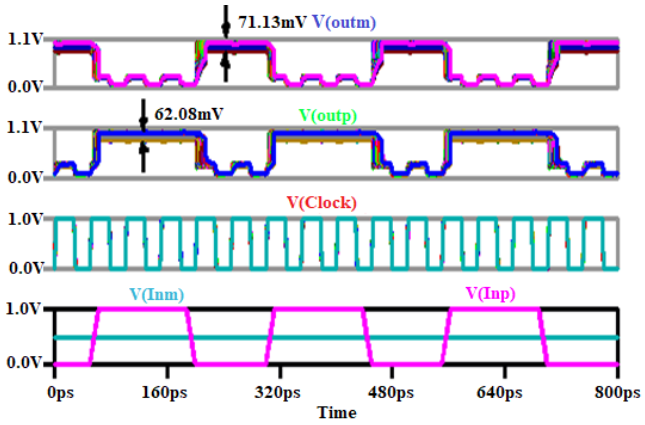

Figure.6. Monte-Carlo simulation results of our DLC for 500 runs.

The proposed design exhibited 8ps time delay during the regeneration process, which involves faster comparison speed. Thanks to the auxiliary transistors, the comparison process is speeded-up by a factor of 33% comparing to that of the circuits proposed in refs [1] and [4]. In Figure.9, the chip layout was designed and a very less die area of 133.15 µm^2 has been achieved, due to mismatch and parasitic reduction during the design process, and mostly to the symmetrical placement of all the MOSFETs consisting the circuits. The transistors have been rigorously sized and their optimal aspect ratios are given in Table.1. This allows achieving accurate and efficient dynamic performance.

C. *Dynamic performance*

The dynamic performance is evaluated by calculating the effective number of bit (ENOB) [11, 12]. Thanks to the smallest input-referred offset (V_{off}) extracted from simulation results, the ENOB is derived from (1) as:

$$V_{off} = \frac{V_{ref}}{2^{ENOB}} \quad (1)$$

where, $V_{ref} = V_{cm} = \frac{V_{DD}}{2}$ was considered for offset simulation with 20Gs/s sampling rate. The ENOB was calculated to be 6.8. Then, a metric applied to latch type comparators and defined as figure of merit (FOM) is used to compare this research with recent state-of-art publications [7]-[10].

$$FOM = \frac{P_d}{2^{ENOB} F_s} \text{ (J/conversion)} \qquad (2)$$

where, Pd is the power consumption of the circuit and F_s being the maximum clock frequency. Based on (2) the FOM was controlled at 0.035fJ/Conversion. That parameter is very important while designing dynamic latch comparator, since the lower the FOM, the higher the efficiency of the circuit [11, 12].

Table.1: Optimized transistors aspect ratio

Transistors	W/L(μm)	Transistors	W/L(μm)
M12,14	0.065/0.065	M1	6.7/0.065
M13,10,11	2/0.065	M2	2.8/0.065
M6	1/0.1	M3	2.8/0.13
M7	0.1/0.1	M4	0.4 /0.32
M15	0.5/0.13	M5	0.1/0.32
M17,16	0.065/0.1	M8,9	3.2/ 0.065

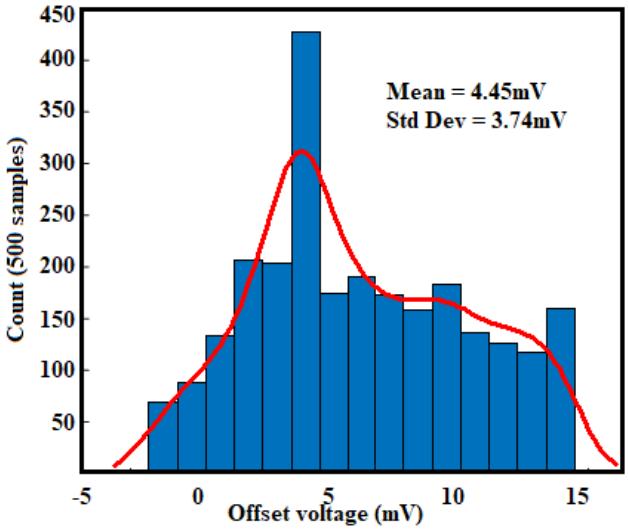

Figure.7. Histogram of the delay extracted from the Mont-Carlo simulation results for 500 runs.

In Table.2, the performance metric of the proposed circuit is highlighted and compared with preceding existing topologies based on simulation. Thanks to the 65 nm CMOS process, we customized a dynamic latch type comparator that achieved 20 GHz sampling rate and consumed only 78 μW of power from 1V supply voltage. Moreover, a less power delay product (PDP) of only 1.114fJ was achieved.

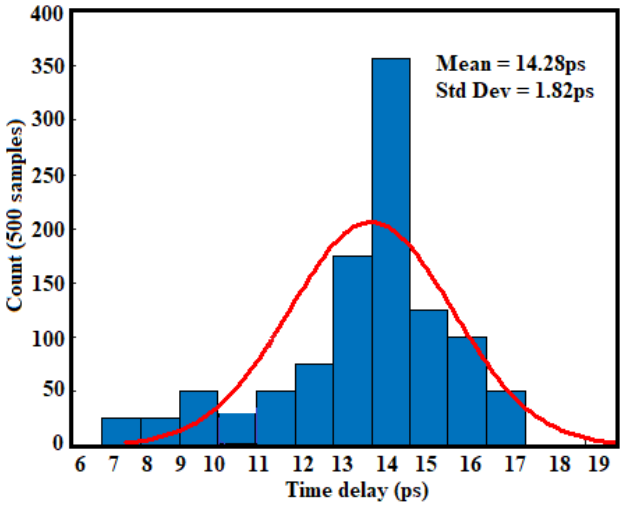

Figure.8. Histogram of the offset extracted from the Mont-Carlo simulation results for 500 runs.

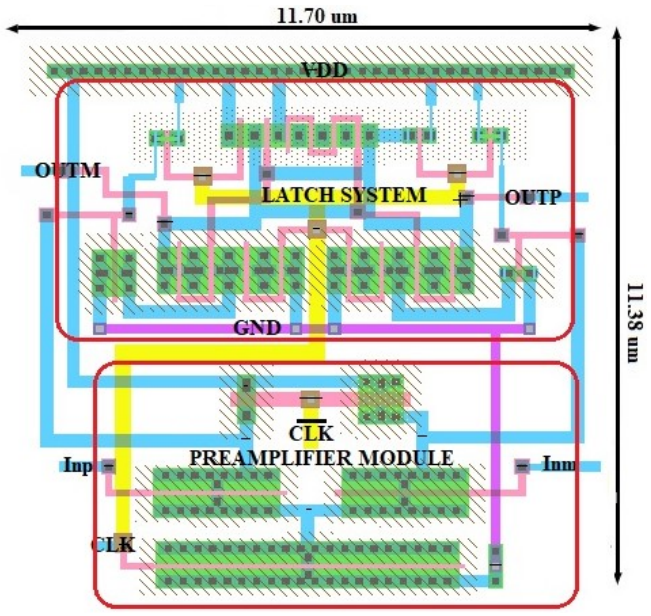

Figure.9. Core circuit layout of our proposed DLC

Table.2: Performance metric of the proposed DLC.

Comparison Properties	[1] 2019	[10] 2019	[4] 2019	[5] 2019	This work
Technology	65nm	180nm	180nm	45nm	65nm
Supply voltage	1.2V	1.8V/ 3.3V	1.8V	0.8V	1V
clock Frequency (GHz)	6	0.625	0.5	14.7	20
Delay (ps)	42.7	N.A	638.91	268	14.28
Power (μW)	381	450	347	5.8	78
Offset (mV)	3.87	0.35	7.78	3.16	4.45
PDP (fJ)	16.3	N.A	221.7	1.55	1.114
FOM (fJ/conversion)	N.A	1.02	N.A	N.A	0.035
Die area (μm^2)	141.7	360	361	26.92	133.15

IV. CONCLUSION

An ultra-high speed dynamic latch comparator has been implemented in this work. The parasitic and mismatch were reduced in the latch stage and the circuit was isolated to ground using auxiliary transistors, which gave a compact architecture to the design. The effective transconductance of cross-coupling inverter of the latch mechanism was improved therefore increased the speed of our circuit. The implementation has been carried out using 65nm CMOS process from TSMC. A maximum clock frequency of 20GHz was achieved and the circuit exhibited an acceptable PDP of 1.114fJ per clock cycle, while a lower input referred-offset of 4.45mV was achieved.

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