

Chair of Circuit Design
Department of Electrical Engineering
School of Computation, Information and Technology
Technical University of Munich
80290 Munich, Germany



Lab CMOS A/D Converter Design

Final Report: SAR Group 1

Daniel Arndt (03739221)

Stefan Hell (03780668)

Alois Höchst (03664726)

Vicente Osorio R. (03800202)

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1 Introduction

The lab project aims at designing a minimum power 10 bit successive approximation register (SAR) analog-to-digital converter (ADC) with a conversion speed of 4 MHz. The device has rail-to-rail input capability, running off a 1.1 V supply. In their role as a translator of physical quantities that are analog in nature to digital numbers that a computer can understand, ADC are an integral part of any technical system interacting with its environment.

There are various topologies available to achieve this, of which delta-sigma, dual slope, and SAR are within the scope of this lab course. Our group is one out of two groups to implement the SAR topology. This report presents the analysis and design of a SAR ADC in order to meet the lab project specifications. The document is organized as follows: Chapter 2 presents the theory of operation of the SAR ADC. Chapter 3 explains the design approach, along with an in-depth view of the design for each sub-circuit. Chapter 4 presents nominal top-level simulations, as well as corner and Monte-Carlo simulations.

2 Theory of operation

2.1 The SAR concept

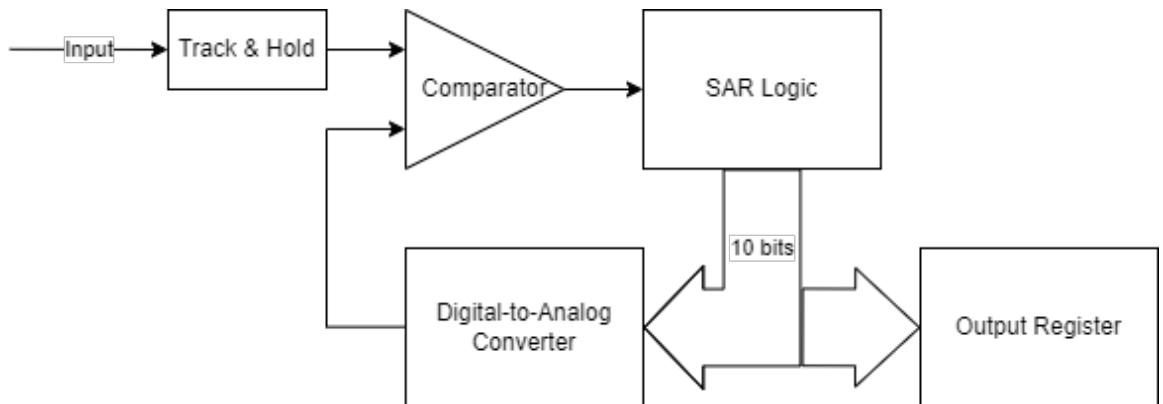


Figure 2.1: Blockdiagram of the complete system

A SAR ADC consists of a sample-and-hold (S&H) circuit, a comparator, a digital-to-analog converter (DAC), and a control logic, along with an output register to store the last valid output code during conversion. Figure 2.1 shows the basic block diagram of the converter.

In each clock cycle, the output voltage of the DAC is compared to the sampled value. In the next clock cycle, the register controlling DAC output is modified depending on the comparison result. In case of the DAC voltage being lower than the sampled input voltage the DAC output is increased, otherwise decreased. The voltage step is halved every cycle, essentially applying binary search to find the right combination of bits. This is illustrated in figure 2.2 at the example of only 4 bit.

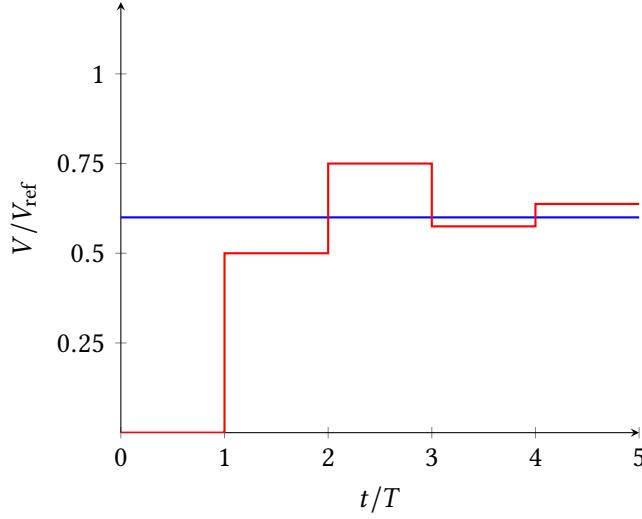


Figure 2.2: Binary search for 4 bit

For a given sampling frequency f_s , the clock frequency f_{clk} is given by

$$f_{\text{clk}} = (N + 2)f_s \quad (2.1)$$

with N being the number of bits. Besides the N cycles required for setting each bit, our design uses an additional clock cycle for the decision about the last bit and another one is needed for reset and sampling.

2.1.1 Logic circuit

The control logic, depicted in figure 2.3, comprises twelve d-flip-flops serving as a shift register and another ten as an approximation register to hold the output word. At the time the ADC gets reset by an external signal, SR_0 is set to one, and all the other flip-flops are set to zero. A single bit is clocked through the shift register, setting one bit after another in the approximation register. The Q value of the current bit is used as a clock for the previous flip-flop. If the comparator value is one, the previous bit remains set. Otherwise, the zero at the comparator output is adopted by the previous bit on the rising edge of the current flip-flop's output, making the voltage go down one step. This circuit architecture is adopted from [1].

After one conversion cycle this process starts again via the feedback from SR_{N+1} to SR_0 . The Q output of the flip-flop SR_0 is used as a clock for the S&H circuit and the \bar{Q} output is used for resetting the approximation register and DAC, and to load the data into the output register. For readability those signals are omitted in figure 2.1 and figure 2.3.

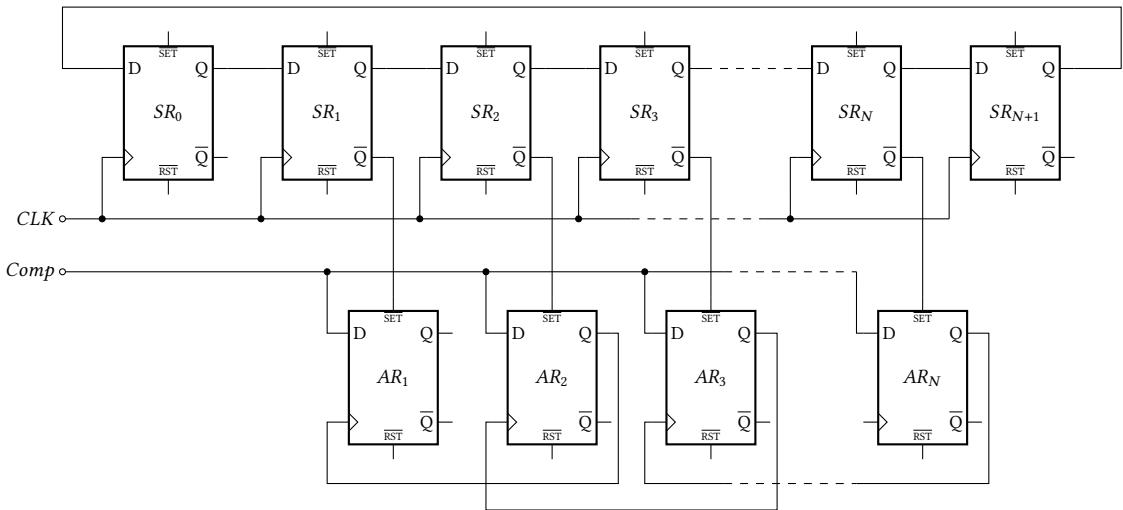


Figure 2.3: SAR logic circuit

2.2 DAC concept

2.2.1 DAC function

The DAC is a converter who receives a digital input signal, usually in form of a bit sequence, which then translates the digital signal to an analog output signal corresponding to the digital input. Figure 2.4 illustrates the input to output conversion.

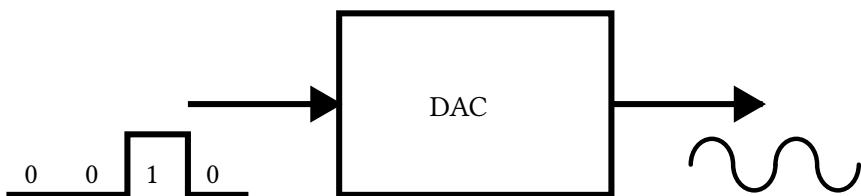


Figure 2.4: DAC function

2.2.2 The ideal DAC

An ideal DAC does not have infinite input impedance therefore no influence on any incoming signal. Also an ideal DAC has zero output impedance so it can drive any other input connected to its output. The input to output conversion speed is unlimited, therefore changes on the input lead to an immediate change at the output. The output has zero offset, resulting in zero volt at the output at a zero input signal. Another characteristic of an ideal DAC are the unlimited common mode rejection and power supply rejection, this leads to no changes on the output if the input or the power supply are affected by common mode changes or power supply changes. The ideal DAC has a perfect rail to rail output. With this the output will reach the power supply voltage on the output without any offset. The output of the ideal DAC also does not have any non linear effect, the output has equal length steps and all steps are strictly monotonous. The Gain is set so the maximum input value

results in the maximum output value. The output of the ideal DAC also has no quantization error with an unlimited amount of steps and therefore a perfect analog output signal. While switching the ideal DAC also does not produce any glitches, therefore the output is not impacted by the internal switching of the DAC.

2.2.3 The DAC with ideal components

Two implementations of an DAC are the one realized with an resistor ladder displayed in figure 2.5 and a switched capacitor on in figure 2.6. Those two layouts can be realized with ideal components, yet still some of the characteristics of the ideal DAC are lost with the layout consisting of ideal components.

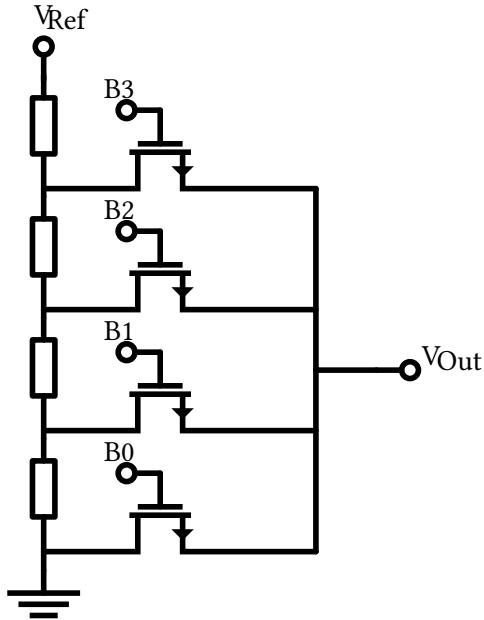


Figure 2.5: Resistor ladder DAC

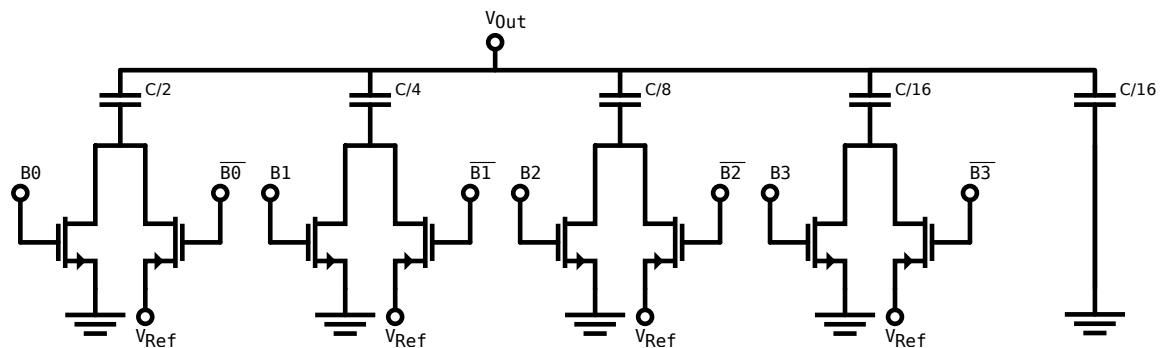


Figure 2.6: Switched capacitor DAC

Both design have only a limited number of quantization steps, therefore the a quantization error

will be added to the output of the DAC. The number of quantization steps is determined by the number of resistors in the ladder or by the number of capacitors in the switched capacitor DAC.

The output impedance of the two designs is limited by the different layouts. For the resistor ladder the output current is limited by the chosen resistor value, the lower the value the higher the output current. The resistor ladder will also have a higher quiescent current, the lower the resistor values are. The output current of the switched capacitor DAC is limited by the size of the capacitors. But bigger capacitors also result in higher losses due to the switching nature of the DAC and the alternating connection between VRef and ground. Figure 2.7 shows the results of the switch capacitor DAC with ideal components. In the Figure 2.7 the single steps that add up to the desired output voltage can be seen.

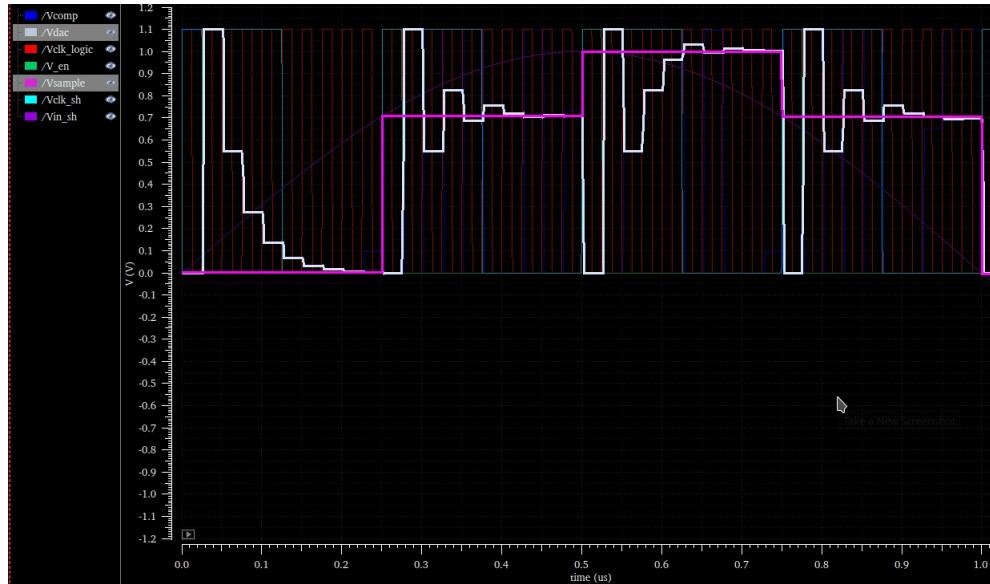


Figure 2.7: Ideal components DAC output

2.2.4 The DAC with real components

For the real implementation the switch capacitor design promises better energy efficiency therefore the resistor ladder is no longer considered. In the real implementation the losses of the switch capacitor DAC are directly linked to the capacitor size chosen. Equation 2.2 demonstrates the relation between capacitance and energy stored in the capacitor. This energy is lost if the capacitor is switched from a high state to a low one.

$$E_{el} = \frac{1}{2}CU^2 \quad (2.2)$$

Where:

- E_{el} : Electrical energy (J)
- C : Capacitance (F)
- U : Voltage (V)

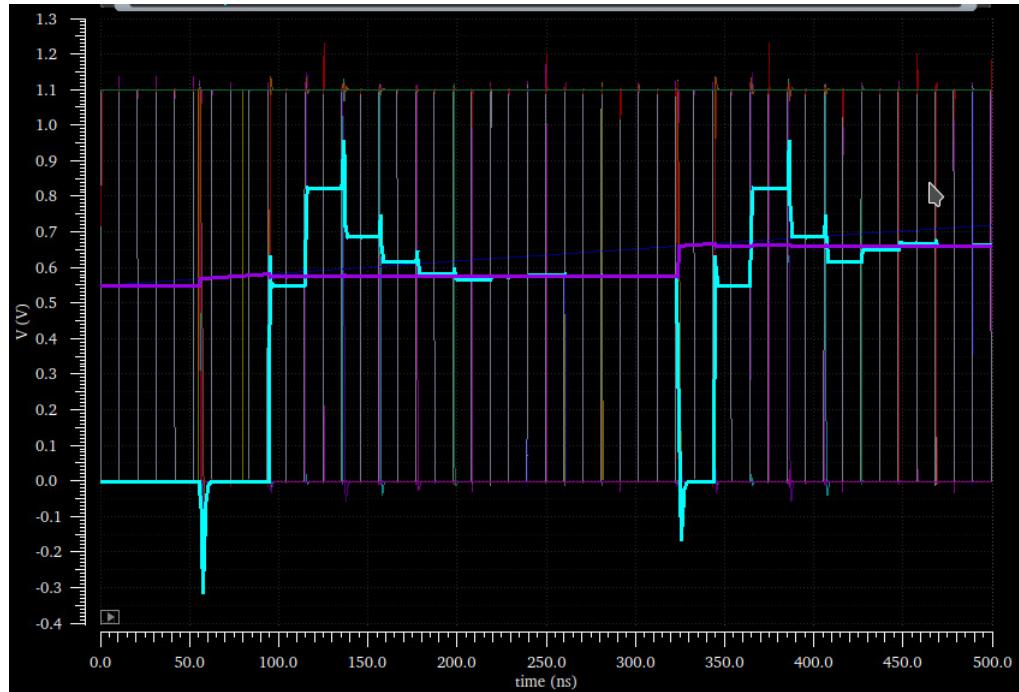


Figure 2.8: Real components DAC output

Figure 2.8 shows the output of the DAC with real components. Compared to figure 2.7 the glitches caused by the switching can be seen at the beginning and at the end of the plateaus.

Equation 2.3 describes the influence of the load capacitance on the output voltage of the DAC. The equation demonstrates that the output voltage will be lowered inverse proportional to increasing load capacitance, therefore the load capacitance should be kept low in order to reduce the offset of the DAC.

$$V_{\text{out}} = V_{\text{DAC}} \cdot \frac{C_{\text{DAC}}}{C_{\text{DAC}} + C_L} \quad (2.3)$$

Where:

- V_{out} : Output voltage (V)
- V_{DAC} : DAC supply voltage (V)
- C_{DAC} : DAC capacitance (F)
- C_L : load capacitance (F)

The input impedance of the DAC is determined by the parasitic capacitance of the transistors so in order to reduce their influence gate length should be kept low, although input impedance is a minor issue in the design process. The linearity of the DAC will be directly influenced by the process variation of the capacitor sizes, if the size differ from their target values, then the output of the DAC will lose linearity by having a variation in the steep size of the associated value.

$$V(t) = V_0 \left(1 - e^{-\frac{t}{RC}}\right) \quad (2.4)$$

Where:

- $V(t)$: Capacitor voltage (V)
- V_0 : Applied voltage (V)
- R : Resistance (Ω)
- C : Capacitance (F)

Equation 2.4 describes the influence of the on resistance of the transistor on the charge time of the capacitor. Higher on resistance of the transistor will result in longer charge times, therefore the size of the transistor should be scaled with the size of the capacitance that will be charged. Figure 2.9 shows this behavior in the red graph. The DAC output shows that for the big capacitance values this behavior is more significant.

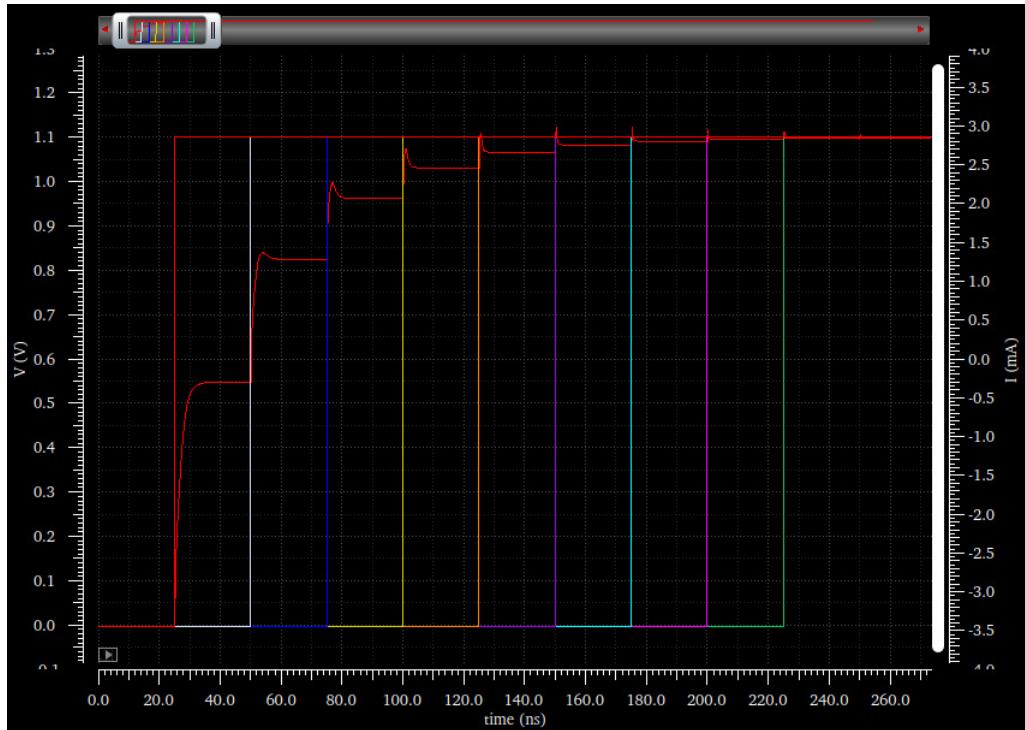


Figure 2.9: Charge slope of the real DAC

Changes on the supply voltage of the DAC will result in a sever change of the output voltage according to equation 2.3. This can only be reduced with a filter on the supply voltage.

Finally the DAC with real components will require an extra switch in order to discharge the output. The real capacitors will have leakage that causes a charge flowing towards the output, which will cause an offset on reset of the capacitance's, resulting in a higher value than zero on

reset. In order to get rid of these charges a extra switch will be installed, that connects the output to ground on reset, resulting in a zero level on the output on reset.

2.3 The S&H concept

2.3.1 The ideal S&H

A S&H is an analog circuit that samples an input voltage and holds its value at the output at a constant level during a defined amount of time. Typically, samples are taken at equally-spanned time intervals, therefore, a sampling frequency can be determined.

The operation of this circuit can be divided into sample mode and hold mode. Both modes do not need to be equal in duration, but their sum must yield the total sampling time. In hold mode, the output value is equal to the last sampled value. In sample mode, the circuit can track the input signal or it can be reset to a fixed value. In the first case, the circuit is commonly named a track-and-hold (T&H) circuit. This variation of a S&H circuit allows continuous tracking in sample mode of the input signal instead of sampling at discrete moments.

An ideal S&H is able to sample a value instantaneously and hold it without any induced error. Figure 2.10 depicts an output signal for an ideal S&H.

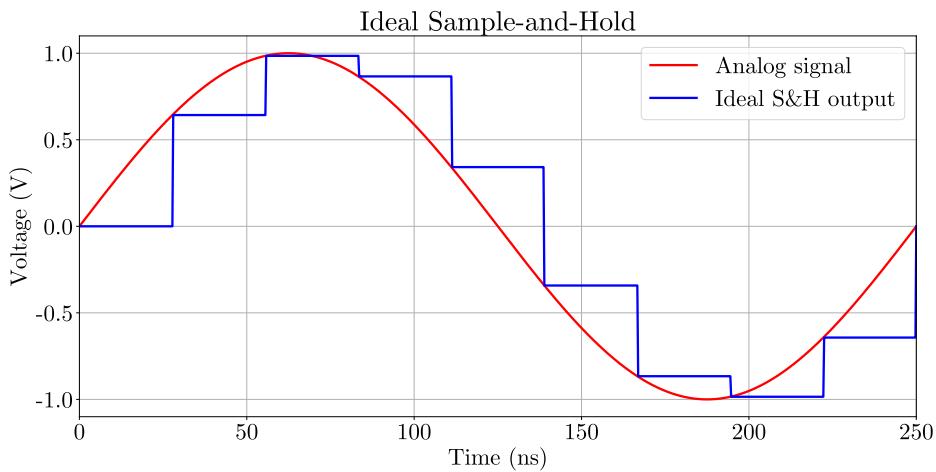


Figure 2.10: Ideal S&H output signal

The implementation of this circuit consists of an ideal switch triggered by a control signal ϕ_S connected to an ideal sampling capacitor C_S , which stores the samples. Figure 2.11 illustrates the ideal circuit for a S&H.

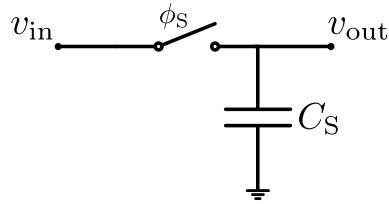


Figure 2.11: Ideal S&H circuit

2.3.2 The real S&H

Nonetheless, for a real implementation, due to the necessity of having enough time to be able to sample a value by charging a capacitor, a tracking phase is needed. This way, the circuit would track the signal and then hold the value. Furthermore, the held value might have an error due to leakage currents in the sampling capacitor and charge injection due to incorrect sizing of the devices involved. Figure 2.12 shows an output signal for a real implementation.

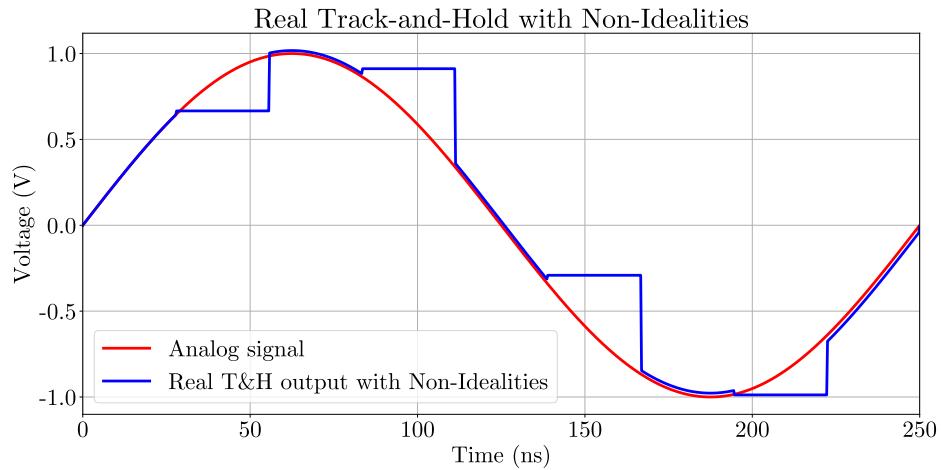


Figure 2.12: Real T&H output signal

The most basic implementation of this circuit replaces the switch with a transistor. Other solutions search to improve the linearity and increase the input range of the switch, thus using more complex solutions like a Bootstrapped Switch. This circuit will be designed and analyzed in section 3.3.

3 Design approach

The starting point of the design procedure is to get an estimate of the circuit dimensions from the ideal models. These results are then refined using simulations of the actual devices from the gpdk045 complementary metal-oxide-semiconductor (CMOS) technology library.

3.1 Performance specifications

The required performance of the final circuit is specified in terms of input voltage range, conversion speed, supply voltage V_{dd} , ground voltage V_{ss} and number of bits N , as given in table 3.1. Power consumption should be as low as possible. The minimum channel length defined in the task description is 150 nm, and the minimum width is 320 nm.

Table 3.1: Specification of performance parameters

parameter	value
ΔV_{in}	1.1 V
f_s	4 MHz
V_{dd}	1.1 V
V_{ss}	0 V
N	10 bit

3.2 Shift Register and Logic

3.2.1 D-type flip-flop with asynchronous preset and clear

The flip-flop needed for the logic circuit introduced in the previous section has to be an edge-triggered d-type with asynchronous preset and clear inputs. We decided to implement this with the circuit shown in 3.2 consisting of transmission gates and NAND gates. The logic gates are implemented as shown in figure 3.3 using minimal-sized transistors.

3.2.2 Real binary search waveform

Figure 3.1 shows the simulation of the real SAR implementation.

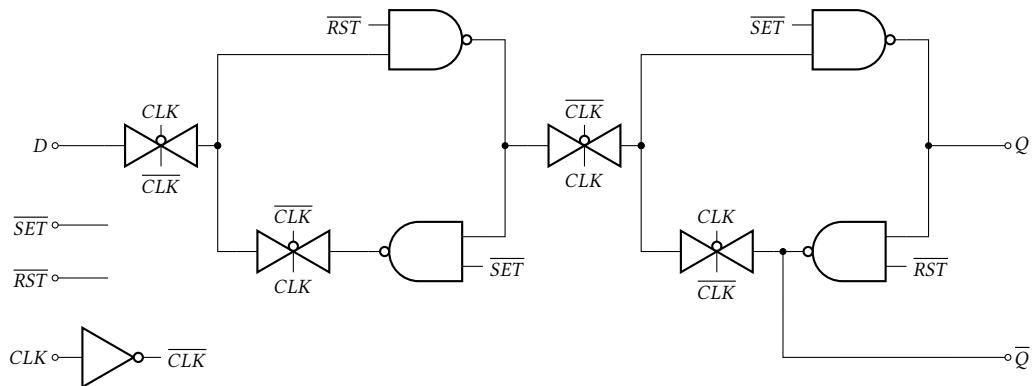


Figure 3.2: Edge-triggered D-type flip-flop implementation

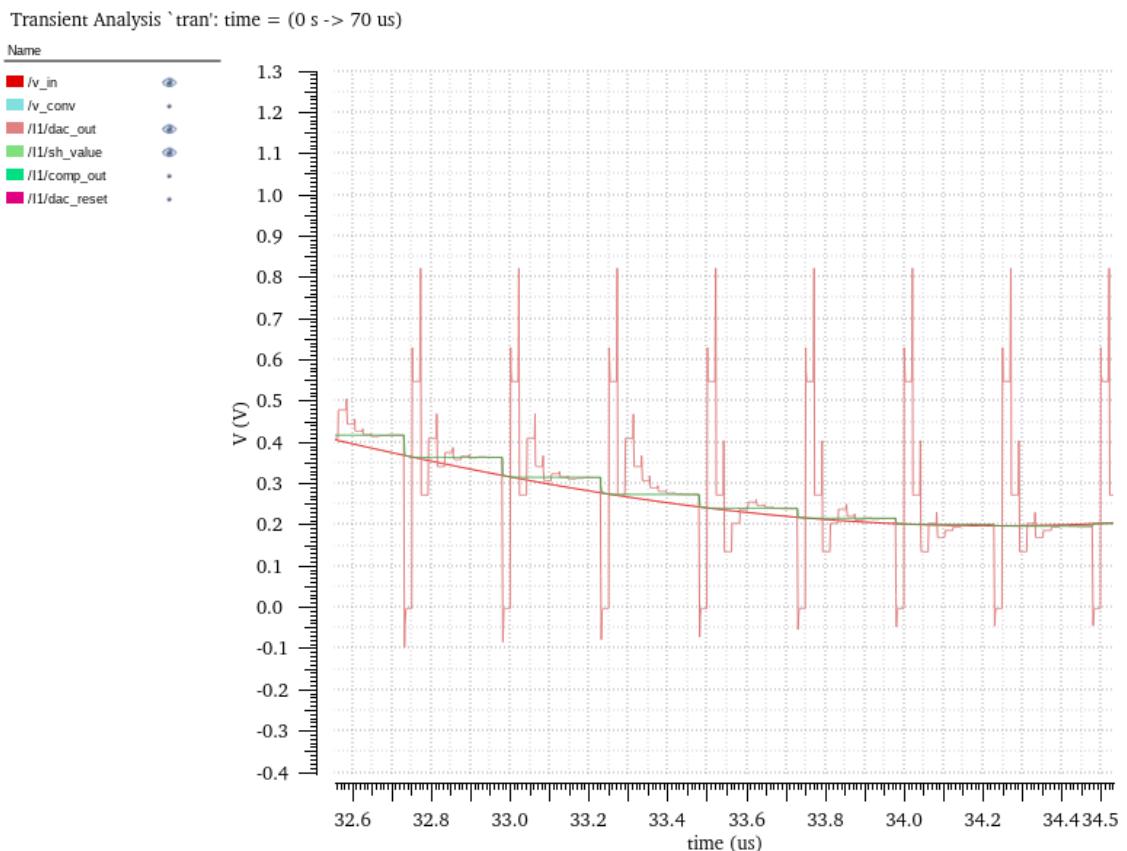


Figure 3.1: Some conversion cycles of the real waveform

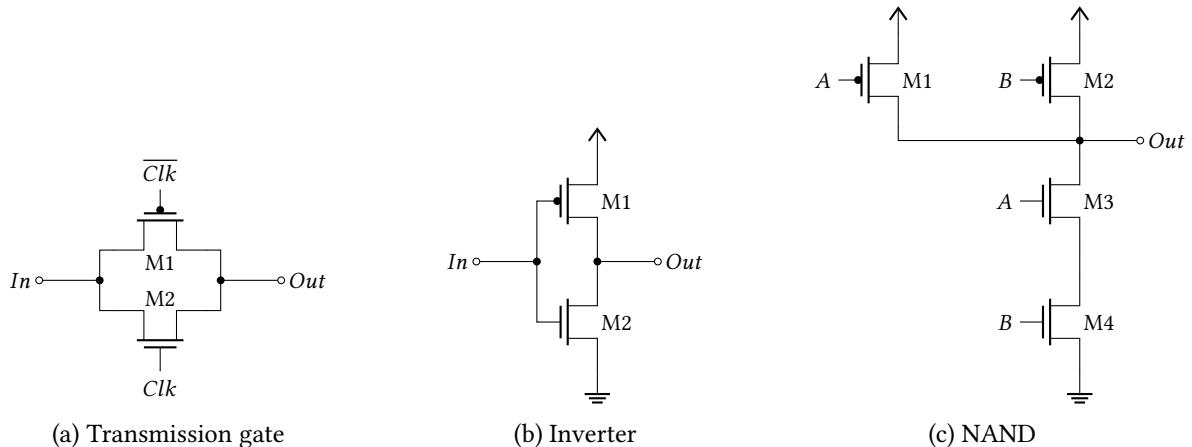


Figure 3.3: Transistor level schematic of logic gates

3.3 S&H design

For the real implementation of the S&H, due to its benefits for linearity and input range, the bootstrapped switch was selected as the switch. For the sampling capacitor and the battery capacitor, a Metal-Insulator-Metal (MIM) capacitor was used as it allowed large units of capacitance.

3.3.1 Design of a Bootstrapped Switch

The bootstrapped switch implemented is extracted from [2] and the design methodology shown in it is used as a reference for this work. The schematic for this circuit is depicted in 3.4.

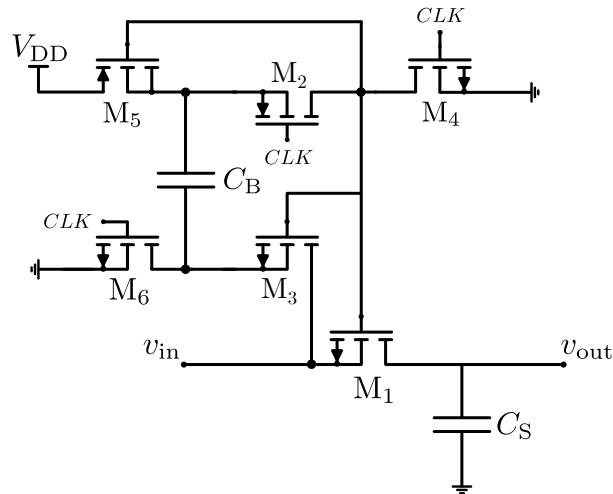


Figure 3.4: Bootstrapped Switch circuit

For an ideal N bit ADC with an input of the form $A\cos(\omega t)$, the ideal signal-to-noise ratio (SNR)

is given by

$$SNR_{\text{ideal}} = \frac{\frac{A^2}{2}}{\frac{\Delta^2}{12}} \quad (3.1)$$

where Δ is the least significant bit (LSB) value and is equal to $2A/2^N$. For $N = 10$, it follows that $SNR = 62$ dB. Therefore, the harmonic distortion (HD) must remain well below -62 dB. The ambition is to achieve an HD of roughly -65 dB in the worst case scenario, namely, when the input amplitude reaches upper and lower rail ($A = 0.55$ V) and when the input frequency f_{in} is near 2 MHz, *i.e.*, at the Nyquist rate. Another requirement is that the noise introduced by the sampler must negligibly degrade the overall SNR. Thus, the kT/C noise associated with M_1 and C_1 must be sufficiently small. The SNR of the sampler-ADC cascade can be expressed as

$$SNR = \frac{\frac{A^2}{2}}{\frac{\Delta^2}{12} + \frac{2kT}{C}} \quad (3.2)$$

For targeting a 1 dB penalty due to kT/C noise, the SNR in (3.2) is divided by the ideal SNR equation in (3.1), 10log of the result is taken and equated to -1 dB. With $\Delta \approx 1.074$ mV and $T = 348$ K, $C_1 \approx 0.4$ pF, giving, thus, a minimum value for C_1 . Furthermore, the low-pass filter formed by M_1 and C_1 must negligibly attenuate the input signal in the track mode. The output amplitude is equal to $A/\sqrt{1 + R_{\text{on1}}^2 C_1^2 \omega_{\text{in}}^2}$, where R_{on1} denotes the on-resistance of M_1 . Aiming for an attenuation less than 0.5 dB at the Nyquist rate yields for $R_{\text{on1}} \approx 139$ k Ω , which gives a good headroom for designing the switch. To achieve this value, the width W_1 of M_1 must be large enough to ensure it as a maximum resistance. This constraint yields when $W_1 \approx 1$ μm for the minimum channel length.

As a first approach, the circuit was implemented with an ideal battery and ideal switches to connect and disconnect M_1 , illustrated in 3.5. This was to verify that the constraints were being met by M_1 . The values of the third harmonic HD_3 and the fifth harmonic HD_5 were below the -65 dB constraint.

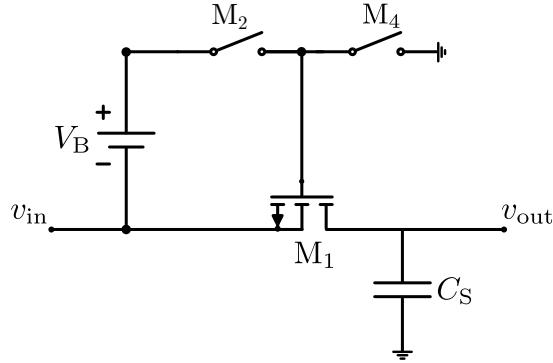


Figure 3.5: Basic sampler with ideal switches

Afterwards, the circuit was modified to the one shown in 3.6, now implementing real switches for M_2 and M_4 . The width for these switches were selected as $W_2 = 2$ μm and $W_4 = 1$ μm , respectively. In this case, M_1 had to be resized to $W_1 = 18$ μm to match the requirements.

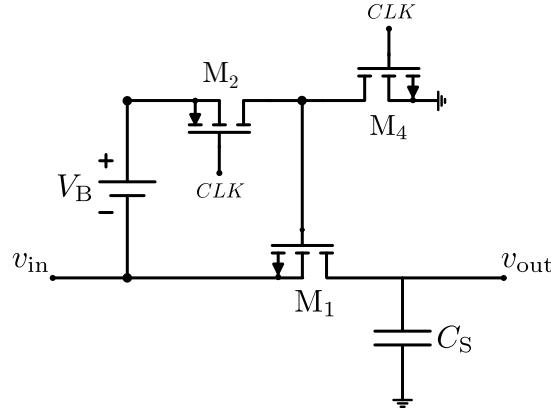


Figure 3.6: Basic sampler with transistor switches

As M_2 fails to turn off for part of the input swing, M_1 does not completely turn off. Therefore, the bootstrapping must be removed completely in hold mode. For this purpose, M_3 and M_6 were added to the circuit. This variation of the circuit is shown in Figure 3.7. The width for these switches were selected as $W_3 = W_6 = 1 \mu\text{m}$, respectively. No modifications were made to the other devices as the constraint is met for both HD_3 and HD_5 .

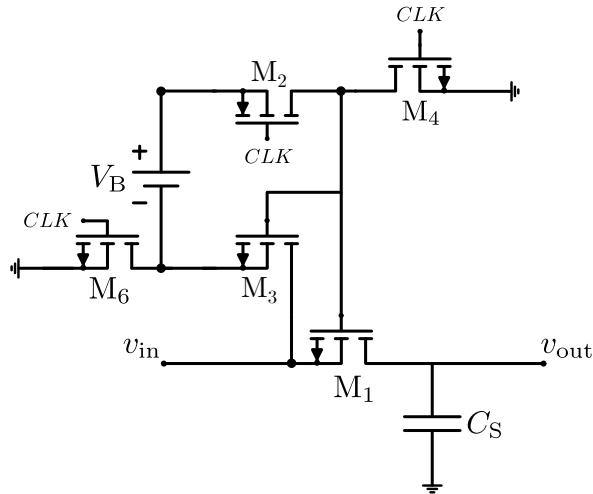


Figure 3.7: Sampler with switches for disconnecting the battery in hold mode

Finally, the battery was replaced by the capacitor C_B and the switch M_5 is added to charge and discharge it, obtaining the circuit previously illustrated in 3.4. The capacitor must be large enough to minimize the voltage loss and the switch, along with M_6 have to be wide enough to achieve a good charge replenishment of this capacitor. These constraints are met by setting $C_B \approx 0.8 \text{ pF}$ and M_5 width $W_5 = 16 \mu\text{m}$ and by enlarging W_6 to $8 \mu\text{m}$.

The final values for HD_3 and HD_5 and the parameter values can be found in tables 3.2 and 3.3, respectively. It is worth noting that every device in the circuit uses the minimum length allowed by the technology.

Table 3.2: Parameters of the Bootstrapped Switch circuit

Parameter	Value
W_1	18 μm
W_2	2 μm
W_3	1 μm
W_4	1 μm
W_5	16 μm
W_6	8 μm
C_B	0.4 pF
C_S	7.5 pF

Table 3.3: Values of harmonic distortion components of the bootstrapped switch circuit for different input frequencies

Harmonic	$f_{in} \approx 514 \text{ kHz}$	$f_{in} \approx 1.78 \text{ MHz}$
HD_3	-72.74 dB	-55.78 dB
HD_5	-69.47 dB	-62.00 dB

When analyzing the output waveform, the held value had an error of approximately 10 mV. This was explained mainly due to charge injection. Due to the complexity of the circuit, a dummy switch was not an option. Thus, the sampling capacitor was set to $C_S \approx 7.5 \text{ pF}$, which allowed to reduce the error to nearly 1 mV. Nonetheless, this error is still not totally acceptable as the desirable figure of merit is $0.5\Delta \approx 0.5037 \text{ mV}$ to ensure a good effective number of bits (ENOB). But this was considered a trade-off towards power consumption, as further enlarging of the sampling capacitor for diminishing the error will increase the losses.

3.4 Comparator

3.4.1 Introduction

The comparator is an important component of the SAR ADC. It must detect very small analog input voltage differences and convert them into a digital output. The basic function of the comparator in this SAR ADC is to compare the output of the S&H with the output of the DAC. Based on this comparison it generates a digital output signal. Key characteristics are minimal offset voltage, to ensure detection of the least significant bit (LSB), a fast response for high conversion rate and high input impedance to avoid charge or discharge of the capacitor network of the DAC. This voltage must remain stable to ensure accurate measurements. Imperfections in a comparator's response can lead to errors, such as noise, distortion or reduced resolution in the final digital output.

3.4.2 Design

The comparator is designed so that it can detect the input voltage difference of the LSB, which is roughly 1 mV, across an input voltage range from 0 to 1.1 V. This means the comparator must be capable of detecting the full input supply range.

3.4.3 Overview

Fig. 3.8 shows a schematic of the full comparator circuit. This comparator design consists of four stages. The first stage is a level shifter. The level shifter converts the input voltage range (0 to 1.1 V) into a for the comparator functional operating voltage. A side effect of the level shifter is that the delta output voltage is less than the delta input voltage, especially close to 0 V and 1.1 V. A pre-amplifier is used to amplify the signal and reduce offset due to transistor mismatch and minimize kickback noise. The StrongARM latch compares the two input values and latches to one side, depending on which input has a higher voltage. High voltage variation in the internal nodes lead to high transient currents which can influences the inputs. This effect is called kickback noise [3]. An SR-latch is used in the final stage to hold the latched value for the duration of the clock period. The comparator is falling edge clocked to provide enough settling time for S&H and DAC.

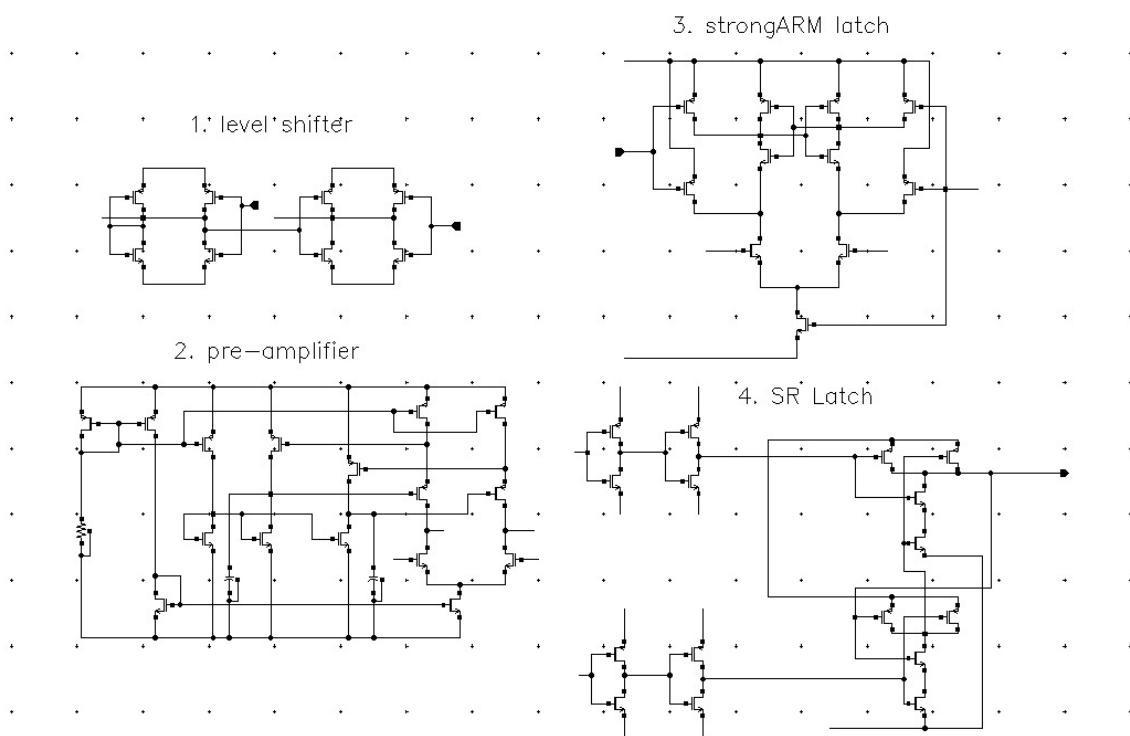


Figure 3.8: Complete comparator circuit

3.4.4 Level shifter

The circuit shown in fig. 3.9 illustrates the level shifter of the comparator. For the input signal, the transistors PM22 and NM20 adjust the bias current of the circuit. For the lower rail, PM23 is in saturation, so more current flows through NM20, resulting in a voltage rise at the output `vin_amp_n`. At higher voltages, the output decreases, and current flows through NM17 and PM22. On `sigref`, the gates of transistors PM24 and NM18 are connected to `sigin` instead of short circuiting the inverter to provide additional gain.

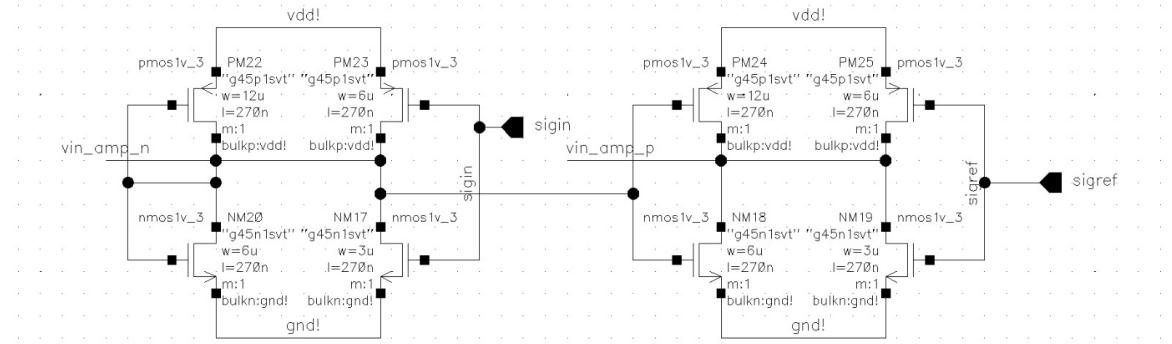


Figure 3.9: Circuit of level shifter

3.4.5 Pre-amplifier

Fig. 3.10 illustrates the pre-amplifier, which is based on an enhanced version of a commonly used differential amplifier. To improve precision and gain, the drain-source voltage of transistors PM1 and PM2 must be maintained at a constant value, independent of the input voltage. This is achieved by transistors PM0 and PM5, which sense the drain voltages of PM1 and PM2. Transistors PM3 and PM4 then regulate the drain-source voltage of PM1 and PM2, ensuring it is set to the desired fixed bias current. The dependence of the drain current from the PMOS on drain source voltage can be seen in the following equation:

$$I_{D,\text{sat}} = \frac{\mu_p \cdot C_{\text{ox}}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 (1 - \lambda V_{DS}) \quad (3.3)$$

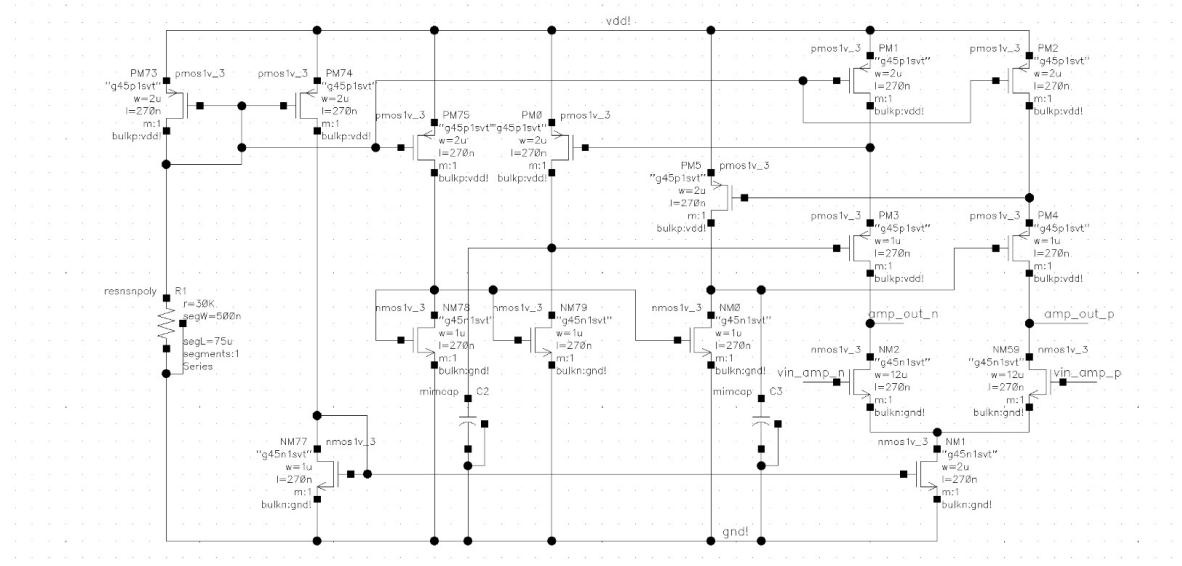


Figure 3.10: Amplifier circuit

3.4.6 Simulation of level shifter and pre-amplifier

A DC simulation was performed to the level shifter and amplifier over the full input voltage range. The input was varied from 0 to 1.1 V with an offset of 1 mV to verify that the amplification of the least significant bit (LSB) is sufficient. Fig. 3.11 shows that the input ramp is shifted and inverted by the level shifter, as shown in the middle part of the figure. It also shows that the slope has been reduced overall, with a significant reduction at the lower rail. This effect results in a reduced output delta voltage at the lower rail, as indicated by the blue signal. Additionally, it shows that extra gain was achieved between the lower and upper rails, as described in the design choices made earlier. The pre-amplifier now amplifies the signal from the level shifter, as shown by the green line. It can be observed that the input at the lower rail was significantly increased, while the input at the upper rail was even decreased. This is primarily an optimization issue. The design was optimized mostly for lower rail performance.

$(VS("/vin_amp_n") - VS("/vin_amp_p")):(VS("/vin_p") - VS("/vin_n")):(VS("/amp_out_p") - VS("/amp_out_n"))$

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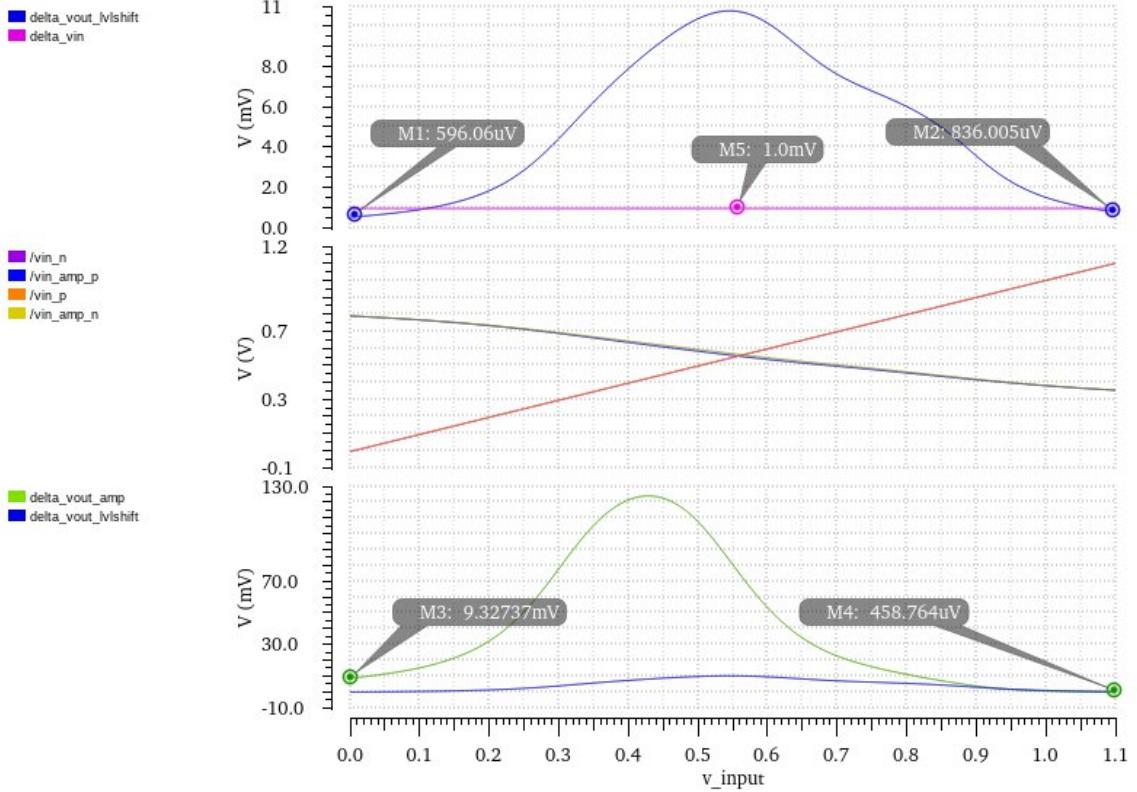


Figure 3.11: Transient simulation result of level shifter and amplifier

3.4.7 StrongARM Latch and SR Latch

The StrongARM Latch is the main component of the comparator. This circuit consists of two clocked, cross-coupled inverters that drive the circuit into a latched state. The clocked, cross-coupled differential pair serves as the input. When the clock is low, the circuit is in an off-state, drawing zero power. After the rising clock edge, the circuit turns on and the cross-coupled inverters are no longer in a fixed state. This leads to a metastable state, which will eventually resolve into a stable state when the inputs are unequal. Even very small differences can flip the inverters into a stable state. After the rising edge and the end of the metastable state, the circuit enters the on-state, with no power consumption. This means the circuit only has dynamic power consumption and zero static power consumption. The low power consumption, digital output, and low offset were the main reasons for choosing this circuit. The SR latch is needed to achieve a steady output state over the clock period and consists of two NAND gates.

3.4.8 Simulation of StrongARM latch and SR latch

The simulation setup is a transient simulation with a fixed reference voltage at the negative input and a constantly rising voltage at the positive input. Fig. 3.12 shows the immediate switching of

the output after the positive node crosses the negative node. An offset of $4.15 \mu\text{V}$ can be observed, as shown in fig. 3.12, when the output q of the SR latch rises. This offset is due to the switching phase of the StrongARM latch and the delay of the SR latch.

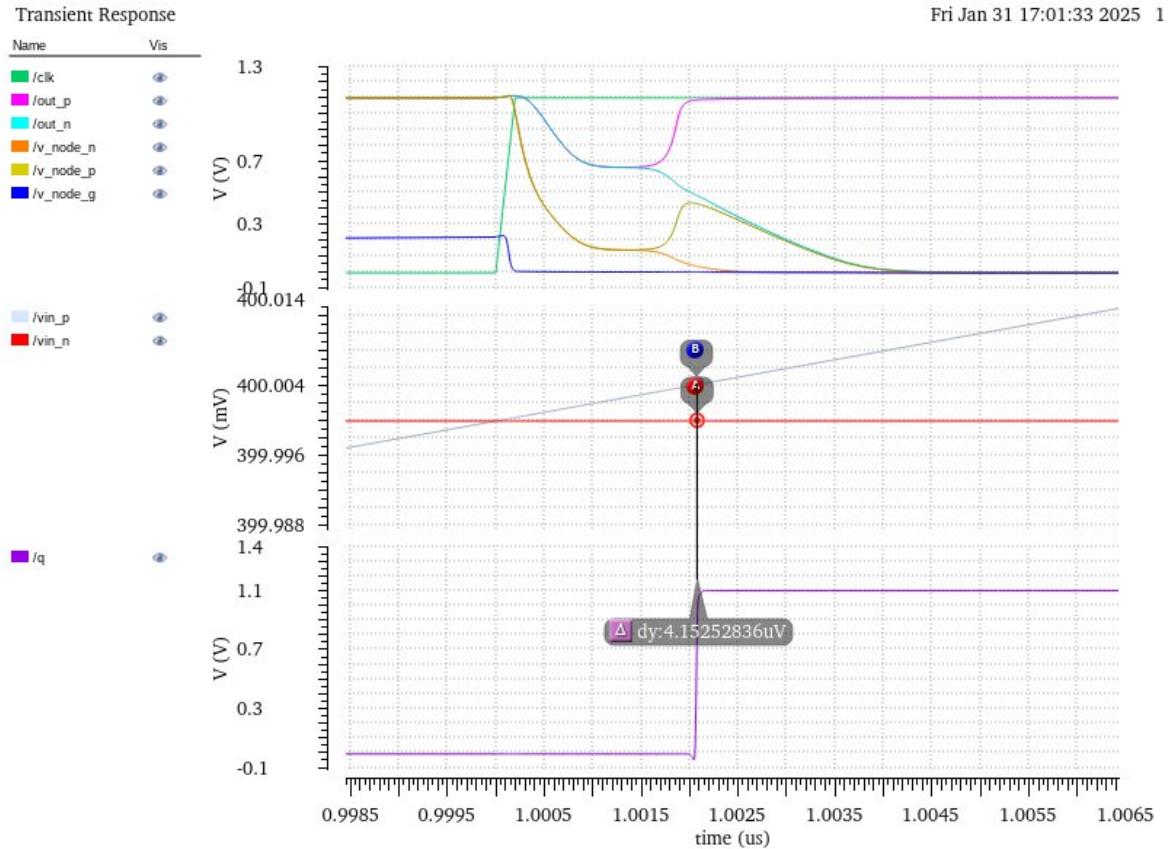


Figure 3.12: Simulation result of strongARM latch and SR latch

3.4.9 Simulation of the comparator

The comparator was tested through transient simulations with different input ranges. The reference voltage was set to 2 mV for the lower rail, 550 mV for the optimal case, and 1.098 V for the upper rail. In fig. 3.13, it clearly shows that across these ranges, the comparator performs well enough to detect the LSB. The worst performance is observed at the upper rail due to the focus on optimizing lower rail performance.

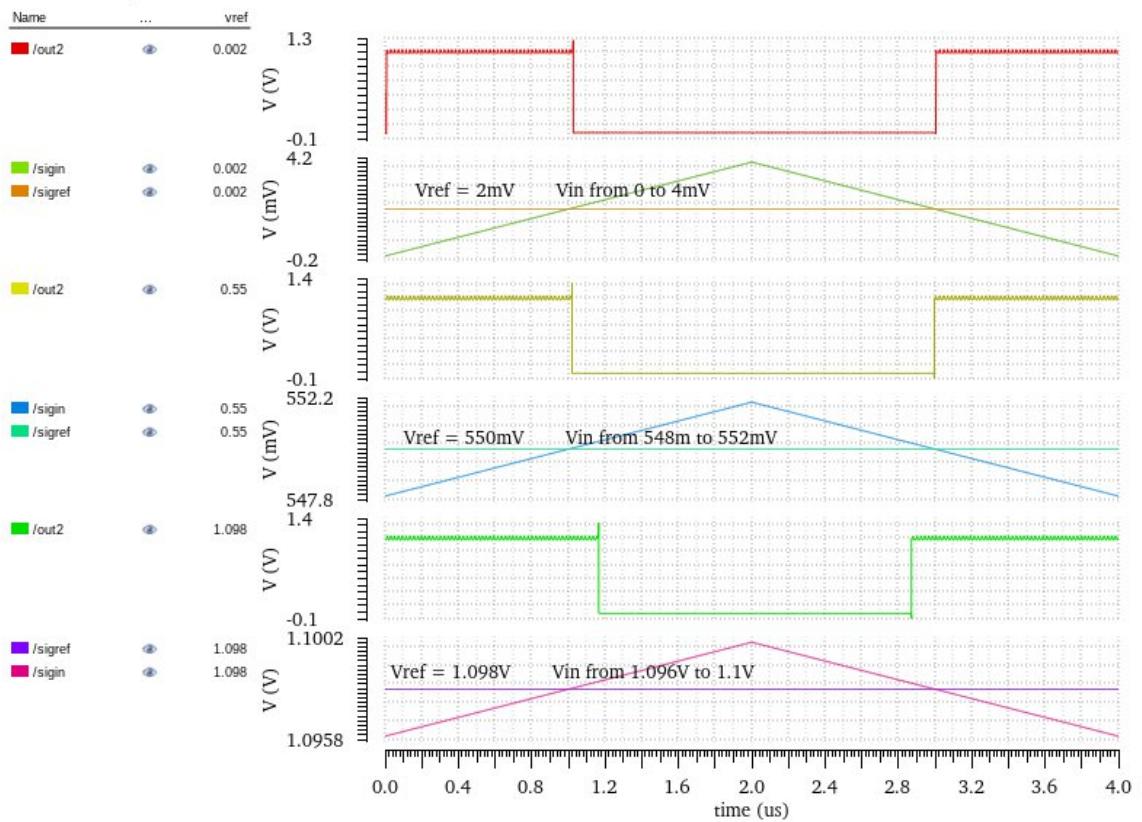


Figure 3.13: Comparator simulation with lower rail, nominal and upper rail

3.4.10 Comparator in real SAR ADC circuit

The comparator was simulated along with the entire SAR ADC using real components. The switching of the LSB was observed in fig. 3.14 to verify if the comparator operates as expected. As shown in 3.14 , the comparator switches when the DAC output is below the S&H.

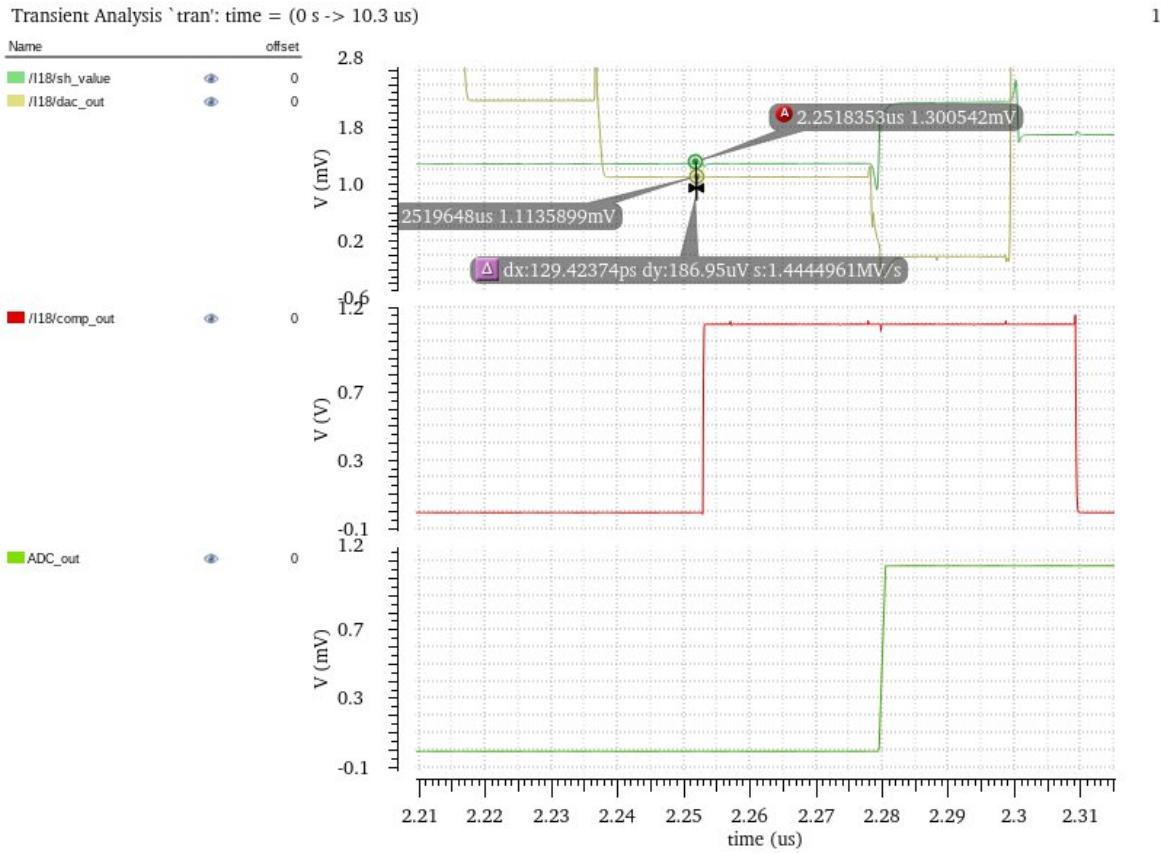


Figure 3.14: Comparator switching at the LSB

3.4.11 Final comparator thoughts

The circuit was optimized and designed for full-range performance, with focus on low-range operation. While the design and its simulation look promising, the overall power consumption is too high to be viable for a low-power design. The pre-amplifier was set to a very high bias current to ensure the comparator operates correctly. Further investigation is needed to optimize the circuit and evaluate the necessity of a high bias current in the pre-amplifier. The level shifter may even provide enough gain between the inputs to drive the circuit without the amplifier, or the specification requirements could be relaxed such that the circuit no longer needs full-range capability. This would allow for the removal of the level shifter and a reduction in bias current, which would significantly reduce power consumption. Monte Carlo simulations also showed poor performance when mismatches occur. One possible reason for this could be the design of the level shifter. If there is a mismatch between the inputs, the circuit performs much worse. This issue also requires further investigation to improve yield.

3.5 DAC design

Figure 3.15 shows a scaled version of the final design of the DAC. On the left is the switch necessary for the reset of the output of the DAC. This switch connects the output to ground with the signal from the B_{Res} bit. The design of the switches connected to the capacitors can be seen in figure 3.16. The switches consist of two transmission gates in order to reduce the on resistance and increase current towards the capacitors. In order to switch the transmission gates an extra signal inverter for each input bit is necessary, because the transmission gate requires both a signal with positive logic and one with negative logic, because of the combination of an N-type metal–oxide–semiconductor (NMOS) and P-type metal–oxide–semiconductor (PMOS).

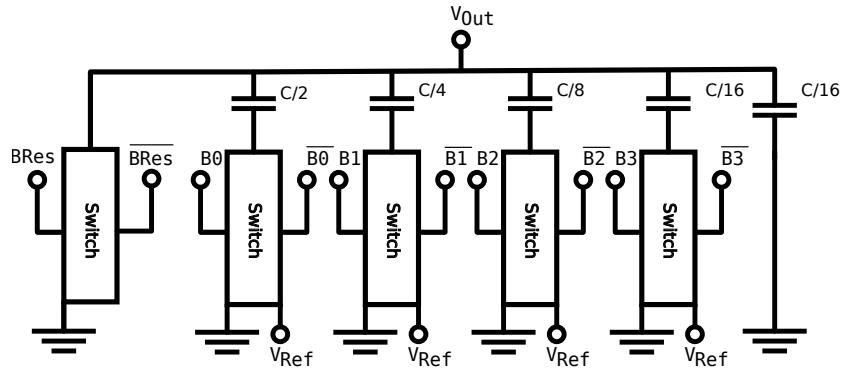


Figure 3.15: DAC design

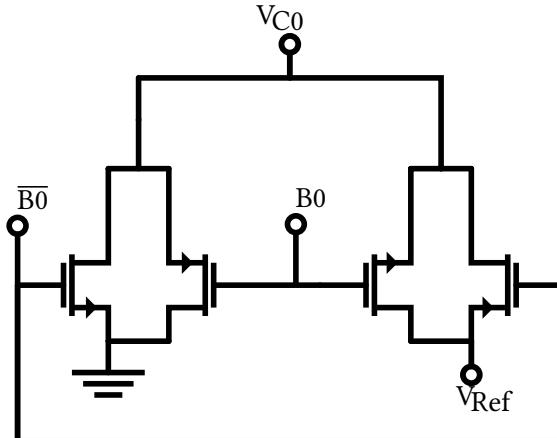


Figure 3.16: DAC switch design

The size of the smallest capacitance is $56fF$ and is then scaled by a factor of two for each one of the ten increasing capacitors. The resulting complete capacitance of the DAC is $57.344pF$. Each one of the switches is also scaled by a factor of two for each increasing capacitance value, with the smallest possible size one the smallest capacitor.

4 Results

4.1 Full range simulation

Fig. 4.1 shows the full-range capability and whether the SAR ADC follows the input voltage accordingly. Glitches can be observed, especially in the lower ranges. This is due to the use of a liberal simulation, which is faster to simulate but sacrifices accuracy especially in analog circuits where high precision is needed. A better understanding of full-range performance will be provided in the next chapter.

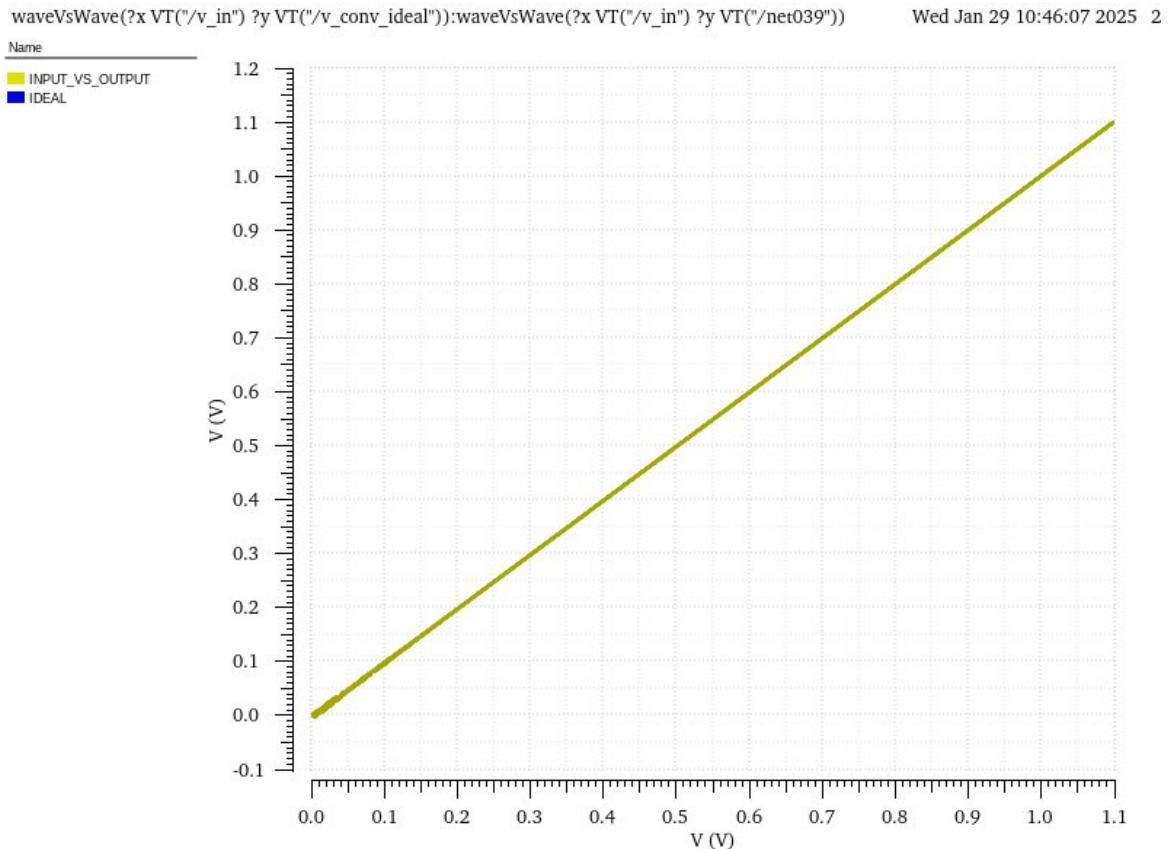


Figure 4.1: Fullrange simulation

4.2 Offset, gain error, INL and DNL

To accurately simulate gain, offset, INL, and DNL, a conservative simulation setup was used. To reduce simulation time, only the first few bits were captured. To gain a general understanding of INL and DNL, the simulation was set up with three ranges: lower rail, upper rail and nominal. The simulation results can be seen in fig. 4.2. What can be immediately observed is that the ADC exhibits both offset and gain errors. The offset error was measured in fig. 4.3 and calculated using the following equation:

$$E_{\text{offset}} = \frac{V_{0\dots1}}{V_{\text{LSB}}} - \frac{1}{2} \quad (4.1)$$

The evaluation of this equation and the measurement show that the ADC has an offset error of 1.5 LSB. The gain error is -2 LSB and was calculated with the following equation:

$$E_{\text{gain}} = \left(\frac{V_{1\dots1}}{V_{\text{LSB}}} - \frac{V_{0\dots1}}{V_{\text{LSB}}} \right) - (2^N - 2) \quad (4.2)$$

The INL and DNL calculations were performed only in the nominal region, as this is the only region where these errors are larger than the simulated sampling error, as seen in fig. 4.2. Both the upper and lower rails indicate that more accurate measurements are needed to simulate these errors. The sample size used, $\frac{V_{\text{LSB}}}{4}$, is too large to measure any errors in those regions because the INL and DNL are lower than this value. The results of INL and DNL in the nominal region can be seen in fig. 4.4.

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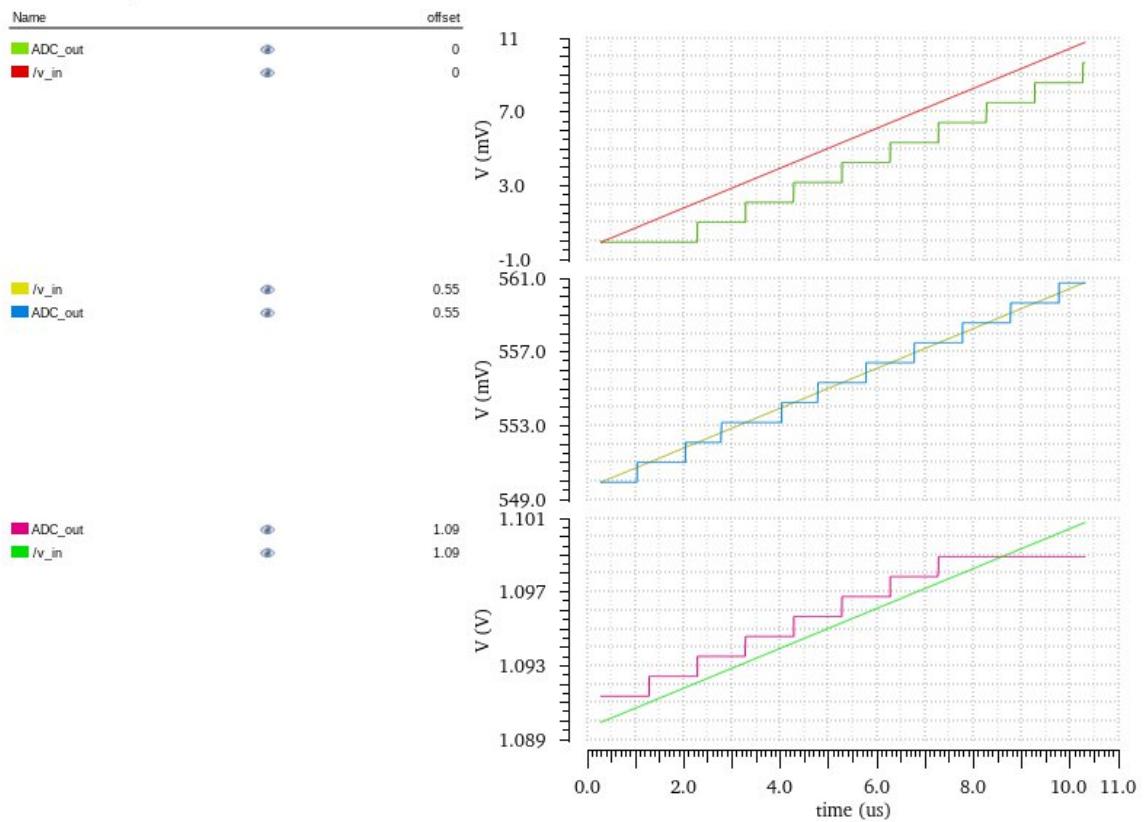


Figure 4.2: Simulation of INL, DNL with upper rail, nominal and lower rail

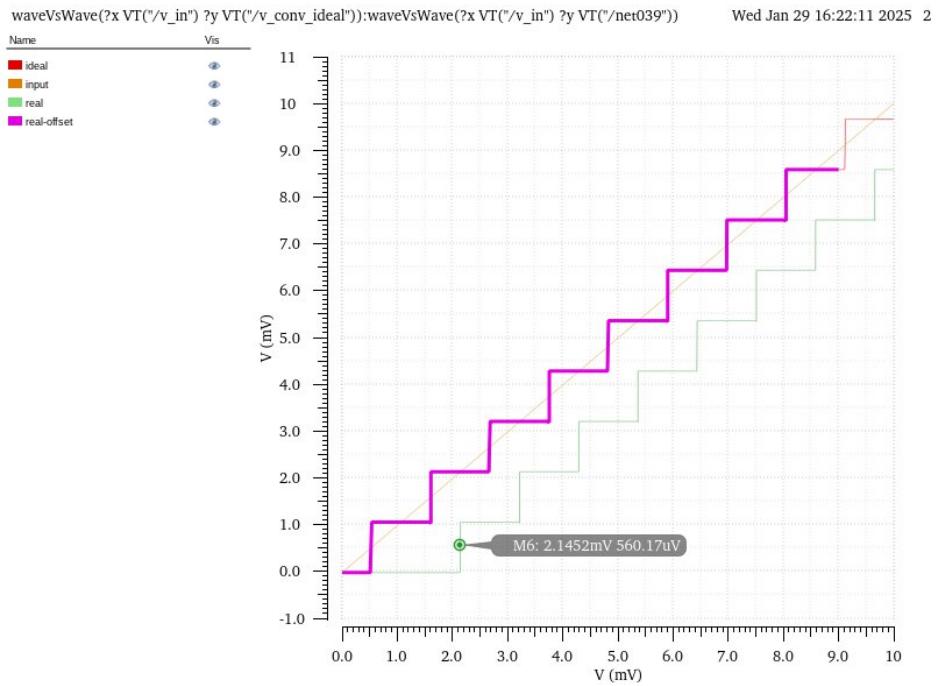


Figure 4.3: Offset simulation

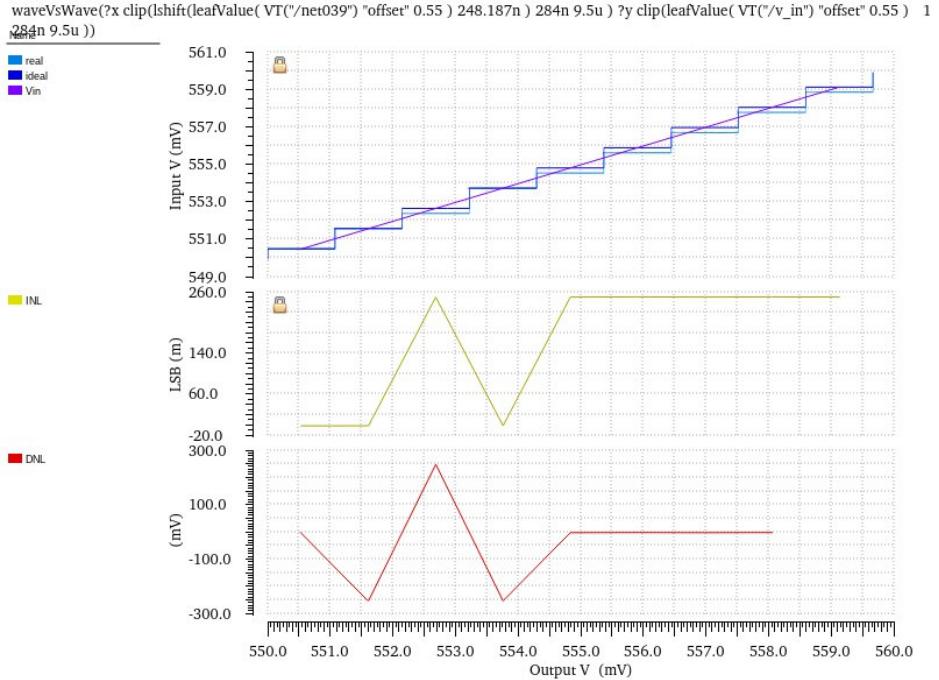


Figure 4.4: INL and DNL simulation

4.3 ENOB and SNR values at different frequencies and amplitudes

In an ideal ADC the only noise present is the noise that is introduced by mapping a continuous input range to a discrete number of digital values this is called signal-to-quantization-noise ratio (SQNR). The SQNR can be calculated as

$$SQNR = (6.02N + 1.76)\text{dB} = 61.96 \text{ dB} \quad (4.3)$$

for the number of bits used in our implementation ($N = 10$).

A common figure used to compare ADC is the ENOB it is the number of bits a ADC with a given SNR would have if all of the noise was due to quantization.

$$ENOB = \frac{SNR_{\text{dB}} - 1.76}{6.02} \quad (4.4)$$

The results presented in table 4.1 show SNR and ENOB values for full-range input ($V_{\text{pp}} = 1.1 \text{ V}$) and approximately 60 % of full-range amplitude at different frequencies across the Nyquist range of the system. It can be observed that at full-range input the ENOB is reduced compared to the lower input voltage. For both input amplitudes SNR gets worse at frequencies closer to the Nyquist frequency.

Table 4.1: Simulation results for SNR and ENOB at different frequencies and amplitudes.

frequency	$V_{\text{pp}} = 0.7 \text{ V}$		$V_{\text{pp}} = 1.1 \text{ V}$	
	ENOB	SNR	ENOB	SNR
109.55 kHz	9.33	57.92 dB	8.07	50.37 dB
672.95 kHz	9.32	57.87 dB	8.12	50.66 dB
1298.95 kHz	9.33	57.91 dB	7.74	48.36 dB
1768.45 kHz	8.90	55.37 dB	6.64	41.77 dB

4.3.1 Monte-Carlo Simulation

Figure 4.6 shows the combined distribution of ENOB values for the same frequencies as in table 4.1. The accumulation of values around 3.5 is due to clipping of the waveform observed in some Monte-Carlo samples illustrated in figure 4.5. This is due to wrong values at the comparator output that seem to be at least partially caused by numeric limitations when simulating in the "liberal" simulation mode.

Transient Response

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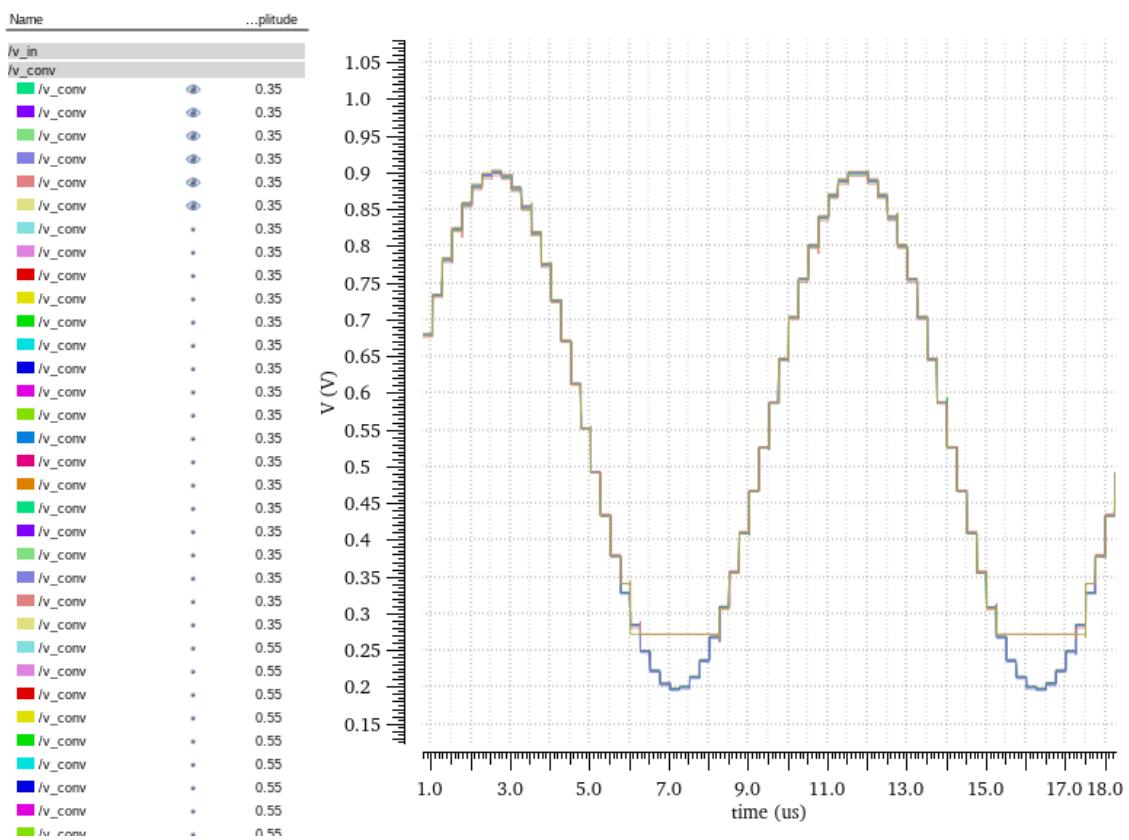


Figure 4.5: Clipping of the waveform at some Monte-Carlo samples

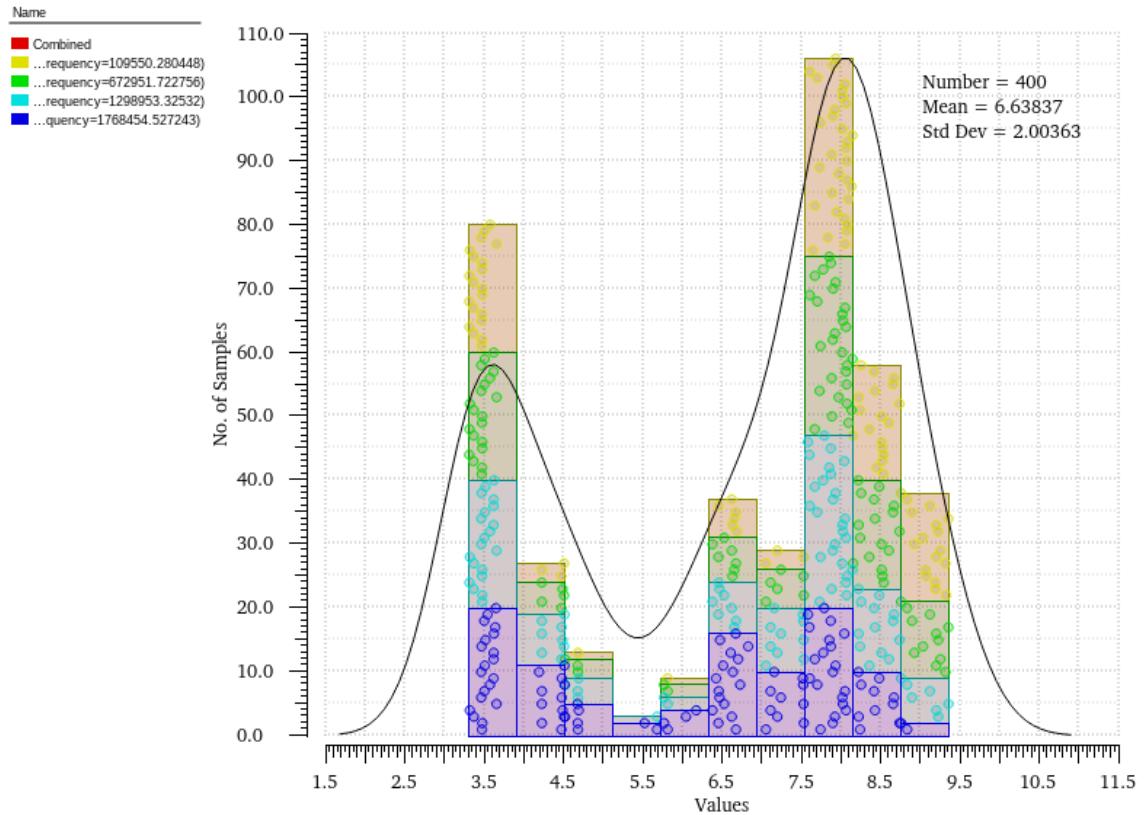


Figure 4.6: Combined ENOB distribution for different frequencies

4.4 ENOB and SNR values at different temperatures and source voltages

Corner simulations for different temperatures and source voltages were made to determine the SNR and ENOB values for a full-range input ($V_{pp} = 1.1$ V) and for approximately 60 % of full-range amplitude. It is worth noting that all corners were simulated for an input sine wave of frequency $f_{in} = 672.95$ kHz. The corner simulations are described in 4.2 and the simulation results can be found in 4.3.

Table 4.2: Corner simulations for different temperatures and source voltages V_{DD}

Corner	Temperature	V_{DD}
Corner 1	27 °C	1.1 V
Corner 2	-40 °C	1.1 V
Corner 3	125 °C	1.1 V
Corner 4	27 °C	0.99 V
Corner 5	27 °C	1.21 V

Table 4.3: Simulation results for SNR and ENOB at different temperatures and source voltages.

Corner Simulation	$V_{pp} = 0.7 \text{ V}$		$V_{pp} = 1.1 \text{ V}$	
	ENOB	SNR	ENOB	SNR
Corner 1	9.32	57.87 dB	8.12	50.66 dB
Corner 2	9.30	57.77 dB	8.19	51.07 dB
Corner 3	9.26	57.51 dB	7.39	46.23 dB
Corner 4	9.22	57.30 dB	3.51	22.87 dB
Corner 5	8.41	52.41 dB	7.19	45.08 dB

It can be observed that at full-range input the ENOB is reduced compared to the lower input voltage, as it was already seen in section 4.3. For both input amplitudes SNR gets notoriously affected at high temperatures. In the full-range case it is worth noting that the SNR decreases drastically when the source voltage decreases. This might have to do with the operation point of the circuit being affected, therefore, not allowing the circuit to operate as intended and thus not being able to drive the signal conversion on its entirety.

4.5 Power consumption

In order to receive values for the power consumption a transient simulation with a 1Mhz rail to rail input signal was run. The power consumption for each component can be seen in figures 4.7, 4.8, 4.9 and 4.10. In figures 4.8 and 4.9 a strong clock dependent power consumption according to their working principle can be seen. Figure 4.7 only shows a large power spike on the initial setup of the ADC but later almost no power consumption. Only at the comparator in figure 4.10 a more consistent current flow can be witnessed leading to the bigger power consumption shown in table 4.4. Both the comparator and the DAC would be targets for optimization in order to reduce the total power consumption.

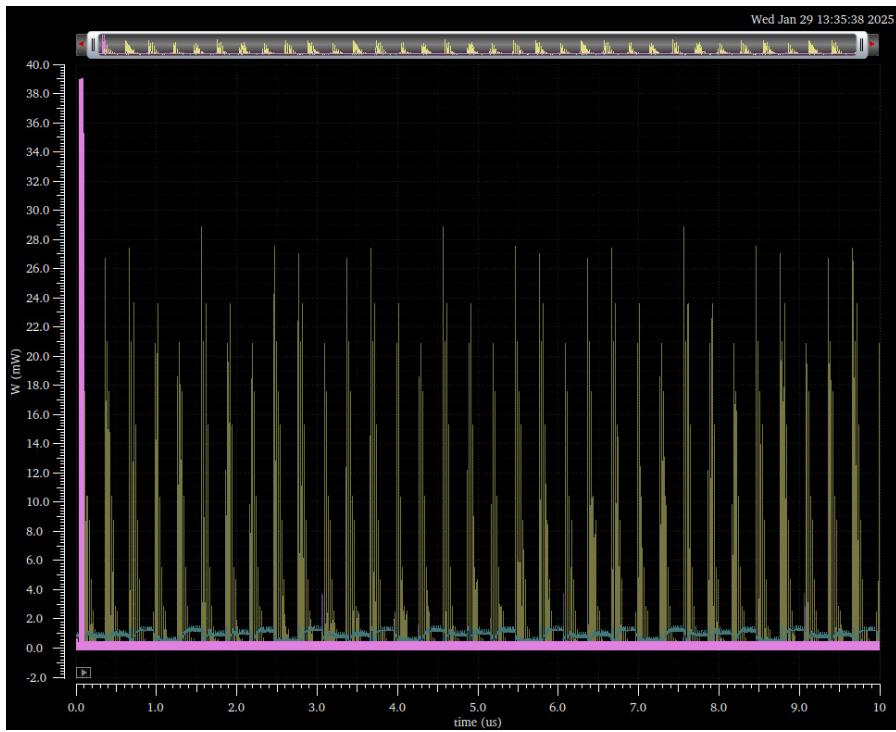


Figure 4.7: Power consumption of the logic

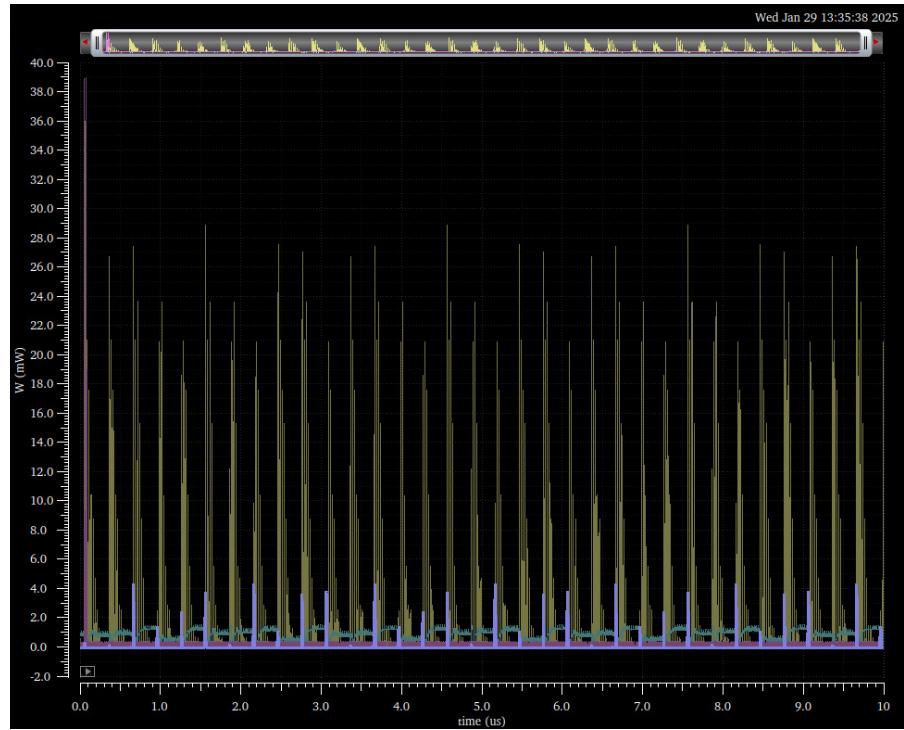


Figure 4.8: Power consumption of the S&H

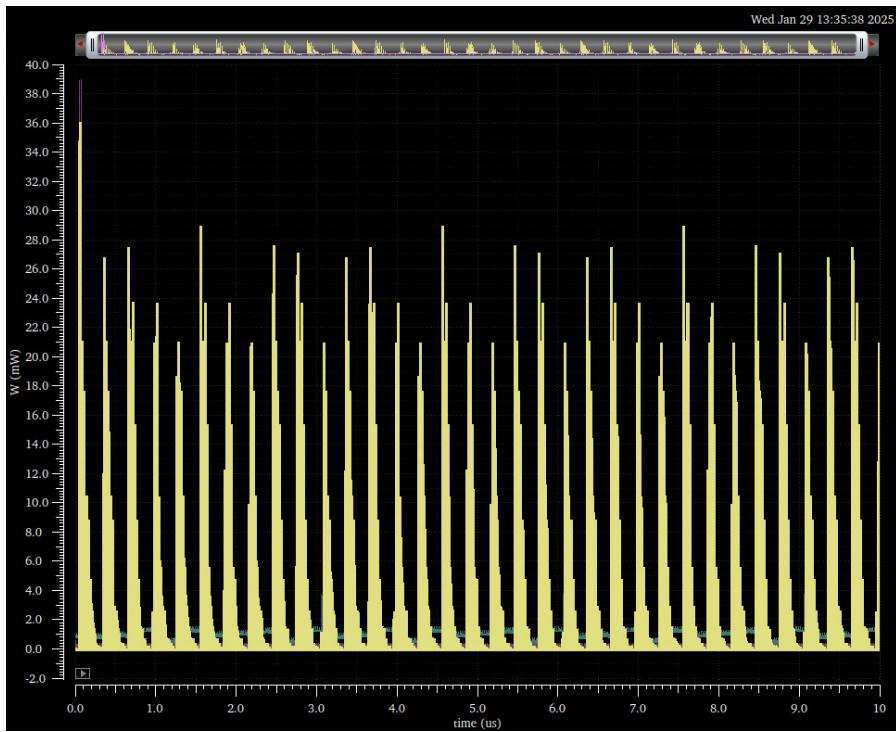


Figure 4.9: Power consumption of the DAC

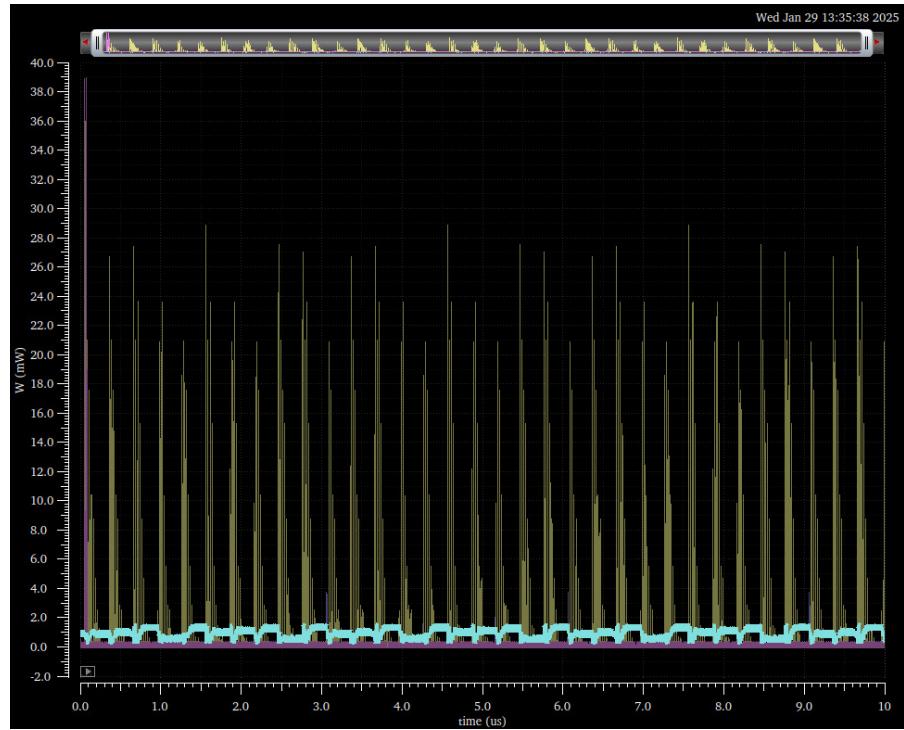


Figure 4.10: Power consumption of the comparator

Table 4.4: Power consumption results.

Logic	5.048E-6
S&H	8.798E-6
DAC	216.3E-6
Comparator	883.1E-6

References

- [1] T. O. Anderson, “Optimum Control Logic for Successive Approximation Analog-to-Digital Converters,” *Deep Space Network Progress Report*, vol. 13, pp. 168–176, Nov. 1972.
- [2] B. Razavi, “The Design of a Bootstrapped Sampling Circuit [The Analog Mind],” *IEEE Solid-State Circuits Magazine*, vol. 13, no. 1, pp. 7–12, 2021.
- [3] B. Razavi, “The StrongARM Latch [A Circuit for All Seasons],” *IEEE Solid-State Circuits Magazine*, vol. 7, no. 2, pp. 12–17, 2015.