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ORIGINAL RESEARCH PAPER

A low-offset low-power and high-speed dynamic latch comparator with a preamplifier-enhanced stage

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Abstract

The preamplifier module is a crucial element while designing dynamic latch comparators. The traditional double tail comparator utilizes a differential pair as the preamplifier stage. The circuit is generally suffered from high power dissipation and low comparison speed. This research reports the design and implementation of a low-offset, low-power and high-speed dynamic latch comparator. In this work, an enhanced differential pair amplifier is employed in the preamplifier stage, to improve the power dissipation and the comparison speed of the device. A custom latch structure with rigorous transistor sizing was implemented to avoid short circuit current and mismatch in the module. The effective trans-conductance of the cross-coupled transistors of the latch was therefore improved for an optimal time delay solution. The equation associated with the delay was derived and the parameters that embody the speed were identified. The design has been validated by corner analysis and post-layout simulation results in 65 nm CMOS technology process, which reveals that the proposed circuit can operate at a higher clock frequency of 20 GHz with a low-offset of 4.45 mV and 14.28 ps propagation delay, while dissipating only 67.8 μW power consumption from 1 V supply and exhibited lowest PDP of 0.968 fJ. Moreover, the core circuit layout occupies only 183.3 μm^2.

1 | INTRODUCTION

The advent of CMOS technology with the miniaturization of MOS transistors sizes allows increasing the capabilities of mixed-mode signal circuits for storing and processing a very big amount of data. Thereby increasing the speed of data processing systems. Generally the signals to be processed are analogue and must therefore be converted into a digital format. Requiring therefore, the utilization of analogue-to-digital converters (ADCs). Due to the increased usage of mixed-signal circuits in a variety of systems such as video systems, wireless communications, Ethernet and health-care systems, the demand for high-speed and low-power ADCs are increasing. Specification of mixed-mode signal circuits heavily relies upon the use of technology [1–4]. With the improvement of CMOS technologies, the supply voltage and the input voltage full-scale range decrease while the threshold voltage off the MOSFET is not scaled down at the same rate as technology. Moreover, mismatch and process variations increase dwindling feature size when devices are also scaled down [1,3,4]. However, device size combined with supply voltage reduction is an important aspect while designing high performance and accurate ADCs. One of the crucial mixed-mode parts circuits of the ADC and most sigma-delta modulators greatly affected by the technology process is the comparator. The development of high-speed and power-efficient sigma-delta ADC has speeded

up the demand of high speed and low-power comparators [1,2,5].

Comparator is the crucial element while designing high-speed data transmission circuits as ADC, since it controls the performance and the accuracy of the device. To empower the performances of such a device, the comparator needs to be power-efficient and exhibited low-noise, high resolution and high-speed. Therefore, high-performance comparators are necessary to amplifier a big output voltage. Consequently, a faster and accurate comparator involves high gain and high bandwidth [5–7]. Thus, for high speed and low-power applications, latch comparators are used instead of static comparators. Because they provide positive feedback, and therefore, charging of output node is faster as compared to the static comparator [8].

The static power dissipation of the Latch-type voltage sense amplifier is inconvenient with scaled-down of transistor sizing [9]. However, due to the several stacked transistors, a high voltage headroom is required for proper operation, which is not appropriate with scaled CMOS technology. The speed and offset of this structure is highly sensitive to input common-mode voltage [10], which is not appropriate for application with input common-mode variation. So, for high-performance design, the positive feedback stage of the latch should be moved away from the inputs.

Recent studies are drawn to design double tail comparator, since it has less stacking transistors, which make it suitable for low voltage, low-power and high-speed applications [9,11]. The amplification and latch stage are separated each other, which enables it to employ low tail current in the former and high current in the latter leading to low offset and high-speed respectively [9,12]. But, increasing the speed and reducing power dissipation, the offset and kickback noise are increased. These are a major concern while designing dynamic latched comparator (DLC). However, a low offset requires, larger transistors; this occupied more area by enlarging the parasitic capacitances, slowing the regeneration process and increasing the power dissipation [10,11,13]. The characteristics of an accurate dynamic latch comparator are defined by its input-referred offset voltage for a given power dissipation, speed and die area.

This paper reports the design of a traditional double tail comparator in terms of time delay and input referred offset. A compact architecture is therefore proposed in order to improve the delay and offset voltage due to kickback noise in the conventional topology. The circuit utilizes the enhancement NMOS load, which reduces the output swing and improves the power consumption and the comparison speed of the circuit. To avoid parallel oscillations and short circuit power dissipation in the latch stage, the cross-coupled transistors consisting that block was isolated to ground state, a suitable transistor sizing was performed during the design process. Therefore, the mismatch and parasitic capacitance were reduced and the trans-conductance of the cross-coupled transistors was improved. An output buffer was adopted in the last stage, in order to filter the residual noise coming from the latch. Detailed analysis of the time delay and power dissipation of the whole circuit has been discussed and compared to state-of-art architectures; a method is therefore proposed to reduce the total delay and the power consumption of the traditional double-tail comparator. That empowered the design and makes the proposed architecture compact for handling low-offset, low-power and very high-speed operations. The design was validated by the Process-Voltage-Temperature (PVT) analysis and post-layout simulation results, implemented in 65 nm CMOS technology process from TSCM using Electric VLSI.

The rest of this paper is organized as follows. Section 2 presents the conventional double-tail comparator (CDTC) and the analysis related to its operating mode and time delay. In Section 3, the proposed dynamic latch comparator is presented; analysis related to its operating mode, power consumption, kickback noise and time delay was discussed and then compared with the one in Section 2. The design considerations are then applied, validated, discussed and compared to previous works in Section 4. The paper has been summarized in Section 5.

2 | CONVENTIONAL DOUBLE-TAIL COMPARATOR

A CDTC is shown in Figure 1. This topology has less tacking compared to the traditional dynamic comparator (single-tail comparator). The double tail enables both a large current in the decision stage and wider M_{tail2}, for fast latching independent of the input common-mode voltage (Vcm), and a small current in the input stage (small M_{tail1}), for low offset [14,15]. The operation of this comparator is as follows. During the reset phase (CLK = 0, M_{tail1} and M_{tail2} are off), transistors M3-M4 pre-charge F2 and F1 nodes to V_{DD}, which in turn causes transistors MR1 and MR2 to discharge the output nodes to ground. During decision-making phase (CLK = V_{DD}, M_{tail1} and M_{tail2} turn on), M3-M4 turn off and voltages at nodes F2 and F1 start to drop with the rate defined by $I_{\text{tail1}}C_{F(1,2)}$ and on top of this, an input-dependent differential voltage $\Delta V(F1, F2)$ will build up. This voltage is transferred on to the latch circuit by transistors MR1 and MR2. Latch regeneration starts once the nodes voltage F1 and F2 are not sufficient for MR1 and MR2 to hold output to zero. Therefore, for V(Inp) > V(Inm), Outp is pulled to V_{DD} and Outm to ground as shown in Figure 2. The double-tail topology is suitable for low-voltage applications due to less stacking; kickback noise should be normally reduced due to the effective shielding of input and output by MR1 and MR2 [16,17], which will enable to handle high-speed and low-offset operations. However, transistors M7 and M8 consisting the cross-coupled inverter are not isolated to the ground state, when the clock rate is very high, there is a period that nodes F2 and F1 pull MR1/MR2 to reach sufficient voltage that may turn it on; at the same time, MR1/MR2 and the corresponding cross-coupled device operating in the regeneration phase, acts as in parallel. That involves parasitic oscillation caused by parallel MOSFETs, which results in a poor reduction of kickback noise in the circuit. Parallel MOSFETs are extremely susceptible to oscillation during switching transitions when there is an imbalance in the current

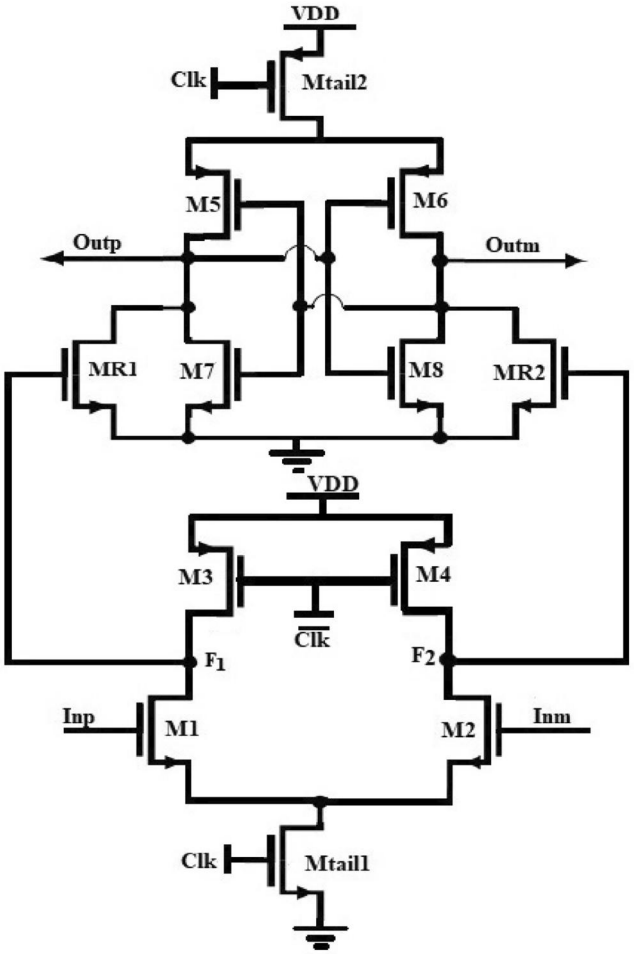

FIGURE 1 Block diagram of conventional double-tail dynamic comparator

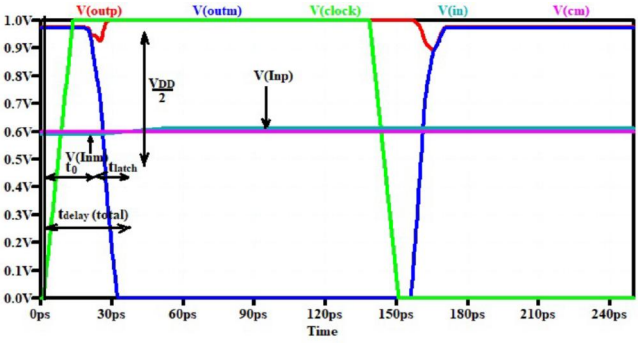

FIGURE 2 Transient simulation of the conventional dynamic latch comparator (V_{DD} = 1 V, V_{cm} = 0.5 V, ΔV_{in} = 5 mV, clk = 20 GHz)

sharing. Moreover, the slow dropping rate of F1 or F2 nodes in the pre-charge mode leads to a significant imbalance between MR1 and MR2, and then produces a significant dynamic offset, since MR1 and MR2 drains are directly connected to the latch output nodes. Therefore, isolating those transistors to the latch output nodes would help in lowering the offset. The delay of the comparator is defined as the time that the output

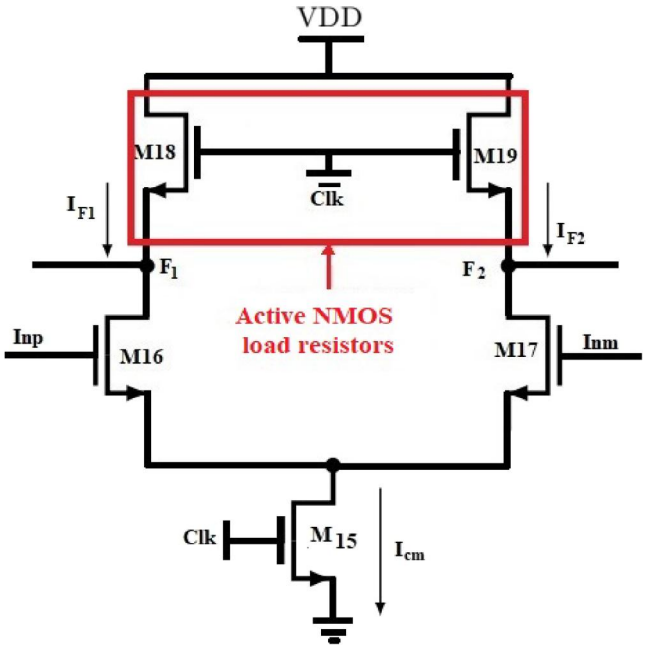

FIGURE 3 Block diagram of proposed preamplifier with enhancement NMOS load

difference takes place to reach $\frac{V_{DD}}{2}$. The total delay of the comparator is composed of latch delay, caused by cross-coupled inverters (M5/M6, M7/M8) and the delay occurred to charge output load capacitance until the first NMOS transistor (M7/M8) turns on [11,18]. Figure 2, shows the time response of the CDTC with a very small differential input voltage of 5 mV.

The analytical expression of the total delay of the conventional double tail comparator can be written as:

$$t_{delay} = t_0 + t_{latch} \tag{1}$$

$$t_0 = \frac{V_{THN} C_{out}}{I_P} = \frac{2 V_{THN} C_{out} \mu_p C_{ox} \frac{W_P}{L_P}}{g_{mP}^2} \tag{2}$$

where C_{ox} is the gate oxide capacitance, μ_p the hole mobility, V_{THN} is the threshold voltage of M7 and M8, C_{out} is the load capacitance of the output nodes, I_P is the current that passes through M5, g_{mP} is the transconductance of the PMOS transistor M5; W_P and L_P are the channel width and length of M5, respectively. However, the total effective transconductance ($g_{m,\mathrm{eff}}$) of the inverter consisting of M5 and M8 and is defined as follow:

$$g_{m,eff} = g_{mP} + g_{mN} \tag{3}$$

where g_{mN} is the trans-conductance of the NMOS device of the inverter. Since the NMOS transistor M8 is off during this period, g_{mN} is negligible. Therefore, t_0 being the period from the rising edge of the clock to the time when Outp and Outm are charged to V_{THN} considered in Ref. [14].

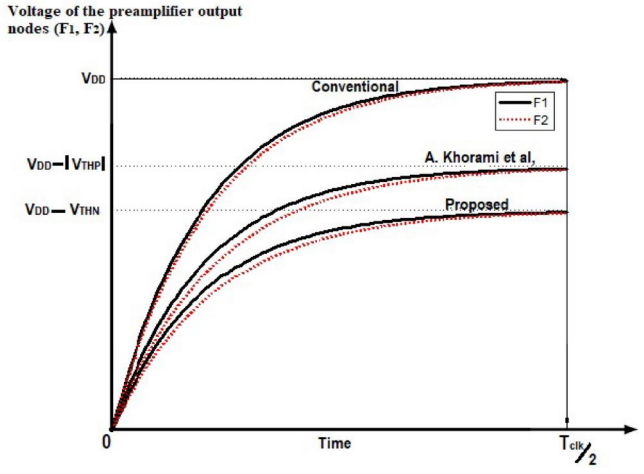

FIGURE 4 Voltage at the preamplifier output nodes during the evaluation phase for both the proposed, conventional and Ref. [21] topologies

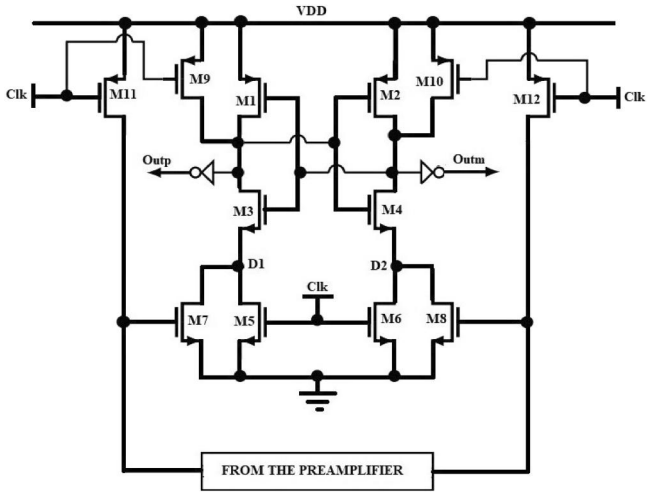

FIGURE 5 Block diagram of the proposed dynamic latch comparator

$$t_0 \simeq \frac{V_{THN}C_{out}}{I_P} = \frac{2V_{THN}C_{out}\mu_p C_{ox}\frac{W_P}{L_p}}{g_{mP}^2} \tag{4}$$

However, the time delay of the latch is given by Equation (5) as follow:

$$t_{latch} = \frac{C_{out}}{g_{m,eff}} \ln\left(\frac{\frac{V_{DD}}{2}}{\Delta V_0}\right) \tag{5}$$

where $\Delta V_{out} = \frac{V_{DD}}{2}$ and ΔV_0 is the difference of the initial output voltage of the latch at the beginning of the regeneration process. Since all the transistors of the cross-coupled inverter are ON during the evaluation process, the total effective trans-conductance is calculated as follow:

$$g_{m,eff} = C_{ox}\frac{W_P}{L_P}(\mu_P(|V_{GSP}| - V_{THP}) + \mu_N(|V_{GSN}| - V_{THN})) \tag{6}$$

Therefore, the total time delay of the conventional double-tail dynamic latch comparator can be expressed as:

$$t_{delay} = \frac{2V_{THN}C_{out}\mu_p C_{ox}\frac{W_P}{L_p}}{g_{mP}^2} + \frac{C_{out}}{g_{m,eff}} \ln\left(\frac{\frac{V_{DD}}{2}}{\Delta V_0}\right) \tag{7}$$

As illustrated in Equation (7), the delay strongly depends on the differential input voltage, the capacitive load of the output nodes of the latch and the trans-conductance (gm) of the input and intermediate transistors. Increasing ΔV_0 results in reducing the delay. At the end, once the decision is completed, both the intermediate transistors (MR1 and MR2) cut-off; since the node F1 and F2 discharge to the ground [11,18], there is no contribution to improve the effective trans-conductance of the latch. Therefore, enhancing the effective trans-conductance of the inverter will help in optimizing the total delay of the comparator; and then increasing the speed of the device.

3 | PROPOSED DYNAMIC LATCH COMPARATOR

The proposed dynamic latch comparator utilizes a differential pair amplifier with the enhancement-NMOS load to achieve sufficient gain for low offset and high-speed solution as depicted in Figure 3. Therefore, the gain of this comparator will be high due to using the enhanced differential amplifier, which leads to improving the power consumption and the comparison speed [11,19]. The NMOS load transistor's source swing from 0 to $V_{\mathrm{DD}}-V_{\mathrm{THN}}$ when its gate and drain are clocked from 0 to V_{DD}; comparing to the PMOS counterpart in which nodes swing from 0 to V_{DD}. So, the differential output nodes (F1 and F2) should be pre-charged from 0 to $V_{DD} - V_{THN}$ Figure 4. Furthermore, For NMOS, the V_{TH} is increased when its body–source voltage is biased to be negative. This is referred to as reverse body biasing [19]. Besides, transistor M15 is sized so that its on-resistance allows the enhanced differential pair to be biased near the weak inversion at the start of the evaluation phase. When clock is high (Clk = VDD), the enhanced differential pair starts a specific tail current (I_{cm}). The large finite resistance of M15 produces an increasing $\frac{g_m}{I_D}$ aspect ratio with decreasing V_{GS}. The variability of V_{THP} and V_{THN} (in PMOS and NMOS transistors) tends to be quite high in nano-metre CMOS technologies [20]. Thus, it must be kept as low as possible through proper transistor sizing to reduce the body effect which lowers the voltage swing at the preamplifier output nodes. The whole circuit works into two phases: reset or pre-charge phase and regeneration or Evaluation phase.

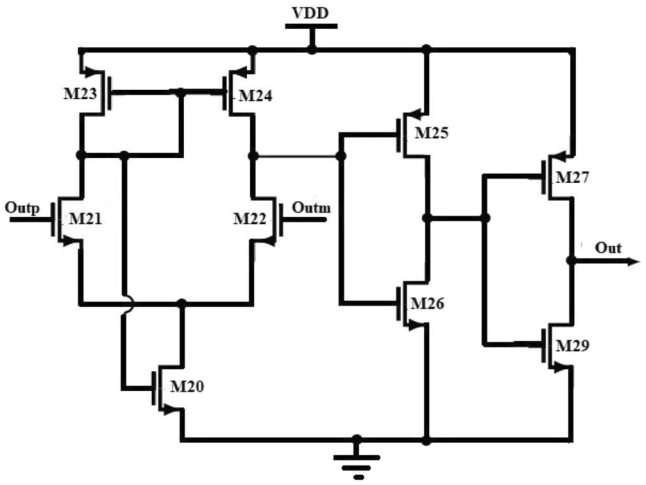

FIGURE 6 Block diagram of the output buffer of the proposed dynamic latch comparator

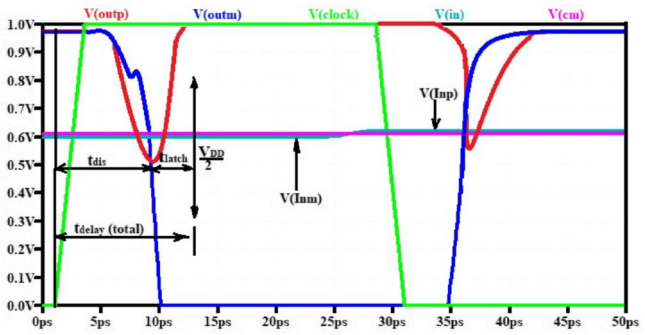

FIGURE 7 Transient simulation of the proposed dynamic latch comparator (V_{DD} = 1 V, V_{cm} = 0.5 V, ΔV_{in} = 5 mV, clk = 20 GHz)

3.1 | The reset phase or pre-charge

In the reset phase, the clock is low; the tail transistor of the sense amplifier (M15) is off. Therefore, the current source of M15 is switched off; ensuring that there is no static power consumption in the first phase. Nevertheless, M19 and M18 are ON, pulling terminal F1 and F2 $V_{DD}-V_{THN}$ to. As a result, M7 and M8 turn ON. Since M5 and M6 are off; M7 and M8 ON; nodes D1 and D2 are discharged to ground. The pull-up transistors (M9 and M10) of the latch as shown in Figure 5, are ON so, the output nodes Outp and Outm are pre-charged to V_{DD}.

3.2 | The evaluation phase

M19, M18, M9, M10, M11 and M12 are Off. Therefore, M4 and M3 begin to conduct. Since Vinp > Vinm, the drain voltage of M16 started to fall at a faster rate than the drain of M17 due to the highest trans-conductance of M16 comparing to M17. The tail transistor of the sense amplifier is ON and begins to conduct. Therefore, the positive feedback from the cross-coupled M2, M3 kicks in; the node D1 drops faster and pulls Voutm to low logic; therefore, M2 turns ON and pulls Voutp to high logic. Ones the decision made, comparator outputs control M4 and M3, which will be turn off to avoid static power dissipation. The opposite effect occurs when Vinm > Vinp; in that case Voutp is pulled to low logic and Voutm to high logic.

To reduce the kickback noise due to the transient at the regeneration nodes D1 and D2, the drains of the transistors forming the input differential pair need to be isolated from the regeneration nodes during the regeneration phase. This is done using switching transistors M7 and M8 between the regeneration node and the drains of the input differential pair. Those switches which are biased to work in strong inversion, are sized to exhibit high trans-conductance for thermal noise prevention. Thus, isolating the regeneration node and the drains of the input differential pair when regeneration starts. However, offset voltage is reduced using custom transistor sizing/matching during the design process, to avoid mismatch and process variation.

Transient simulations showing the outputs settling to inputs that are very close to the trip points of the latch circuit are given in Figure 6. Suitable transistor sizing/matching was performed to obtain very small offset voltage at the input common mode voltage of 0.5 V. As depicted on that figure, the comparator will become very slow and its outputs may not settle to a valid level. The differential input voltage is set to 5 mV, that value is very small and closed to the offset voltage, this affects the time response of the circuit which enters in a metastable state. Meta-stability is a problem that occurs in all latching comparators when the input is near the comparator decision point. That phenomenon is mostly due to parasitic; the interconnects between the transistors and the bulk silicon include a lot of parasitic capacitances. Those capacitances, particularly at the nodes with the positive feedback of the latch (M2, M3), are seriously influencing meta-stability and the regeneration process. To avoid that, we used a symmetrical placement of all the transistors while laying-out the design [22], the Enhancement NMOS load in the preamplifier stage, and all the other NMOS transistors of the circuit were designed to handle a zero potential between the source and substrate. This will reduce to a great extent the source-substrate parasitic capacitance and therefore lowering the probability of having meta-stabilities.

3.3 | Power dissipation

For low-noise and energy efficiency requirements, the weak inversion model was adopted for the transistors in Figure 3. Transistors were biased and designed by keeping the ratio $\frac{g_m}{I_D}$ sufficiently high to optimize mismatch along with other analogue performance such as the gain-bandwidth product GBW [23]. Since moving from strong to weak inversion and from a design perspective (i.e. constant current), two balancing phenomena occur: the mismatch increases for a given transistor size but decreases with increasing transistors surface [24,25]. So using high $\frac{g_m}{I_D}$ is obviously of high interest for low-

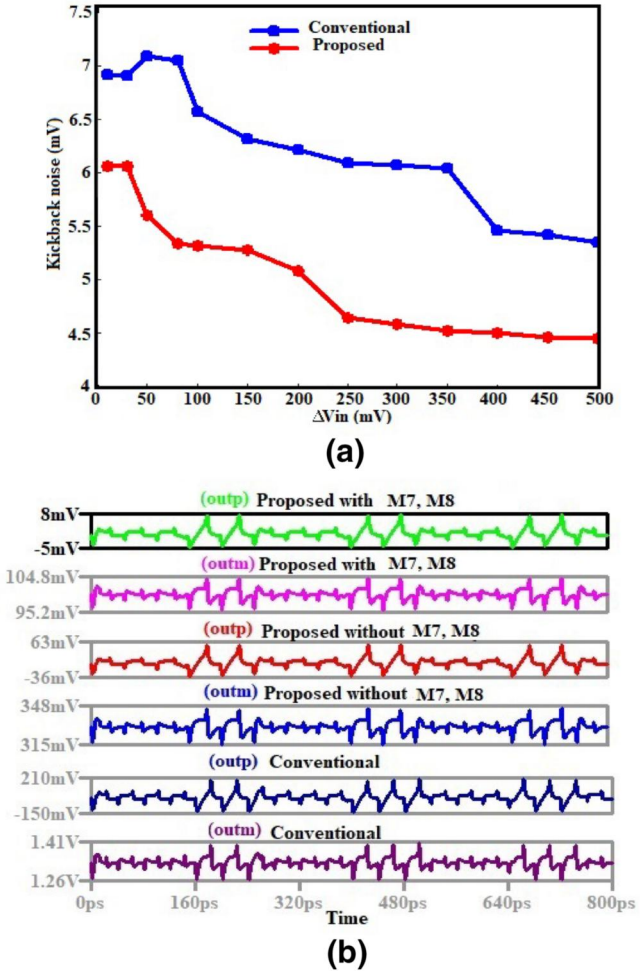

FIGURE 8 Kickback noise error on the comparators output voltage versus differential input voltage (a) and Transient simulation showing the Kickback noise error at the comparator outputs for both the conventional double-tail comparator and the proposed circuit in the absence & presence of M7, M8 transistors (b) $\Delta V_{in} = 20$ mV

voltage and low-power applications [25]. The output common-mode voltage of the preamplifier discharges by $\Delta V_{Fi,cm}$ from the pre-charge to V_{DD}, with an average discharge current I_{cm} and during integration time T_{int}. Therefore, the common-mode voltage drop at the preamplifier output nodes is defined as:

$$\Delta V_{Fi,cm} = \frac{I_{cm} T_{int}}{C_L} \tag{8}$$

Power consumption is optimized based on load transistor modelling and the time variance of the preamplifier output nodes. The average power of the supply voltage during one period of the comparison is obtained from the well-known formula [21],

$$P_{total}(t) = \frac{1}{T_{clk}} \int_0^{T_{Clk}} V_{DD}(I_{cm}).dt \tag{9}$$

where,

$$I_{cm} = I_{F1} + I_{F2} \tag{10}$$

Since the NMOS load transistor's source swing to $V_{DD}-V_{THN}$ when it gate and drain are biased by V_{DD}, the differential output nodes (F_1 and F_2) should be pre-charged from 0 to $V_{DD}-V_{THN}$. Considering the threshold voltages of MOS devices provided by the Predictive Technology Model website in 65 nm CMOS process ($V_{DD}-V_{THN} < V_{DD} - V_{THP}$), using the NMOS load device would help in lowering the preamplifier power consumption. However, the power consumption of the latch is negligible compared to the power consumption of the preamplifier [21]. Therefore, the total power dissipated in the design can be derived as follow:

$$P_{total} = \frac{2C_L V_{DD}(V_{DD} - V_{THN})}{T_{clk}} \tag{11}$$

Based on Equation (11), the percentage of power reduction increases by a factor α is given by Equation (12).

Considering the average of the typical value in 65 nm CMOS technology, the power reduction is around 42%. By using the NMOS load instead of the PMOS counterpart, a factor of 6% of the total power dissipation is saved from comparing to Ref. [14].

$$\alpha = 100 \times \frac{V_{THN}}{V_{DD}} \tag{12}$$

3.4 | Kickback noise

When the regeneration phase starts, the switch opens and the two cross-coupled inverters implement positive feedback; this makes the output voltages go towards 0 and V_{DD}, according to the small output voltage found at the end of the reset phase. Besides, the effects of the internal capacitances of the MOS devices and local mismatch on transistors can exacerbate the situation [26]. The input voltage is disturbed, which may degrade the accuracy of the converter. This disturbance is usually called kickback noise. Generally, high-speed and high power-efficient comparators generate more kickback noise [27,28]. Figure 7a shows the peak output voltage error as function of ΔV_{in} for both the conventional and the proposed comparator. It can be observed that increasing ΔV_{in} result in lowering the noise effect in our design. In fact, at the pre-charged phase, the input differential voltage is applied and amplified, while the regeneration process not yet started, no disturbance occurs [10]. At the beginning of the comparison phase, these auxiliary transistors

are turned on and help the circuit to start the decision-making and then the regeneration process [1,26]. Also, those transistors which are in the triode region are parallel with input differential pair transistors and help in keeping the drain of the input transistors to sense a less voltage variation, which leads to less kickback noise [1,28] as depicted on Figure 7b. On that figure, the kickback noise error at the comparator outputs is simulated in the absence and in the presence of M7, M8 devices and is compared to that produced by the CDTC for 20 mV differential input voltage ($\Delta V_{\text{in}} = 20$ mV) during the reset-to-regeneration transition. The proposed comparator exhibited low kickback noise due to using the auxiliary transistors M7, and M8 to isolate the preamplifier output nodes first, and secondly reducing mismatch effect and parasitic capacitance of the transistors while designing the devices. Therefore, the offset reduction in the feedback loop consisted of suitable transistor sizing operating in the weak inversion region and mismatch optimization [25,29].

3.5 | Thermal noise

The proposed enhanced differential pair which devices operate in weak inversion mode exhibited high gain, provided by $g_{m16,17}$. There is a possible increase of input noise at the differential input therefore [1]. During the evaluation phase, M19, M18, M9, M10, M11 and M12 are Off; so do not contribute to the noise behaviour of the proposed circuit. However, M1-M4 devices are cascaded, so their noise effect is negligible at low frequencies [1]. Thus, the total input referred noise voltage of the comparator consists of M5-M8, M16/M17 noise contribution. M16/M17 devices are sized identically to produce the same/similar input referred offset [30]. The input referred noise of those devices consisting the input differential amplifier for weak inversion operation is well analysed in Ref. [30] and given at a time $t = T_{int}$ as:

$$v^2_{n,th,in}(T_{int}) = \frac{2nkT}{C_L.\Delta V_{Fi,cm}(T_{int}).\left(\frac{g_{m16,17}}{I_{cm}}\right)_{T_{int}}} \tag{13}$$

where, n, is a process constant, $I_{\text{cm}}(t)$ is the tail current, T_{int} the integration time, k the Boltzmann constant and T is Kelvin's temperature.

Moreover, M7-M8 can be seen as complementary input which thermal noise can be modelled as a voltage source in series with the input. Thus, exploiting the analysis given in Ref. [1], the thermal noise contribution of M5-M8 at the output of the comparator is given as:

$$V^2_{n,th,out}(T_{int}) = \left(I^2_{n,5,th} + I^2_{n,6,th} + I^2_{n,7,th} + I^2_{n,8,th}\right)\left(R^2_{out}\right) = 8kT\gamma\left(g_{m5,6} + g_{m7,8}\right)R^2_{out} \tag{14}$$

where, γ is the channel thermal coefficient and R_{out} the output impedance of the latch system. The input referred noise for M5-M8 can be derived as,

$$V^2_{n,th,in}(T_{int}) = \frac{V^2_{n,th,out}(T_{int})}{A^2_{latch}} \tag{15}$$

where A_{latch} is the voltage gain of the latch. Henceforth, considering the operating state of each transistor in the evaluation phase, the latch gain can be given as,

$$A_{latch} = \left(g_{m5,6} + g_{m7,8}\right)R_{out} \tag{16}$$

substituting A_{latch} from Equation (16), Equation (15) leads to

$$V^2_{n,th,in}(T_{int}) = \frac{8kT\gamma}{g_{m5,6} + g_{m7,8}} \tag{17}$$

By adding those two components, the total input referred noise of the designed comparator is given as:

$$E^2_{n,th,in},(T_{int}) = \frac{2nkT}{C_L.\Delta V_{Fi,cm}(T_{int}).\left(\frac{g_{m16,17}}{I_{cm}}\right)_{T_{int}}} + \frac{8kT\gamma}{g_{m5,6} + g_{m7,8}} \tag{18}$$

As highlighted in Equation (18), it is evident that a large $\left(\frac{g_{m16,17}}{I_{cm}}\right)$ combined with a large $g_{m5,6}$ & $g_{m7,8}$, is needed for improving the noise performance of our proposed design. To get the lowest possible noise at a given current, it is desirable to maximize $\left(\frac{g_m}{I_{cm}}\right)$ for the differential input, which means that it is desirable to let M16 and M17 operate in weak inversion until the latch stage makes decision [30]. It can be concluded that by using the auxiliary devices sized to keep their transconductance sufficiently high and increasing $\left(\frac{g_{m16,17}}{I_{cm}}\right)$ for the differential input amplifier, the thermal noise of the proposed dynamic latch comparator is reduced.

3.6 | Time delay of the proposed DLC

The total delay time in this design is the addition of two components; the delay of the load capacitive discharge (t_{dis}) which is the period from the rising edge of the clock to the time when Outp and Outm are charged to V_{THN}; and the delay of the latch due to the regeneration (t_{latch}).

$$t_{delay} = t_{dis} + t_{latch} \tag{19}$$

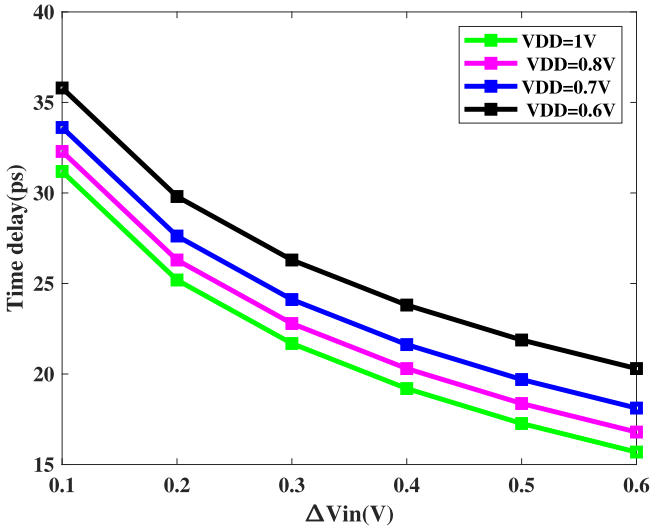

FIGURE 9 Delay of the proposed comparator versus differential input voltage (V_{DD} = 1 V, V_{cm} = 0.5 V, Clk = 20 GHz)

$$t_{dis} = \frac{V_{THN} C_{out}}{I_P} = \frac{2V_{THN} C_{out} \mu_p C_{ox} \frac{W_P}{L_p}}{g_{m,eff}^2} \tag{20}$$

$$g_{m,eff} = g_{mP} + g_{mN} = g_{mP}\left(1 + \frac{g_{mN}}{g_{mP}}\right) \tag{21}$$

$$g_{mP} = \mu_P C_{ox} \frac{W_P}{L_P} (|V_{GSP}| - V_{THP}) \tag{22}$$

$$g_{mN} = \mu_N C_{ox} \frac{W_N}{L_N} (V_{GSN} - V_{THN}) \tag{23}$$

Therefore, t_{dis} can be derived as follow:

$$t_{dis} = \frac{2V_{THN} C_{out} \mu_p C_{ox} \frac{W_P}{L_p}}{g_{mP}^2 \left(1 + \frac{g_{mN}}{g_{mP}}\right)^2} = \frac{t_0}{\left(1 + \frac{g_{mN}}{g_{mP}}\right)^2} \tag{24}$$

where t_0 is the period from the rising edge of the clock to the time when Outp and Outm are charged to V_{THN} considered in the conventional DLC [14]. However, the delay of the latch is given by equation.

$$t_{latch} = \frac{C_{out}}{g_{m,eff} + g_{m11,12}} \ln\left(\frac{\frac{V_{DD}}{2}}{\Delta V_0}\right) \tag{25}$$

$g_{m,\text{eff}}$, being the effective trans-conductance of the back-to-back inverter, and ΔV_0 the difference of the initial output voltage of the latch at the beginning of the regeneration process.

$$\Delta V_0 = g_{m16,17}(g_{m5,6} + g_{m7,8}) \frac{\Delta V_{in}}{C_{out}} t_{dis} \tag{26}$$

Equations (25) and (26) lead to the following formula of the total time delay.

$$t_{delay} = \frac{t_0}{\left(1 + \frac{g_{mN}}{g_{mP}}\right)^2} + \frac{C_{out}}{g_{m,eff} + g_{m11,12}} \ln\left(\frac{\frac{V_{DD}\left(1 + \frac{g_{mN}}{g_{mP}}\right)^2}{2}}{g_{m16,17}(g_{m5,6} + g_{m7,8}) \frac{\Delta V_{in}}{C_{out}} t_0}\right) \tag{27}$$

Further computations of Equation (27) lead to the developed expression given as;

$$t_{delay} = \frac{t_0}{\left(1 + \frac{g_{mN}}{g_{mP}}\right)^2} + \frac{t_{latch}}{1 + \frac{g_{m11,12}}{g_{meff}}} + \frac{2C_{out}}{g_{m,eff} + g_{m11,12}} \ln\left(\frac{1 + \frac{g_{mN}}{g_{mP}}}{g_{m16,17}(g_{m5,6} + g_{m7,8})}\right) \tag{28}$$

where, t_0 and t_{latch} are the delay of the pre-charge and the evaluation phases respectively in the CDTC and in the comparator in Ref. [14]. In this equation, the third term has a negative contribution since, M5-8, M16 and M17 are designed so that, $g_{m16,17}(g_{m5,6} + g_{m7,8}) > \left(1 + \frac{g_{mN}}{g_{mP}}\right)$. Therefore, the total delay time is reduced at a great extent.

Equation (28) represents the effect of various parameters on the total delay time. As depicted in that equation, the time delay of the preamplifier in the proposed structure is a fraction of the corresponding delay for the conventional structure. For a better optimization of time delay, furthers analysis should be carried on depending on the correlation between time delay and each of those parameters [14].

4 | SIMULATION OUTCOMES AND DISCUSSION

4.1 | Simulation and implementation framework

To achieve high-performance behaviour, our comparator is optimized with custom transistor sizing during the design process. The performances of the proposed circuit were verified using LTSpice simulator and the layout was implemented in 65 nm CMOS technology process from TSMC, using Electric VLSI. For general simulation purpose, the supply voltage was V_{DD} = 1 V, the common-mode voltage V_{cm} = 0.6 V, the differential input voltage level ΔV_{in} = 10 mV, the frequency of the clock signal was set to 20 GHz and the frequency of the input signal to 4 GHz. The load capacitance C_L and the output one C_{out} was set as 3.8 fF during the simulations. Monte-Carlo

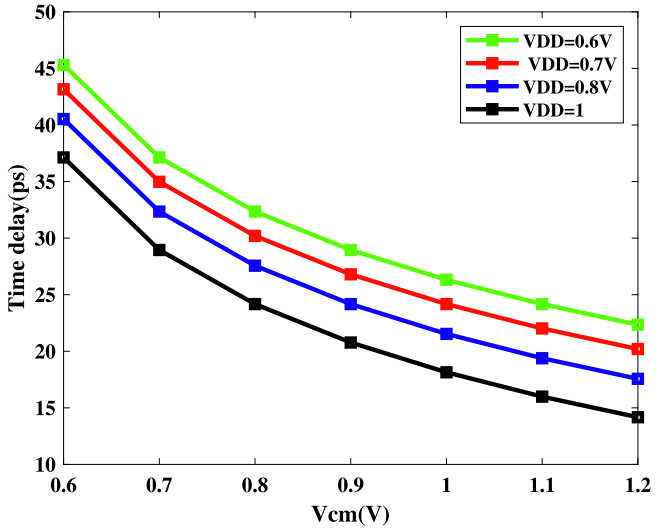

FIGURE 10 Delay of the proposed comparator versus input common mode voltage (V_{DD} = 1 V, ΔV_{in} = 0.5 V, Clk = 20 GHz)

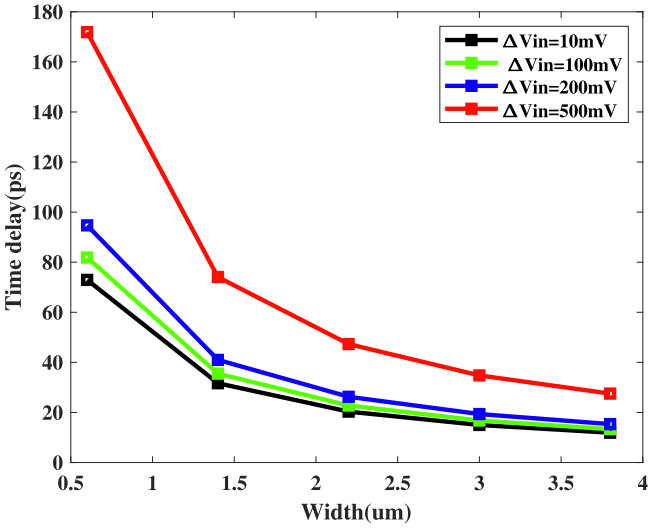

FIGURE 11 Delay of the proposed comparator versus the width of switches M5 and M6

simulation was performed for 500 runs and the histograms of the offset voltage and time delay were extracted.

4.2 | Result and discussion

The design parameters of the proposed comparator were improved as compared to CDTC and comparators which have been proposed in Ref. [21] and refs [1,15,18]. Figure 8 demonstrates the dependency of the proposed comparator delay on various differential input voltages level at different supply voltages. For a given V_{DD} = 1 V, the delay is 35.6 ps at differential input voltage level $\Delta V_{in} = 10\ mV$. This delay falls from 35.6 to 14.8 ps while ΔV_{in} varies from 10 to 500 mV. Furthermore, at a particular ΔV_{in}, the higher the supply voltage (V_{DD}), the higher the comparator delay will be. The worst-case delay of 35.6 ps for V_{DD} = 1 V for ΔV_{in} = 10 mV and the best of 14.8 ps for V_{DD} = 0.8 V and ΔV_{in} = 500 mV; the common-mode voltage being set to 500 mV (0.5V_{DD}). The effect of the input common-mode voltage (V_{cm}) on the delay of the comparator was simulated for 500 mV differential input under different supply voltages, and the results are shown in Figure 9. When V_{DD} = 1 V and V_{cm} = 500 mV, the delay is found to be 47 ps. For a fixed value of V_{DD}, the delay decreases while the input common-mode voltage (V_{cm}) increases. As illustrated in Figure 9, the delay is sensitive to the input common-mode voltage. The worst-case delay of 47 ps is exhibited for $V_{cm} = V_{DD}$ = 0.5 V and the best case of 14.4 ps was controlled for $V_{cm} = V_{DD}$ = 1 V.

Figure 10 shows the simulated delay of the proposed comparator with different widths of switches M5,6. As illustrated in Figure 10, when the width of those switches is larger than 3 µm, increasing the width would not help to reduce significantly the delay. For instance, at a given ΔV_{in} = 10 mV, the delay drops from 77 to 13.8 ps, as width drops from 0.6 to 4 µm. The delay becomes almost constant

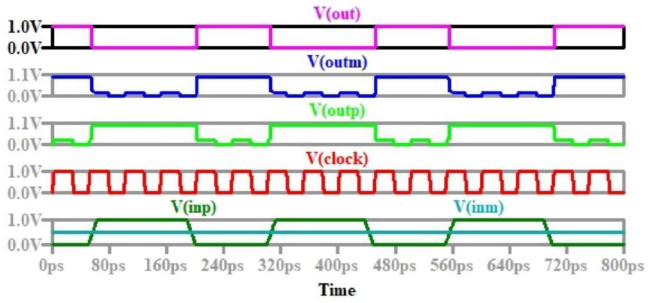

FIGURE 12 Post layout simulation of the time response of the proposed dynamic latch comparator (V_{DD} = 1 V, V_{cm} = 0.5 V, ΔV_{in} = 0.5 V, Clk = 20 GHz, C_{out} = 3.8fF)

for widths larger than 3.2 µm. In these considerations, the extracted value of the delay is found to be 13.8 ps.

The proposed dynamic comparator was simulated using 65 nm TSCM technology. The lengths of NMOS and PMOS are taken as 65 nm except M5 and M6 which lengths are 0.13 µm. The widths are sized to guarantee low offset, optimal time delay and small die area by reducing the $\frac{W}{L}$ ratio. For instance, as depicted in Figure 9, the widths of switches M5 and M6 are found to be 3.2 µm, for and optimal time delay of 12.15 ps. The clock frequency was set to 20 GHz and the input signal frequency to 4 GHz. The voltage supply was 1 V with common-mode input voltage of 0.5 V and 100 mV ΔV_{in}. The post-layout simulation of the proposed comparator is illustrated in Figure 11, with 3.8fF as extracted load capacitor at the Outm and Outp nodes of the latch. It is observed from Figure 11 that, with 1 V positive step for the input V_{inp} and keeping V_{inm} fixed to 0.5 V, V_{cm} = 0.5 V and Clk = 20 GHz the proposed dynamic latch comparator can switch successfully. V_{outp} and V_{outm} are the latch's output voltages and V_{out} stands for the comparator's output voltage after filtering noise

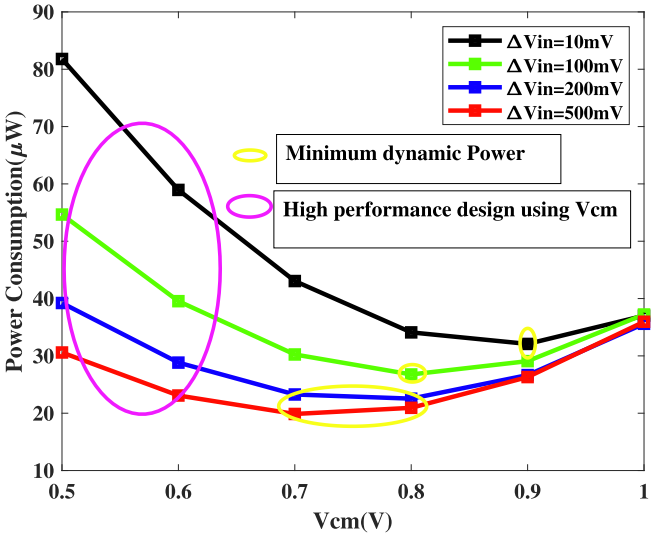

FIGURE 13 Simulation results of the power consumption versus input common-mode voltage, at various ΔV_{in} (Clk = 20 GHz and V_{DD} = 1 V)

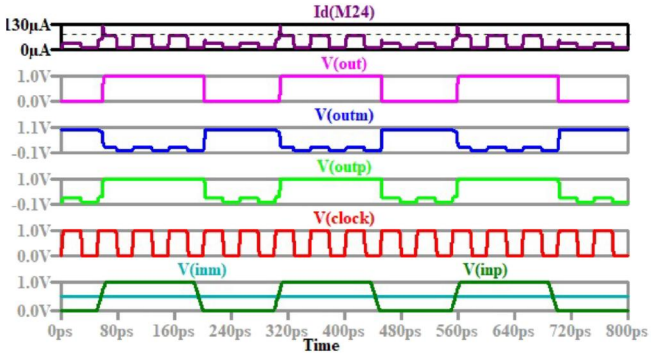

FIGURE 14 Post-layout simulation results for the average current of the proposed dynamic latch comparator

coming from the latch. In fact, the last stage of the circuit, which is a buffer as shown in Figure 12, plays an important role in filtering the noise coming from the latch. Due to the hysteresis present in the output buffer, the output transition will take place only when the latch output is sufficiently high or low resulting in sharp, well-defined digital data [24,28,30]. Definitely, V_{out} is immune to noise and the delay can be evaluated easily.

The effect of the common-mode voltage, V_{cm}, on power dissipation at various ΔV_{in} is simulated and the results are presented in Figure 13. It can be seen that power dissipation decreases with increase in V_{cm} from 0.5 to 0.9 V, at particular ΔV_{in}. However, for V_{cm} swing from 0.9 to 1 V, power dissipation increases but remains lower when compared to previous amplitude. For $\Delta V_{in} = 10\ mV$, the power dissipation is reduced from 81 μW at V_{cm} = 0.5 V to 38 μW at V_{cm} = 1 V. In general as depicted in Figure 13, the proposed comparator has less dependency on the V_{cm} due to the absence of the static power dissipation. The impact of transistor

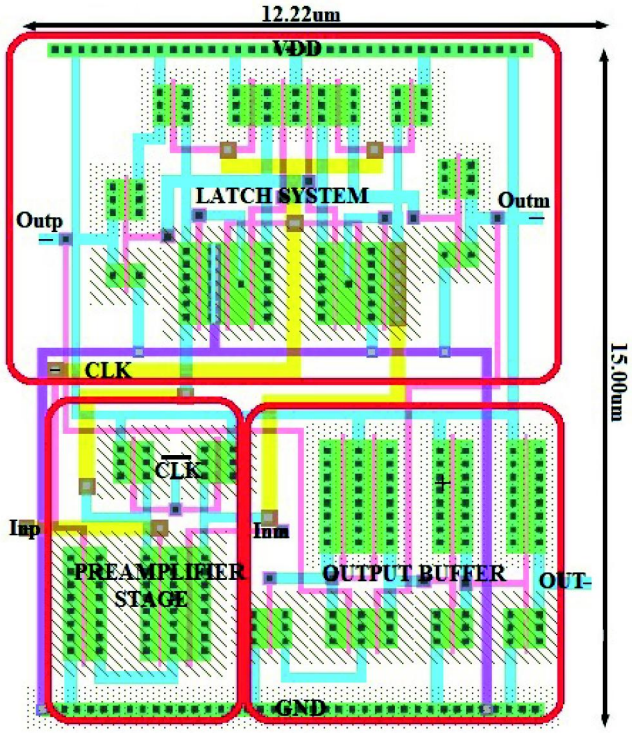

FIGURE 15 Layout diagram of proposed dynamic latch comparator using TSMC 65 nm CMOS technology

mismatch was evaluated while performing Monte-Carlo simulation.

Our design consumes very low amount of current exhibited in Figure 14. The post-layout simulation results show that the comparator circuitry requires only 67.8 μA, which is an average current for 20 GHz clock frequency. Moreover, the power dissipation of the design is 67.8 μW under 1 V voltage supply. The factor that significantly embodies the speed of a dynamic comparator is the propagation delay [22]. Generally, that parameter is inversely proportional to the input voltage applied. Moreover, a larger input voltage applied will increase the propagation delay [10,24,30]. The maximum operating frequency of the latch circuit is set by the propagation delay. In this work, the average propagation delay was extracted taking into account robustness of the design against process variation through a statistical analysis.

The circuit core layout is presented in Figure 15 where the chip occupies a small die area of 183.3 μm2. The mismatch and parasitic capacitance were reduced during the design process, using a parallel arrangement of all the transistors of the circuits. The post-layout Monte-Carlo simulation results for the offset voltage and time delay was performed to verify the reliability and the robustness of the design as depicted in Figure 16a,b) for 500 runs, respectively when ΔV_{in} = 0.5 V, V_{cm} = 0.5 V and the clock frequency being set to 20 GHz while using 1 V supply voltage. As shown on those plots, the average offset voltage of the circuit was controlled at 4.45 mV, while the standard deviation was 3.74 mV. Moreover, the average delay of the proposed design was only 14.28 ps while the delay

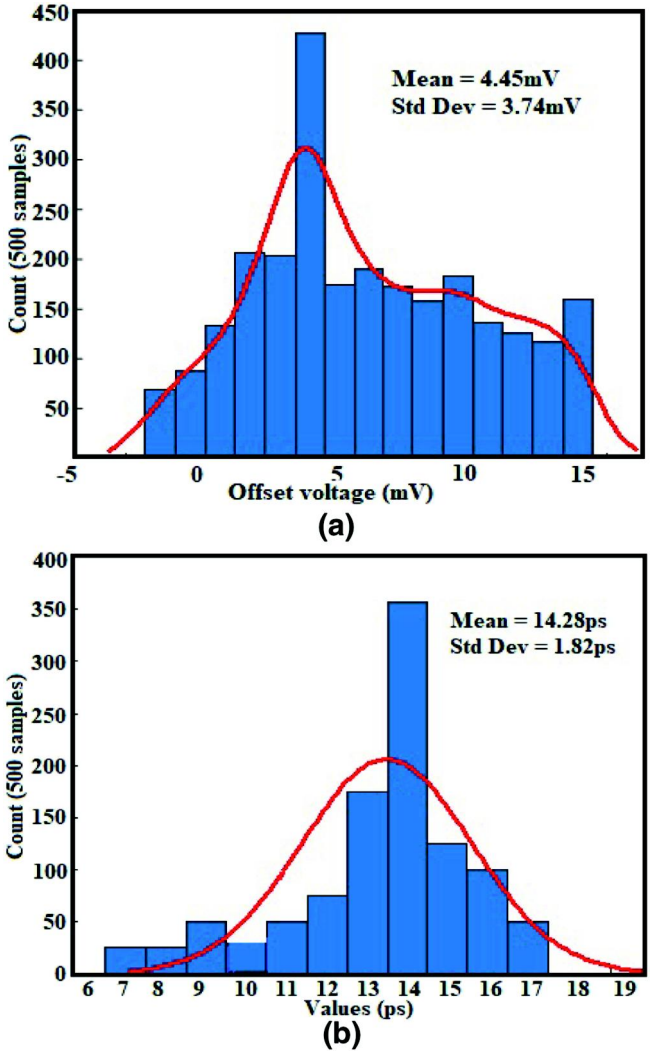

FIGURE 16 Monte Carlo results of both the offset voltage (a) and time delay of the proposed dynamic latch comparator (b) for 500 runs (V_{DD} = 1 V, V_{cm} = 0.5 V, ΔV_{in} = 0.5 V, Clk = 20 GHz, C_{out} = 3.8 fF)

standard deviation was controlled at 1.82 ps. By the way, the effects of the internal capacitances of the MOS devices is taking into account through the extracted parasitics. That affects the output voltage of the latch circuit, involving kickback noise rather than affecting the speed of the device. The achieving delay makes the clock of the latch signal faster up to 20 GHz, and achieves therefore a low-power behaviour with high-speed operations. Furthermore, the delay due to the amplification (regeneration phase) achieved in this design, is about 8 ps which represents 0.67 t_0; t_0 being the delay during the reset phase in Ref. [21]. So, adopting the auxiliary transistors help in lowering up to 33% the time delay of the amplification phase proposed in Ref. [21].

Corner analysis was performed via PVT variations for several different process corners (FF, FS, SF and SS) and temperatures, to demonstrate the global variation of the power consumption as depicted in Figure 17. Mismatch being a function of threshold voltage (V_{TH}) and supply voltage (V_{DD}), low V_{TH} (LVT) transistors have a reduced mismatch impact

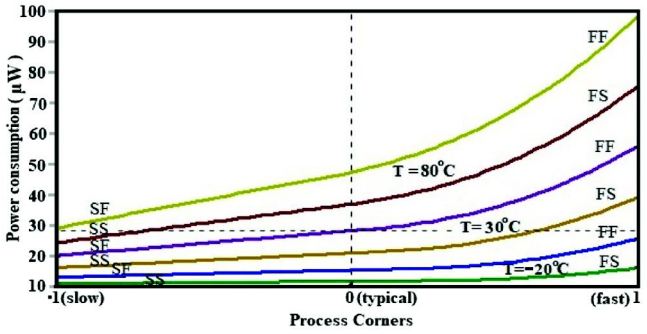

FIGURE 17 Simulation showing power consumption versus process variations and temperature

due to higher $\frac{V_{DD}}{V_{TH}}$ ratio than standard V_{TH} (SVT) or high V_{TH} (HVT) transistors [20,26]. The proportionate change in temperature from SVT to HVT is much larger as compared to that from LVT to SVT. Thus, it is more advantageous to move from HVT transistors to SVT devices, but this result in high power dissipation with the different corner process (FF and FS) for temperature of 80°C [26]. Although the increase in HVT can reduce percentage mismatch and power dissipation at temperature (−20°C and 30°C) for FF and FS corners. Large MOS devices increase the intrinsic parasitic which leads to more kickback noise and offset, but also reduce local head transfer and mismatch for LVT [26]. Taking into account trade-off between transistor size and mismatch, the optimal design technique (transistors sizing/matching) consisted of parallel arrangement of the devices to reduce the parasitic and mismatch effects, cancelling therefore the short circuit power generated by those parasitics. Difference in the NMOS and the PMOS characteristics can create short-circuit power consumption [25,26]. Moreover, local mismatch effects on transistors can exacerbate the situation. The effect is relatively small compared to switching and leakage power. It can be shown on Figure 17 that SS and SF corners at different temperatures (−20°C, 30°C and 80°C) were prone to ultra-low power dissipation design, but would slow down the changing rate of the transistors. A such of condition would have significant effect on the input transistors (M16 and M17) of the preamplifier and the pull-up transistors (M9 and M10) of the latch, thus producing low-speed operations.

In Table 1, the comparison of the proposed circuit for special overall performance parameters is illustrated with some preceding existing topologies. Using 65 nm CMOS technology process, the circuit exhibited lowest power delay product (PDP) of 0.968 fJ at 1 V supply voltage with 20 GHz clock frequency. The smallest time delay, PDP and highest clock frequency were achieved for the purpose. Then, exhibited a higher speed with a satisfactory amount of power consumption and die area.

The comparator in Ref. [1] has a lower offset voltage and die area from simulation result, but its power consumption is more than 4x higher than that of our proposed comparator. The comparators in Ref. [15] and Ref. [18] have lower power dissipation but suffer both from lower speed and larger offset

TABLE 1 Performance comparison of the proposed dynamic latch circuit with previous works

Comparison properties	[18][a]	[14][b]	[21][a]	[17][a]	[1][a]	[15][a]	[This work][a]
Technology (nm)	90	180	180	45	65	90	65
Supply voltage (V)	1	1.2	1.8	0.8	1.2	1	1
Clock frequency (GHz)	1	0.5	0.5	14.7	6	1	20
Delay time (ps)	51.76	268.6	638.91	268	42.7	148.23	14.28
Power consumption (μW)	32.62	72.2	347	5.8	381	14.46	67.8
Offset voltage (mV)	7.7	7.3	7.78	3.16	3.87	1.35	4.45
PDP (fJ)	1.67	19.4	221.7	1.55	16.3	2.144	0.968
FOM (fJ/Conv)	32.62	112.5	694	63.5	63.5	1.35	3.39
Die area (μm2)	58.32	252	361	26.92	141.7	74.32	183.3

[a]Simulation.
[b]Measurement.

voltage. The proposed topology achieves the maximum clock frequency of 20 GHz. As results, this comparator can be used to boost the performances of high-speed ADCs. The inconvenience of the NMOS transistor's source driving $V_{DD}-V_{THN}$ when its gate and drain are biased by V_{DD} is used in the load transistors of the differential amplifier, as an advantage in reducing the output nodes swing of the preamplifier and then lowering the power dissipation of the proposed comparator up to 42% of the power dissipation of the conventional comparator and 6% comparing to Ref. [21]. A figure of merit (FOM) must be agreed upon for comparison with previous research works. The following FOM was defined to highlight the performances of this design with recently published work Ref. [32].

$$FOM = \frac{P_d}{F_s}(J/Conversion) \tag{29}$$

where, P_d is the power dissipation and F_s being the comparator's sampling frequency. From Table 1, the proposed DLC exhibited a quite low and satisfactory FOM.

5 | CONCLUSION

The problems and shortcomings of the conventional double tail comparator have been analysed in terms of time delay and offset voltage. The topology was customized to improve the regeneration speed and power dissipation of the circuit. New dynamic latch comparator architecture is therefore proposed. The design uses a differential pair based NMOS enhancement active load as preamplifier stage; this reduces the power dissipation and increases the comparison speed. Short circuit current was reduced in the latch stage thanks to auxiliary transistors which isolated the latch module to the ground state. The parasitic and mismatch were reduced adopting custom design and transistors matching/sizing during the design process. A compact architecture was therefore obtained and the regeneration process was speeded up. Thus, offset and kickback noise were reduced and the time delay was improved. Simulations were carried out in 65 nm CMOS technology and the results confirm that the parameters are improved to a great extent. Analytical results were validated by post-layout simulation results. The post layout Monte-Carlo simulation outcomes clearly reveal that the circuit achieves a maximum operating speed of 20 GS/s, with an average offset voltage of 4.45 mV and 3.74 mV standard deviation while propagating with 14.28 ps delay time with 1.82 ps standard deviation. Furthermore, the proposed comparator exhibited lowest PDP of 0.968 fJ and dissipates only 67.8 μW of power from 1 V supply. The percentage improvement in power consumption for the designed comparator is 42% and 6% as compared to the CDTC and comparator of Ref. [21] respectively. Moreover, chip layout of the proposed design occupies only 183.3 μm2 active die area. The achieved results are better than recently published researches and make the proposed comparator very suitable for accurate and high-speed ADCs.

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