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Design of a CMOS Comparator for A/D Converter Application

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Abstract

Design of a CMOS comparator with preamplifier-latch circuit is reported in this paper. Design has specially concentrated on low power consumption, low offset and high speed. The design has been simulated for performance verification in 0.18µm UMC Technology. Simulation results are obtained with this design about power dissipation 0.27mV, frequency 100MHz and offset voltage 280.7nV. Finally results have been compared with earlier published work and improvements are obtained in the design parameters. This design will be very useful for young researcher, ADC designer and manufacturers.

Keywords: CMOS Comparator, Low Power, Low Offset, High Speed and A/D Converter

1. Introduction

A high-speed, low-offset, low-power consumption comparators are very important for many applications, such as memory sensing circuits, Analog to Digital Converters (ADC) and data receivers. In conventional designs, pre-amplifiers are used to reduce offset voltage [1]. However, these techniques require high voltage gain to reduce the offset voltage and loosing effectiveness with the reduction of the drain resistance due to the technology scaling. While the technology scaling of MOS transistors enables high-speed and low-power operation, the offset voltage of the comparator is increased due to the transistor mismatch [2]. The latched comparator used for the clock signal and indicate, through their digital output level, whether its differential input signal is positive or negative [3]. They use a positive feedback mechanism to regenerate the analog input signal into a full scale digital signal (regenerative amplification), because this is much faster and power efficient than performing multi-stage linear amplifications [4]. The preamplifier latch comparator [5], which combines an amplifier and a latch comparator can be obtained high speed and low power dissipation. The amplifier which is added before the latch can reduce offset voltage to obtain a high resolution. Thus, by considering factors of speed and resolution, preamplifier latch comparator are the choice for a high speed ADC [6]. This type of latched comparator was also used for high speed and low power performance [7]. The offset of this stage is dependent on both the input amplifiers and the latching stage. Input-offset voltage can be a particularly difficult problem in comparator design. In precision applications, such as high-resolution converters, large input-offset voltages cannot be tolerated [8]. While systematic offset can nearly be eliminated with proper design (though still affected by process variations), random offsets still remain and are unpredictable. Fortunately there are techniques in MOS technology to remove a large portion of the input offset using offset-cancellation techniques. These techniques are available in MOS because of the nearly infinite input resistance of MOS transistors. This characteristic allows long-term storage of voltages on the transistor's gate. As a result, offset voltages can be measured, stored on capacitors, and summed with the input so as to cancel the offset [9]. Figure 1 shows the offset-cancellation arrangement for offset voltage measurement.

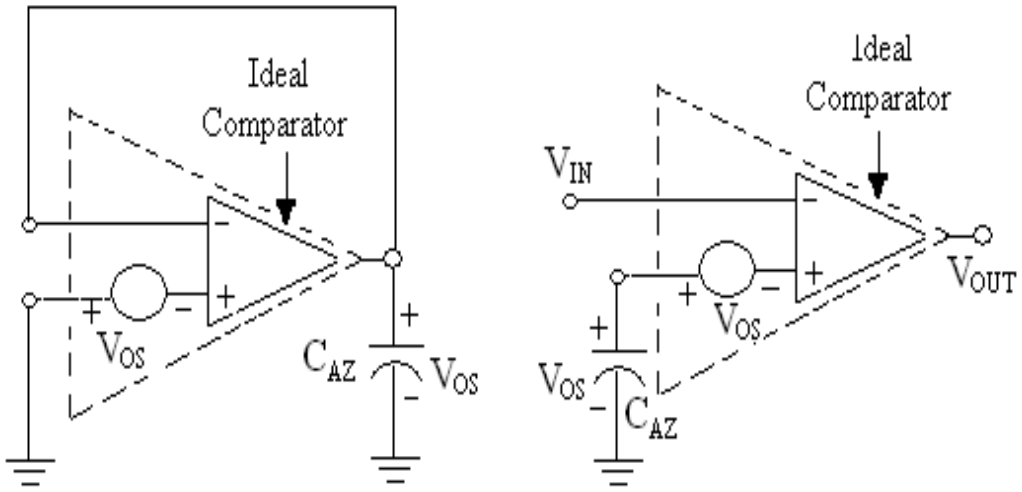

Figure 1: Offset-cancellation arrangement for offset voltage measurement

Thus, the proposed offset cancellation achieves not only low offset voltage but also low Power consumption. Moreover, the proposed circuit topology can improve the comparator noise and reduce the clock driving requirement compared with a conventional comparator.

2. Determination of clock frequency & power dissipation

The clock frequency "*fc*" is defined as the reciprocal of the time interval *T*, as:

$$fc = 1/T \qquad (1)$$

The clock frequency has to be equal or greater than twice of the frequency bandwidth of analog signals [10]. We were primarily considering high speed and low voltage. Dynamic comparator power dissipation resembles that of digital gates, which have a power dissipation given approximately by [11]:

$$p = fcv_{DD}^{2} \qquad (2)$$

Where, f = output frequency,
V_{DD} = supply voltage
C = output capacitance

3. Design of a CMOS comparator

The comparator presented in this paper is made up of the preamplifier –latch circuit schematic view of the design is shown in figure 2. In this design when clk is low, the latch is disabled and difference between the input and reference is amplified by the front-end amplifier. If clk is goes high, the amplifier is disabled and the latch is being to amplify the difference established at its input to generate logic levels at the output. Preamplifier consists of two different inputs, which are made up of NM0, NM6, NM7 and NM5. PM2, PM3, connect crossways in order to turn into positive feedback and also increase the plus of preamplifier. NM9, NM1, NM4, PM14 are considered as switches. The flow of circuit operating: when clock (Clk) is low, the latch comparator is reset, and at this time Clk1 is high, latch-comparator can receive the amplified signal of preamplifier.

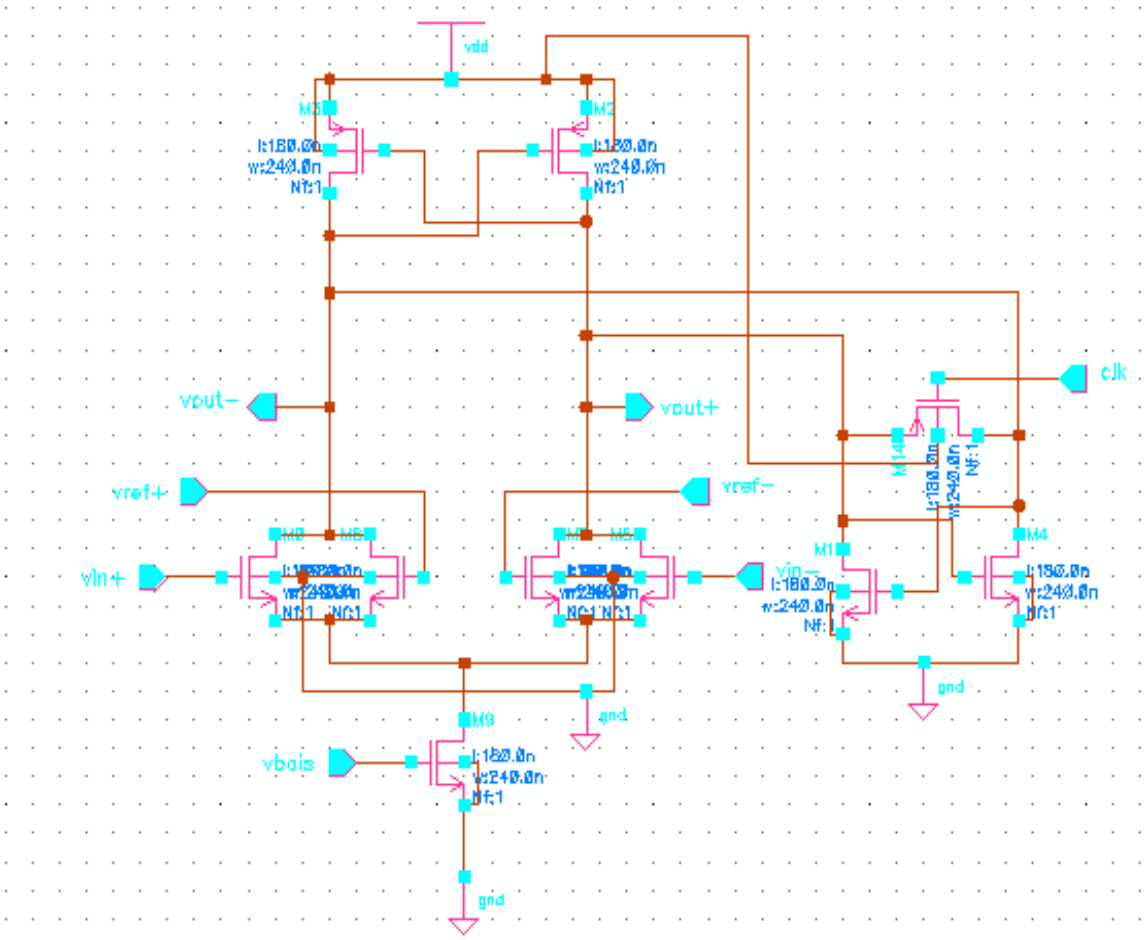

Figure 2: Schematic view of preamplifier-latch comparator

4. Simulation results

Simulation of reported design has been done using the 0.18 µm CMOS technology under the 2V power supply by Cadence spectre. Comparator able to work at the high clock frequency as 100MHz and clock period was 10ns can be used where Low power, high speed and Low offset voltage is the main requirements and it is very much useful for ADC designer. Finally simulation results of the comparator are shown in Figure 3. In addition we are also presenting the results of offset voltage given in Figure 4 and 5 respectively. Table 1 has given the comparison of present work with earlier reported work and got improvement in these design parameters.

Table 1: Comparison of present results with earlier Reported work

Parameters	Ref.[12]	Ref.[13]	This work
Power supply	5V	2V	2V
Clock frequency	100 MHz	10 MHz	100 MHz
Offset voltage	6.5 mV	300µV	280.7 nV
Power Dissipation	0.49 mW	1.8mW	0.27 mW
Technology	0.35µm	1µm	0.18µm

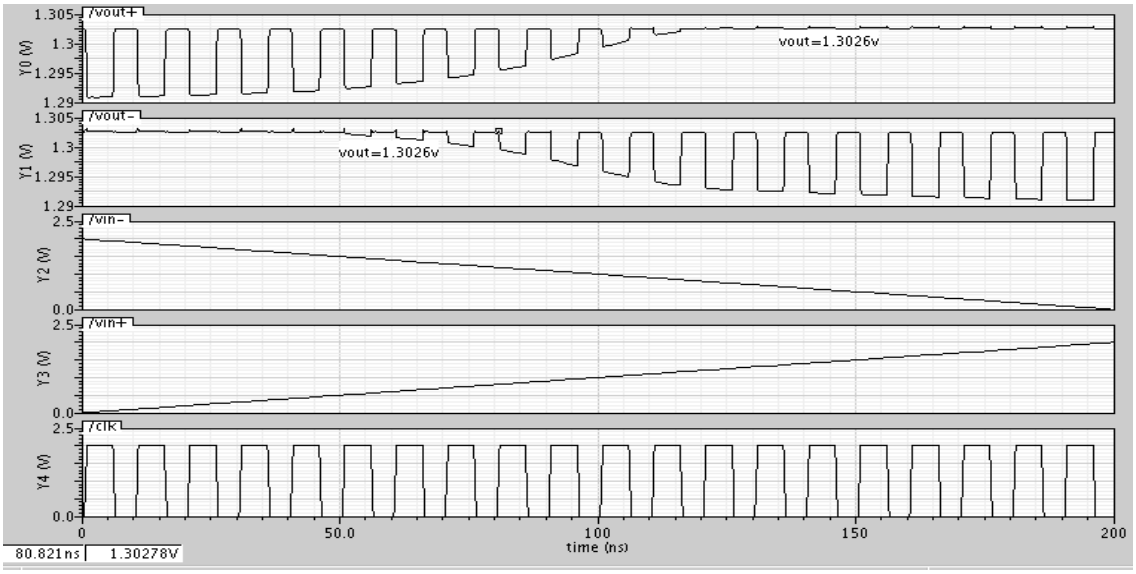

Figure 3: Simulation results of comparator

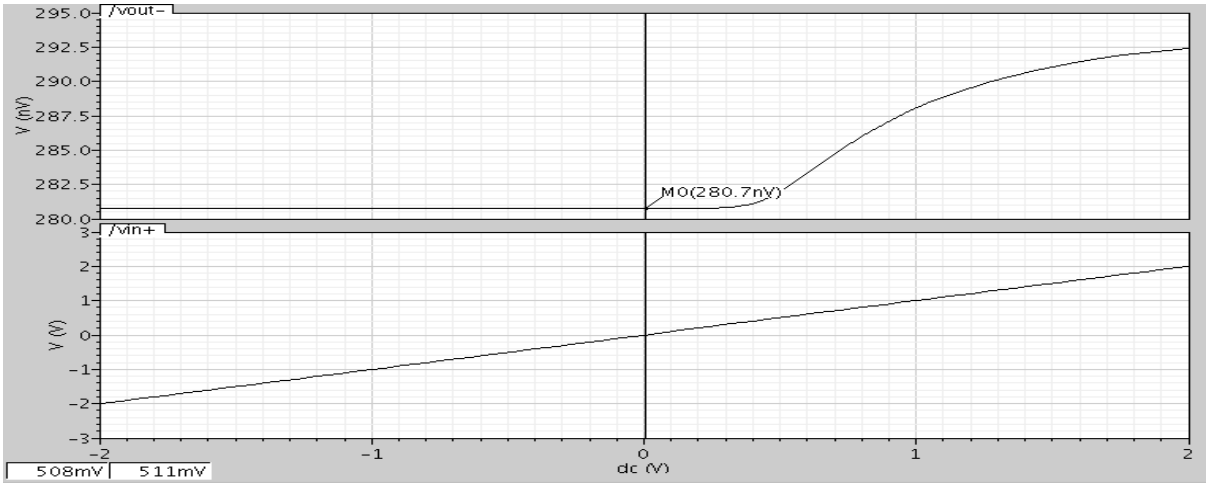

Figure 4: Simulation results of offset voltage

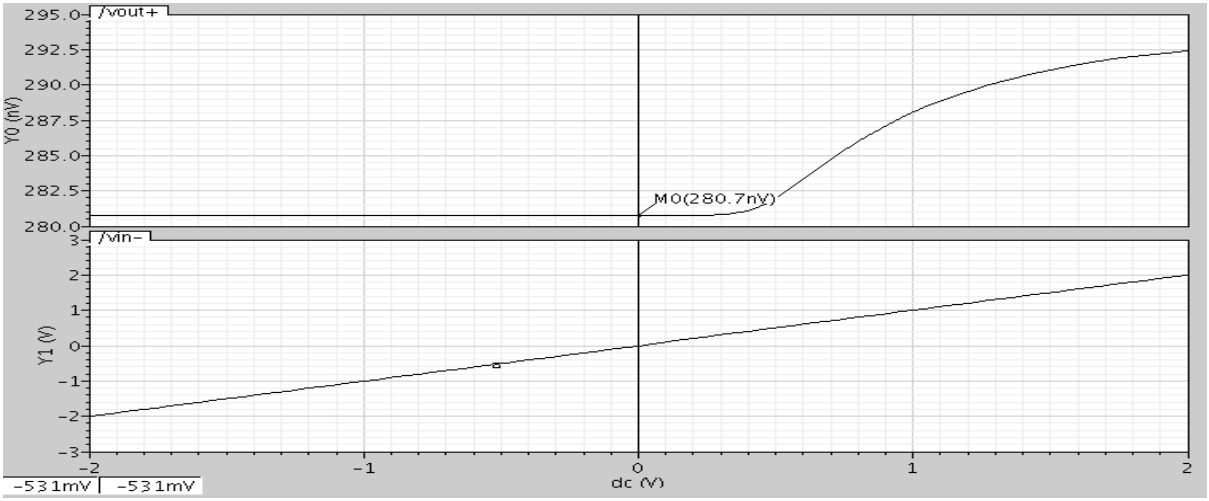

Figure 5: Simulation results of offset voltage

5. Conclusion

The comparator is designed and simulated cadence spectre in 0.18µm UMC Technology. Simulation results show that the circuit can work under as high clock frequency as 100MHz and its maximum offset voltage is about 280.7 nV. During the amplification stage drain current as 139µA. In this design we compare our results and observed that present results have improvement as shown in table 1. This design will be very beneficial for ADC designer, young researcher and manufacturer.

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