

# Chapter 1

## Fundamentals of

## Analog/Mixed-Signal Electronics



## Outline

- Integrated resistors
- Integrated capacitors
- Integrated MOS transistors
- Operational amplifiers
- Noise

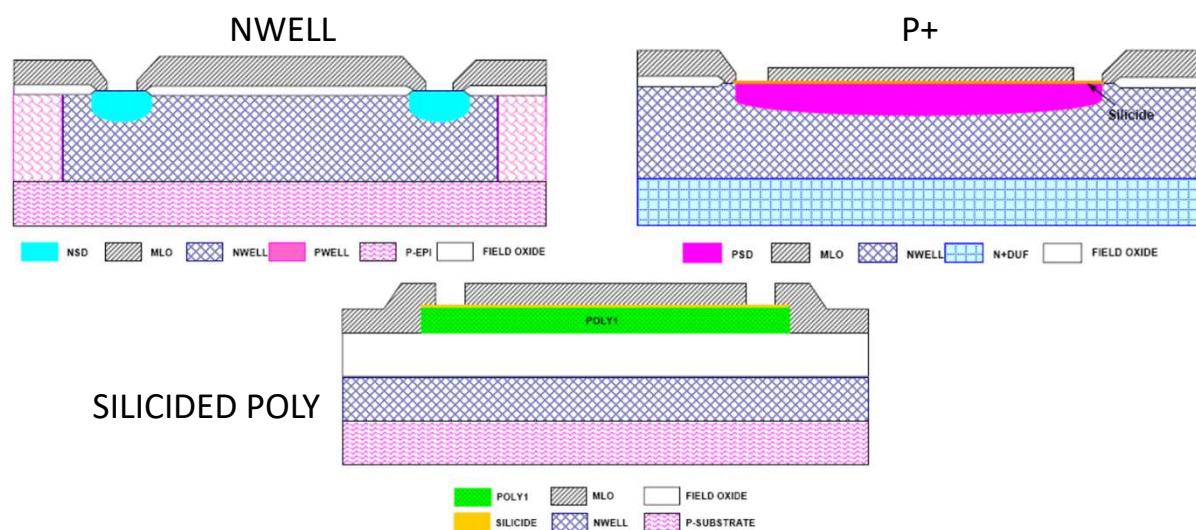


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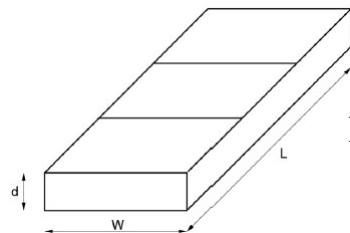
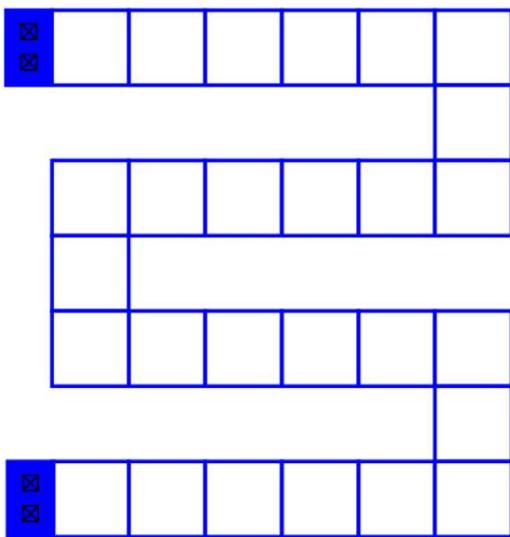
3

# MOS Technology Resistors



4

## Sheet Resistance

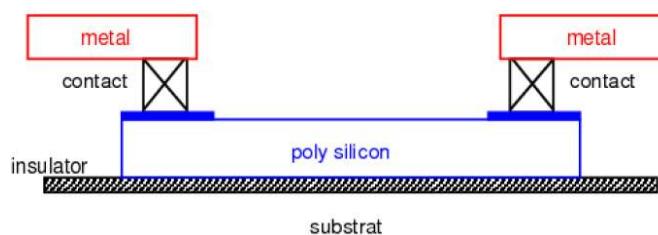


$$R = \rho \frac{L}{Wd} = R_{\square} \frac{L}{W}$$

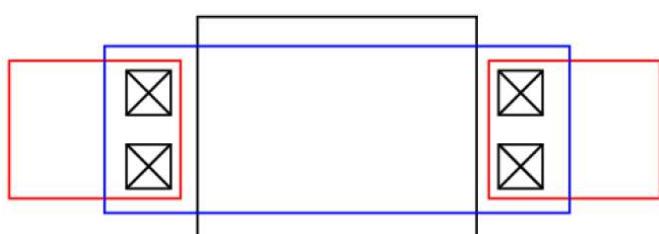
Sheet resistance:

- poly-Si:  $5-30 \Omega/\square$
  - diffusion (n+ or p+):  $30-100 \Omega/\square$
  - n-well:  $1-4 k\Omega/\square$
  - metal:  $30-50 m\Omega/\square$
- area intensive → expensive

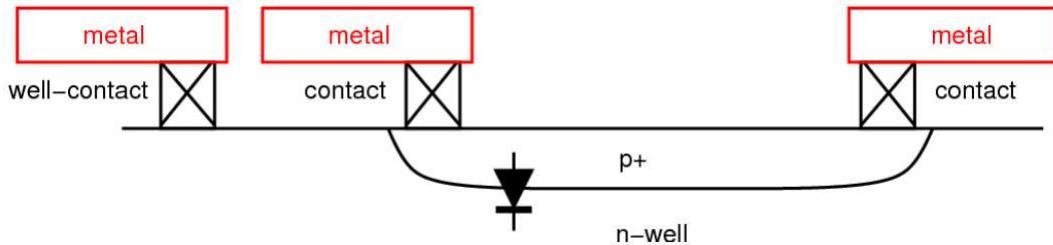
## Poly-Si Resistor



- Sheet resistance:  $5-30 \Omega/\square$
- High variability (up to +/-30%)
- Good linearity
- Isolated from substrate



## Diffusion Resistor



- Sheet resistance:  $30\text{-}100 \Omega/\square$
- High variability (up to  $\pm 30\%$ )
- Parasitic diode
- High parasitic capacitances

7



## Resistor Non-Idealities

- Voltage coefficient  
→ non-linearity
- Absolute value variation due to process and temperature  
→ important for: oscillators, filter time constants, bias current generators
- Matching – ratio variation
  - systematic (metal, contacts, vias...)
  - gradients on the wafer
  - random between devices (lithography)
  - important for: opamp feedback ratios, resistive DACs, voltage references
- In digital CMOS, available only :
  - silicided poly
  - n+/p+
  - nwell

Up to  $\pm 30\%$   
Can't control.

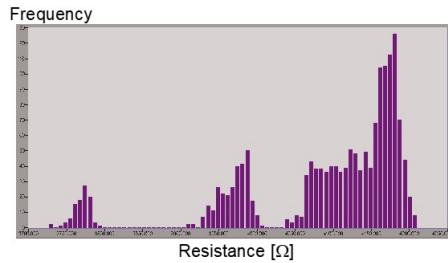
2% or better!  
Can be improved by 10x or more by  
large area and good layout techniques.



8

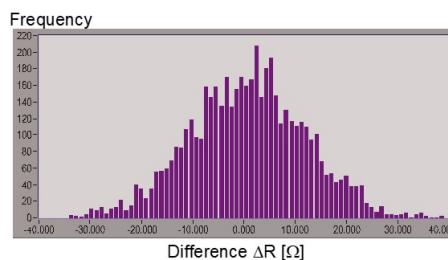
## Resistor Mismatch

Wafer related distribution of measured  $R$  values of high-ohmic poly-Si resistors



**Systematic mismatch**  
→ improved by:  
careful layout (metal,  
via, force/sense  
considerations)

Wafer related distribution of measured  $\Delta R$  values of high-ohmic poly-Si resistors

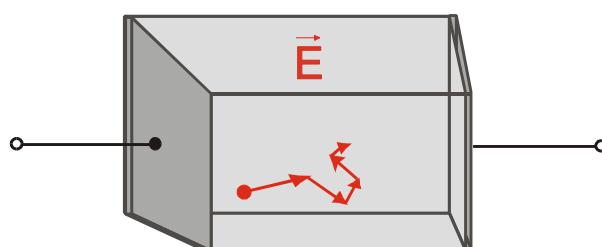


**Random mismatch**  
→ improved by:  
- more area  
- better layout

$$\frac{\Delta R}{R} = r * \frac{1}{\sqrt{L * W}}$$

9

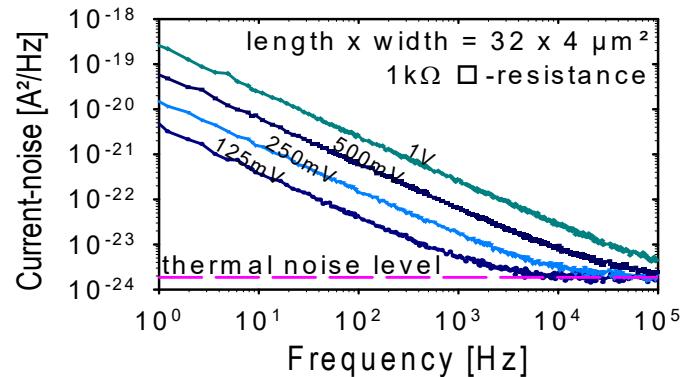
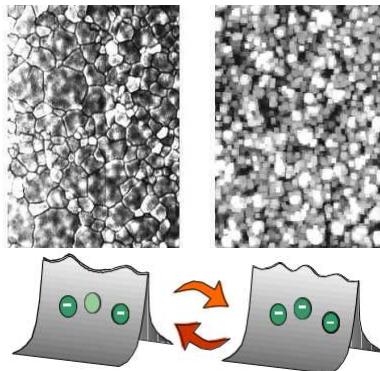
## Thermal Noise in Resistors



- Thermal noise arises from the random thermal motion of the carriers in addition to the drift in the field.
- The contribution of a carrier to the total noise at a certain location in the device is proportional to the conductance in that region:

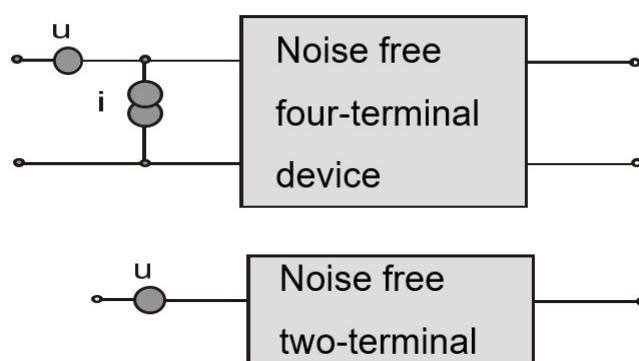
$$v^2 = 4kT \cdot \Delta f \cdot \int_0^L dr = 4kT \cdot R \cdot \Delta f$$

## Noise Spectrum of a Poly-Si Resistor



- At higher frequencies thermal noise dominates in resistors.
- At low frequencies and high currents, 1/f-noise is present in practical CMOS resistors as well (e.g. due to carrier trapping effects at grain boundaries).

## Noise in Devices



- A noisy device can always be treated as an ideal device with external noise sources.
- ... same for mismatch

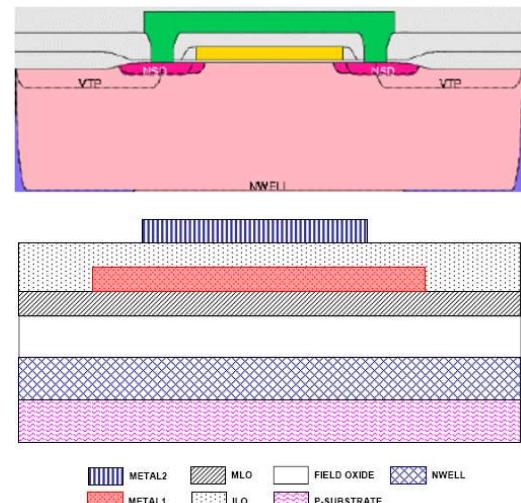
# Outline

- Integrated resistors
- **Integrated capacitors**
- Integrated MOS transistors
- Operational amplifiers
- Noise

13

# Integrated Capacitors

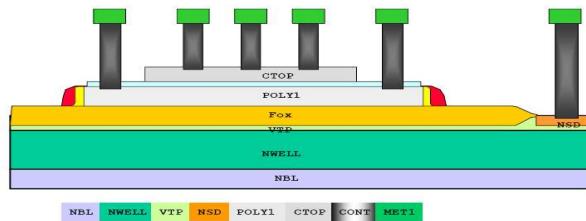
- MOS gate capacitor:
  - large capacitance density
  - highly non-linear
  - large variability
  - large parasitics
- Metal-metal capacitor:
  - low capacitance density
  - linear
  - lateral comparable to vertical
  - large parasitics



14

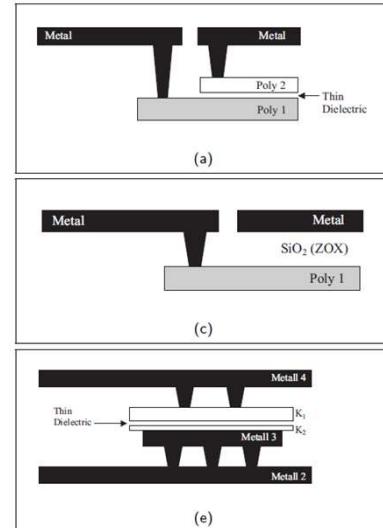
# Integrated Capacitors

- Poly-poly and other capacitors:
  - good density
  - linear
  - good matching
  - additional masks/process steps



High density → opamp compensation, bypass

High accuracy → feedback, sampling, ADCs, filters



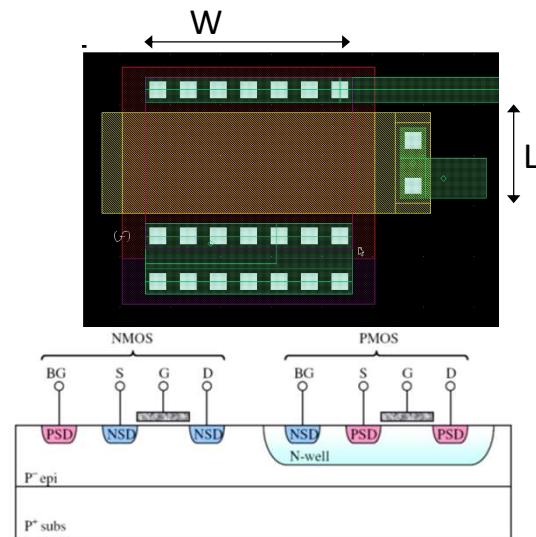
15

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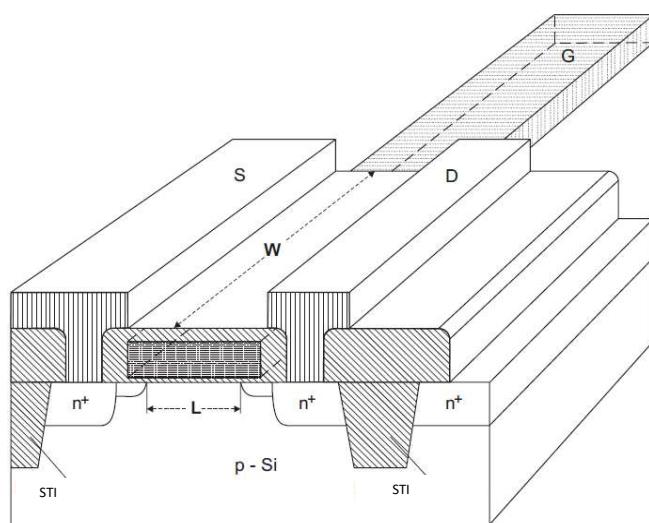
## MOS Transistors

- NSD/PSD – n/p source-drain implant (high doping)
- Transistor length “L” – poly-Si gate between drain and source
- Transistor width “W” – stretch of thin oxide under the gate along source and drain
- $V_{TH}$  – MOS threshold voltage



17

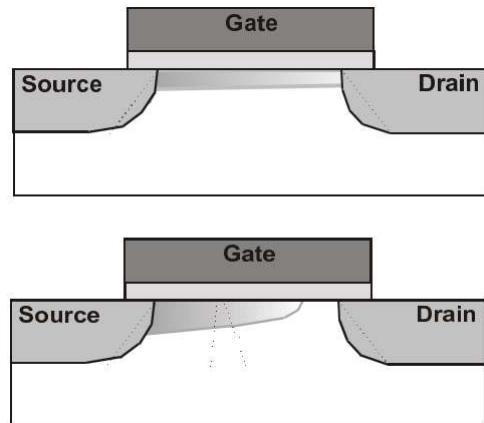
## NMOS Transistor 3D View



18

## MOS Operating Regions

- Triode/ohmic/linear region:
  - A flat inversion layer forms in the channel – carriers are free to flow from drain to source.
  - Transistor behaves as a (voltage controlled) resistor at very low  $V_{DS}$ .
- Saturation region:
  - It is entered when pinch-off region appears.
  - The channel is not fully formed and in a small drift /saturation/pinch-off region carriers are passing at maximum speed.
  - In reality, the current increases slightly with  $V_{DS}$  – finite output resistance.

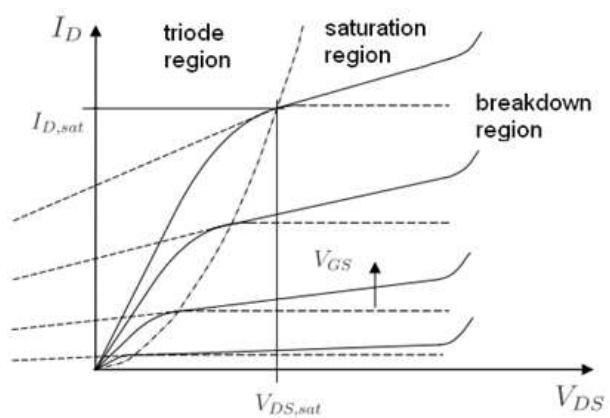


19

## MOS I-V Curves

Strong inversion:  $V_{GS} > V_{TH}$

- Triode/ohmic/linear region:  
 $V_{DS} < V_{GS} - V_{TH}$   
 $I_D \cong \mu C_{ox} \frac{W}{L} \left( V_{GS} - V_{TH} - \frac{V_{DS}}{2} \right) V_{DS}$
- Saturation region  
 $V_{DS} > V_{GS} - V_{TH}$   
 $I_D \cong \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2$
- $K = \mu C_{ox}$  → technology dependent



20

## MOS I-V Curves

- Strong inversion:

$$V_{GS} > V_{TH}, V_{DS} > V_{GS} - V_{TH}$$

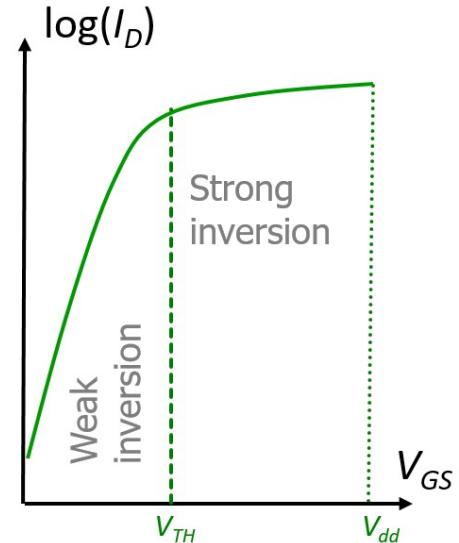
$$I_D \cong \frac{1}{2} K \frac{W}{L} (V_{GS} - V_{TH})^2$$

- Weak inversion

$$V_{GS} < V_{TH}, V_{DS} > 4k_B T/q$$

$$I_D \cong K_w \frac{W}{L} \exp\left(\frac{V_{GS} - V_{TH}}{nk_B T/q}\right)$$

- $n, K_w \rightarrow$  technology dependent
- current due to diffusion rather than drift
- current gain exponential near the threshold voltage



21

## MOSFET Transconductance ( $g_m$ )

- Key small-signal parameter for transistors.
- Measures a change of drain current for a given change of  $V_{GS}$ .
- Determines the amplification properties (in saturation).
- In strong inversion:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \Big|_{V_{DS}=\text{const.}} \quad I_D \cong \frac{1}{2} \beta (V_{GS} - V_{TH})^2, \quad \beta = \mu C_{ox} \frac{W}{L}$$

$$= \beta (V_{GS} - V_{TH}) = \sqrt{2\beta I_D} = \frac{2I_D}{V_{GS} - V_{TH}}$$

22

## MOSFET On-Resistance ( $R_{\text{out}}$ )

- Linear region:

$$I_D \cong \beta \left( V_{GS} - V_{TH} - \frac{V_{DS}}{2} \right) V_{DS}, \quad \beta = \mu C_{\text{ox}} \frac{W}{L}$$

small  $V_{DS}$ :  $I_D \cong \beta(V_{GS} - V_{TH})V_{DS}$

- Output conductance:

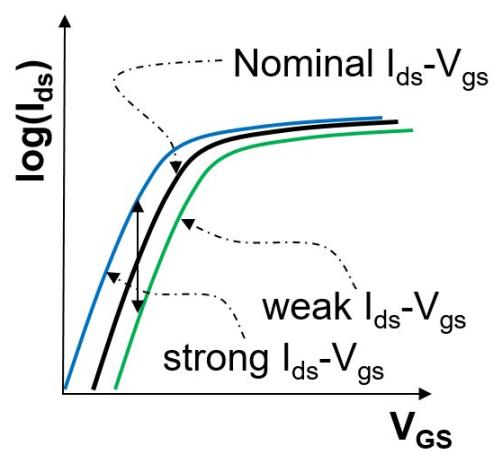
$$g_{\text{out}} = \frac{1}{R_{\text{out}}} = \frac{\partial I_D}{\partial V_{DS}} \Big|_{V_{GS}=\text{const.}} \cong \beta(V_{GS} - V_{TH})$$

→ voltage-controlled resistance

23

## Technology Manufacturing Variability

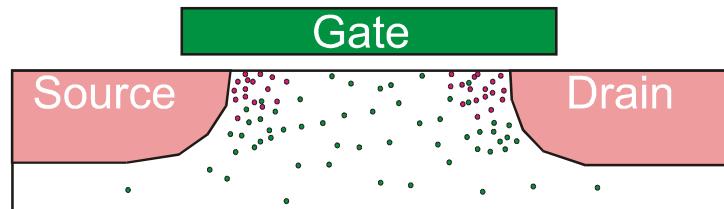
- Inaccuracies in the manufacturing process are unavoidable  
→ performance gradients for all devices
- E.g., threshold voltage variability



24

## Local Variability in MOS Technology

- On top of manufacturing tolerances, there are statistical reasons for  $V_{TH}$  fluctuations in MOS devices.



- Mismatch in long channel devices is mainly determined by the dopant fluctuations and is estimated by the following formula:

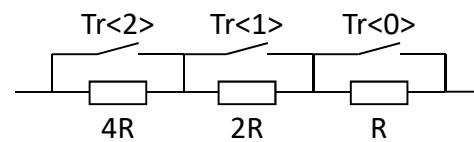
$$\sigma_{Vt} \propto t_{ox, el} \cdot \sqrt[4]{N_{dop}} \cdot \frac{1}{\sqrt{WL}}$$

→ scales with  $\text{sqrt(area)}$

25

## Trimming

- Static technique for variability mitigation
- Adjustment of one or more on-chip component(s) (resistor, capacitor, transistor) through digital encoding  
→ trimming DAC (digital-to-analog converter)
- Performed during production, once per component per chip
- Requires
  - test equipment (to measure)
  - on-chip memory (to store trim code)

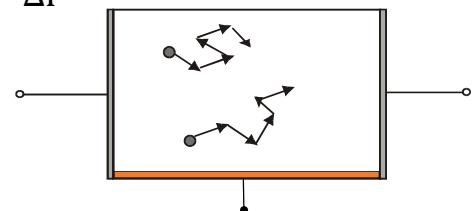


26

## Thermal Noise of a MOSFET

- The contribution of a carrier to the total noise at a certain location in the device is proportional to the conductance in that region:

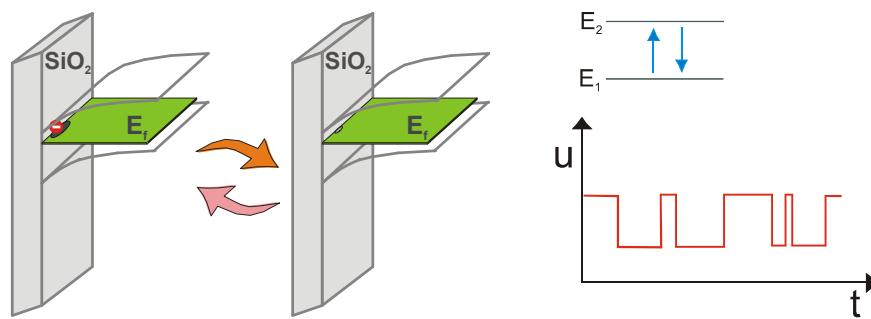
$$i_{ds}^2 = 4kT \cdot \Delta f \cdot \int_0^L dg = 4kT \cdot g_m \cdot f(V_{gs}, V_{ds}) \cdot \Delta f$$



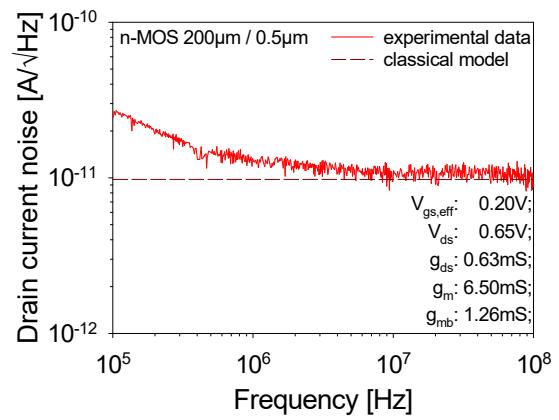
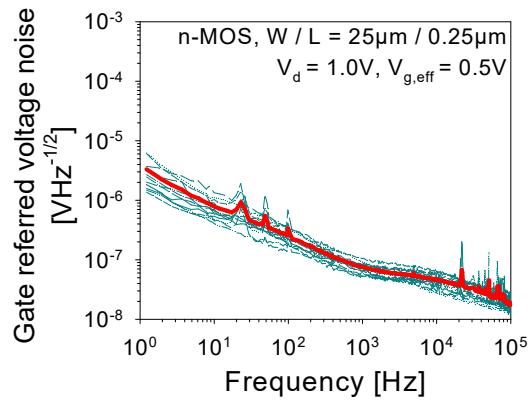
- The noise magnitude is frequency dependent since the number of carriers participating at the current transport is a function of time.
- In non-linear regimes there is a noise modification factor  $f(V_{gs}, V_{ds})$ , e.g.  $\sim 2/3$  in saturation region (often higher for advanced technology nodes).

## Flicker Noise (1/f Noise) of a MOSFET

- Traps at the Si/SiO<sub>2</sub> boundary frequently capture and re-emit free carriers. They modify current transport through the MOSFET channel both by number and mobility fluctuation.
- Only traps close to the Fermi level significantly contribute to fluctuations in current of the MOSFET surface channel.



## MOSFET Noise Spectrum



- Low frequency: flicker (1/f) noise dominates
- High frequency: thermal noise dominates

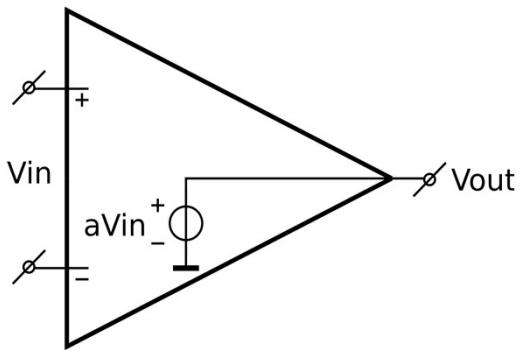
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# The Ideal Operational Amplifier

Key properties:

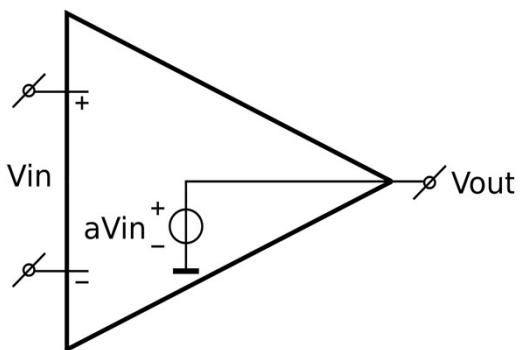
1. Input terminals have infinite impedance  
(no current into pin)
2. Infinite gain from  $V_{in}$  to  $V_{out}$   
→ equal input voltages  
in feedback configurations
3.  $V_{out}$  is an ideal voltage source  
(zero output impedance)



# The Ideal Operational Amplifier

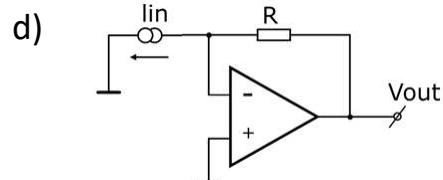
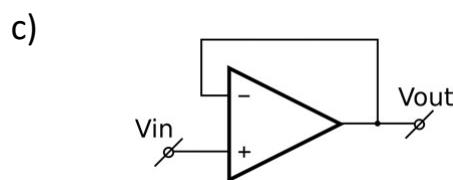
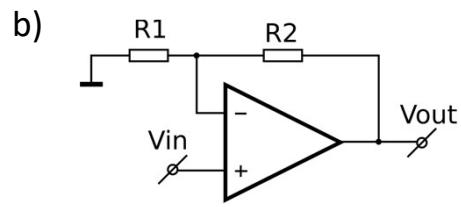
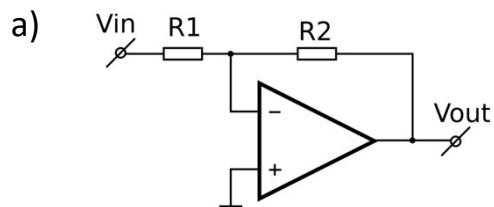
Further properties:

4. Zero offset
5. Infinite common-mode rejection
6. Infinite power-supply rejection
7. Infinite bandwidth
8. Rail-to-rail common-mode input range
9. Rail-to-rail output range

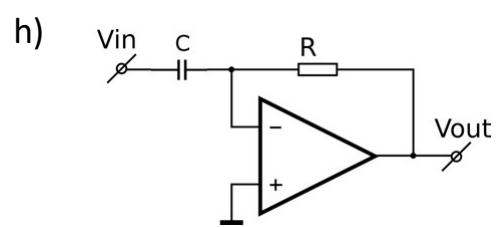
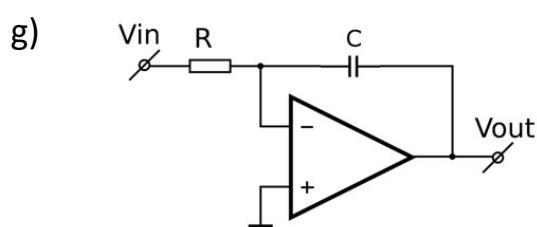
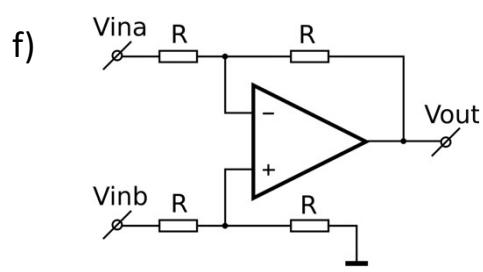
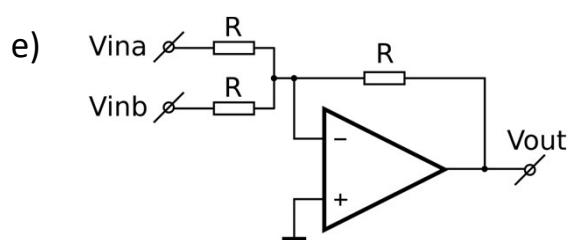


## Exercise 1

Consider the following opamp feedback configurations. For each of them, express the output voltage in dependence of the input voltage(s) and specify the function of the circuit.

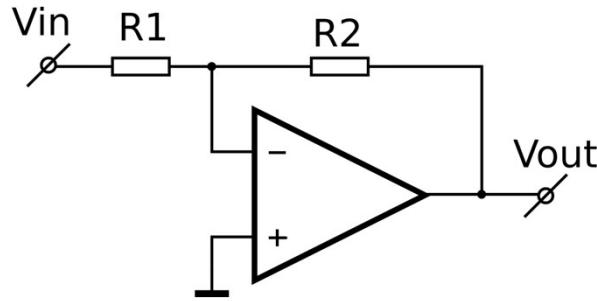


## Exercise 1



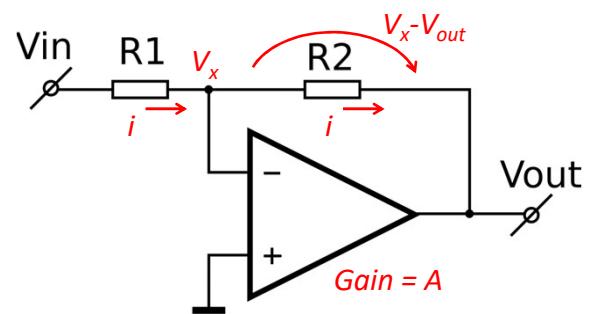
## Exercise 2

Consider an inverting opamp configuration. The opamp has a finite gain A. Calculate  $V_{out}$  in dependence of  $V_{in}$ ,  $R_1$ ,  $R_2$  and A.



35

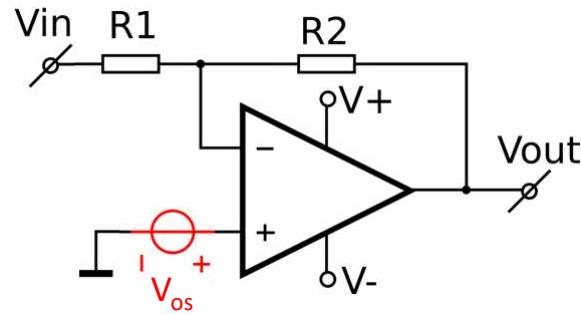
## Exercise 2 – Solution



36

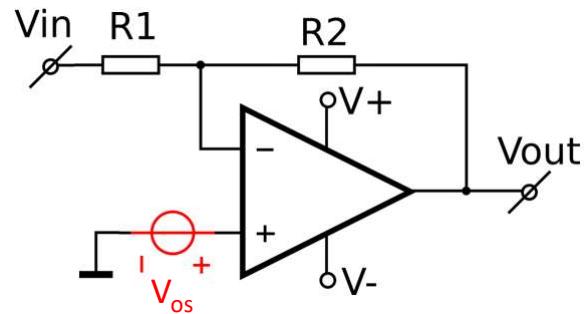
## Exercise 3

Consider an inverting opamp configuration. The opamp has infinite gain and an offset  $V_{os}$ . Calculate  $V_{out}$  in dependence of  $V_{in}$ ,  $R_1$ ,  $R_2$  and  $V_{os}$ .



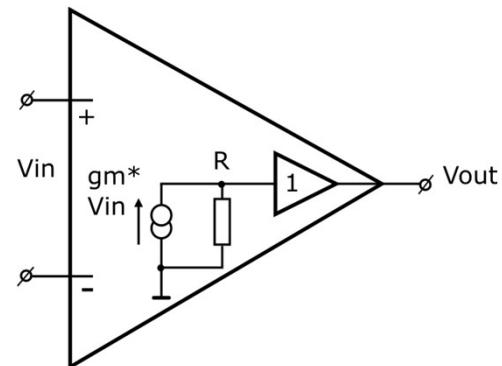
## Exercise 3 – Solution

superposition:



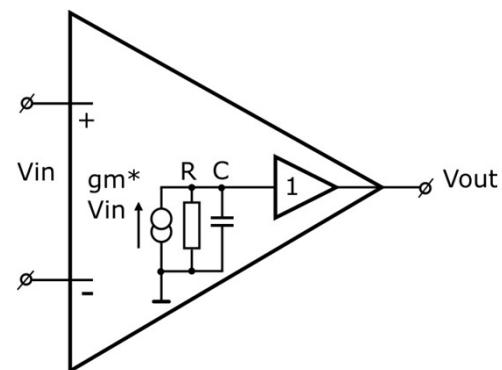
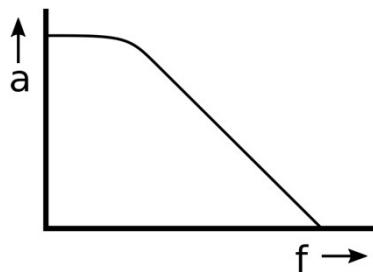
## Opamp Gain – DC Model

- Simplest model of a real opamp
- Only DC gain modeled
- Input voltage  $V_{in}$  → current  $g_m V_{in}$   
→ current flows into R  
→ output voltage  $V_{out} = g_m R V_{in}$   
→ gain  $A = g_m R$
- Ideal output buffer
- Infinite bandwidth → not realistic



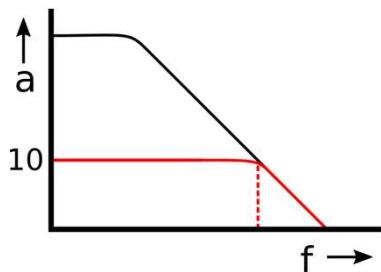
## Opamp Open-Loop Gain – AC Model

- Capacitor added to model AC behavior
- DC gain still  $A = g_m R$
- Gain roll-off vs. frequency
- First-order filter → -20dB/dec



## Open-Loop and Closed-Loop Gain

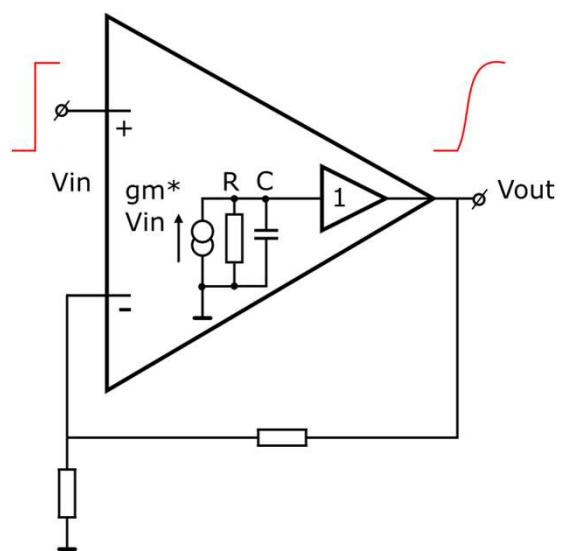
- Loop gain equation:  $A \left( \frac{R_1}{R_1+R_2} \right) \gg 1$
- If closed-loop gain is 10  
→ open-loop gain needs to be  $>10$  for feedback to work
- At the frequency where open-loop gain drops to 10, feedback can no longer set closed-loop gain → bandwidth limit



41

## Opamp Slew Rate

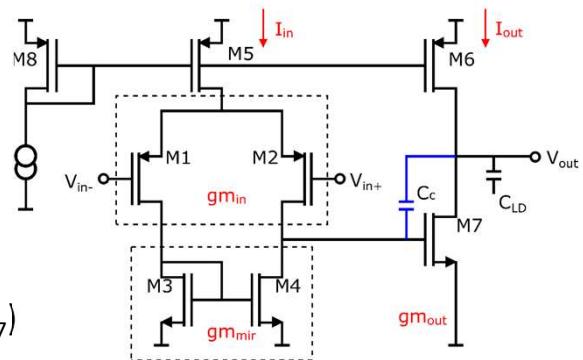
- Large input step applied
- Model predicts current  $g_m V_{in}$  to charge capacitor  $C$
- In practice: upper limit on current  
→ limited current to charge  $C$   
→ upper limit on  $dV_{out}/dt$   
→ opamp slew rate



42

## Basic Topology – Limitations

- Basic topology: two-stage opamp with Miller compensation
- Common mode limit to positive supply  
 $V_{IN,CM} < V_{DD} - V_{DSAT} - V_{GS}$
- Common mode limit to negative supply  
 $V_{IN,CM} > V_{SS} + V_{DSAT}$
- Output current capability  
 $I_{out}$
- Limited common mode rejection  
 (because of finite  $r_{ds5}$ )
- Limited open-loop gain  
 (because of finite  $r_{ds2} || r_{ds4}$  and  $r_{ds6} || r_{ds7}$ )



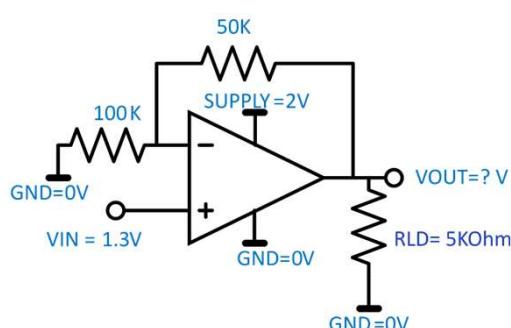
43



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## Exercise 4

- a) Consider a non-inverting opamp configuration.  
 Calculate the closed-loop gain A and the output voltage  $V_{OUT}$ .



44



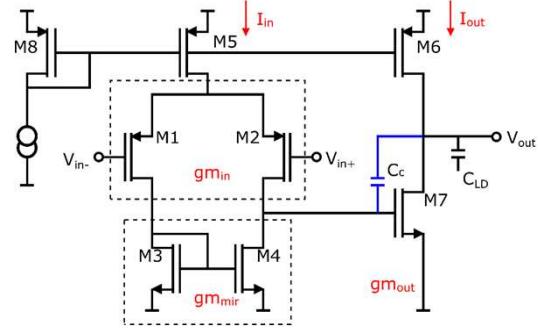
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## Exercise 4

- b) Consider the transistor-level opamp implementation. Identify 3 limitations because of which the previous configuration doesn't work as intended.

Assume that:

- all transistors have  $|V_{GS}|=0.7$  and  $|V_{DSAT}|=0.2V$
- the currents are  $I_{in}=20\mu A$ ,  $I_{out}=200\mu A$
- the load resistance is  $R_{LD}=5k\Omega$



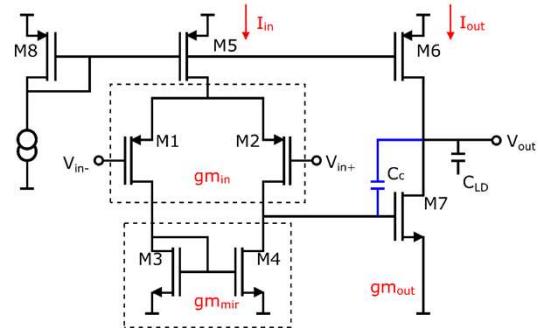
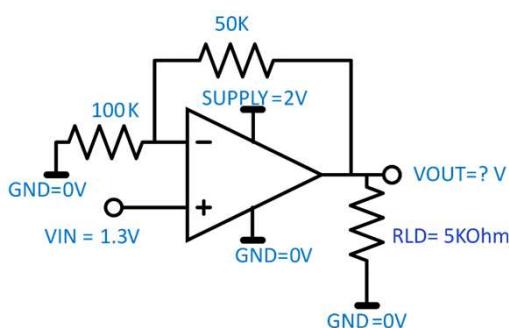
45



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## Exercise 4 – Solution

b)



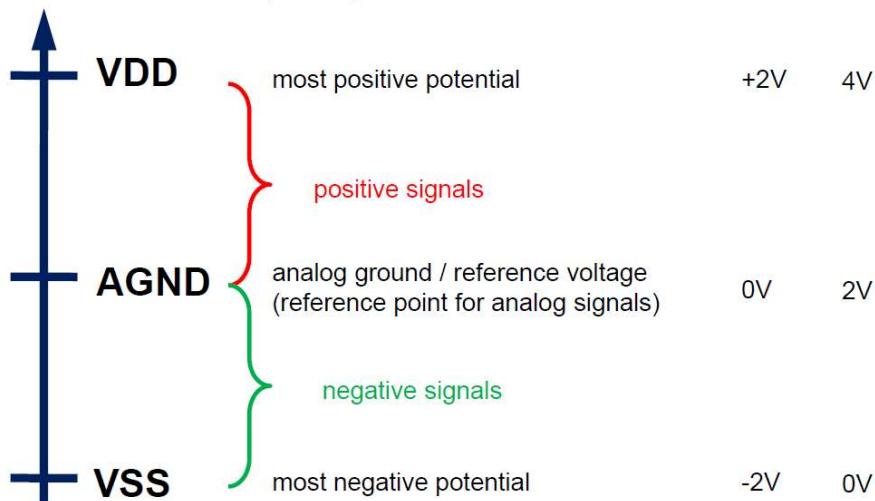
46



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# Supply Voltages of Mixed-Signal Circuits

General case: use of bipolar signals



47



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## Outline

- Integrated resistors
- Integrated capacitors
- Integrated MOS transistors
- Operational amplifiers
- Noise

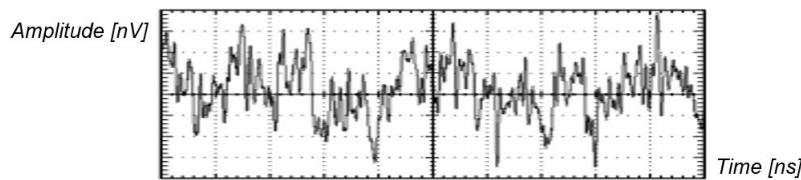
48



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## Noise

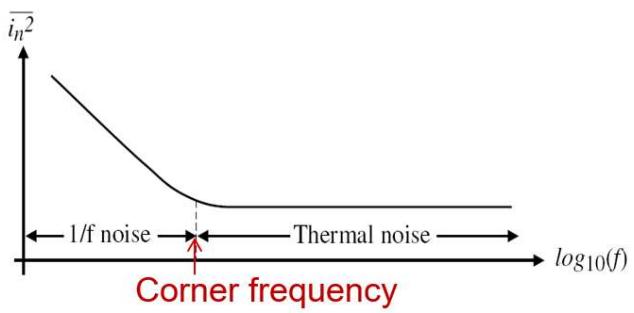
- Noise is a random process/signal, meaning one cannot predict exact future signal values from past values.
- In electronics, inherent noise means random processes caused by undesired physical mechanism, not deterministic signals caused by crosstalk, interference, etc.  
→ Noise is always unwanted, but not all unwanted signals are noise.
- Inherent noise can be significantly reduced through proper circuit design, such as device size, power levels, circuit topology and process choice.



49

## Noise Types

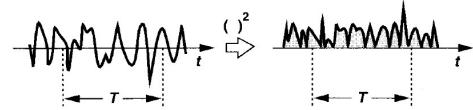
- Noise limits achievable resolution.
- Noise can be averaged out by multiple (longer) measurements  
→ oversampling → noise power  $\sim 1/N_{\text{samples}}$
- Flicker noise: increases in magnitude with lowering frequency  
→ dominates at low frequency
- Thermal noise: constant magnitude with frequency  
→ dominates at high frequency



50

## Quantifying Noise

- Noise is random in nature.  
→ Its instantaneous value can't be predicted.  
→ Statistics can be used to quantify it.



- Root mean square (rms):

$$V_{n(\text{rms})} = \sqrt{\frac{1}{T} \int_0^T v_n^2(t) dt} \quad I_{n(\text{rms})} = \sqrt{\frac{1}{T} \int_0^T i_n^2(t) dt}$$

- Normalized (to a  $1\Omega$  resistor) noise power of a signal:

$$P_v = \frac{V_{n(\text{rms})}^2}{1\Omega} = V_{n(\text{rms})}^2$$

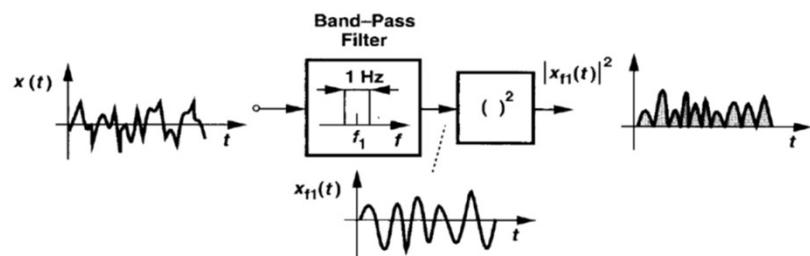
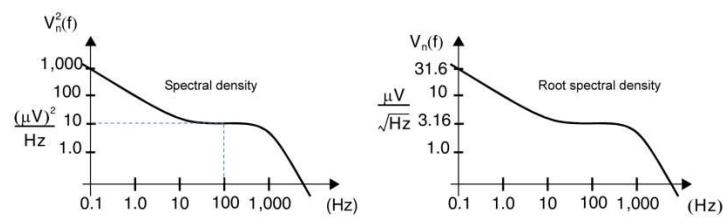
- Signal-to-noise ratio (SNR) → sets lower limit for detectable signals

$$\text{SNR[dB]} = 10 \log \left[ \frac{\text{signal power}}{\text{noise power}} \right] = 20 \log \left[ \frac{V_x(\text{rms})}{V_n(\text{rms})} \right]$$

51

## Noise Power Spectral Density (PSD)

- To calculate noise power, integrate PSD over frequency  
→  $V_n^2 = \int_0^\infty v_n^2(f) df$
- Noise can be filtered  
→ noise power reduced

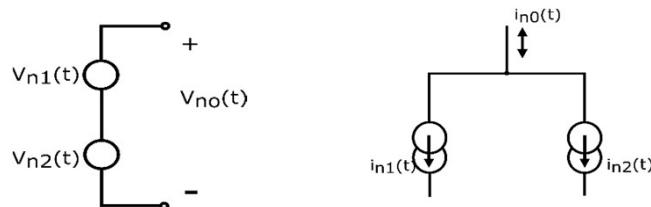


52

## Quantifying Noise

- Noise power:  $V_{n(\text{rms})}^2 [\text{V}^2]$
- Noise voltage:  $V_{n(\text{rms})} [\text{V}]$
- Noise power spectral density:  $\overline{v_n^2}(f) [\text{V}^2/\text{Hz}]$
- Noise voltage spectral density:  $\overline{v_n}(f) [\text{V}/\sqrt{\text{Hz}}]$
- With ideal filter:  $V_{n(\text{rms})}^2 = \int_{f_{\min}}^{f_{\max}} \overline{v_n^2}(f) df$
- **Attention:** when integrating noise density over a bandwidth to calculate total noise, need to use **power spectral density**, not voltage spectral density!

## Additive Noise



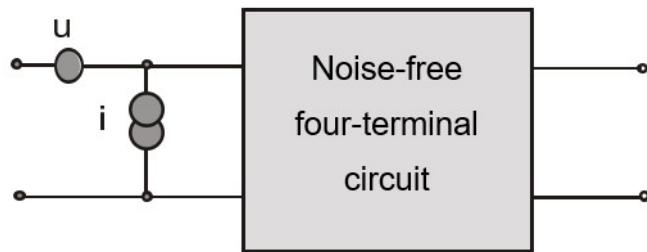
- In case of two uncorrelated signals (as most inherent noise sources in an amplifier):

$$V_{n,\text{total}(\text{rms})} = \sqrt{V_{n1(\text{rms})}^2 + V_{n2(\text{rms})}^2}$$

→ Importance of smaller number quickly vanishes!

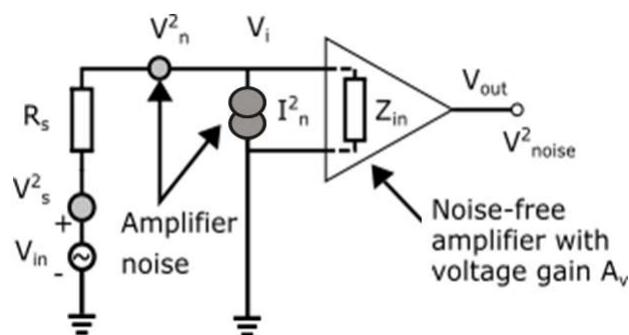
## Noise in Circuits

- A noisy circuit can always be treated as an ideal circuit with external noise sources



## Noise – Amplifier Representation

- For noise analysis combine voltage and current noise contributors into input referred voltage and current noise source.



## Exercise 5

Calculate the thermal noise voltage of a  $1\text{k}\Omega$  resistor in the frequency band between 1Hz and 1kHz.

Boltzmann constant:  $k = 1.38 \cdot 10^{-23}$  [International System units]

Temperature:  $T = 300\text{K}$

## Exercise 6

Consider the following simulated noise power spectral density of a system.

The power spectral density of the  $1/f$  noise is described as:

$$\overline{v_n^2} = K' \frac{1}{f}$$

- a) Calculate the noise power and the noise voltage in the band of interest.

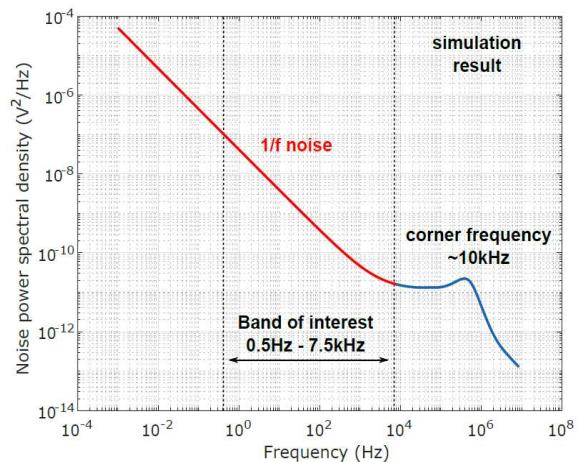


Figure: U. Nurmetov et al., A CMOS Temperature Stabilized 2-Dimensional Mechanical Stress Sensor with 11-bit Resolution, IEEE JSSC, 2020

## Exercise 6 – Solution

a)

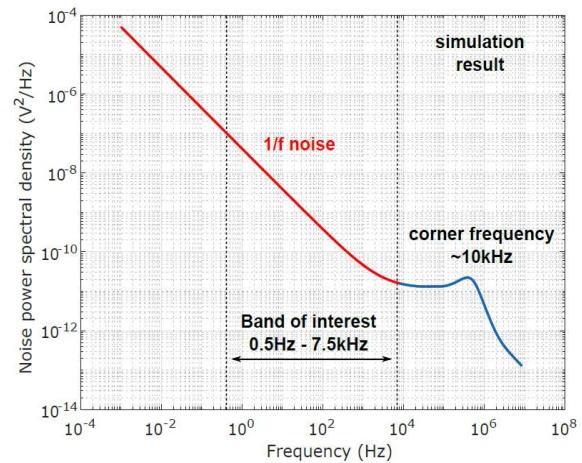


Figure: U. Nurmetov et al., A CMOS Temperature Stabilized 2-Dimensional Mechanical Stress Sensor with 11-bit Resolution, IEEE JSSC, 2020



## Exercise 6

- b) The output is sampled at a rate  $f_s = 15.3\text{kHz}$  and  $N_{\text{samples}} = 30720$  are averaged (oversampling for noise reduction).  
Before sampling, the output (together with the noise) is low-pass filtered for the Nyquist condition to be fulfilled.  
Calculate the noise power and the noise voltage.  
Compare to the previous values.



## Exercise 6 – Solution

b)

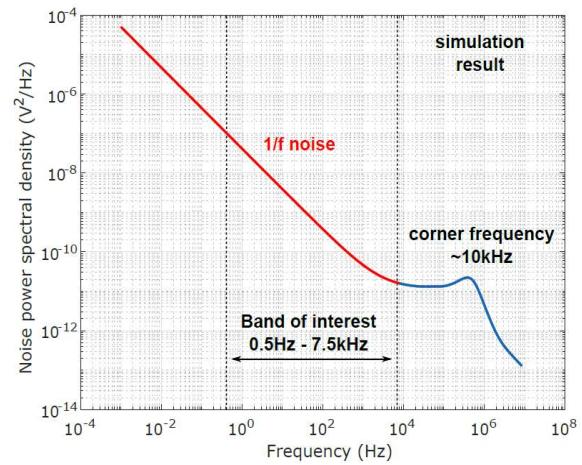
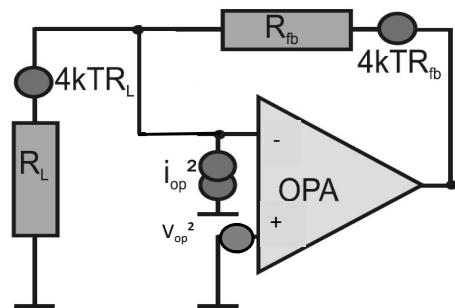


Figure: U. Nurmetov et al., A CMOS Temperature Stabilized 2-Dimensional Mechanical Stress Sensor with 11-bit Resolution, IEEE JSSC, 2020



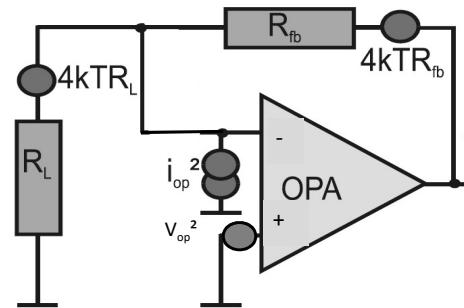
## Exercise 7

Calculate the noise power at the output of the opamp.



## Exercise 7 – Solution

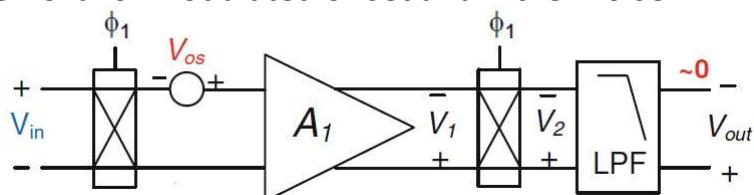
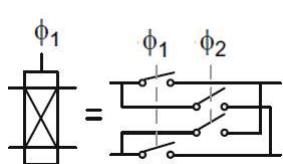
*Superposition:*



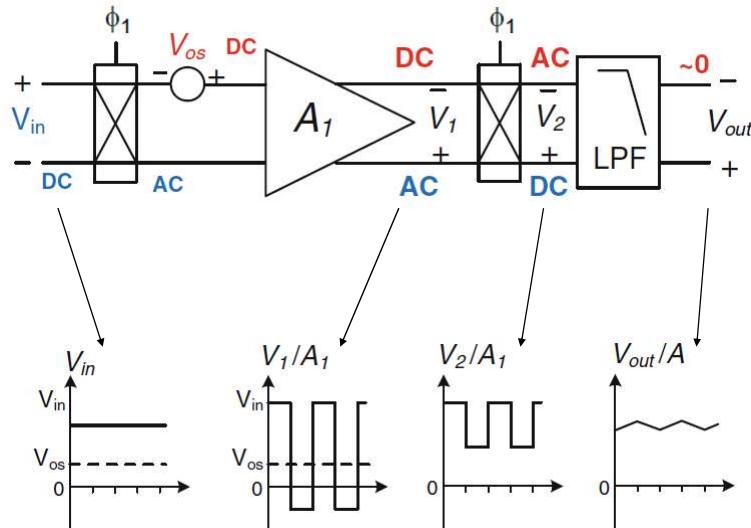
$$A = \left( 1 + \frac{R_{fb}}{R_L} \right)$$

## Chopping

- Dynamic technique for offset cancellation and flicker noise reduction
- Continuous-time technique → input/output signal continuously available
- Input signal modulated and then demodulated
- Offset and flicker noise modulated away from DC, then filtered out
- $\Phi_1$ :  $V_{os}$  added to  $V_{in}$   
 $\Phi_2$ :  $V_{os}$  subtracted from  $V_{in}$   
 Averaging through LPF → removal of modulated offset and flicker noise

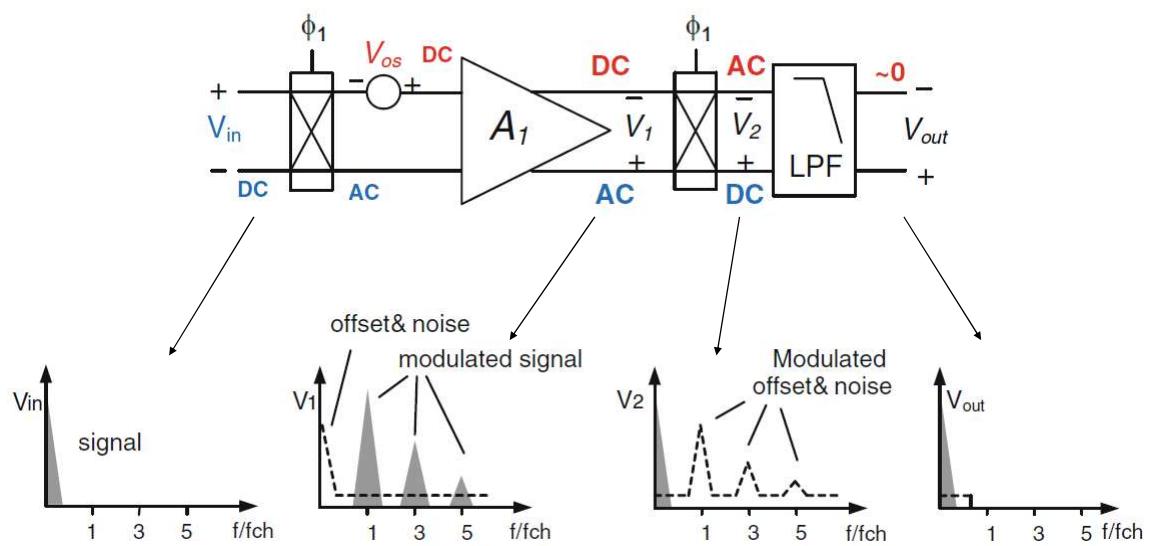


## Chopping – Time Domain



Illustrations: R. Wu, J. Huijsing, K. Makinwa, Precision Instrumentation Amplifiers and Read-Out Integrated Circuits, Springer 2013 65  
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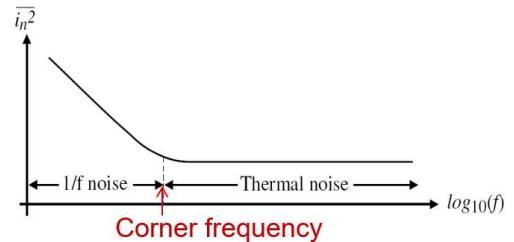
## Chopping – Frequency Domain



Illustrations: R. Wu, J. Huijsing, K. Makinwa, Precision Instrumentation Amplifiers and Read-Out Integrated Circuits, Springer 2013 66  
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## Chopping Frequency

- Requirements:
  - higher than the  $1/f$  corner frequency, to remove flicker noise
  - significantly lower than the amplifier bandwidth, to ensure good settling
  - not too high, because it decreases input impedance
  - duty cycle must be exactly 50%, to average modulated offset to 0



67

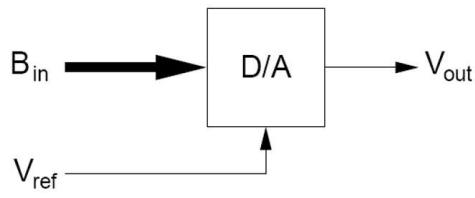
# Chapter 2

## Fundamentals of Data Converters

Dr. Florin Burcea (revised by)  
Courtesy of Dr. Stephan Henzler

68

## Ideal D/A Conversion



$$V_{\text{out}} = B_{\text{in}} \cdot V_{\text{LSB}}$$

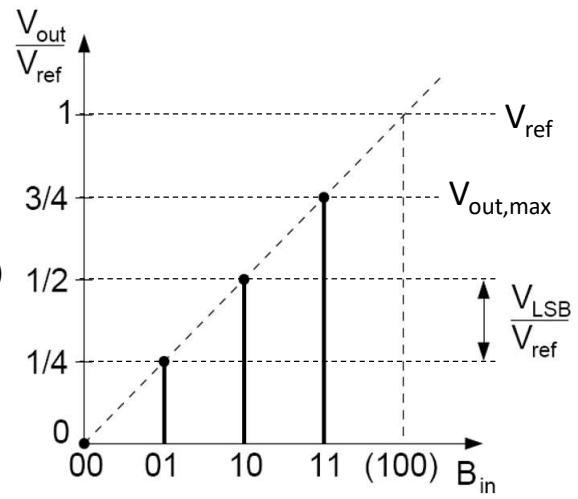
$$B_{\text{in}} = 2^N(b_1 2^{-1} + b_2 2^{-2} + \dots + b_N 2^{-N})$$

$$= 2^N \sum_{i=1}^N b_i 2^{-i}$$

$$V_{\text{LSB}} = V_{\text{ref}} / 2^N$$

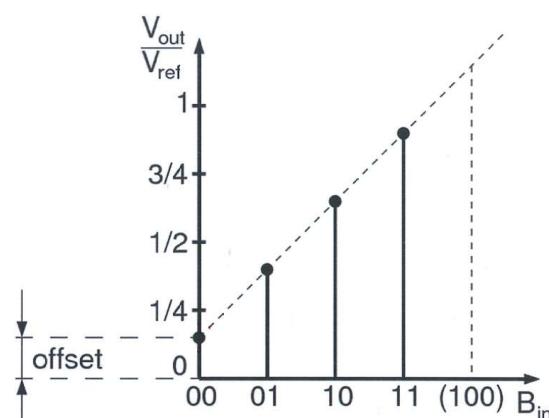
$b_1$ :MSB,  $b_N$ :LSB

$$V_{\text{out},\text{max}} = V_{\text{ref}} - V_{\text{LSB}}$$



69

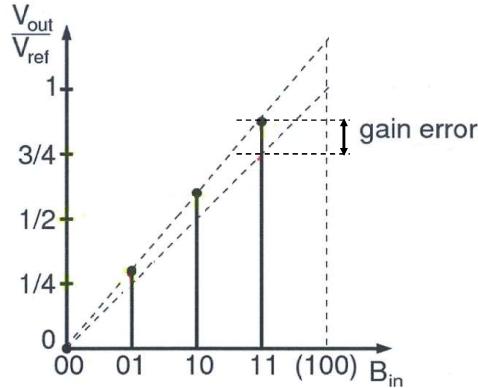
## DAC Offset Error



$$E_{\text{offset,DAC}} = \left. \frac{V_{\text{out}}}{V_{\text{LSB}}} \right|_{0 \dots 0} [\text{LSB}]$$

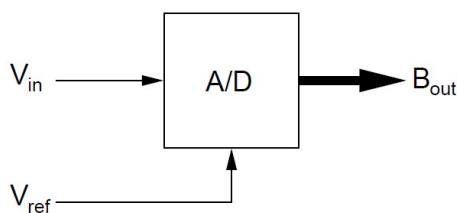
70

## DAC Gain Error



$$E_{\text{gain,DAC}} = \left( \frac{V_{out}}{V_{LSB}} \Big|_{1\dots1} - \frac{V_{out}}{V_{LSB}} \Big|_{0\dots0} \right) - (2^N - 1) [\text{LSB}]$$

## Ideal A/D Conversion

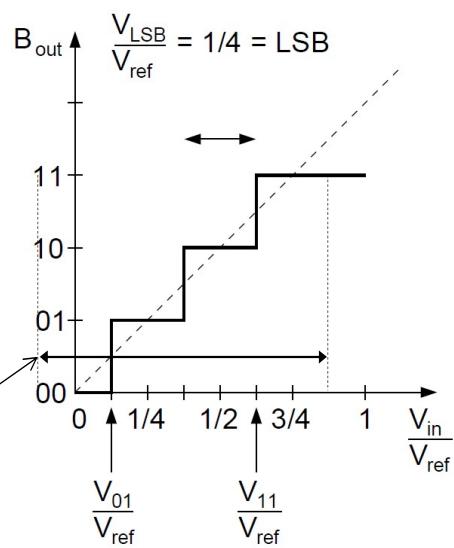


Quantized voltage:  $V_{LSB} \cdot B_{out} = V_{in} + V_Q$

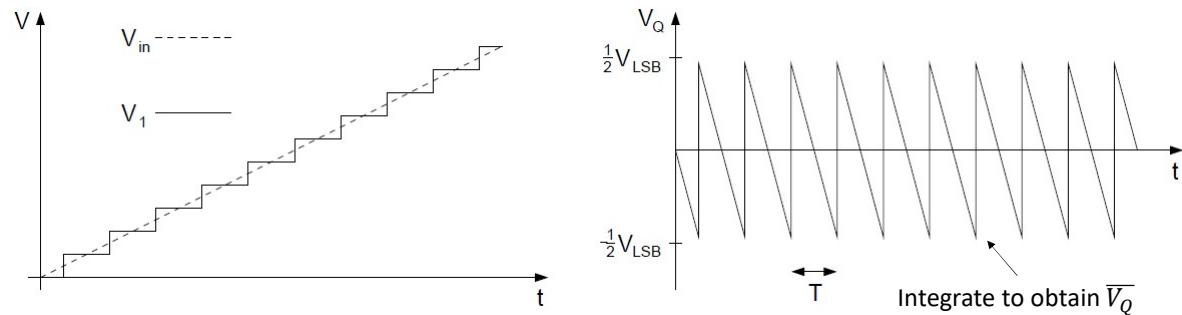
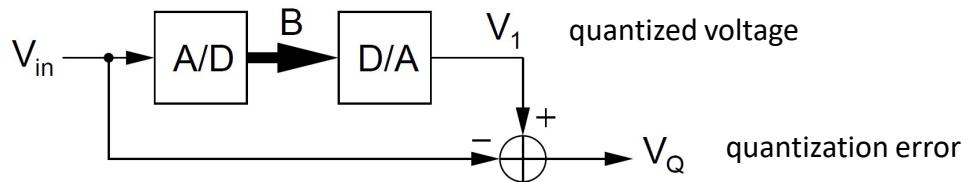
$$-\frac{1}{2^{N+1}} V_{ref} \leq V_Q \leq \frac{1}{2^{N+1}} V_{ref} = \frac{1}{2} V_{LSB}$$

$V_Q$ : quantization error  $|V_Q| \leq 0.5 \text{ LSB}$

$$\text{Operating range: } -\frac{V_{ref}}{2^{N+1}} \leq V_{in} \leq \left(1 - \frac{1}{2^{N+1}}\right) V_{ref}$$



## Quantization in A/D Converters



## Quantization Error

- Consider a saw-tooth signal:

$$V_Q = (-)\frac{V_{LSB}}{T}t \quad -\frac{T}{2} \leq t \leq +\frac{T}{2}$$

- Mean quantization error:

$$\bar{V}_Q = \frac{1}{T} \int_{-T/2}^{T/2} V_Q(t) dt = 0$$

- Power of quantization error:

## Signal-to-Noise Ratio (SNR)

- Signal-to-(Quantization)-Noise Ratio S(Q)NR:  
sine input, maximum range

$$\hat{V} = V_{\text{ref}}/2 \quad \text{signal power } P_S: \frac{\hat{V}^2}{2} = \frac{V_{\text{ref}}^2}{8}$$

$$\text{noise power: } P_N = \frac{V_{\text{LSB}}^2}{12} = \frac{V_{\text{ref}}^2}{12 \cdot 2^{2N}}$$

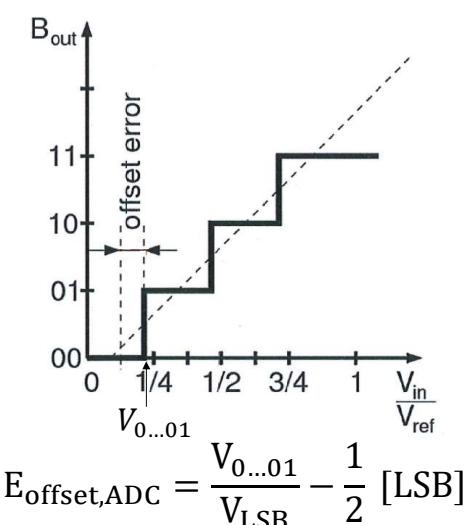
$$\begin{aligned} S(Q)\text{NR[dB]} &= 10 \log \left( \frac{P_S}{P_N} \right) = 10 \log \left( \frac{V_{\text{ref}}^2}{8} \cdot \frac{12 \cdot 2^{2N}}{V_{\text{ref}}^2} \right) \\ &= 20N \log(2) + 10 \log \left( \frac{12}{8} \right) = 6.02N + 1.76 \end{aligned}$$

(not considering additional physical noise)

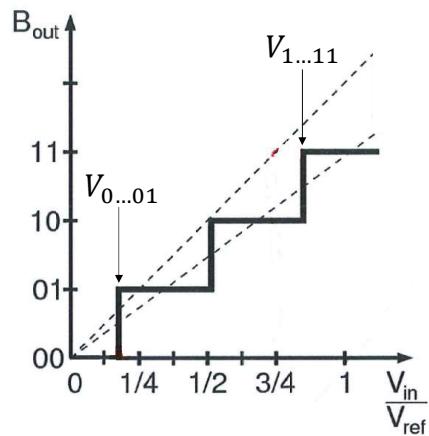
→ every additional bit increases the S(Q)NR by 6dB

- SQNR: maximum achievable SNR for given number of bits

## ADC Offset Error

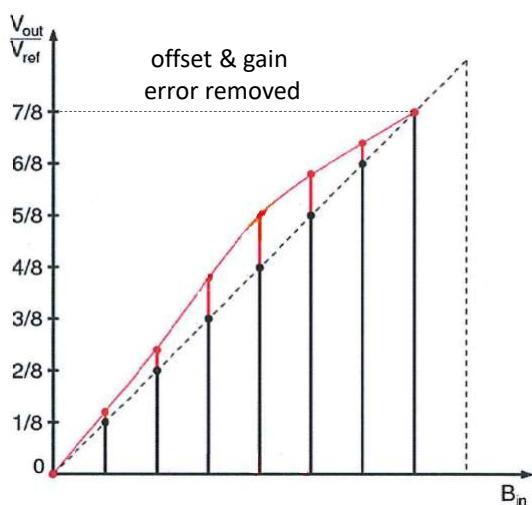


## ADC Gain Error



$$E_{\text{gain,ADC}} = \left( \frac{V_{1\dots11}}{V_{\text{LSB}}} - \frac{V_{0\dots01}}{V_{\text{LSB}}} \right) - (2^N - 2) \text{ [LSB]}$$

## Nonlinearity in Data Converters

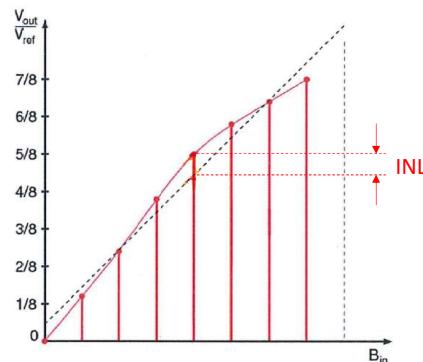
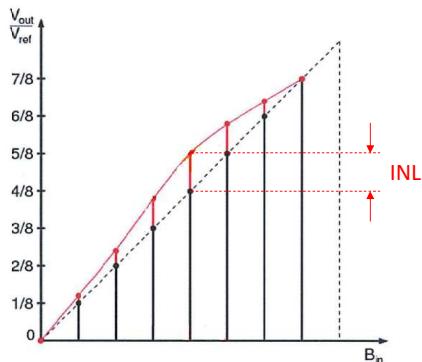


### Accuracy:

The absolute inaccuracy is defined as the maximum deviation of the analog value from the ideal one. It includes offset, gain and linearity errors and may be different for every individual quantization value.

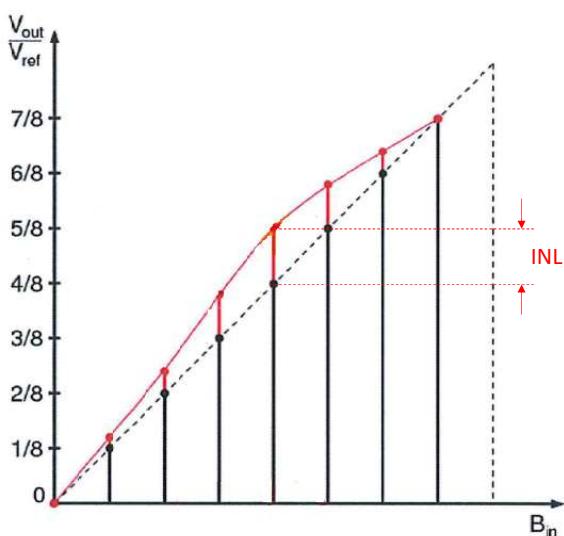
The relative inaccuracy is defined as the deviation that remains after offset and gain error have been removed.

## DAC Integral Nonlinearity (INL)



- The INL error is defined as the deviation of each analog value from a straight line.
- If the straight line through the end points of the converter is chosen as reference (left), then INL equals the relative inaccuracy.
- Alternatively, a regression line can be used as reference (right). In this case, INL is smaller.
- It depends on the application which definition should be applied.

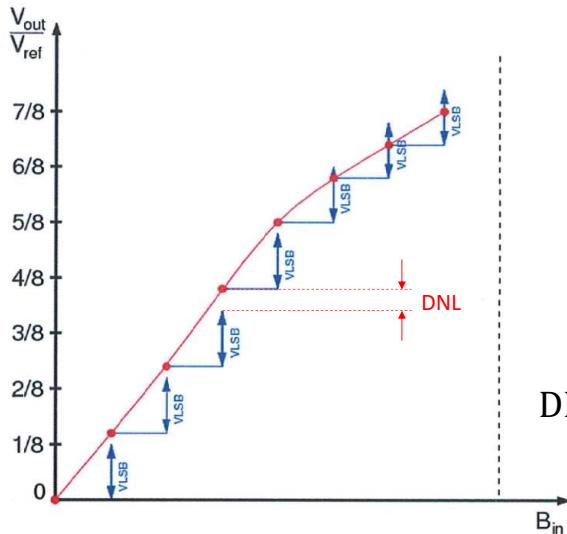
## DAC Integral Nonlinearity (INL)



$$\text{INL}(i) = \left| \frac{V_{out}^{\text{measured}}}{V_{LSB}} \Big|_i - \frac{V_{out}^{\text{ideal}}}{V_{LSB}} \Big|_i \right|$$

$$i = 0, 1, \dots, 2^N - 1$$

## DAC Differential Nonlinearity (DNL)



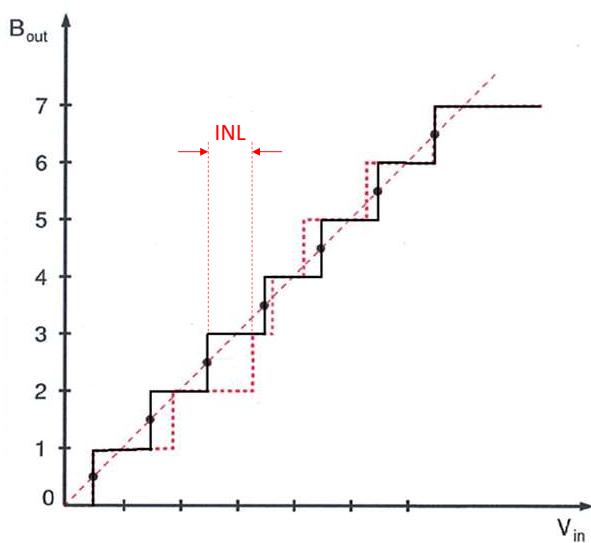
- The DNL error is defined as the deviation of the analog step size from  $V_{\text{LSB}}$  (after removal of gain and offset error).
- Like the INL, the DNL is defined individually for each digital word.
- Monotonicity:** The output signal of a monotonic DAC increases or at least remains unchanged as the input increases.

$$\text{DNL}(i) = \left| \frac{V_{\text{out}}^{\text{measured}}}{V_{\text{LSB}}} \Big|_i - \frac{V_{\text{out}}^{\text{measured}}}{V_{\text{LSB}}} \Big|_{i-1} \right| - 1$$

$$i = 1, 2, \dots, 2^N - 1$$

81

## ADC Integral Nonlinearity

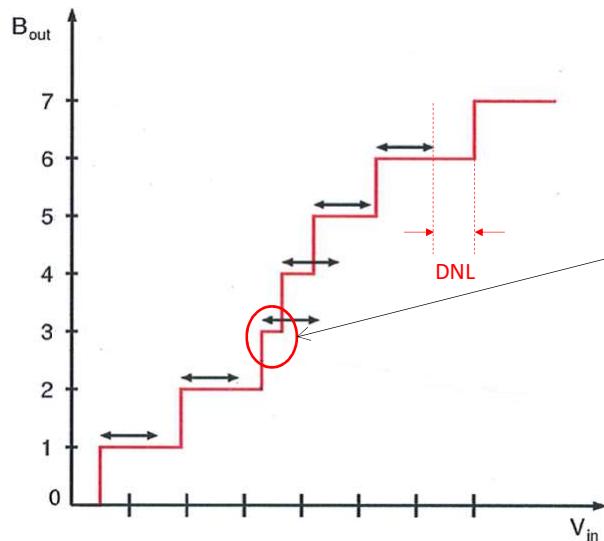


$$\text{INL}(i) = \left| \frac{V_i^{\text{measured}}}{V_{\text{LSB}}} - \frac{V_i^{\text{ideal}}}{V_{\text{LSB}}} \right|$$

$$i = 1, 2, \dots, 2^N - 1$$

82

## ADC Differential Nonlinearity



- **Missing codes:** If one step vanishes completely, the ADC is said to have a missing code.
- In practice, the criterion for a missing code is a step width smaller than  $0.1V_{LSB}$ .

$$DNL(i) = \frac{V_i^{\text{measured}} - V_{i-1}^{\text{measured}}}{V_{LSB}} - 1$$

$$i = 2, 3, \dots, 2^N - 1$$

83



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## INL and DNL Properties

### DAC

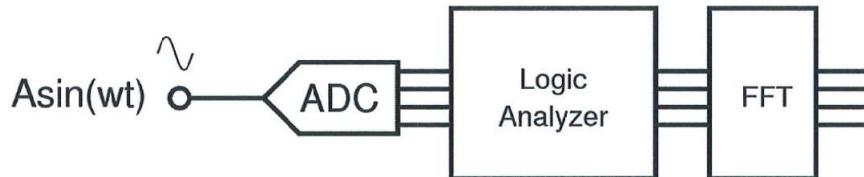
- $\text{INL}(0) = \text{INL}(2^N - 1) = 0$
- $\text{DNL}(1) = \text{INL}(1)$
- $\text{DNL}(i) = \text{INL}(i) - \text{INL}(i - 1),$   
 $i = 1, 2, \dots, 2^N - 1$
- $\text{INL}(i) = \sum_{j=1}^i \text{DNL}(j),$   
 $i = 1, 2, \dots, 2^N - 1$
- $\sum_{i=1}^{2^N - 1} \text{DNL}(j) = 0$

### ADC

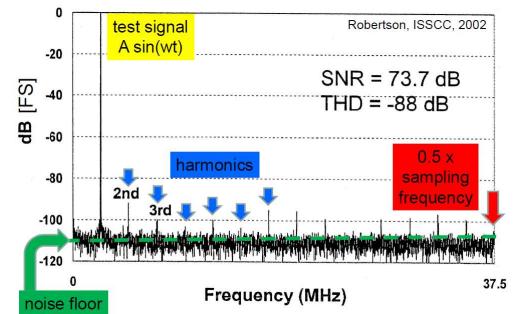
- $\text{INL}(1) = \text{INL}(2^N - 1) = 0$
- $\text{DNL}(2) = \text{INL}(2)$
- $\text{DNL}(i) = \text{INL}(i) - \text{INL}(i - 1),$   
 $i = 2, 3, \dots, 2^N - 1$
- $\text{INL}(i) = \sum_{j=2}^i \text{DNL}(j),$   
 $i = 2, 3, \dots, 2^N - 1$
- $\sum_{i=2}^{2^N - 1} \text{DNL}(j) = 0$

84

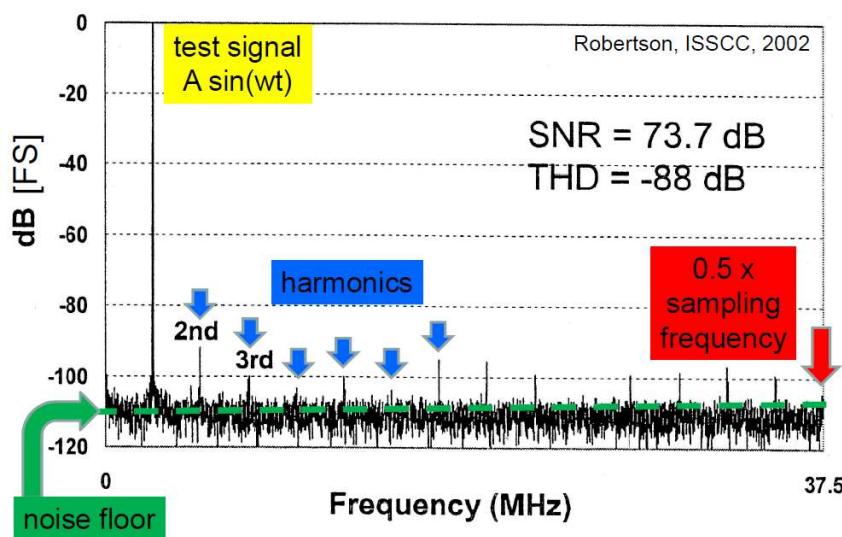
## Dynamic ADC Measurement



- ADC transfer curve describes static measurements.
- In dynamic measurements, an input voltage waveform (usually sine) is converted continuously and analyzed in the frequency domain (much more realistic, considering noise, crosstalk etc.).

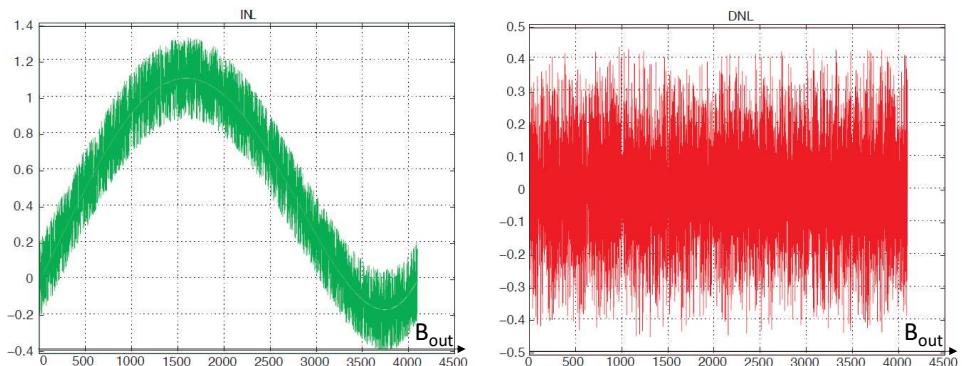


## Interpretation of the Output Spectrum



## INL and DNL Effects on Signal Spectra

12-bit ADC example



- ADCs with large INL show harmonic distortion
- Large DNL → large INL with large random components
- The resulting noise is added to the quantization and degrades the SNR.



Illustration: F. Maloberti, Data Converters, Springer 2007

87

## INL and DNL Effects on Signal Spectra

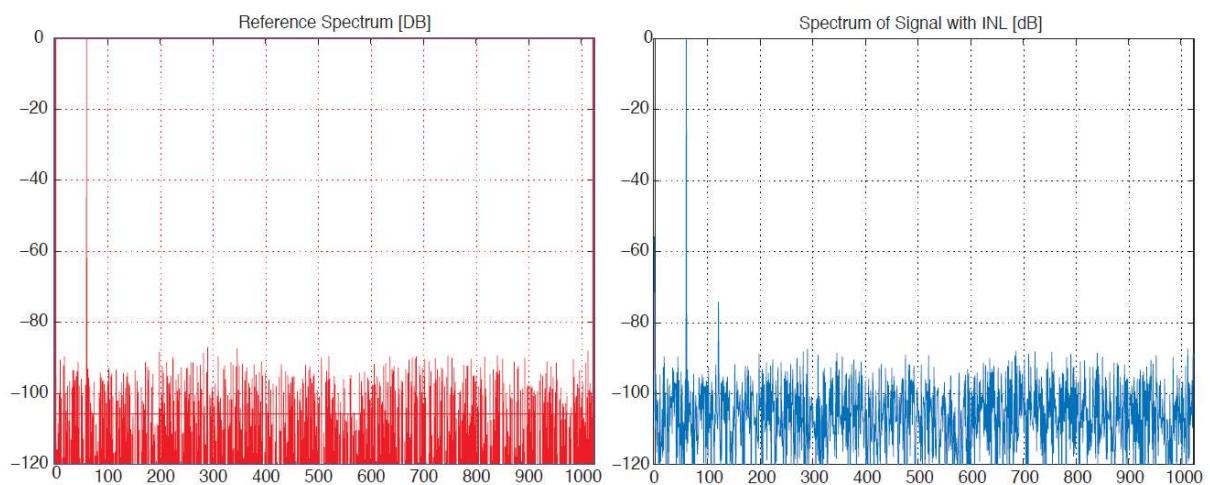


Illustration: F. Maloberti, Data Converters, Springer 2007  
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88

## Harmonic Distortion Caused by Nonlinearity

- Spectrum allows computation of:

- signal power  $P_{\text{signal}}$
- power of harmonic components  $P_{\text{harmonics}}$
- noise power  $P_{\text{noise}}$

- Signal-to-Noise Ratio (SNR):

$$\text{SNR[dB]} = 10 \log \left( \frac{P_{\text{signal}}}{P_{\text{noise}}} \right)$$

- Signal-to-Noise-and-Distortion Ratio (SNDR/SINAD):

$$\text{SNDR[dB]} = 10 \log \left( \frac{P_{\text{signal}}}{P_{\text{noise}} + P_{\text{harmonics}}} \right)$$

## Harmonic Distortion Caused by Nonlinearity

- Total Harmonic Distortion (THD):

$$\text{THD} = 20 \log \sqrt{\frac{V_2^2 + V_3^2 + V_4^2 + \dots}{V_1^2}}$$

$$\text{THD} = 10 \log \left( \frac{P_{\text{harmonics}}}{P_{\text{signal}}} \right)$$

- Second Harmonic Distortion (SHD):

$$\text{SHD} = 20 \log \frac{V_2}{V_1}$$

## Effective Number of Bits

- An ideal ADC suffers only from quantization noise:

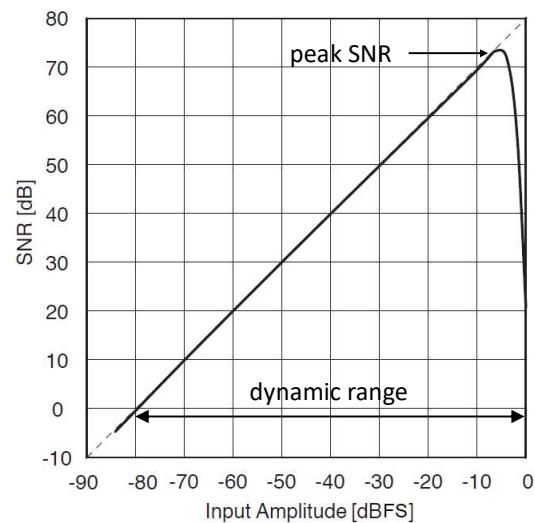
$$\text{SNR} = \text{SQNR} = 6.02N + 1.76 \text{ [dB]}$$

- Actual ADCs have lots of impairments (noise, nonlinearity) that limit the effective resolution.  
→ Effective Number Of Bits (ENOB):

$$\text{ENOB} = \frac{\text{SNDR[dB]} - 1.76}{6.02}$$

## Signal-to-Noise Ratio over Input Signal

- Some ADC types (typically sigma-delta) obtain maximum SN(D)R for input level less than 0 dBFS (FS = full scale)
- Dynamic range:  
input level at which SN(D)R=0dB



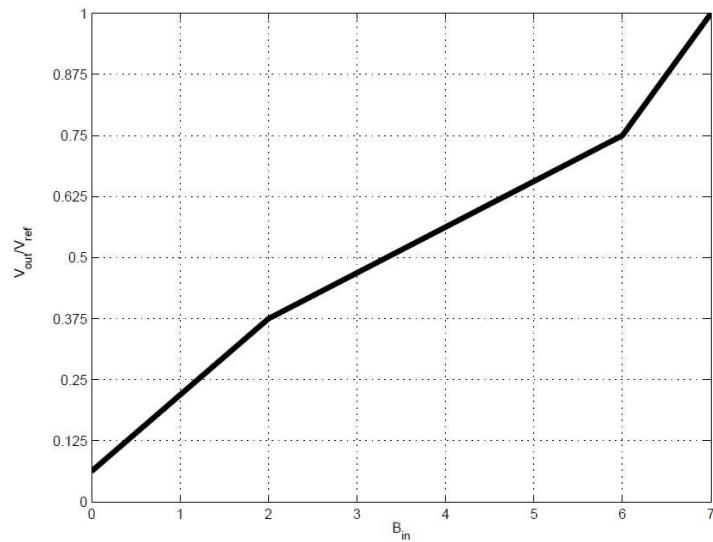
# Tutorial

## Exercise 1

Consider the following DAC transfer characteristic.

- a) Determine the offset error and carry out the offset compensation.
- b) Determine and compensate for the gain error.
- c) Sketch the absolute inaccuracy in the diagram.
- d) Sketch the relative inaccuracy in the diagram.
- e) Sketch the integral non-linearity in the diagram.
- f) Sketch the differential non-linearity in the diagram.

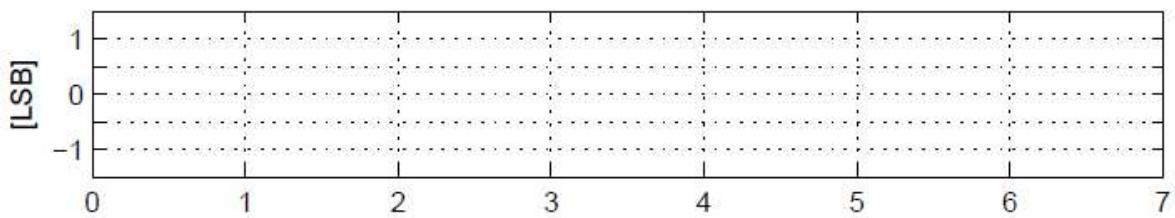
## Exercise 1



95

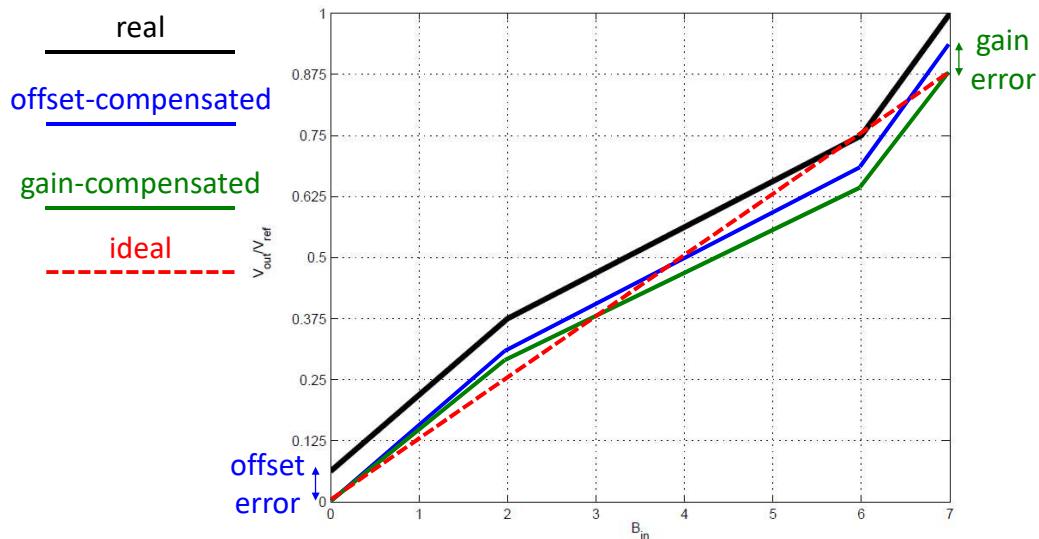
## Exercise 1

Diagram:



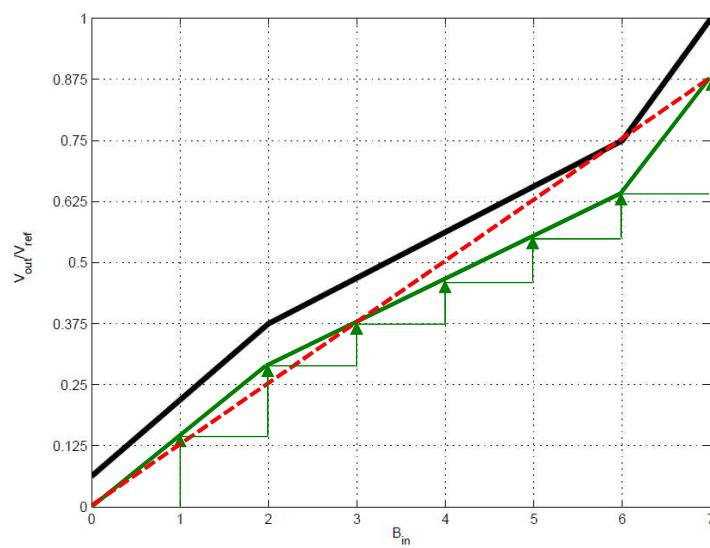
96

## Exercise 1 – Solution



97

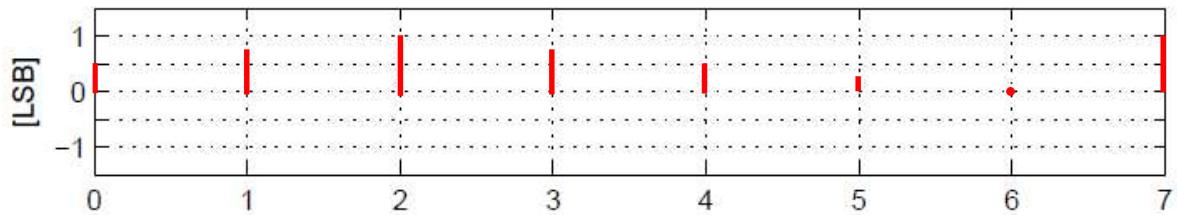
## Exercise 1 – Solution



98

## Exercise 1 – Solution

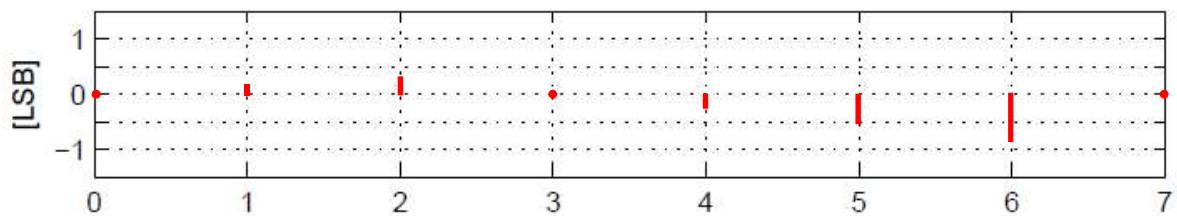
c) Absolute inaccuracy = real curve – ideal curve



99

## Exercise 1 – Solution

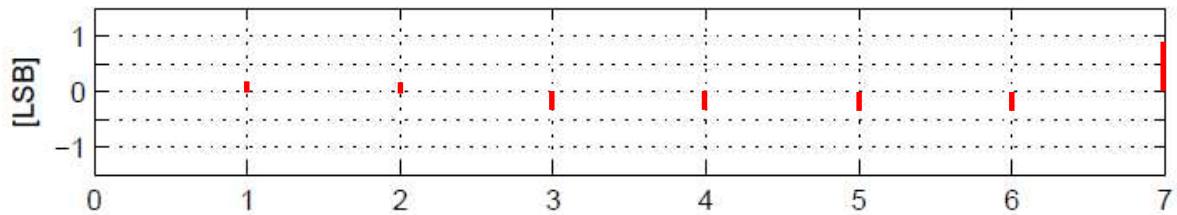
d),e) INL = relative inaccuracy = gain compensated curve – ideal curve



100

## Exercise 1 – Solution

f) DNL



101



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## Exercise 2

Consider the following DAC transfer characteristic.

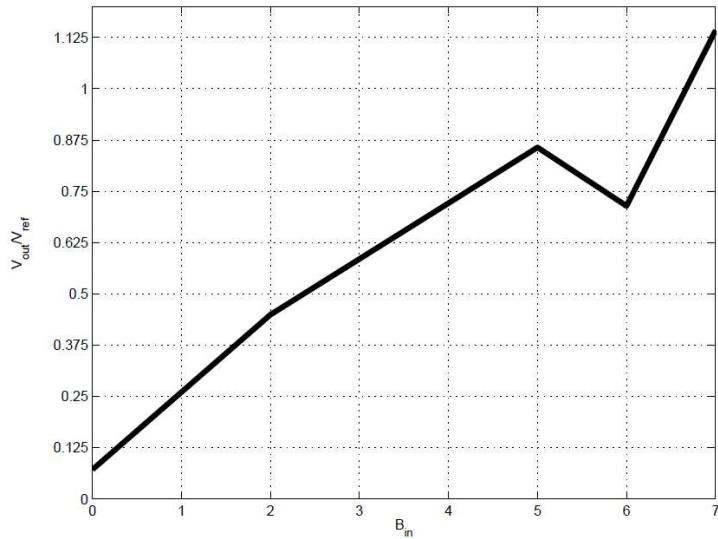
- a)-f) Same as exercise 1.
- g) Is this converter monotonic? What is the general condition of monotonicity in terms of DNL?

102



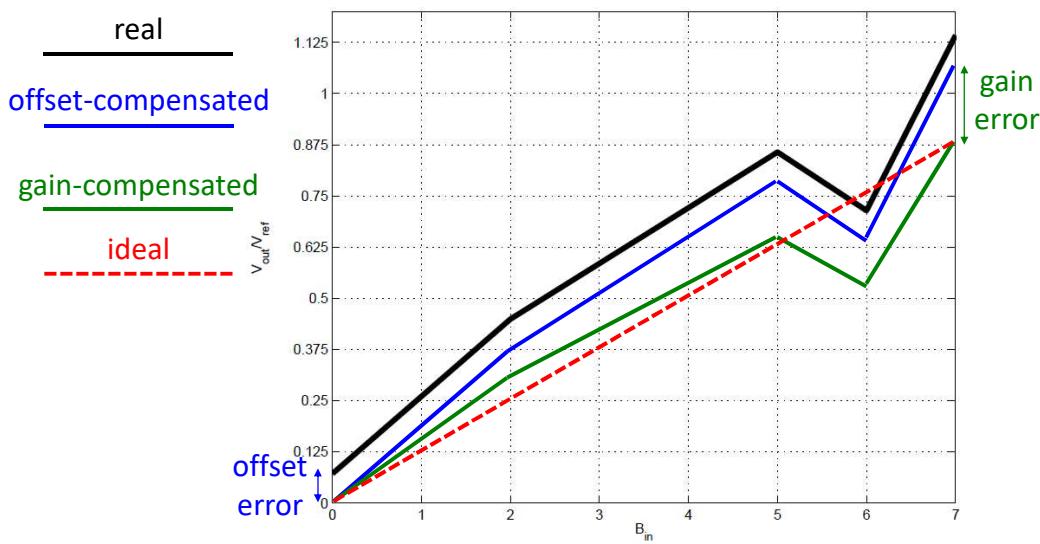
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## Exercise 2



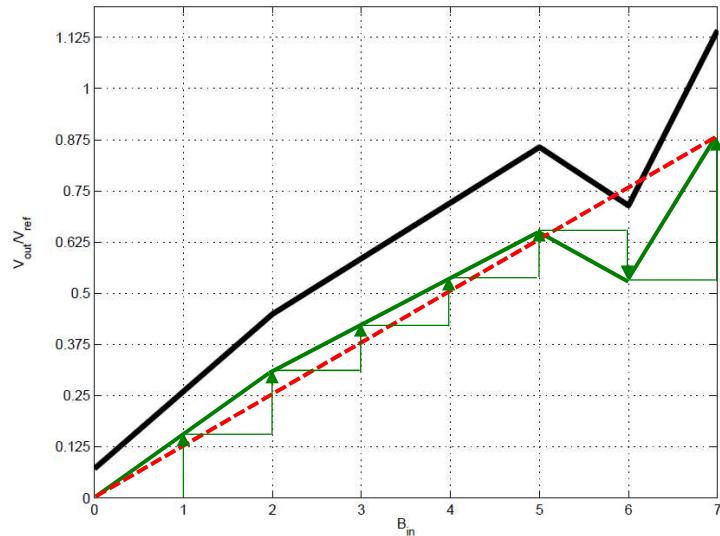
103

## Exercise 2 – Solution



104

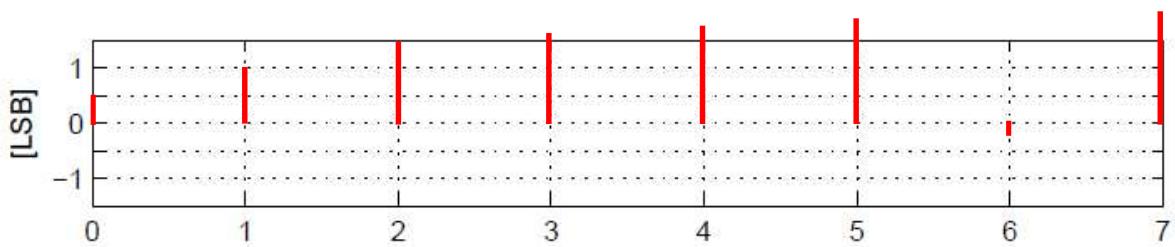
## Exercise 2 – Solution



105

## Exercise 2 – Solution

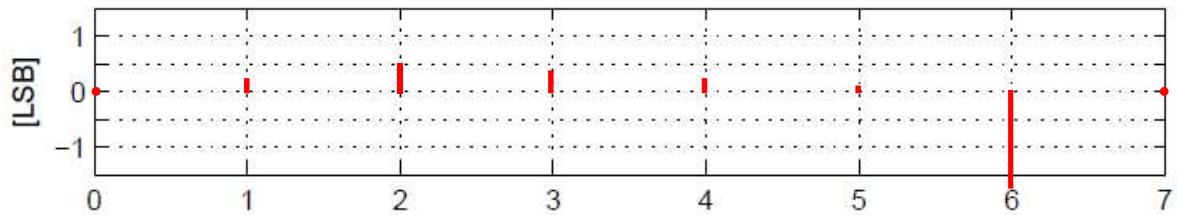
c) Absolute inaccuracy = real curve – ideal curve



106

## Exercise 2 – Solution

d),e)  $INL = \text{relative inaccuracy} = \text{gain compensated curve} - \text{ideal curve}$



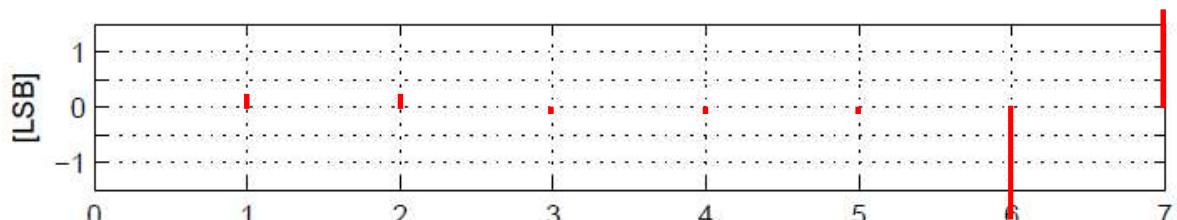
107



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## Exercise 2 – Solution

f)  $DNL$



g) Non-monotonicity: output signal decreases with increasing code

non-monotonicity from code 5 to code 6,  $DNL(6) < -1$

In general: monotonicity  $\leftrightarrow DNL \geq -1\text{ LSB}$

108



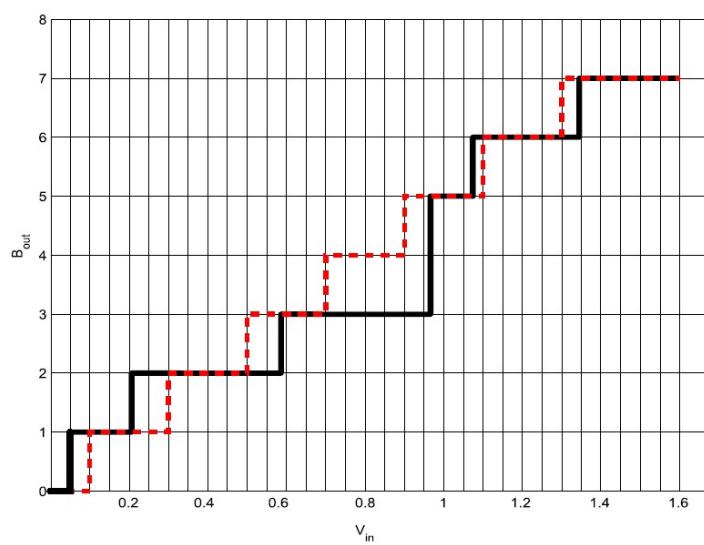
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## Exercise 3

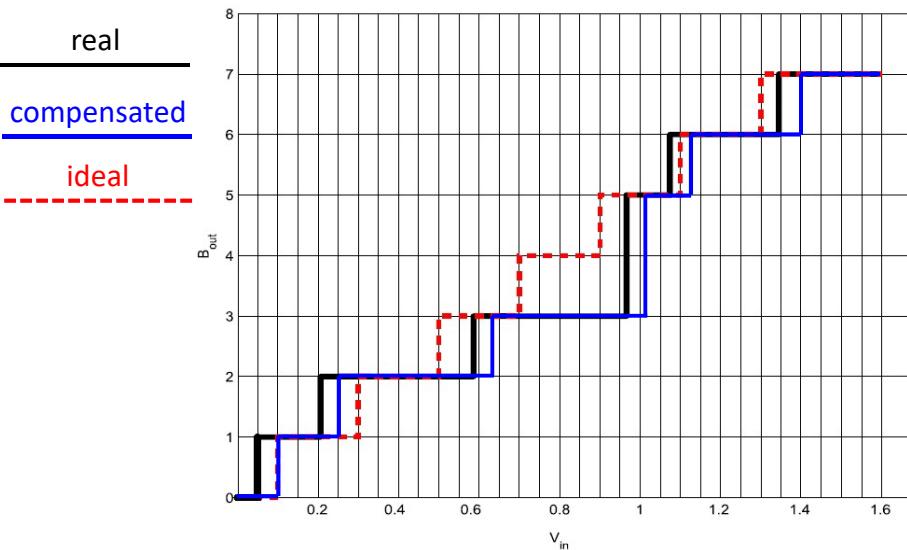
Consider the following transfer characteristic of a 3-bit ADC. Additionally, the ideal transfer curve is shown.

- What is the reference voltage?
- What is the quantization step?
- Determine the offset error and carry out the offset compensation.
- Determine the gain error.

## Exercise 3



## Exercise 3 – Solution

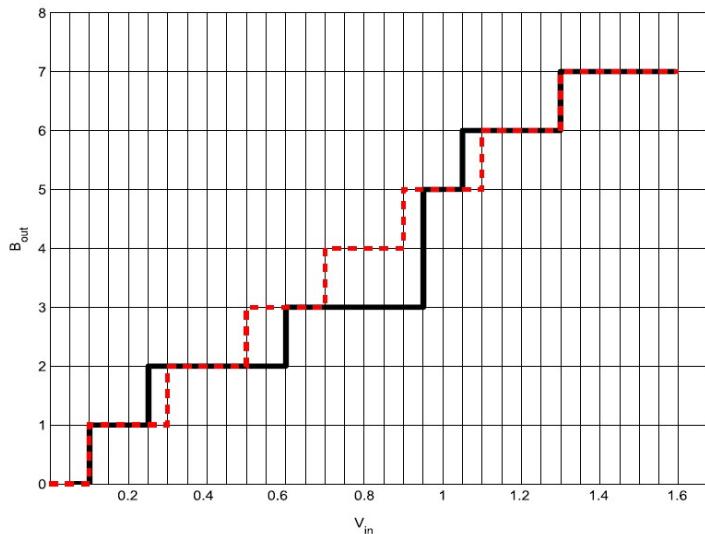


## Exercise 3

The next figure shows the transfer curve of the same ADC after offset and gain error compensation.

- e) Determine the integral non-linearity and the differential non-linearity for each step of the input voltage.
- f) Does this converter suffer from missing codes? If yes, which code is missing?
- g) What is the value of DNL for a missing code?

## Exercise 3



113

## Exercise 3 – Solution

e)

	<i>Code transition</i>	<i>INL[LSB]</i>	<i>DNL[LSB]</i>
	$0 \rightarrow 1$		
	$1 \rightarrow 2$		
	$2 \rightarrow 3$		
	$3 \rightarrow 4$		
	$4 \rightarrow 5$		
	$5 \rightarrow 6$		
	$6 \rightarrow 7$		

f) Missing code:

g) Missing code:  $DNL(4+1)=$ 

114

## Exercise 4

Consider a 12-bit ADC ( $N=12$ ).

- a) Calculate the signal-to-quantization-noise ratio SQNR.
- b) The following values of the signal-to-noise ratio (SNR) and the total harmonic distortion (THD) are measured on the output spectrum:  
 $\text{SNR} = 70\text{dB}$ ,  $\text{THD} = -77\text{dB}$ .  
Calculate the effective number of bits, ENOB.

## Exercise 4 – Solution

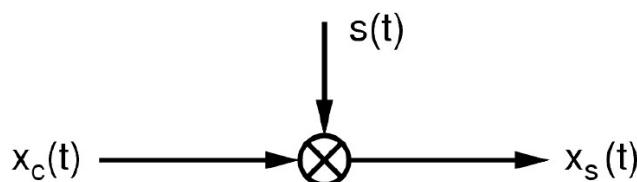
# Chapter 3

## Fundamentals of Discrete-Time Signal Processing

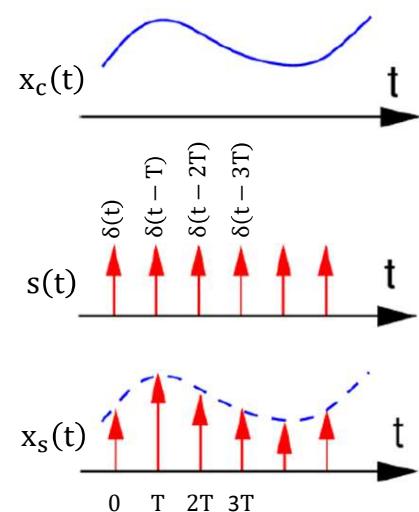
Dr. Florin Burcea (revised by)  
Courtesy of Dr. Stephan Henzler



## Representation of Discrete-Time Signals



$$x_s(t) = x_c(t)s(t) = x_c(t) \sum_n \delta(t - nT)$$

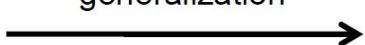


## Spectral Transformation

- Fourier transform:

$$X(\omega) = \int_{-\infty}^{\infty} x(t) e^{-j\omega t} dt \quad x(t) = \frac{1}{2\pi} \int_{-\infty}^{\infty} X(\omega) e^{j\omega t} d\omega$$

- Laplace transform:

generalization  
       $X(s) = \int_{-\infty}^{\infty} x(t) e^{-st} dt$   
 $s = j\omega$

119

## Spectral Transformation

- Insertion of sampled signal in the Fourier formula:

$$X(\omega) = \int_{-\infty}^{\infty} \sum_n x(nT) \delta(t - nT) e^{-j\omega t} dt$$

→ Fourier transform of sampled signal

120

## Spectral Transformation

$$X(\omega) = \sum_n x(nT)e^{-j\omega nT}$$

- Normalization of frequency to sampling frequency:  $\Omega = \omega T = 2\pi \frac{f}{f_s}$
- $f = f_s \rightarrow \Omega = 2\pi$

$$X(\Omega) = \sum_n x[n]e^{-j\Omega n}$$

Fourier transform  
of discrete sequence

—————>  
generalization  
 $z = e^{j\Omega} = e^{j\omega T}$

$$X(z) = \sum_n x[n]z^{-n}$$

Z transform



## Z Transform – Useful Properties

$$X(z) = \sum_n x[n]z^{-n}$$

- Linearity:

$$a \cdot x[n] + b \cdot y[n] \rightarrow a \cdot X(z) + b \cdot Y(z)$$

- Delay

$$x[n - 1] \rightarrow z^{-1}X(z)$$

- Unity step function

$$u[n] \rightarrow \frac{1}{1-z^{-1}}$$

$$u(t) := \begin{cases} 0 & t < 0 \\ 1 & t \geq 0 \end{cases}$$



## Spectrum of a Sampled Signal

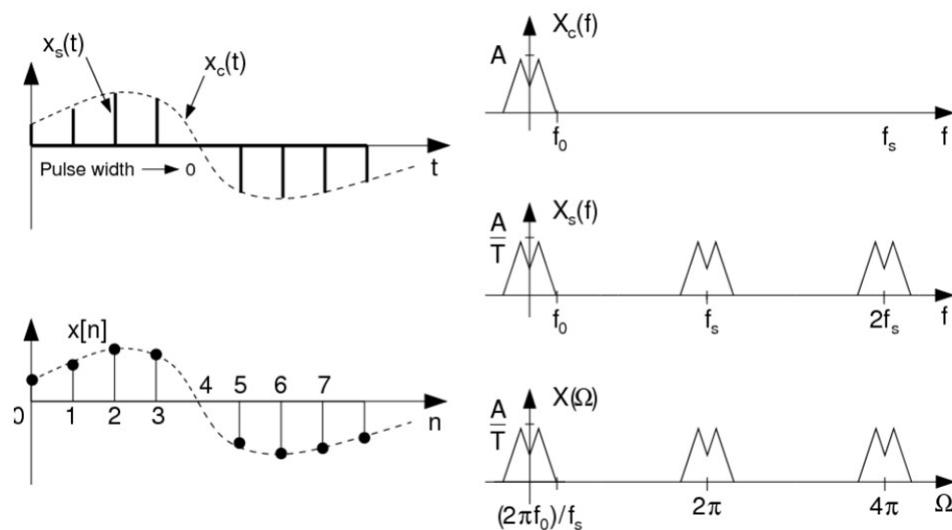
$$\begin{aligned} s(t) &= \sum_n \delta(t - nT) & \longleftrightarrow & S(\omega) = \frac{2\pi}{T} \sum_k \delta(\omega - k\omega_s) \\ x_s(t) &= x_c(t)s(t) & \longleftrightarrow & X_s(\omega) = \frac{1}{2\pi} X_c(\omega) * S(\omega) \\ &= \sum_n x_c(nT)\delta(t - nT) & & = \frac{1}{T} \sum_k X_c(\omega - k\omega_s) \end{aligned}$$

Convolution:  $F(\omega) * G(\omega) = \int_{-\infty}^{\infty} F(\omega - \theta) G(\theta) d\theta \rightarrow$  see appendix

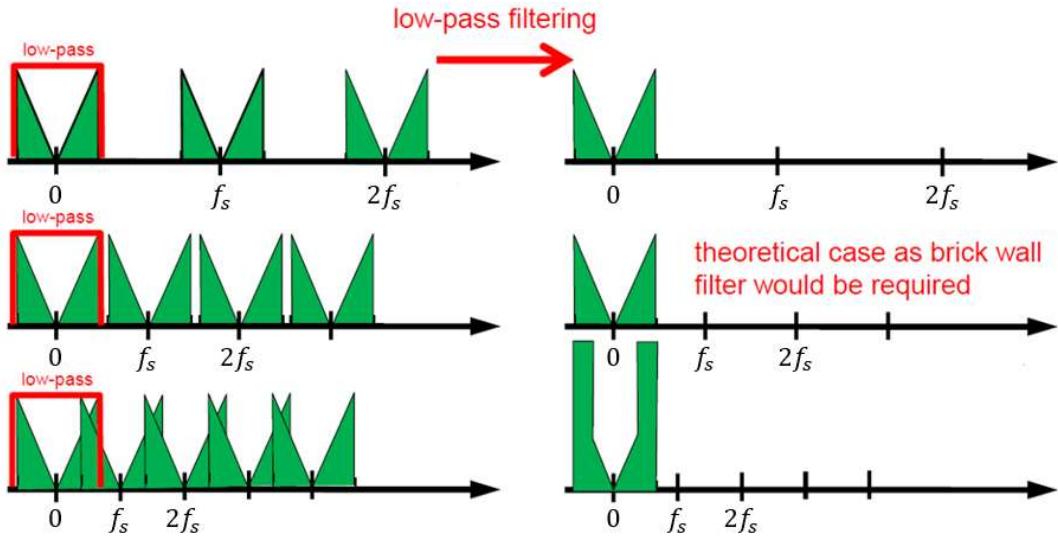
Sampling:

- Time domain: multiplication of continuous-time signal with pulse train  
→ train of weighted pulses
- Frequency domain: convolution of signal spectrum with spectrum of pulse train  
→ copy and shift of the spectrum to multiples of the sampling frequency

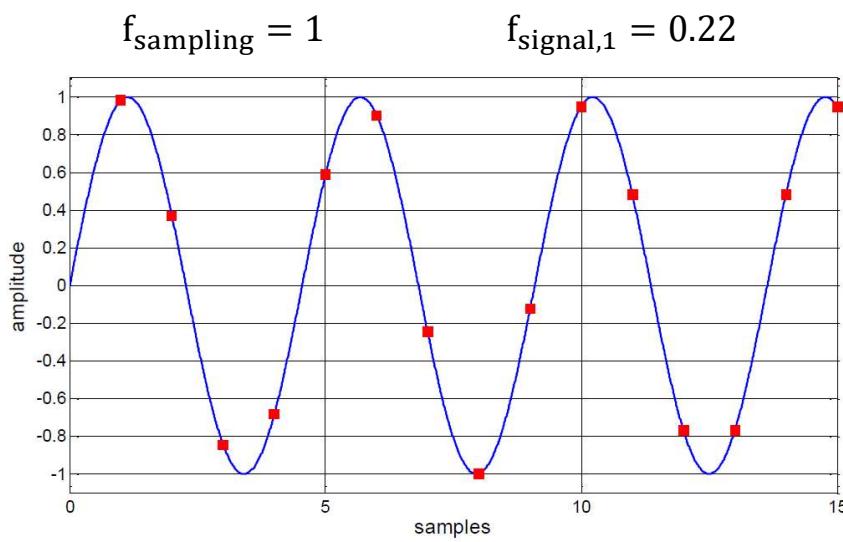
## Spectrum of a Sampled Signal



## Aliasing in the Frequency Domain



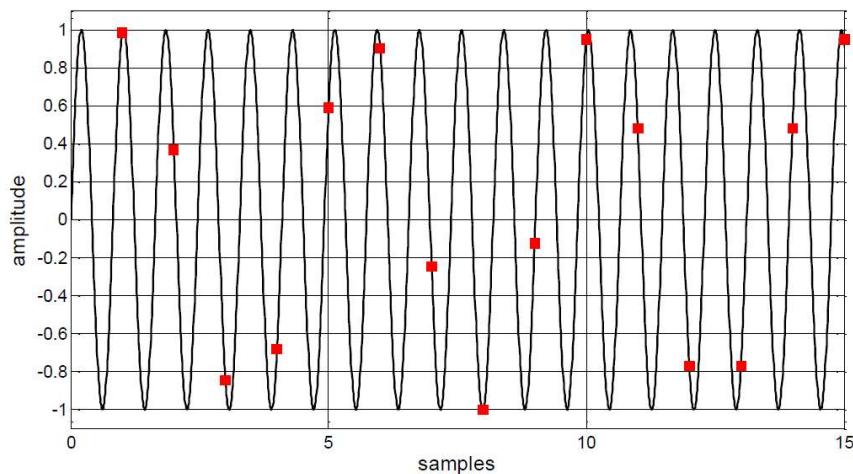
## Sampling and Aliasing



## Sampling and Aliasing

$$f_{\text{sampling}} = 1$$

$$f_{\text{signal},2} = 0.22 + f_{\text{sampling}}$$

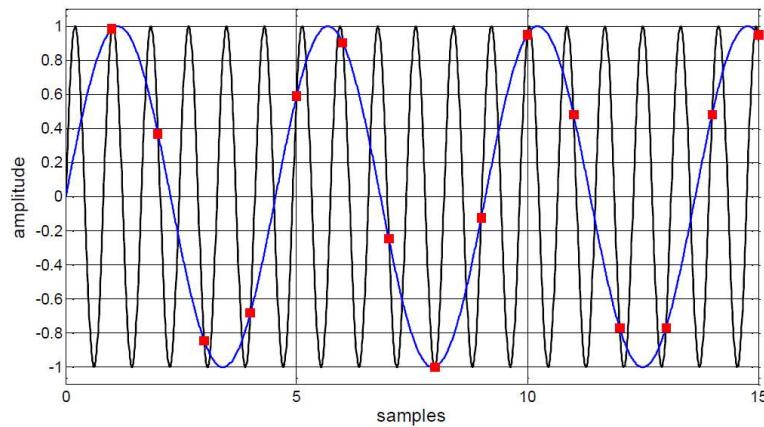


127

## Sampling and Aliasing

Nyquist criterion:  $f_{\text{signal}} < f_{\text{sample}}/2$

→ ensures that the samples represent the signal unambiguously



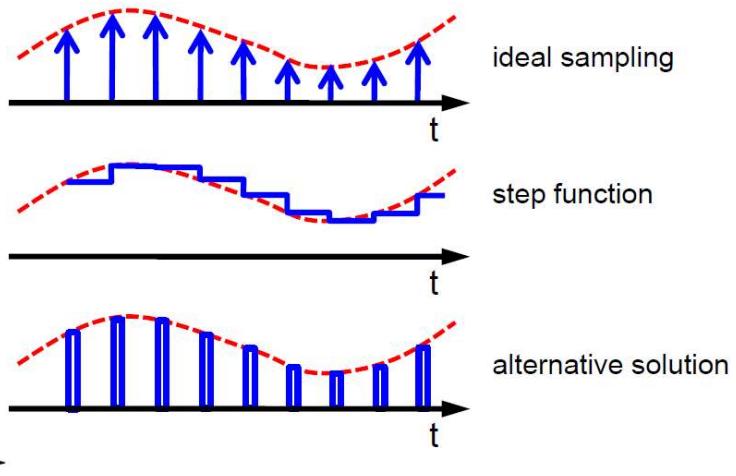
$$f_{\text{signal},1} = 0.22$$

$$f_{\text{signal},2} = 0.22 + f_{\text{sampling}}$$

128

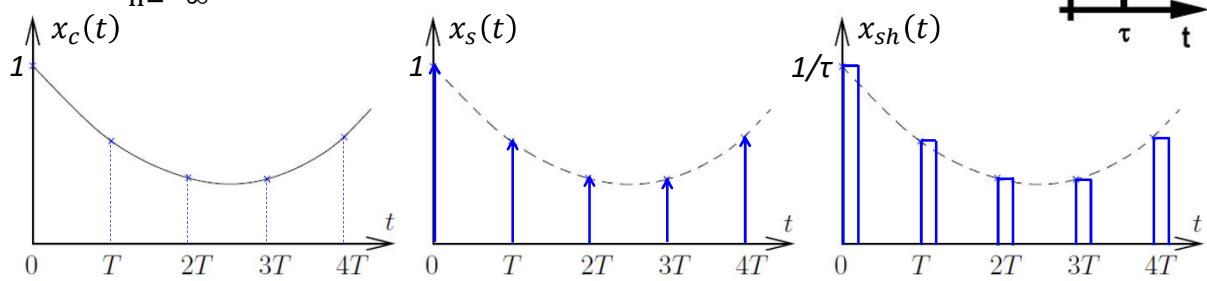
## Practical Sampling: Sample & Hold

- Physical signals have:
  - finite slope ( $dx/dt$ )
  - non-zero pulse width, i.e. finite bandwidth
  - finite value, i.e. finite energy
- Sampling = SAMPLE & HOLD



## Sampling with Non-Zero Pulse Width

$$\begin{aligned} h(t) &= \frac{1}{\tau} [u(t) - u(t - \tau)] \\ x_{sh}(t) &= x_s(t) * h(t) = \int_{-\infty}^{\infty} x_s(t - \theta) h(\theta) d\theta \\ &= \dots = \sum_{n=-\infty}^{\infty} x_c[n] \frac{1}{\tau} [u(t - nT) - u(t - nT - \tau)] \quad (\text{see appendix}) \end{aligned}$$



## Sampling and Hold – Spectral Transformation (1)

$$x_{sh}(t) = \sum_{n=-\infty}^{\infty} x_c[n] \frac{1}{\tau} [u(t - nT) - u(t - nT - \tau)]$$

$$X_{sh}(\omega) = \frac{1}{\tau} \int_{-\infty}^{\infty} \sum_{n=-\infty}^{\infty} x_c[n] [u(t - nT) - u(t - nT - \tau)] e^{-j\omega t} dt$$



## Sampling and Hold – Spectral Transformation (2)

$$X_{sh}(\omega) = -\frac{1}{j\omega\tau} \sum_{n=-\infty}^{\infty} x_c[n] (e^{-j\omega nT} e^{-j\omega\tau} - e^{-j\omega nT})$$

$$= \sum_{n=-\infty}^{\infty} x_c[n] e^{-j\omega nT} \frac{1}{j\omega\tau} (1 - e^{-j\omega\tau})$$

ideal sampling      impact of hold

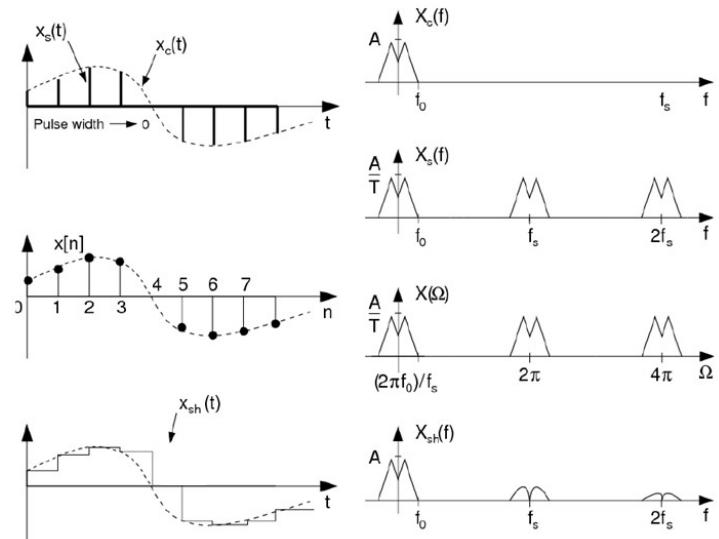
$$= X_s(\omega) e^{-j\omega\tau/2} \frac{e^{j\omega\tau/2} - e^{-j\omega\tau/2}}{2j(\omega\tau/2)}$$

$$= X_s(\omega) e^{-j\omega\tau/2} \frac{\sin(\omega\tau/2)}{\omega\tau/2} = X_s(\omega) e^{-j\omega\tau/2} \operatorname{sinc}(\omega\tau/2)$$



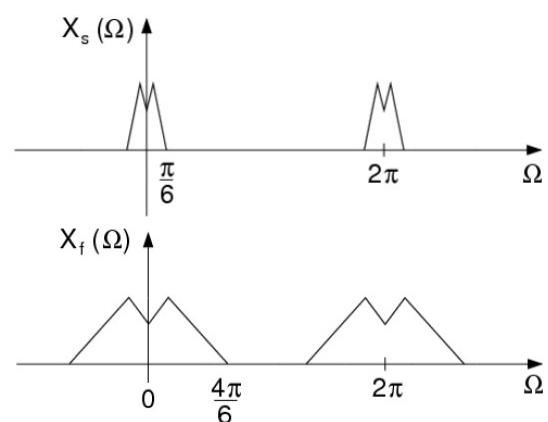
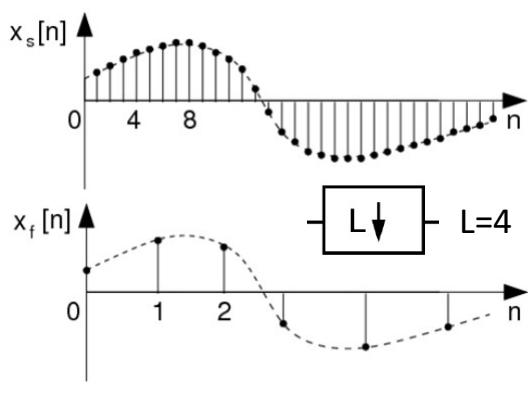
## Sampling and Hold – Spectrum

- Distortion of base band
- Damping of mirror spectra
  - not visible in A/D converter
  - visible in D/A converter
- During an A/D conversion, only one discrete amplitude value will be created at a discrete time point, even though conversion takes some time



133

## Downsampling

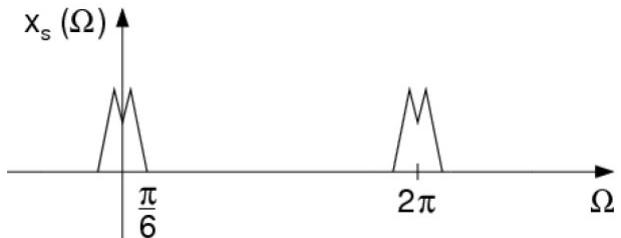


- Remove all sample, keep 1 out of  $L$
- Equivalent to sampling with the low rate

134

## Downsampling

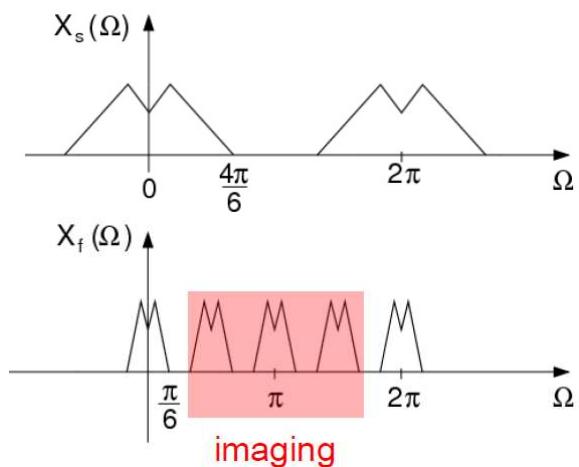
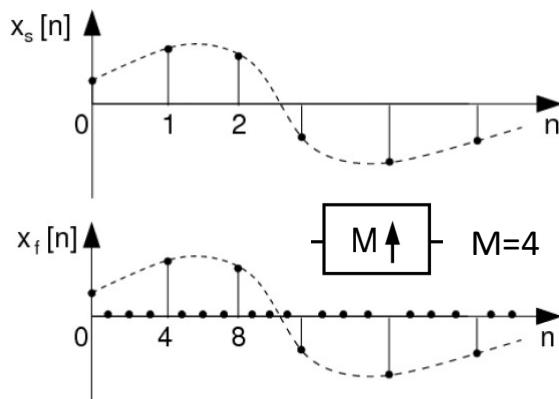
decimation filter



- In reality, there is signal energy between baseband and mirror spectra (e.g. noise)
- Avoid aliasing
  - low-pass filter in front of downsampling block
  - decimation filter (decimator)

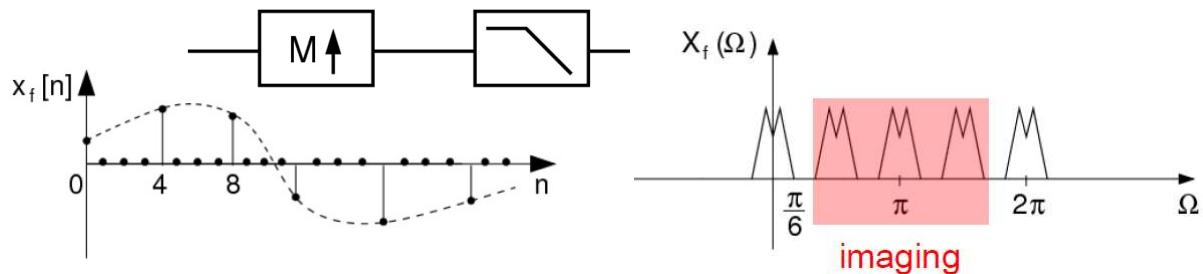


## Upsampling



## Upsampling

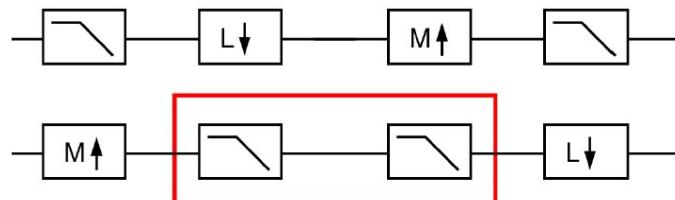
- Zero padding → higher sampling rate
- Imaging → replica in-between 0- $2\pi$
- Low-pass filter removes images
  - frequency domain: replica only at multiples of sampling frequency
  - time domain: zeros move on real signal curve



137

## Fractional Sample Rate Conversion

- Change sample rate by non-integer factor  $M/L$
- Two possibilities:
  - downsampling by  $L$ , upsampling by  $M$
  - upsampling by  $M$ , downsampling by  $L$

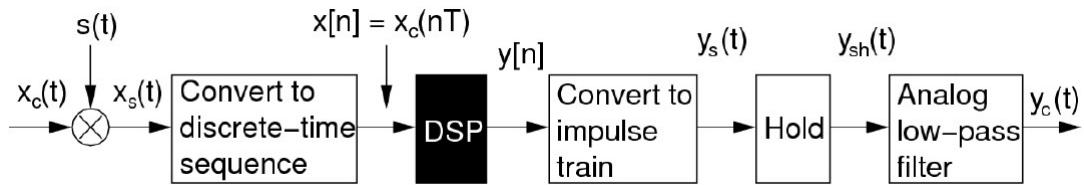


- If  $M$  and  $L$  are relatively prime, the order can be changed without any change in input/output behavior.
- Second option better → shared low-pass filter

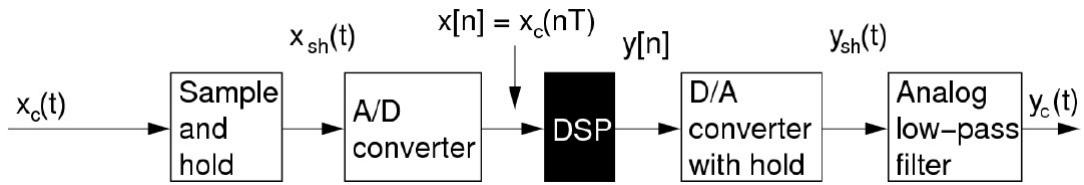
138

# Generic Structure of Mixed-Signal Systems

- System perspective



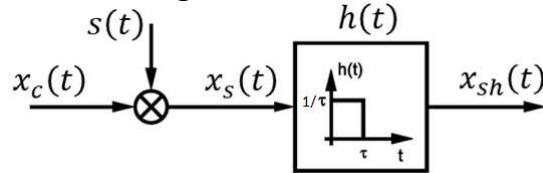
- Circuit perspective



# Tutorial

## Exercise 1

A continuous-time signal  $x_c(t)$  is sampled by a sampling pulse with a non-zero duration  $\tau$ , as described in the figure below.



- For the given signal  $x_c(t)$  sketch the signals  $x_s(t)$  and  $x_{sh}(t)$ . Find a relationship between  $x_{sh}(nT)$  and  $x_c(nT)$ .
- Express through the unity step function a pulse which is non-zero in the interval  $[nT, nT+\tau]$  and has an area of one. The unity step function is:

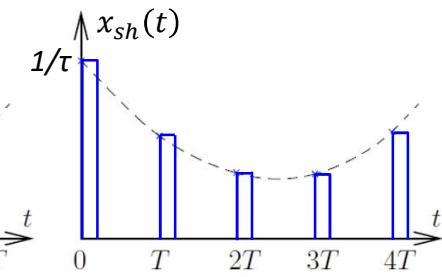
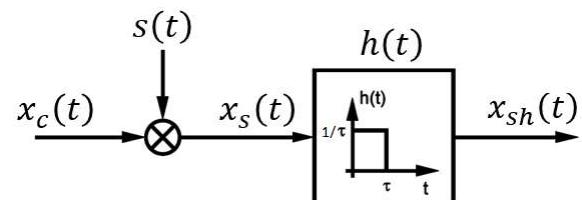
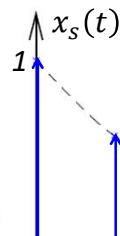
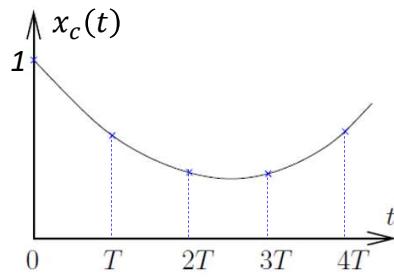
$$u(t) := \begin{cases} 0 & t < 0 \\ 1 & t \geq 0 \end{cases}$$

## Exercise 1 – Solution

a)  $x_{sh}(nT) =$

b)  $h(t) =$

$h_n(t) =$



## Exercise 1

- c) The signal  $x_{sh}(t)$  can be described by a series of weighted pulses, i.e.

$$x_{sh}(t) = \sum_{n=-\infty}^{\infty} x_{sn}(t)$$

Find an expression for  $x_{sn}(t)$ .

- d) Compute  $X_{sn}(\omega)$  and therewith  $X_{sh}(\omega)$ .
- e) Compare the spectrums  $X_{sh}(\omega)$  and  $X_s(\omega)$ . Which term describes the non-zero pulse length? Transform this term back into the time domain and check the result for plausibility.
- f) Calculate this term for  $\tau=T$ .
- g) Compare the limit of  $X_{sh}(\omega)$  when  $\tau$  approaches zero to  $X_s(\omega)$ .



## Exercise 1 – Solution

$$c) x_{sn}(t) = x_c(nT)h_n(t) = \frac{x_c(nT)}{\tau} [u(t - nT) - u(t - nT - \tau)]$$

$$d) X_{sn}(\omega) = \frac{x_c(nT)}{\tau} \int_{-\infty}^{\infty} [u(t - nT) - u(t - nT - \tau)] e^{-j\omega t} dt$$



## Exercise 1 – Solution

$$X_{sn}(\omega) = x_c(nT)e^{-j\omega n} e^{-j\omega\tau/2}\text{sinc}(\omega\tau/2)$$

$$x_{sh}(t) = \sum_n x_{sn}(t)$$

$$\rightarrow X_{sh}(\omega) = \sum_n X_{sn}(\omega)$$

e)  $H(\omega) = e^{-j\omega\tau/2}\text{sinc}(\omega\tau/2)$        $X_{sh}(\omega) = H(\omega)X_s(\omega)$

$$u(t - \tau) \leftrightarrow \frac{e^{-j\omega\tau}}{j\omega}$$

$$H(\omega) = \frac{1}{j\omega\tau} (1 - e^{-j\omega\tau}) \leftrightarrow$$

f)  $\tau = T = 2\pi/\omega_s$

g)



## Exercise 1

- h) What are the challenges of a real implementation of a sampling system with sampling pulses of non-zero duration?
- i) What is the consequence of the non-zero pulse width when the signal is converted to the digital domain?



## Appendix 1 – Spectrum of a Sampled Signal

$$x_s(t) = x_c(t)s(t) \quad \Leftrightarrow X_s(\omega) = \frac{1}{2\pi} X_c(\omega) * S(\omega)$$

$$s(t) = \sum_n \delta(t - nT) \quad \Leftrightarrow S(\omega) = \frac{2\pi}{T} \sum_k \delta(\omega - k\omega_s) \quad \omega_s = 2\pi/T$$

$$\begin{aligned} \rightarrow X_s(\omega) &= \frac{1}{2\pi} X_c(\omega) * S(\omega) = \frac{1}{2\pi} \int_{-\infty}^{\infty} X_c(\omega - \theta) S(\theta) d\theta \\ &= \frac{1}{T} \int_{-\infty}^{\infty} X_c(\omega - \theta) (\sum_k \delta(\theta - k\omega_s)) d\theta \\ &= \frac{1}{T} \sum_k \int_{-\infty}^{\infty} X_c(\omega - \theta) \delta(\theta - k\omega_s) d\theta \\ &= \frac{1}{T} \sum_k X_c(\omega - k\omega_s) \end{aligned}$$



## Appendix 2 – Sample and Hold

$$h(t) = \frac{1}{\tau} [u(t) - u(t - \tau)] \quad x_s(t) = x_c(t) \sum_n \delta(t - nT)$$

$$\begin{aligned} x_{sh}(t) &= x_s(t) * h(t) = \int_{-\infty}^{\infty} x_s(t - \theta) h(\theta) d\theta \\ &= \int_{-\infty}^{\infty} \left( x_c(t - \theta) \sum_{n=-\infty}^{\infty} \delta(t - \theta - nT) \right) h(\theta) d\theta \\ &= \sum_{n=-\infty}^{\infty} \int_{-\infty}^{\infty} \frac{1}{\tau} x_c(t - \theta) [u(\theta) - u(\theta - \tau)] \delta(t - \theta - nT) d\theta \\ &= \sum_{n=-\infty}^{\infty} x_c(nT) \frac{1}{\tau} [u(t - nT) - u(t - nT - \tau)] \end{aligned}$$



# Chapter 4

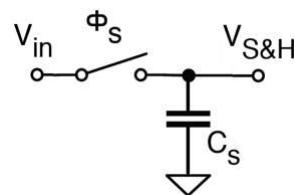
## Sample-and-Hold Circuits

Dr. Florin Burcea (revised by)  
Courtesy of Dr. Stephan Henzler

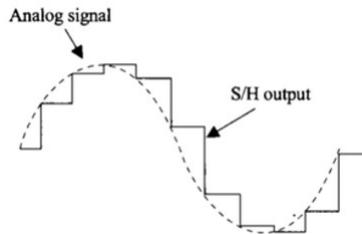


### Sample and Hold (S&H)

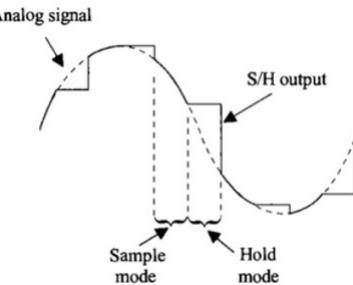
- Switch on: sample (track)
- Switch off: hold



Ideal S&H:

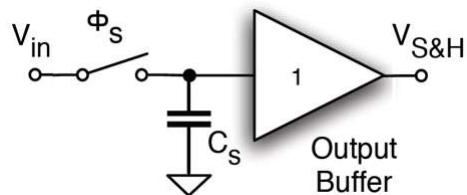


Ideal T&H:

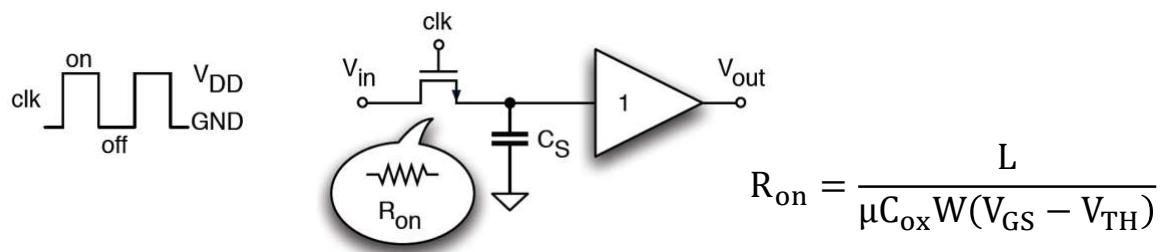


## CMOS S&H: Switch, Capacitor and Buffer

- Buffered output:



- Switch: MOS transistor



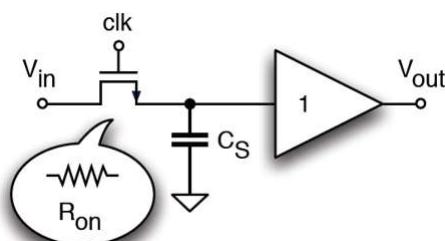
$$R_{on} = \frac{L}{\mu C_{ox} W (V_{GS} - V_{TH})}$$



Illustrations: F. Maloberti, Data Converters, Springer 2007  
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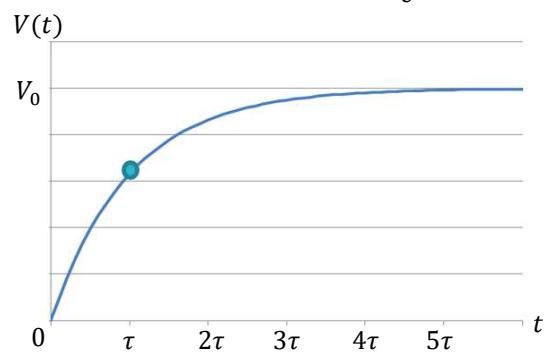
151

## Non-ideality #1: Finite Bandwidth



$$V(t) = V_0 [1 - e^{-t/\tau}]$$

$$\tau = R_{on} C_s = 1 / 2\pi f_c$$



- RC settling time

$$\begin{aligned} 1RC &\approx 62\% \\ 2RC &\approx 86\% \\ 3RC &\approx 95\% \\ 4RC &\approx 98\% \\ 5RC &\approx 99\% \end{aligned}$$

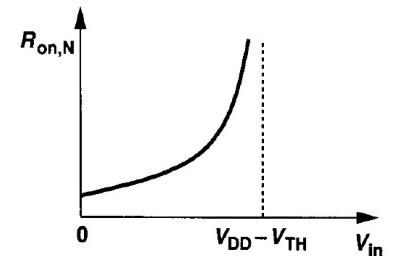
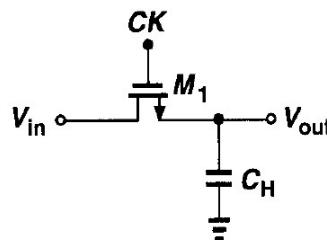


Upper illustration: F. Maloberti, Data Converters, Springer 2007  
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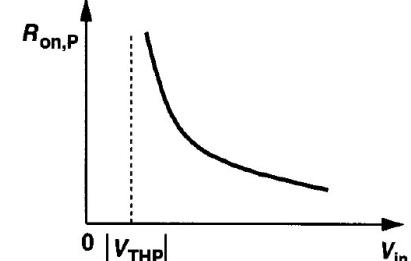
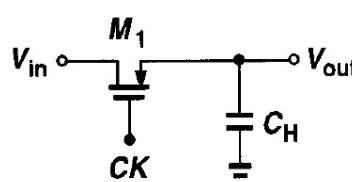
152

## Non-ideality #2: Input Range

- NMOS switch on:



- PMOS switch on:



Switch on:  $V_{out} \approx V_{in}$

$$R_{on} = \frac{L}{\mu C_{ox} W (|V_{GS}| - |V_{TH}|)}$$

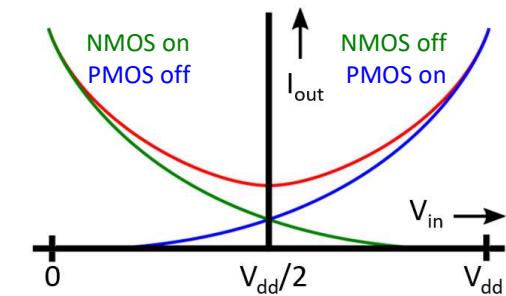
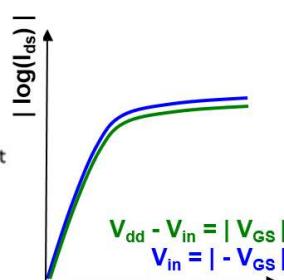
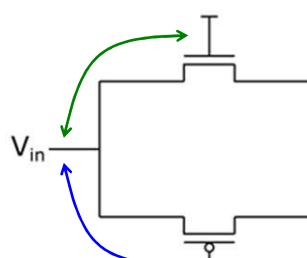


Illustrations: B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill 2001

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153

## CMOS Transmission Gate



- On-resistance  $R_{on}$  at different  $V_{in}$  depends on  $V_{GS}$ .
- n-MOS good at low  $V_{in}$ , p-MOS good at high  $V_{in}$ .
- CMOS transfer gate/transmission gate/pass gate:
  - combination of n- and p-MOS
  - highest on-resistance (lowest conductance) at medium voltages between the rails.



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154

## Non-ideality #3: Non-linearity

- Switch on-resistance:

$$R_{on} = \frac{1}{\beta(V_{GS} - V_{TH})} \quad \beta = \mu C_{ox} \frac{W}{L}$$

- $V_{GS} = V_G - V_S$   
 $V_G = V_{DD}$ : constant,  $V_S \cong V_{in}$ : varying  
 →  $V_{GS}$  varying  
 →  $R_{on}$  dependent on the input signal  
 → RC constant time-dependent  
 → distortion, non-linearity

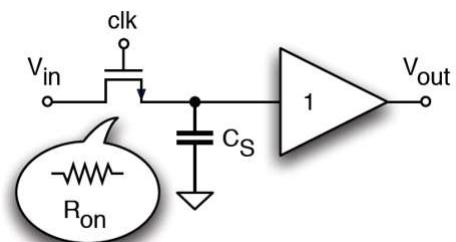
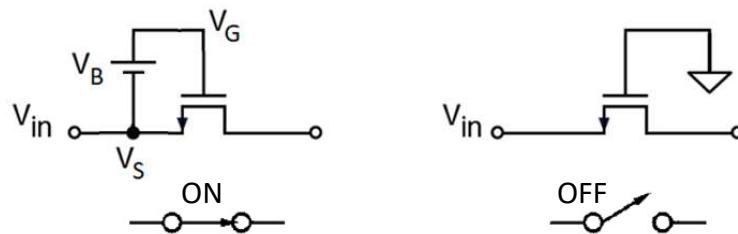


Illustration: F. Maloberti, Data Converters, Springer 2007  
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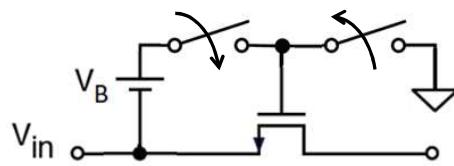
155

## Bootstrapped Switch

- $V_S$  varying → make similar kind of variation in  $V_G$   
 $V_{GS}=V_B$  constant



- Additional switches needed to turn off the main switch
- Bootstrap circuit:



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156

## Bootstrapped Switch

- Bootstrapping battery  $V_B$ : implemented as capacitor  $C_B$

- Hold phase

- $M_1$  off
- $C_B$  charges to  $V_{DD}$

- Track phase

- $C_B$  charged to  $V_{DD}$
- $V_{GS1} = V_{DD}$
- $M_1$  on

- Bootstrapping:

- improves linearity/reduces distortion
- increases input range

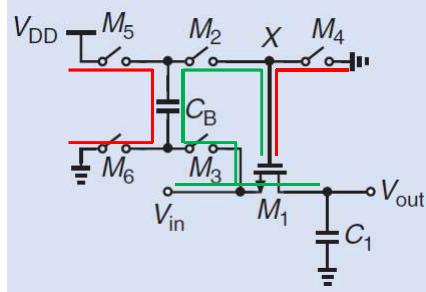
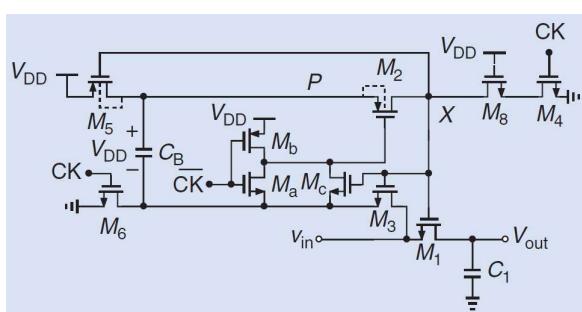


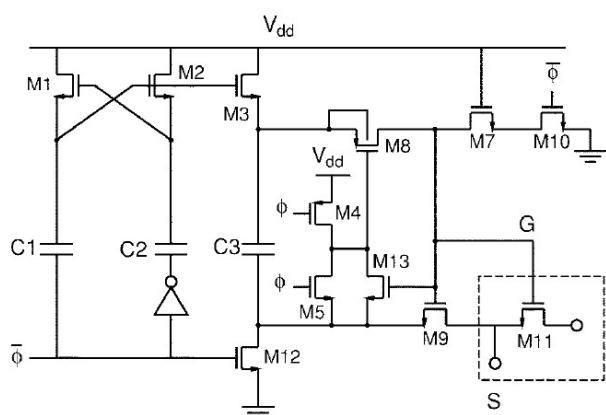
Illustration: B. Razavi, The Design of a Bootstrapped Sampling Circuit, IEEE SSC Magazine, 2021  
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157

## Bootstrapped Switch – Practical Examples



B. Razavi, The Design of a Bootstrapped Sampling Circuit,  
IEEE SSC Magazine, 2021



A. Abo and P. Gray, A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline  
Analog-to-Digital Converter, IEEE JSSC, 1999



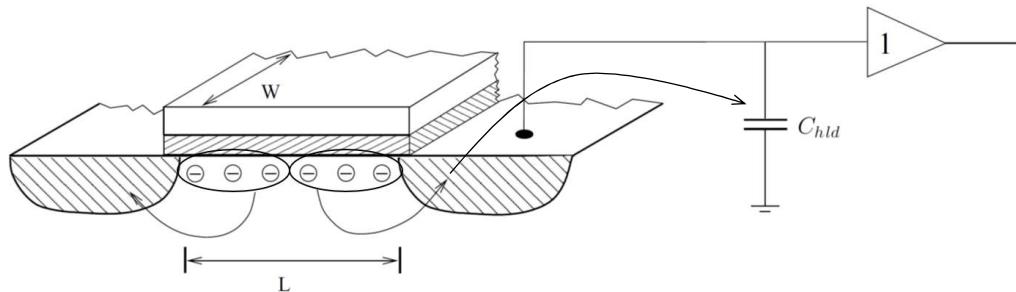
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158

## Non-ideality #4: Charge injection

- Transistor switched off  $\rightarrow$  mobile carriers removed
- Channel gets cut  $\rightarrow$  charge from one side stored on  $C_{\text{hld}}$
- 1:1 approximation for fast switching

$$\Delta Q = \frac{1}{2} Q_{\text{ch}} = -\frac{1}{2} W L C_{\text{ox}} (V_{\text{gs}} - V_{\text{th}}) \Rightarrow \Delta V_{\text{out}} = \frac{\Delta Q}{C_{\text{hld}}}$$



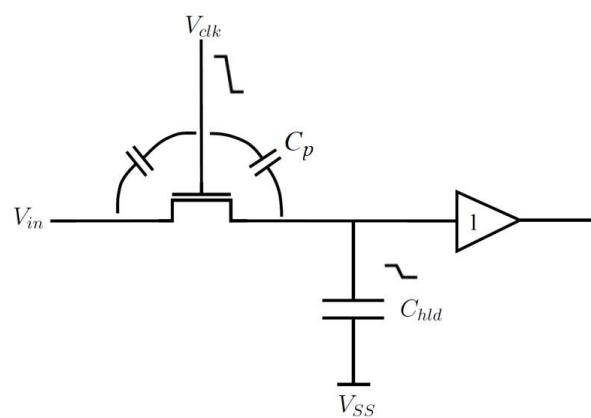
159

## Non-ideality #5: Clock Feedthrough

- Capacitive coupling
- Capacitive divider

$$\Delta V_{\text{clk}} = V_{\text{SS}} - V_{\text{DD}}$$

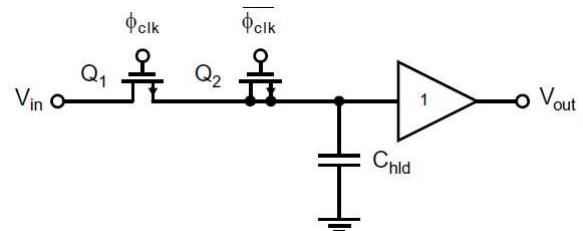
$$\Delta V_{\text{out}} = \frac{C_p}{C_p + C_{\text{hld}}} \Delta V_{\text{clk}}$$



160

## Dummy Transistor

- Compensates (completely in the first-order assumption)
  - charge injection
  - clock feedthrough
- $W_{\text{dummy}} = (1/2)W_{\text{switch}}$   
 $L_{\text{dummy}} = L_{\text{switch}}$



- Other measures against charge injection and clock feedthrough (however, only partial compensation, even in the first-order assumption)
  - CMOS transmission gate: complementary switches
  - differential sampling: error appears only as common-mode

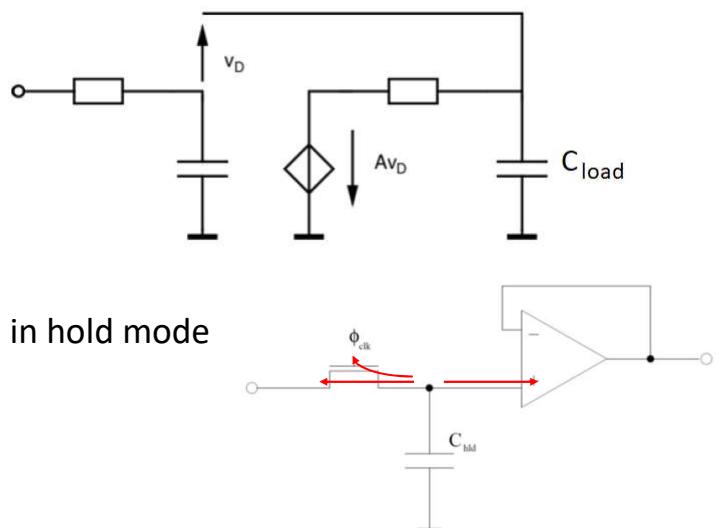


Illustration: T. Carusone, D. Johns, K. Martin, Analog Integrated Circuit Design, Wiley 2012  
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161

## Non-idealities #6-7

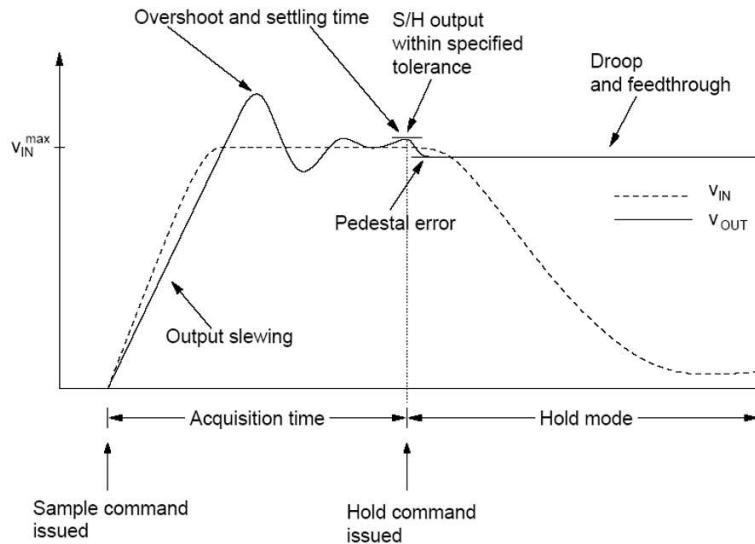
- Buffer dynamics
  - Finite settling time
  - Output slewing
  - Overshoot
  - Ringing
  - Varying load impedance
- Leakage (droop) currents  
 $\rightarrow$  discharge hold capacitance in hold mode



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162

## S&H Output Signal



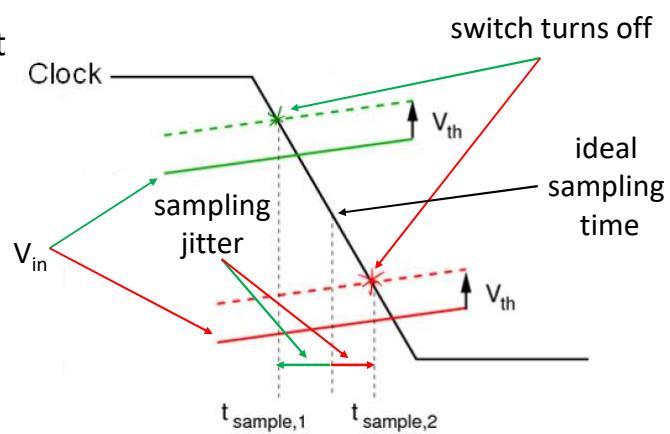
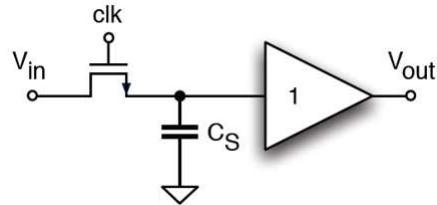
163



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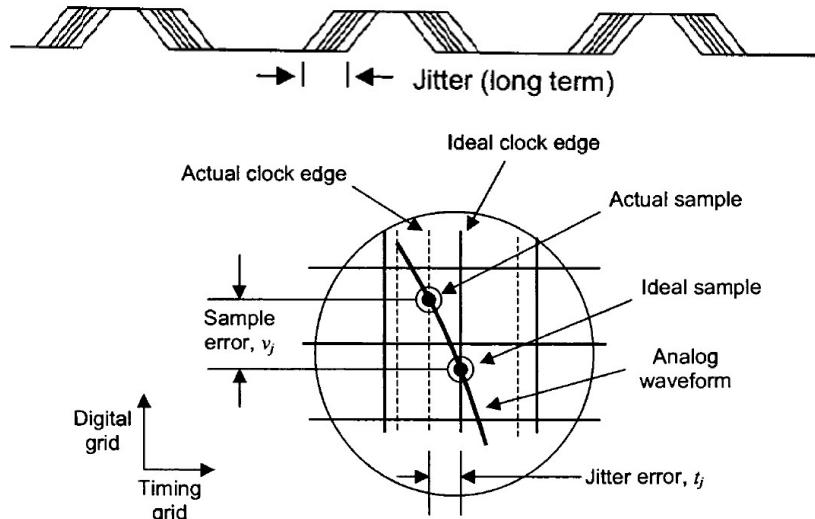
## Non-ideality #8: Sampling (Aperture) Jitter

- Finite slope of clock signal → sampling time jitter
  - signal dependent
  - threshold voltage dependent

Left illustration: F. Maloberti, Data Converters, Springer 2007  
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164

## Non-ideality #9: Clock Jitter



Illustrations: M. Burns, G. Roberts, An Introduction to Mixed-Signal IC Test and Measurement, Oxford 2001

165

## Impact of Jitter on S&H Performance

- Sinusoidal signal:  $v(t) = A \cdot \sin(\omega t)$
- Signal power:  $\overline{v^2} = \frac{A^2}{2}$
- Rate of change:  $\frac{dv(t)}{dt} = A\omega \cdot \cos(\omega t)$
- Jitter: random variation of sampling instance

$$t_s = nT + \Delta t_n$$

$$p_{\Delta t} = \frac{1}{\sqrt{2\pi}\sigma} \exp\left(-\frac{\Delta t^2}{2\sigma^2}\right)$$

- Sampling error:

$$\Delta v = \frac{dv(t)}{dt} \cdot \Delta t = A\omega \Delta t \cdot \cos(\omega t)$$

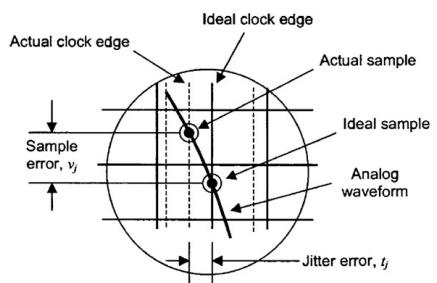


Illustration: M. Burns, G. Roberts, An Introduction to Mixed-Signal IC Test and Measurement, Oxford 2001  
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166

## Impact of Jitter on S&H Performance

- Noise power resulting from sampling error:

$$\overline{\Delta v^2} = \int_0^T \int_{-\infty}^{\infty} \Delta v^2 p_{\Delta t} p_t d(\Delta t) dt$$

$$p_{\Delta t} = \frac{1}{\sqrt{2\pi}} \exp\left(-\frac{\Delta t^2}{2\sigma^2}\right) \quad p_t = \frac{1}{T}$$

$$\bullet \overline{\Delta v^2} = A^2 \omega^2 \frac{1}{T} \int_0^T \cos^2(\omega t) dt \int_{-\infty}^{\infty} \Delta t^2 p_{\Delta t} d(\Delta t) = \frac{1}{2} A^2 \omega^2 \sigma^2$$

- Signal-to-noise ratio:  $\text{SNR} = 10 \log_{10} \frac{\overline{v^2}}{\overline{\Delta v^2}} = 20 \log_{10} \frac{1}{\omega \sigma}$

- maximum achievable SNR for given jitter
- frequency dependent: larger bandwidth → higher clock requirements

## Non-ideality #10: Sampling Noise



- Resistance → white noise with power spectral density:  $\overline{v_n^2} = 4kTR_s$
- Low-pass filter →  $H(j\omega) = \frac{1}{1+j\omega R_s C_s}$
- Sampled noise power spectral density:  $\overline{v_{n,C_s}^2}(\omega) = \frac{4kTR_s}{1+(\omega R_s C_s)^2}$
- Total noise power (referred to 1Ohm):  $P_{n,C_s} = \int_0^{\infty} \overline{v_{n,C_s}^2}(f) df$

## Non-ideality #10: Sampling Noise

- Total noise power:

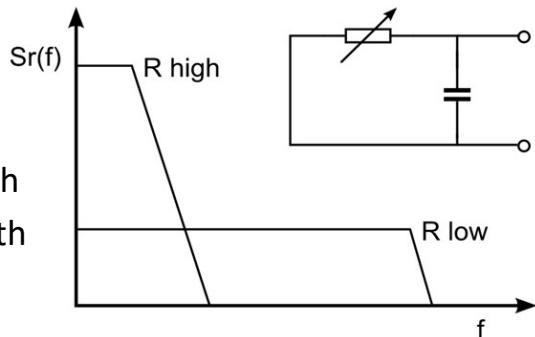
$$P_{n,C_s} = \int_0^\infty v_{n,C_s}^2(f) df = 4kT R_s \int_0^\infty \frac{1}{1+(2\pi f R_s C_s)^2} df = \dots = \frac{kT}{C_s}$$

→ independent of  $R_s$

- Voltage noise on capacitor

$$v_{n_{rms},C_s} = \sqrt{P_{n,C_s}} = \sqrt{\frac{kT}{C_s}}$$

- Low  $R$ : low voltage noise & high bandwidth
- High  $R$ : high voltage noise & low bandwidth
- Total noise = area under graph = constant



169

## Non-ideality #10: Sampling Noise

- $kT/C$  noise:

- independent of  $R_s$
- fundamental limit: minimum amount of noise at every sampling point (extra noise may get sampled along with the signal)

- Noise reduction techniques:

- **oversample** (sample the same input signal multiple times) and **average**

$$\text{Noise power} \propto \frac{1}{\text{OSR}}$$

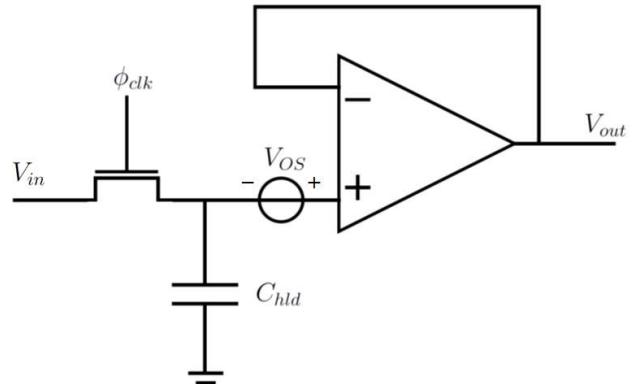
OSR: oversampling ratio

- increase sampling capacitance → must settle within given time → requires higher power of driver/buffer

170

## Non-ideality #11: Offset

- Offset voltage of opamp  
→ modeled as voltage source in series with the input
- Offset voltage directly visible at output terminal  
→  $V_{out} = V_{in} + V_{os}$



171

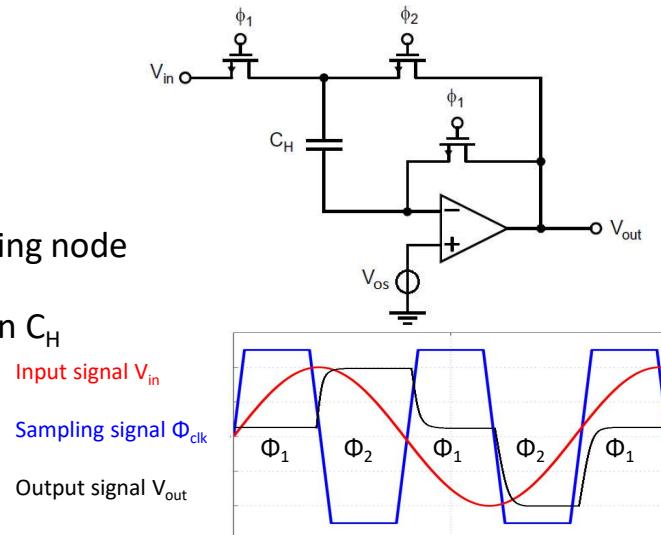
## Auto-Zeroing

- Class of dynamic techniques for offset cancellation
- Sample offset, then subtract
- Sampled data technique, discrete-time
- Example: correlated double sampling

172

## Correlated Double Sampling

- Phase  $\Phi_1$ :
  - opamp = voltage follower
  - $V_{\text{out}} = V_{\text{os}}$
  - $V_C = V_{\text{in}} - V_{\text{os}}$  (tracking  $V_{\text{in}}$ )
- Phase  $\Phi_2$ :
  - opamp negative input  $\rightarrow$  floating node  
 $\rightarrow$  no capacitor discharge
  - $\rightarrow$  sampled  $V_C$  remains stored on  $C_H$
  - $V_{\text{out}} = V_C + V_{\text{os}} = V_{\text{in}}$



Upper illustration: T. Carusone, D. Johns, K. Martin, Analog Integrated Circuit Design, Wiley 2012

173

## Offset Reduction Techniques – Summary

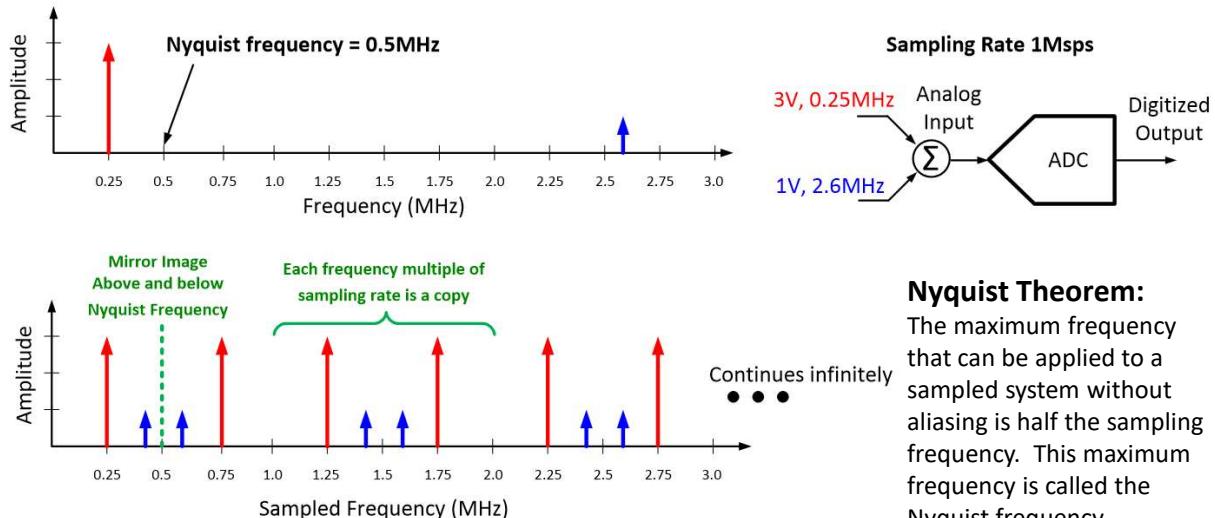
- Static: trimming
- Dynamic
  - **Auto-zeroing** (e.g. correlated double sampling):
    - sample offset, then subtract
    - discrete time
  - Chopping:
    - modulate offset, then filter
    - continuous time (input/output signal continuously available)



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174

## Non-ideality #12: Aliasing



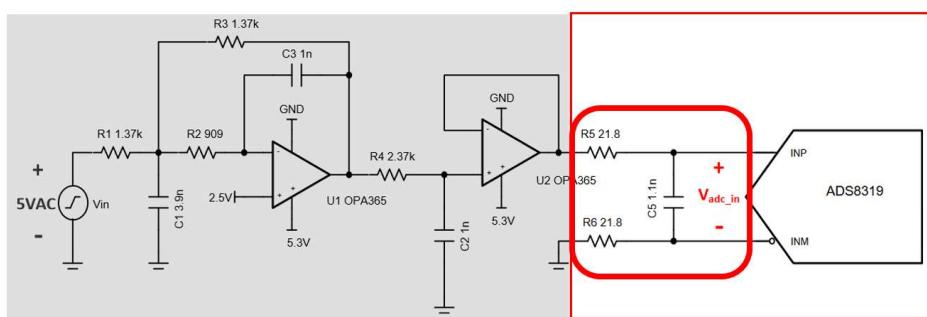
### Nyquist Theorem:

The maximum frequency that can be applied to a sampled system without aliasing is half the sampling frequency. This maximum frequency is called the Nyquist frequency.



## Input Anti-aliasing Filter

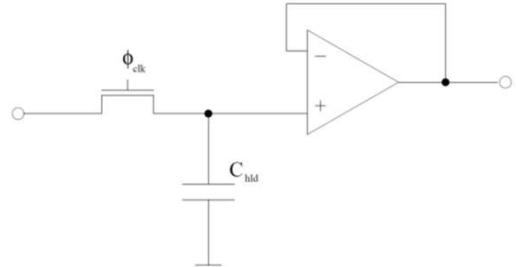
- It is essential to remove high-frequency noise and signals before sampling
- Antialiasing low-pass filter is a must at the input of an A/D converter!
  - Always an analog filter.
  - Simple RC LPF is usually enough.
  - Complex active filters are sometimes used.



# Tutorial

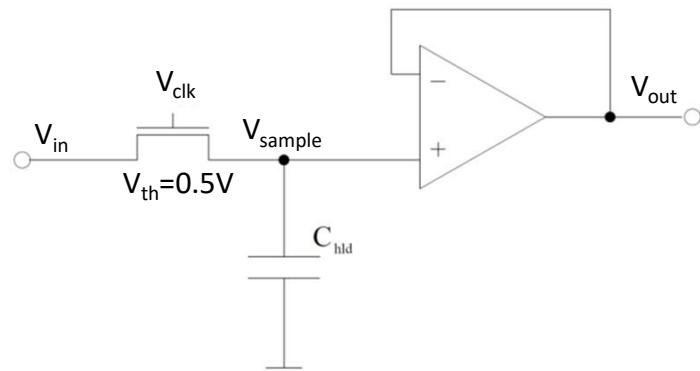
## Exercise 1

- a) What limits the speed of this basic sample&hold circuit?
- b) How to size the hold capacitance  $C_{\text{hld}}$  if the sampling frequency is to be increased? What is the disadvantage?



## Exercise 2

- Mark the ideal and the real sample times. The NMOS switch has  $V_{th}=0.5V$ .
- Sketch the output signal considering:
  - sampling jitter
  - output slewing
  - leakage

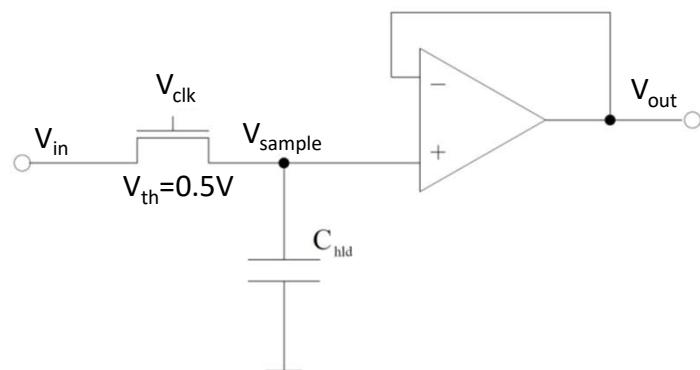


179

## Exercise 2 – Solution

- To sample:

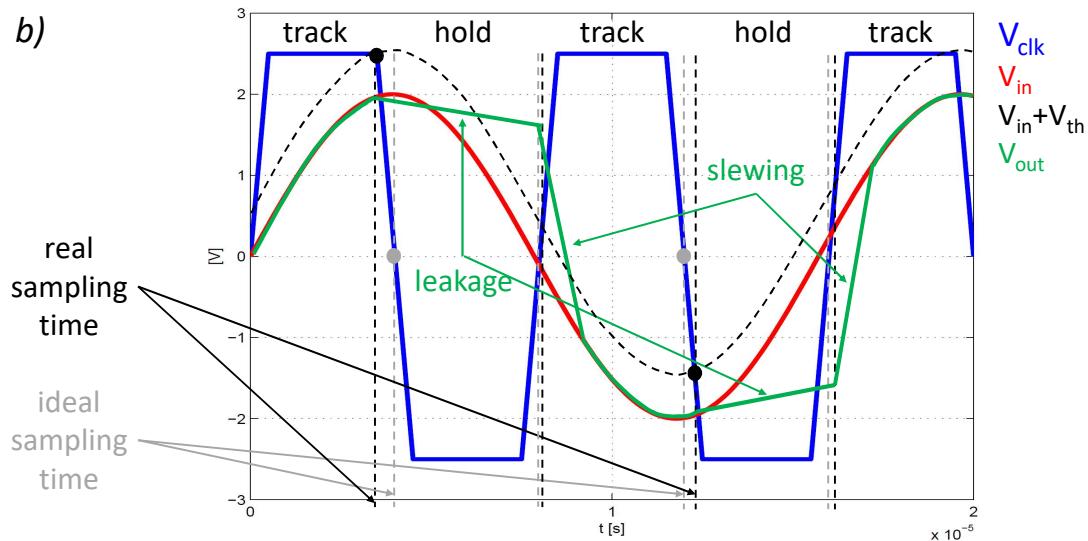
$$\begin{aligned} V_{sample} &\approx V_{in} \\ V_{GS} - V_{th} &> 0 \end{aligned}$$



180

## Exercise 2 – Solution

b)



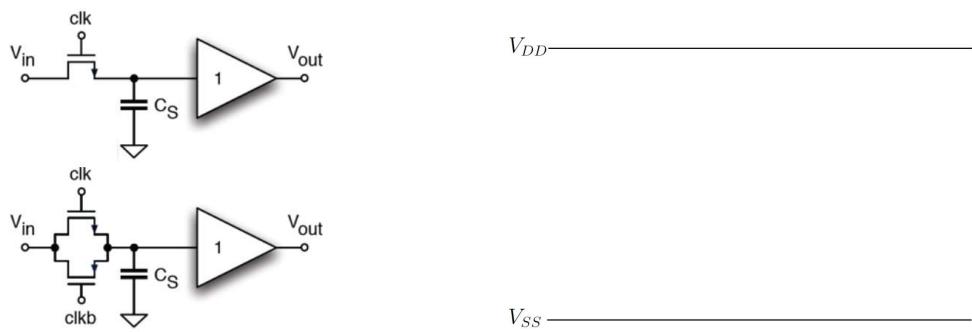
181



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## Exercise 3

- What is the difference between an NMOS pass gate and a CMOS transmission gate with respect to the input voltage?
- What is the difference between a CMOS transmission gate and an ideal switch?

Left illustrations: F. Maloberti, Data Converters, Springer 2007  
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182

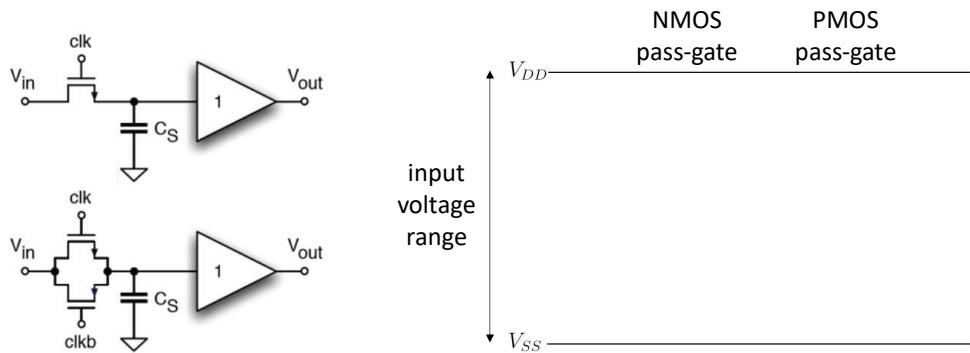
## Exercise 3 – Solution

a)

NMOS on:

PMOS on:

*CMOS transmission gate can conduct over the full input range*



Left illustrations: F. Maloberti, Data Converters, Springer 2007

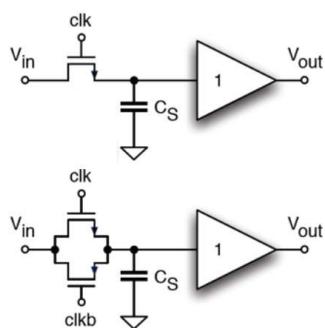
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183

## Exercise 3 – Solution

b) Compared to an ideal switch, CMOS transmission gate has:

- on resistance
- capacitive coupling
- leakage currents



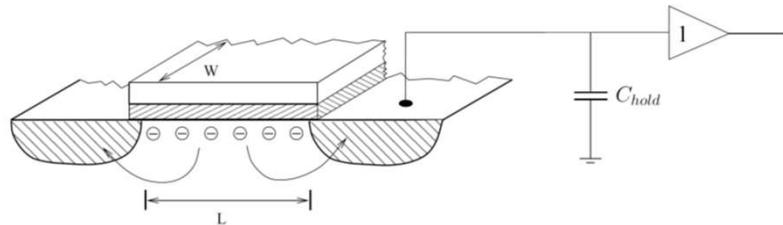
Left illustrations: F. Maloberti, Data Converters, Springer 2007

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184

## Exercise 4

- Calculate the error of the output signal due to charge injection in dependence of the switch sizing and the hold capacitance.
- Is the error signal-dependent? What is the consequence?



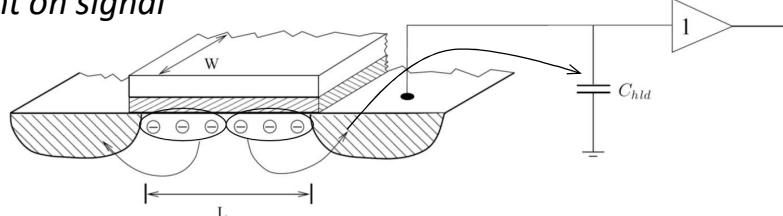
185

## Exercise 4 – Solution

- Total channel charge:  $Q_{ch} = -WLC_{ox}(V_{gs} - V_{th})$   
We assume half of the charge goes to  $C_{hld}$

- Error: linearly dependent on signal

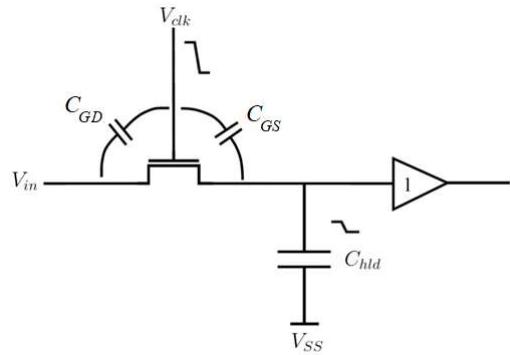
→ gain error  
+ constant term  
→ offset error



186

## Exercise 5

- Calculate the ratio between the hold capacitance and the gate-source capacitance for a clock feedthrough error smaller than 100mV (in absolute value). The rail-to-rail supply voltage is  $V_{DD}-V_{SS}=5V$ .
- Is the clock feedthrough error signal-dependent?



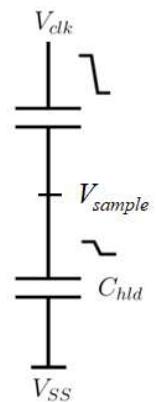
187



## Exercise 5 – Solution

a)  $V_{clk} = V_{DD} \rightarrow$   
 $V_{clk} = V_{SS} \rightarrow$

- b) Clock feedthrough error: constant  
 $\rightarrow$  offset error



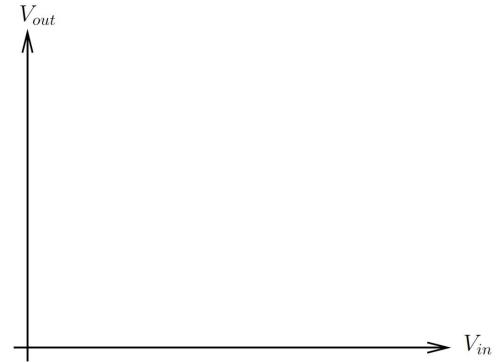
188



## Exercise 6

What is the output voltage of the sample & hold circuit considering the errors calculated in the previous two exercises?

Draw the characteristic and discuss the results.



189

## Exercise 6

*charge injection:*

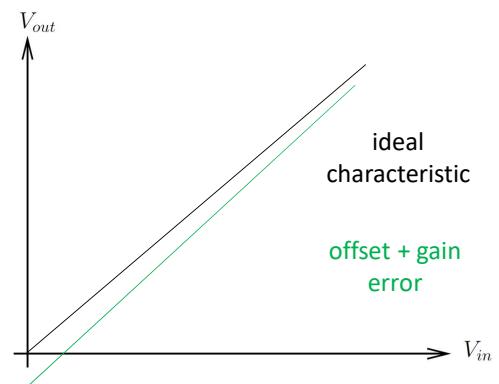
*(linearly) signal-dependent error →*

$$\begin{aligned}\Delta V_{out} = \Delta V_{sample} &= \frac{\Delta Q}{C_{hld}} = -\frac{1}{2} \frac{WL C_{ox}}{C_{hld}} (V_{dd} - V_{in} - V_{th}) \\ &= -\frac{1}{2} \frac{WL}{C_{hld}} C_{ox} (V_{dd} - V_{th}) + \frac{1}{2} \frac{WL}{C_{hld}} C_{ox} V_{in}\end{aligned}$$

*clock feedthrough:*

*constant error →*

$$\Delta V_{out} = -\frac{C_{GS}}{C_{GS} + C_{hld}} (V_{DD} - V_{SS})$$



190

## Exercise 7

Insert a dummy transistor to compensate for charge injection and clock feedthrough.

- What signal should drive the dummy gate?
- Find the dimensions of the dummy transistor. Show that the dummy transistor with these dimensions compensates the two errors.

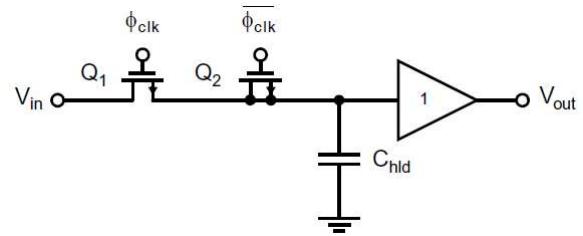


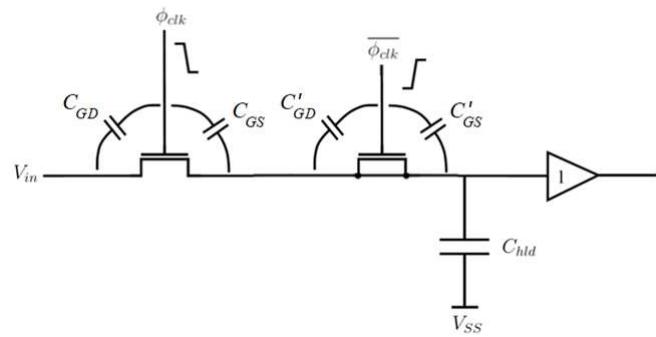
Illustration: T. Carusone, D. Johns, K. Martin, Analog Integrated Circuit Design, Wiley 2012

191

## Exercise 7 – Solution

- The opposite of the clock signal.
- $W_{\text{dummy}} = (1/2)W_{\text{switch}}$   
 $L_{\text{dummy}} = L_{\text{switch}}$

charge injection:



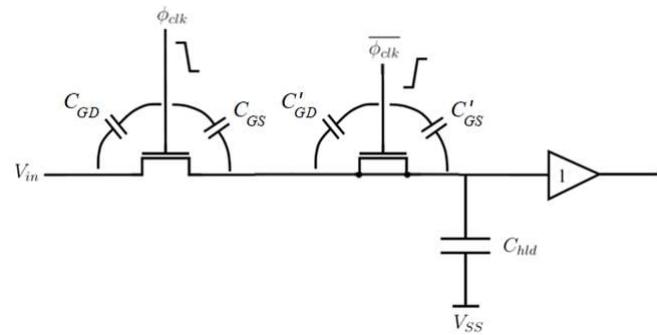
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192

## Exercise 7 – Solution

b) clock feedthrough:

*Superposition* →

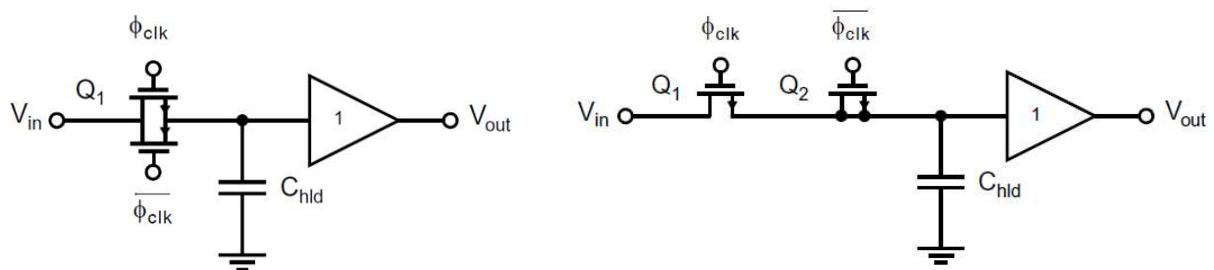


*The dummy transistor does not completely cancel, but minimizes the errors.*



## Exercise 8

Compare a CMOS transmission gate with an NMOS pass gate with dummy transistor with respect to charge injection and clock feedthrough.



## Exercise 8 – Solution

- NMOS pass gate with dummy  
charge injection cancelled irrespective of input voltage (in a 1st-order approximation) → see ex. 7
- CMOS transmission gate  
NMOS and PMOS have inverse carries → charge injection reduced  
To cancel completely:  
 $\Delta Q_n + \Delta Q_p = 0$   
 $\rightarrow (1/2)(WL)_n C_{ox} (V_{DD} - V_{in} - V_{th,n})$   
 $= (1/2)(WL)_p C_{ox} (V_{in} - V_{SS} - |V_{th,p}|)$   
 $\rightarrow (WL)_n (V_{DD} - V_{in} - V_{th,n}) = (WL)_p (V_{in} - V_{SS} - |V_{th,p}|)$   
 $\rightarrow$  cancellation occurs only for one input voltage

## Exercise 8 – Solution

- NMOS pass gate with dummy  
clock feedthrough cancelled (in a 1st order approximation) → see ex. 7
- CMOS transmission gate  

$$\Delta V_{sample} = \frac{C_{GS,n}}{C_{GS,n} + C_{GS,p} + C_{hld}} \Delta V_{clk} + \frac{C_{GS,p}}{C_{GS,n} + C_{GS,p} + C_{hld}} (-\Delta V_{clk})$$

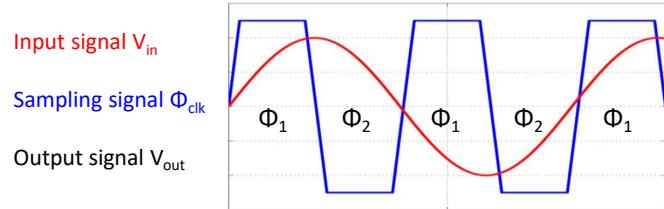
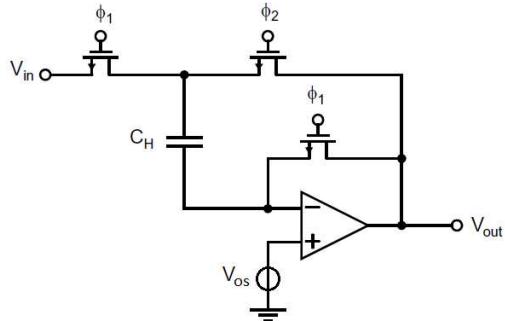
$$= \frac{C_{GS,p} - C_{GS,n}}{C_{GS,n} + C_{GS,p} + C_{hld}} (V_{DD} - V_{SS})$$

Gate-source capacitances of NMOS and PMOS are not equal  
→ clock feedthrough reduced, but not cancelled completely

## Exercise 9

Consider the following circuit with correlated double sampling.

- Sketch the output signal.
- What requirements do you expect for the operational amplifier?
- Discuss the effect of charge injection in this circuit.



Left illustration: T. Carusone, D. Johns, K. Martin, Analog Integrated Circuit Design, Wiley 2012  
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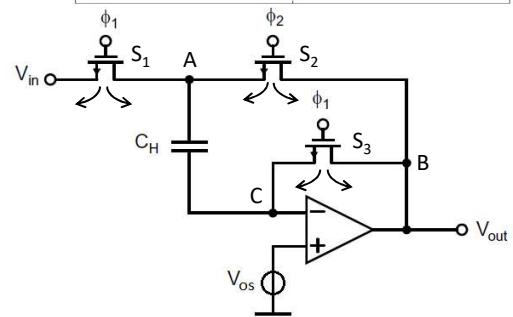
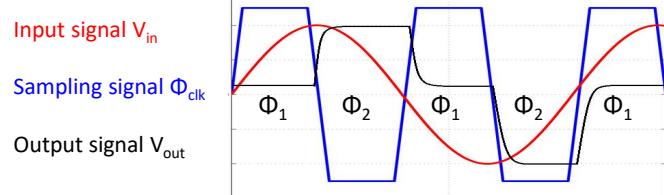
197

## Exercise 9 – Solution

a)

- b) - Good slew rate  
- Fast settling (enough phase margin but not too much)

- c) - node A: charge from  $S_1$  injected to  $S_2$  and viceversa  $\rightarrow$  charge cancels;  
also: low-impedance on both phases  
- node B: low-impedance node,  
circuit operation not affected  
- node C: high-impedance node,  
charge from  $S_3$  injected  $\rightarrow$  offset error



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198

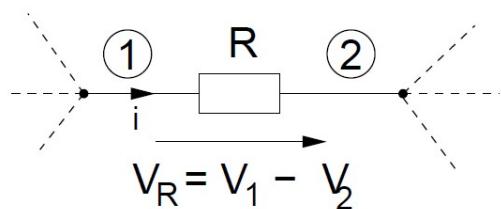
# Chapter 5

## Switched-Capacitor Circuits

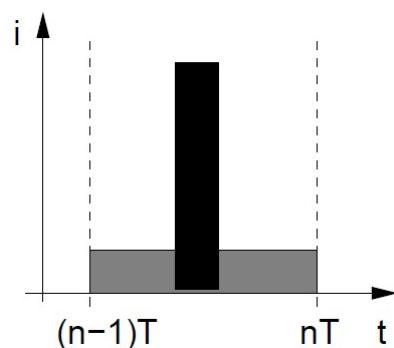
Dr. Florin Burcea (revised by)  
Courtesy of Dr. Stephan Henzler



### Effect of Resistor Between Two Nodes

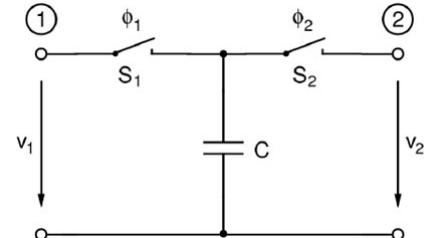


- Continuous-time point of view:  
 $i = \frac{V_1 - V_2}{R}$  → in a short time interval  $\Delta t$ , charge  $\Delta q = i \cdot \Delta t$  transferred from ① to ②.
- Discrete-time point of view:
  - state at discrete instances  $nT$  relevant
  - state transition not relevant



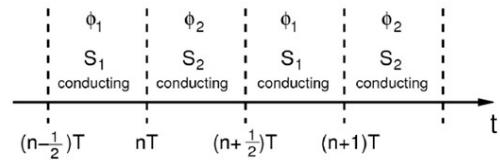
## Switched-Capacitor Resistor Emulation

- $t = nT$  ( $S_1$  on,  $S_2$  off):



- $t = (n + 1/2)T$  ( $S_1$  off,  $S_2$  on):

- Charge  $\Delta Q$  pumped from ① to ②:



- Average current:

- Equivalent resistance:**

201

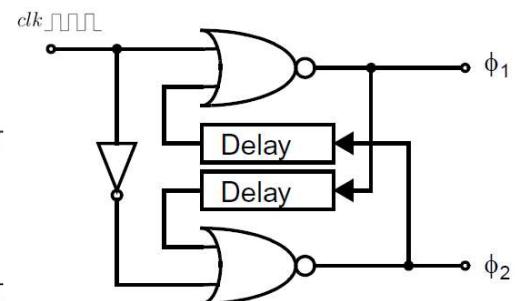
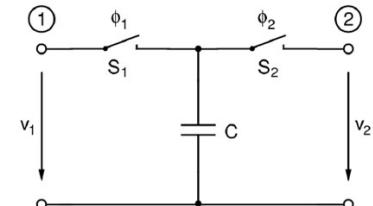
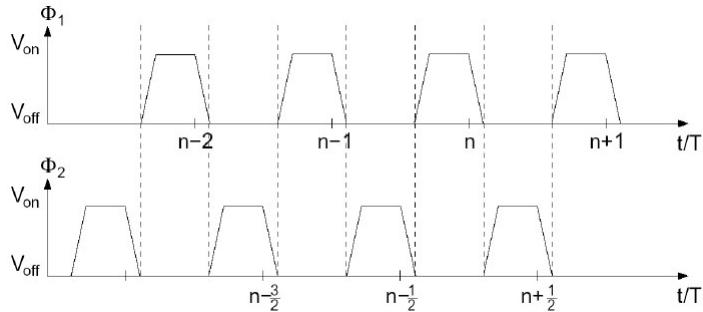
## Resistor Equivalents

circuit	equivalent resistor	type	
parallel equivalent	$\frac{T}{C}$	transimpedance	
series equivalent	$\frac{T}{C}$	resistance or transimpedance	
bilinear equivalent	$\frac{T}{4C}$	resistance or transimpedance	

202

## Non-overlapping Multiphase Clocking

- Both clocks active at the same time would cause short-circuit currents



203



## Parameter Variation in SC Circuits

- Variation of an RC time constant:

$$\tau = RC$$

- $dC/C, dR/R$ : typically 20-30%, statistically **uncorrelated**



204

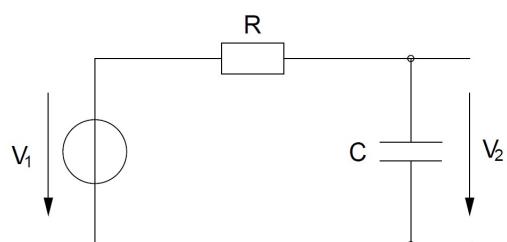
## Parameter Variation in SC Circuits

- Switched-capacitor equivalent:

$$R_{eq} = \frac{T}{C_{sc}} \rightarrow \tau = T \frac{C}{C_{sc}}$$

- $C, C_{sc}$ : matched devices  
 →  $dC/C, dC_{sc}/C_{sc}$ : statistically **correlated**  
 →  $\frac{d(C/C_{sc})}{(C/C_{sc})}$ : very small

## Continuous-Time RC Low-Pass Filter



$$H(j\omega) = \frac{V_2(j\omega)}{V_1(j\omega)} = \frac{1}{1 + j\omega/\omega_p}$$

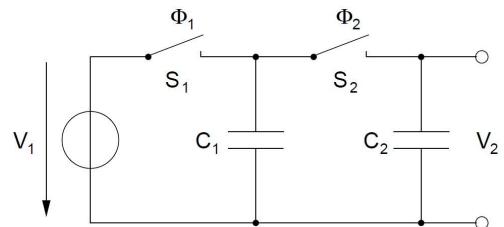
$$\omega_p = 1/(RC)$$

## Switched-Capacitor Low-Pass Filter

- $t = (n - 1)T$ :  $S_1$  on,  $S_2$  off

- $t = (n - 1/2)T$ :  $S_1$  off,  $S_2$  on

- $t = nT$ :  $S_1$  on,  $S_2$  off



207

## Limitations of SC Equivalence

- Z-transform:

$$V_2(z) = \frac{C_1 z^{-1} V_1(z) + C_2 z^{-1} V_2(z)}{C_1 + C_2}$$

$$H(z) = \frac{V_2(z)}{V_1(z)} = \frac{1}{z(1+\alpha)-\alpha}$$

$$x[n-1] \rightarrow z^{-1}X(z)$$

$$\alpha := \frac{C_2}{C_1}$$

$$\text{continuous-time: } H(j\omega) = \frac{1}{1+j\omega/\omega_p}$$

$$z = e^{j\omega} = \cos(\omega T) + j \sin(\omega T) \cong 1 + j\omega T$$

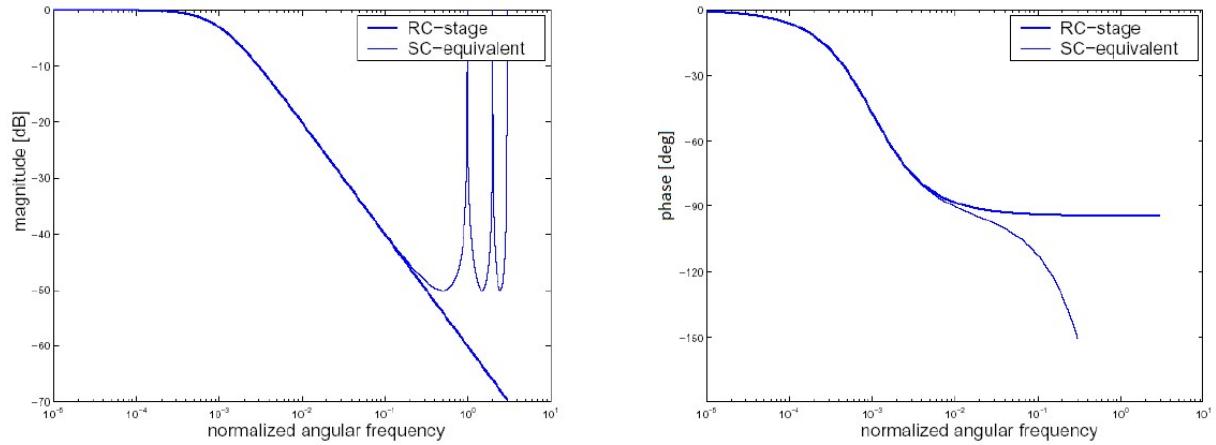
$$\omega T \ll 1 \\ (\text{small frequencies})$$

$$H(j\omega) = \frac{1}{(1+\alpha) \cos(\omega T) - \alpha + j(1+\alpha)\sin(\omega T)} \cong \frac{1}{1+j\omega(1+\alpha)T}$$

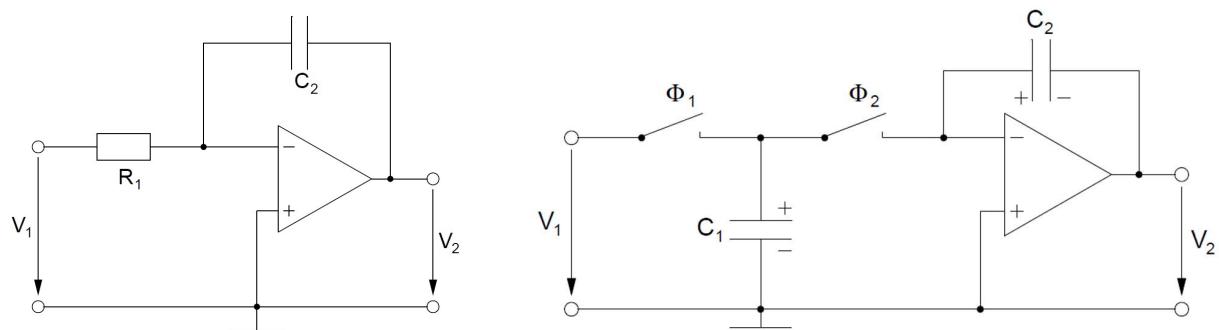
$$1/\omega_p = (1 + \alpha)T$$

208

## Limitations of SC Equivalence



## Switched-Capacitor Integrator

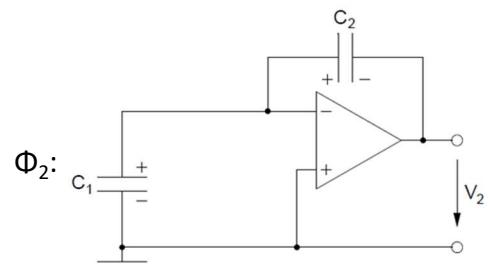
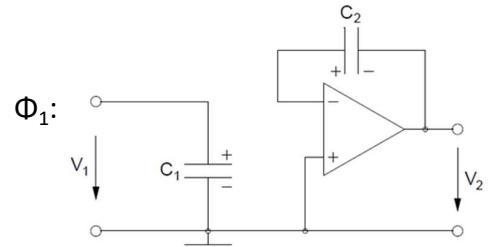


Continuous-time integrator:

$$H(j\omega) = -\frac{1}{j\omega/\omega_0} \quad \omega_0 = \frac{1}{R_1 C_2}$$

## SC Integrator – Charge Balance Analysis

- $\Phi_1: t = (n - 1)T$
- $\Phi_2: t = (n - 1/2)T$



211

## SC Integrator – Spectral Analysis

$$V_2[n] = V_2[n-1] - \frac{C_1}{C_2} V_1[n-1]$$

- Z-transform:

- Approximation on unit circle:

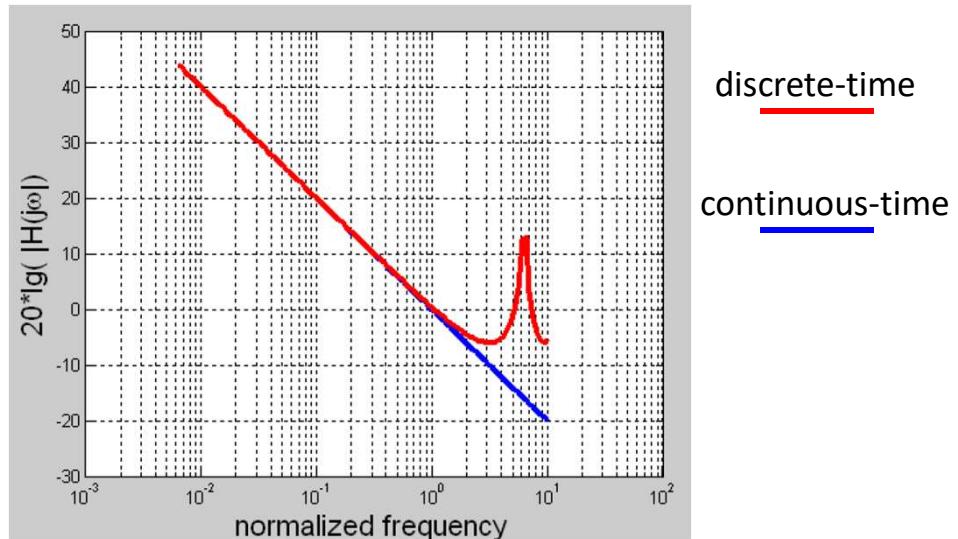
$$H(j\omega) = -\frac{C_1}{C_2} \frac{\exp(-j\omega T/2)}{2j \sin(\omega T/2)} \cong -\frac{C_1}{C_2} \frac{1}{j\omega T}$$

$$\omega_0 = \frac{C_1}{TC_2} \equiv \frac{1}{R_1 C_2}$$

$$\text{continuous time: } H(j\omega) = -\frac{1}{j\omega/\omega_0}$$

212

## Spectral Analysis



213

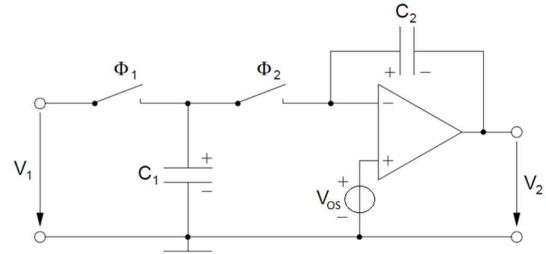
## Analysis of Switched-Capacitor Circuits (Cookbook)

1. Mark polarity of all capacitors, such that the positive plates are connected to the floating node. Do not change this polarity during the analysis.
2. Draw equivalent circuits for each clock phase.
3. Charge conservation analysis for full cycle
  - assume steady-state conditions for each time step
  - compute  $Q_{\text{tot}}$  at the floating node(s)
4. Apply Z-transform
5. Calculate transfer function
6. Evaluate transfer function on unit circle of Z-plane

214

## SC Integrator – Impact of Offset

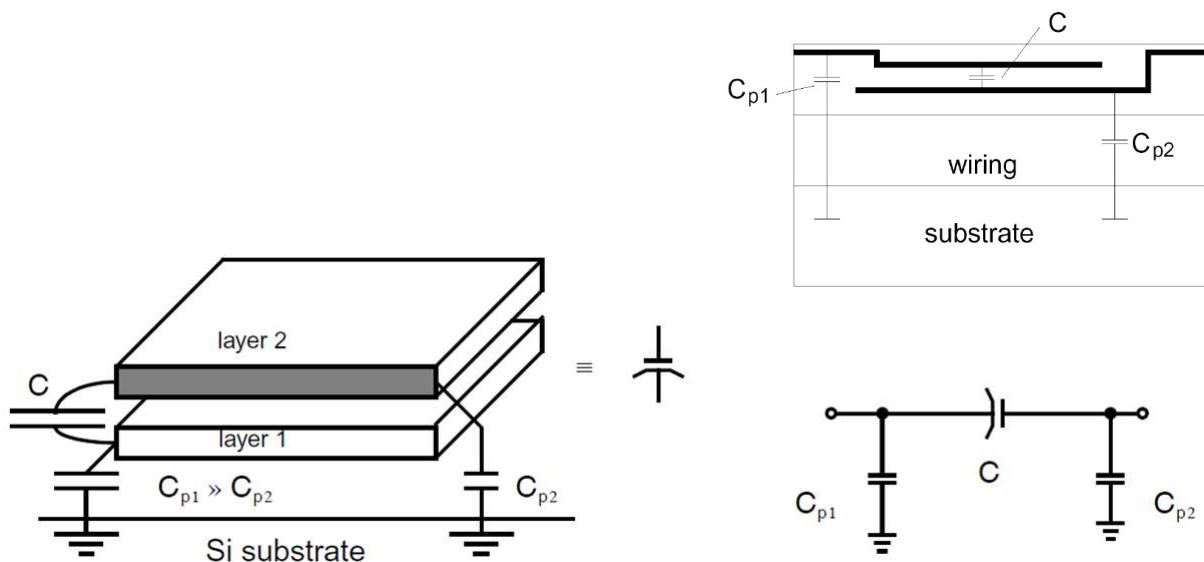
- $\Phi_1$ :  $t = (n - 1)T$
- $\Phi_2$ :  $t = (n - 1/2)T$



- $\Phi_1$ :  $t = nT$

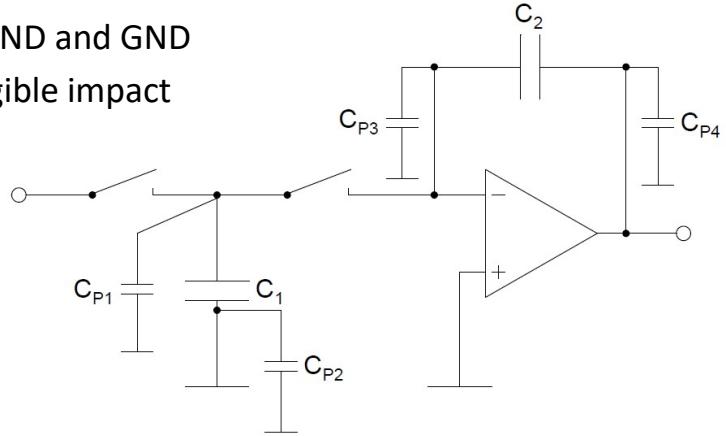
- Integrated signal:  $V_1' = V_1 - V_{os}$  instead of  $V_1$   
→ amplifier offset directly added to/subtracted from the input signal

## Implementation of Integrated Capacitors



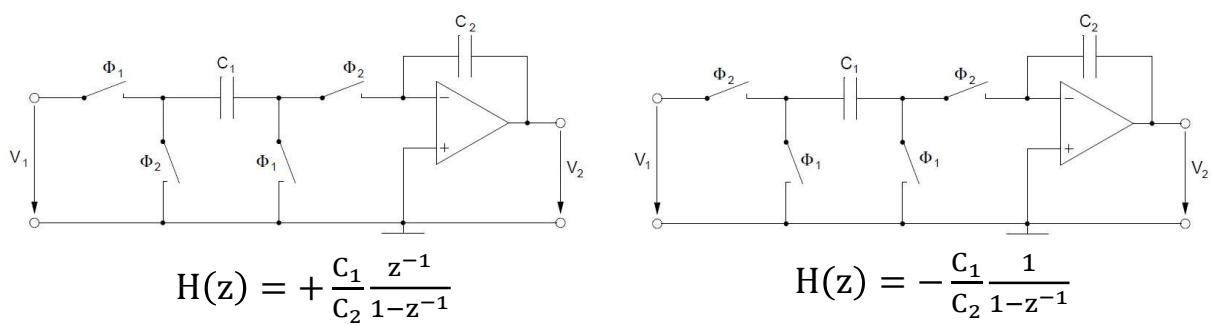
## Impact of Parasitic Capacitances

- $C_{p1} \parallel C_1 \rightarrow$  direct impact on transfer function
- $C_{p2}$  shorted
- $C_{p3}$  shorted between virtual GND and GND
- $C_{p4}$  at opamp output  $\rightarrow$  negligible impact



217

## Alternative Integrator Architectures



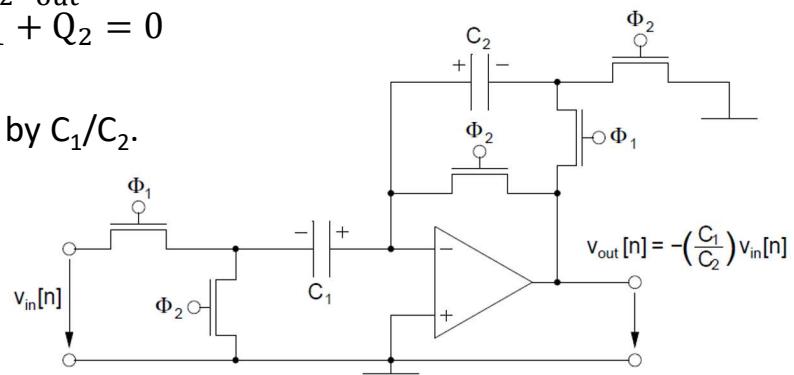
- Transfer function insensitive to parasitic capacitances.
- By exchanging the clock phases, the input sign can be changed.

Further reading: B. Razavi, The Switched-Capacitor Integrator, IEEE SSC Magazine, 2017

218

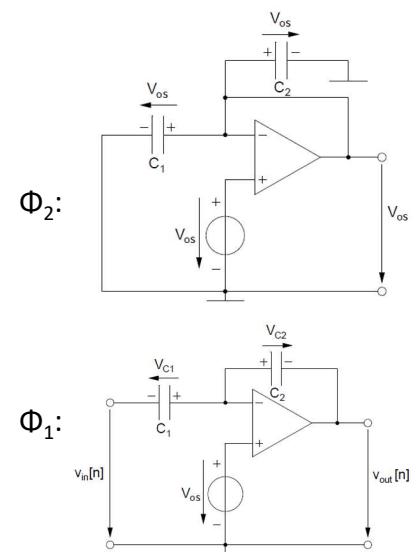
## Switched-Capacitor Amplifier

- $\Phi_2$ :  
 $C_1, C_2$  discharged, opamp reset
- $\Phi_1$ :  
 $Q_1 = -C_1 V_{in}, Q_2 = -C_2 V_{out}$   
Charge conservation:  $Q_1 + Q_2 = 0$   
 $\rightarrow \frac{V_{out}}{V_{in}} = -\frac{C_1}{C_2}$
- Gain can be programmed by  $C_1/C_2$ .



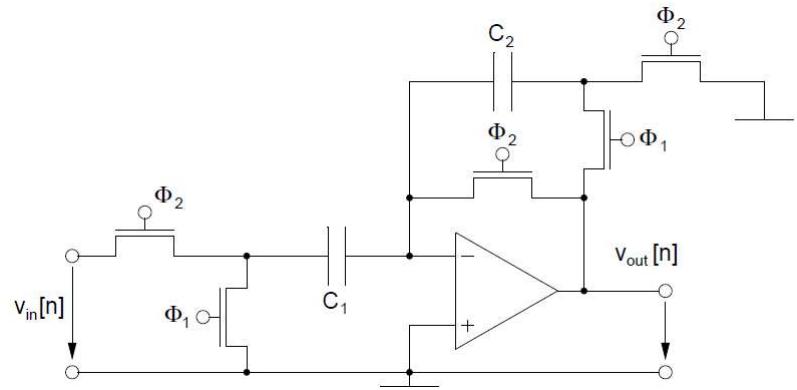
## SC Amplifier – Impact of Offset

- $\Phi_2$ : reset phase  
 $V_{out} = V_{os}, Q_1 = C_1 V_{os}, Q_2 = C_2 V_{os}$
- $\Phi_1$ : amplification phase  
 $Q_1 = C_1(V_{os} - V_{in}), Q_2 = C_2(V_{os} - V_{out})$   
Charge conservation  $\rightarrow -C_1 V_{in} - C_2 V_{out} = 0$   
 $\rightarrow \frac{V_{out}}{V_{in}} = -\frac{C_1}{C_2}$
- Offset effect is eliminated.



## SC Amplifier – Exchanged Clock Phases

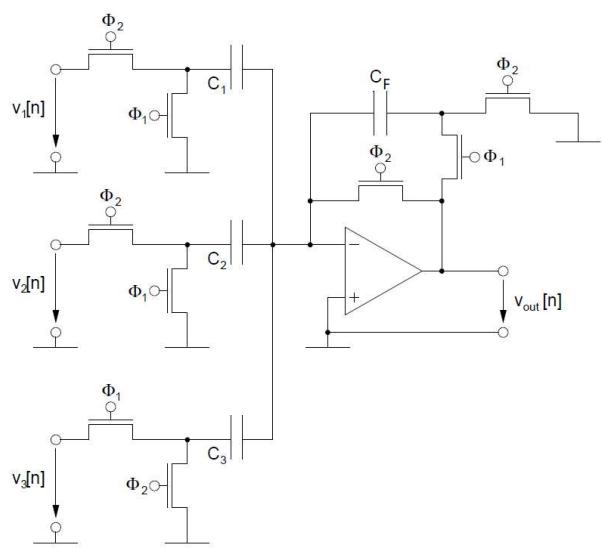
$$H(z) = \frac{V_{\text{out}}(z)}{V_{\text{in}}(z)} = \frac{C_1}{C_2} z^{-1/2}$$



221

## Superposition Theorem in SC Circuits

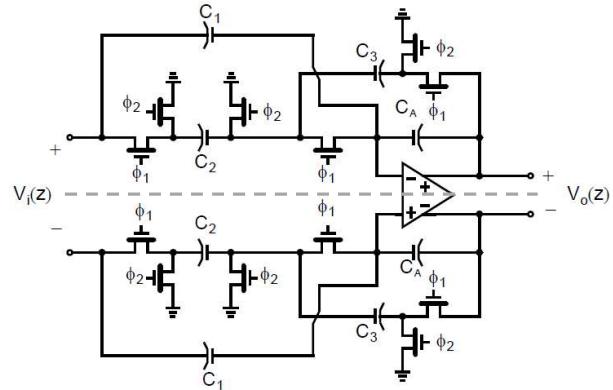
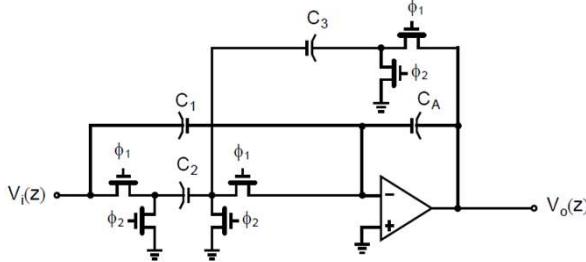
$$\begin{aligned} V_{\text{out}}(z) = & +\frac{C_1}{C_F} z^{-1/2} V_1(z) \\ & + \frac{C_2}{C_F} z^{-1/2} V_2(z) \\ & - \frac{C_3}{C_F} V_3(z) \end{aligned}$$



222

## Fully Differential SC Circuits

- Fully differential version: 2 copies of the single-ended circuit
- Single-ended version: keeps one side of the fully differential circuit; the other side is grounded.
- Common-mode feedback required.



Illustrations: T. Carusone, D. Johns, K. Martin, Analog Integrated Circuit Design, Wiley 2012  
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223

## SC Common-Mode Feedback (CMFB)

- Sensing common-mode (CM) output ( $V_{out,CM} = (V_{out,1} + V_{out,2})/2$ ):  
 - by resistors:  
 - small → considerable gain reduction, limited output current capability  
 - large → expensive (area)  
 - by MOSFETs: limited linear range
- SC CMFB:  
 - avoids previous difficulties  
 - circuit must be refreshed periodically
- SC resistor emulation:  
 $\text{Ex. } F_{clk}=100\text{kHz}, C=10\text{fF} \rightarrow R_{eq}=1\text{G}\Omega$

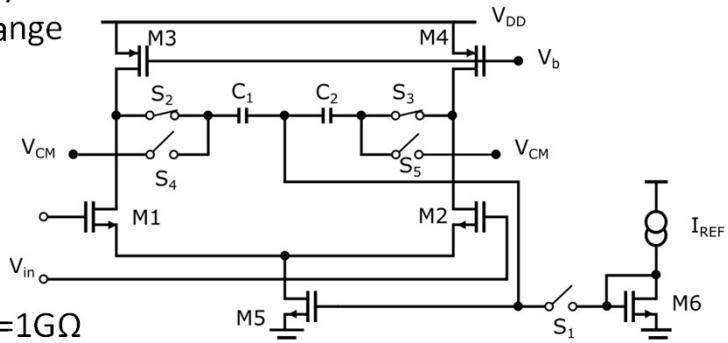


Illustration: B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill 2001  
 Technische Universität München | Lehrstuhl für Schaltungsentwurf

224

## SC Voltage Converter (Charge Pump)

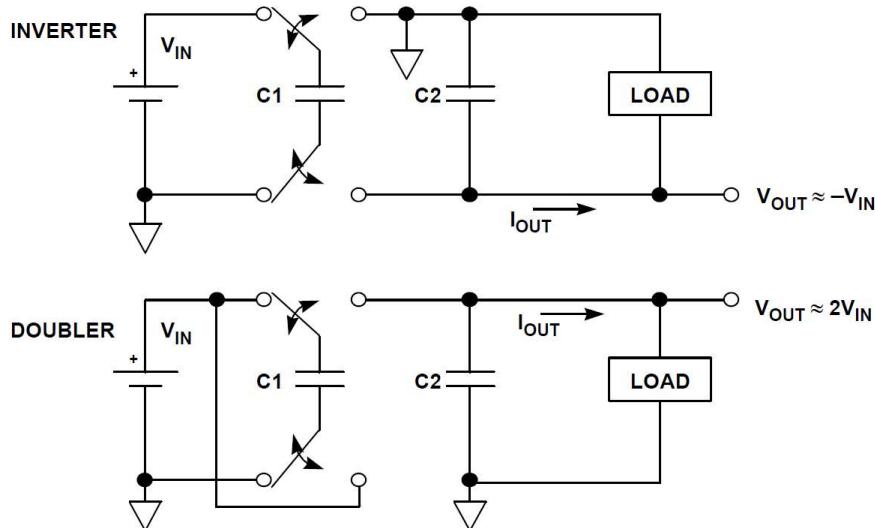


Illustration: W. Kester, B. Erisman, G. Thandi, Switched Capacitor Voltage Converters  
Technische Universität München | Lehrstuhl für Schaltungsentwurf

225

# Tutorial

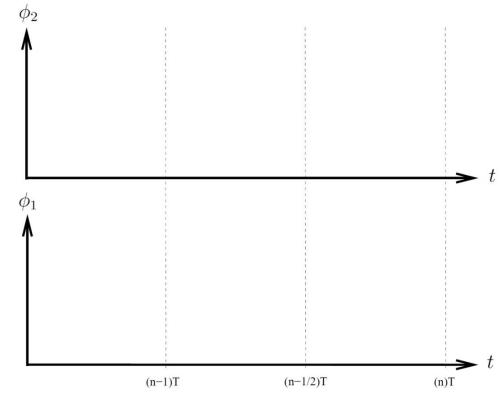
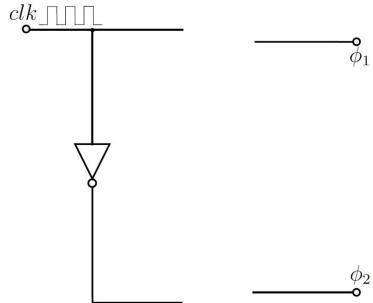


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226

## Exercise 1

- Sketch the non-overlapping clock pair required for the operation of a switched-capacitor circuit.
- Design a digital circuit to generate the non-overlapping clock pair out of a single-phase clock signal.

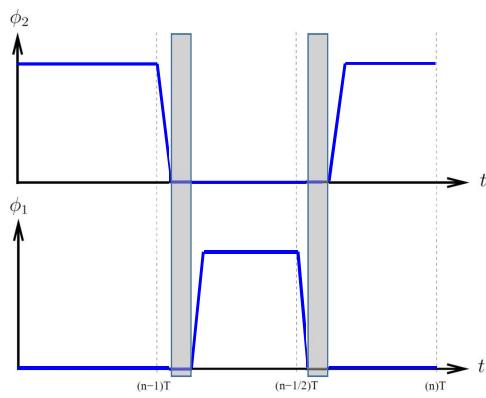


227



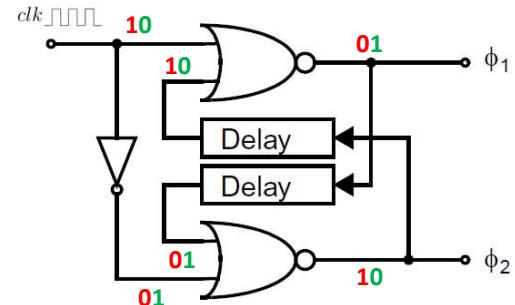
## Exercise 1 – Solution

a)



b)

A	B	A NOR B
0	0	1
0	1	0
1	0	0
1	1	0



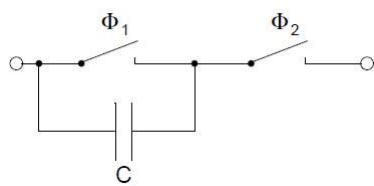
228



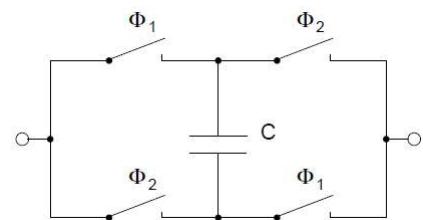
## Exercise 2

Calculate the equivalent resistance of the given circuits:

a)



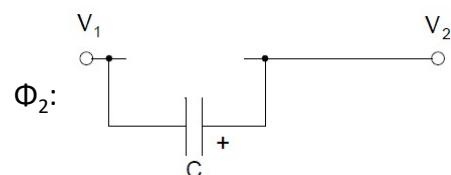
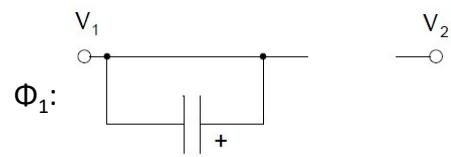
b)



## Exercise 2 – Solution

a)

- $\Phi_1$ :  $t = (n - 1)T$
- $\Phi_2$ :  $t = (n - 1/2)T$
- $\Phi_1$ :  $t = nT$
- $R_{eq} =$

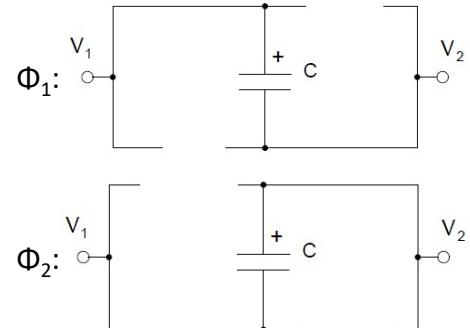


## Exercise 2 – Solution

b)

- $\Phi_1: t = (n - 1)T$
- $\Phi_2: t = (n - 1/2)T$

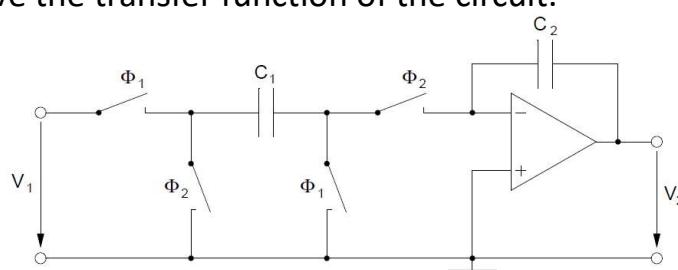
- $R_{eq} =$



231

## Exercise 3

- a) Consider the following circuit. Draw the equivalent circuit for the two clock phases. Derive the transfer function of the circuit.



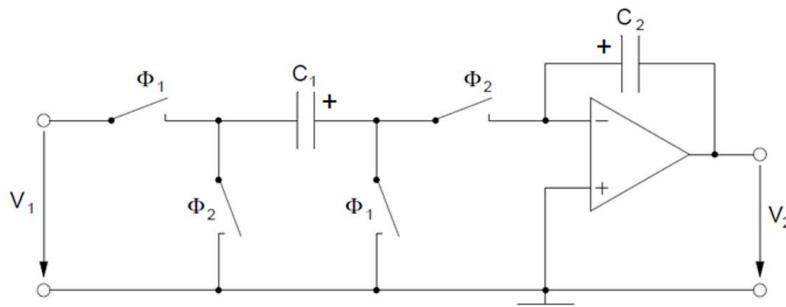
- b) Change the clock phases of the switches at the input and derive the new transfer function.  
c) What is the impact of amplifier offset in each case?

232

## Exercise 3 – Solution

a)

1. *Mark polarity of all capacitors, such that the positive plates are connected to the floating node. Do not change this polarity during the analysis.*



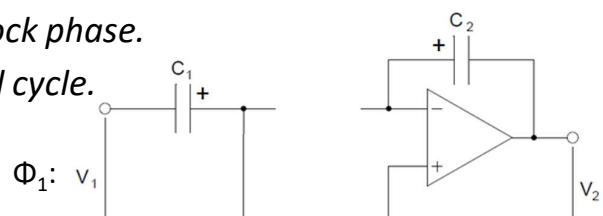
233

## Exercise 3 – Solution

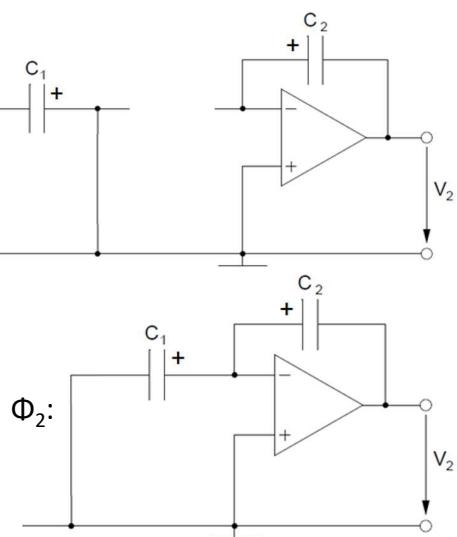
2. *Draw equivalent circuits for each clock phase.*

3. *Charge conservation analysis for full cycle.*

- $\Phi_1: t = (n - 1)T$



- $\Phi_2: t = (n - 1/2)T$

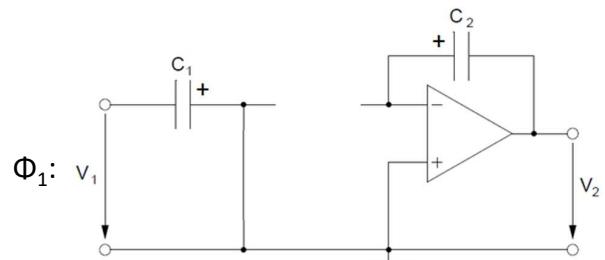


234

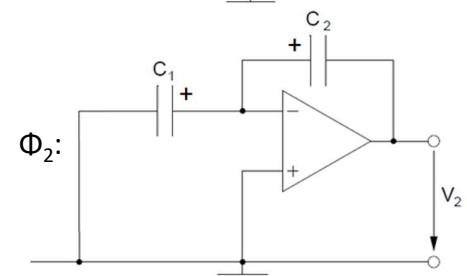
## Exercise 3 – Solution

- $\Phi_1: t = nT$

4. Apply Z-transform



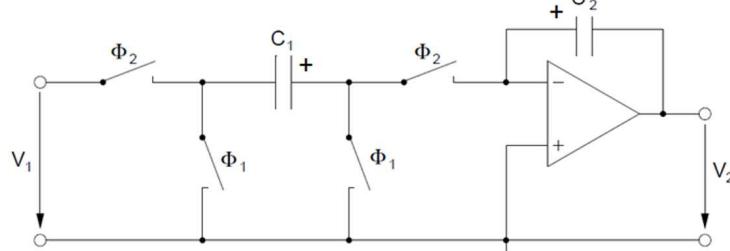
5. Calculate transfer function



6. Approximation on unit circle:

## Exercise 3 – Solution

b)



## Exercise 3 – Solution

b)

- $\Phi_2: t = (n - 1)T$

$$Q_1[n - 1] = -C_1 V_1[n - 1]$$

$$Q_2[n - 1] = -C_2 V_2[n - 1]$$

- $\Phi_1: t = (n - 1/2)T$

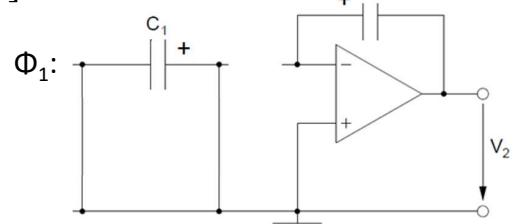
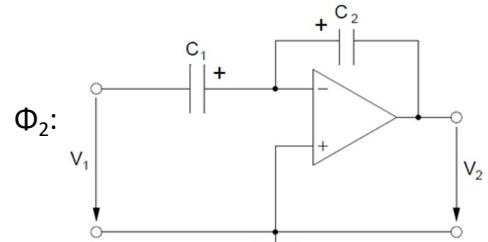
$$V_{c1} = 0 \rightarrow Q_1[n - 1/2] = 0$$

$$Q_2[n - 1/2] = Q_2[n - 1] = -C_2 V_2[n - 1]$$

- $\Phi_2: t = nT$

$$Q_1[n] = -C_1 V_1[n]$$

$$Q_2[n] = -C_2 V_2[n]$$



237



## Exercise 3 – Solution

- *Charge conservation:*

$$Q_2[n] + Q_1[n] = Q_2[n - 1/2] + Q_1[n - 1/2]$$

$$\rightarrow V_2[n] = V_2[n - 1] - \frac{C_1}{C_2} V_1[n]$$

- *Z-Transform:*

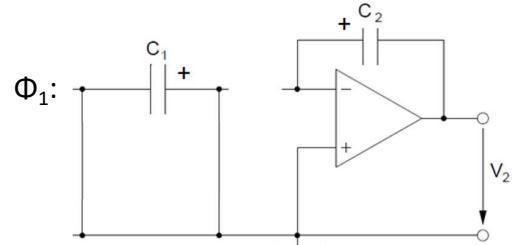
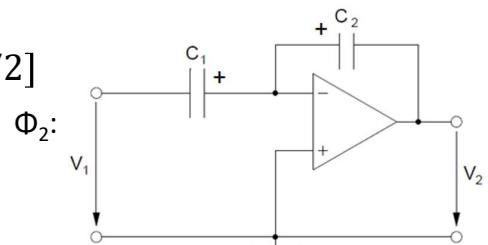
$$V_2(z) = z^{-1} V_2(z) - \frac{C_1}{C_2} V_1(z)$$

- *Transfer function:*

$$H(z) = \frac{V_2(z)}{V_1(z)} = -\frac{C_1}{C_2} \frac{1}{1-z^{-1}}$$

- *Unit circle:*

$$H(j\omega) = -\frac{C_1}{C_2} \frac{\exp(+j\omega T/2)}{2j \sin(\omega T/2)} \cong -\frac{C_1}{C_2} \frac{1}{j\omega T}$$



238



## Exercise 3 – Solution

c) Repeat charge conservation analysis →

- a)  $\rightarrow V_2[n] = V_2[n - 1] + \frac{C_1}{C_2}(V_1[n - 1] + V_{os})$

$\rightarrow$  amplifier offset added to the input signal

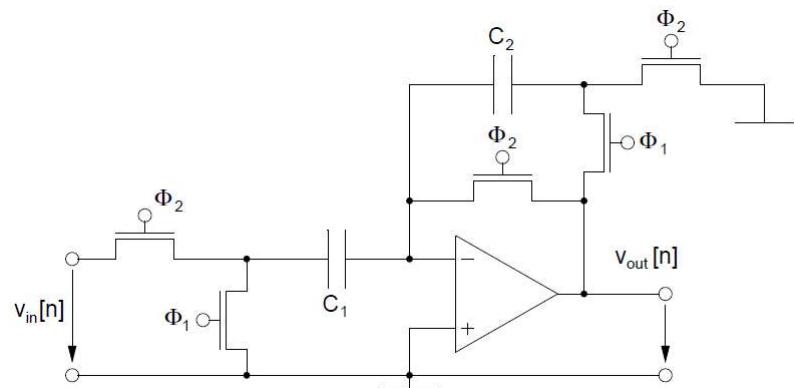
- b)  $\rightarrow V_2[n] = V_2[n - 1] - \frac{C_1}{C_2}(V_1[n] - V_{os})$

$\rightarrow$  amplifier offset subtracted from the input signal

## Exercise 4

The circuit below is the switched-capacitor amplifier from the lecture slides with the clock phases exchanged for the input transistors.

Analyze the circuit. What is the drawback of this implementation?

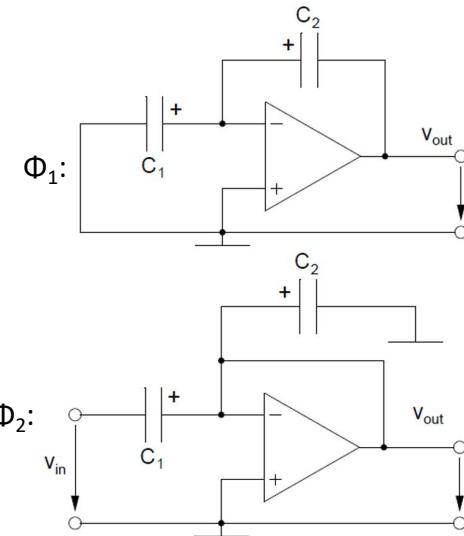


## Exercise 4 – Solution

- $\Phi_2: t = (n - 1/2)T$

- $\Phi_1: t = nT$

- Drawback: delay of  $z^{-1/2}$



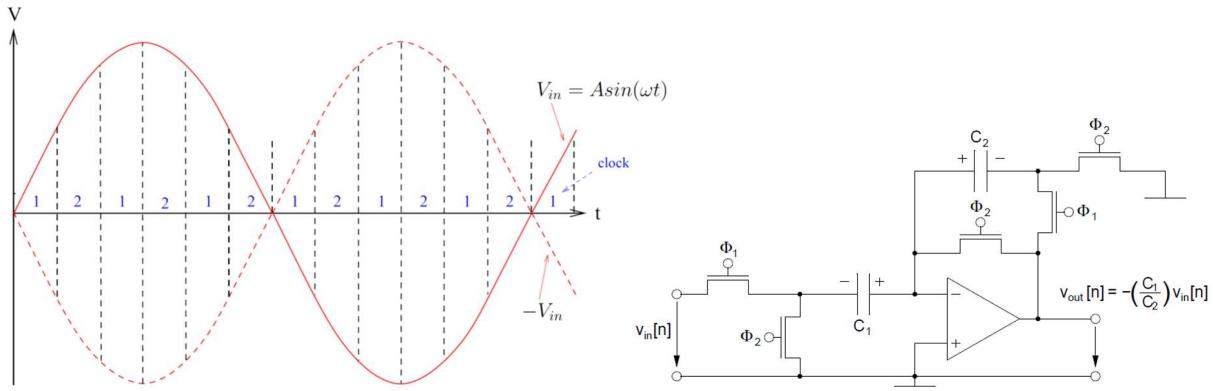
241



## Exercise 5

Sketch the output signal  $V_{out}(t)$  of a switched-capacitor amplifier, considering  $C_1=C_2=C$  and the input signal  $V_{in}(t)=A \cdot \sin(\omega t)$ .

Which requirements result from this waveform for the operational amplifier?



242

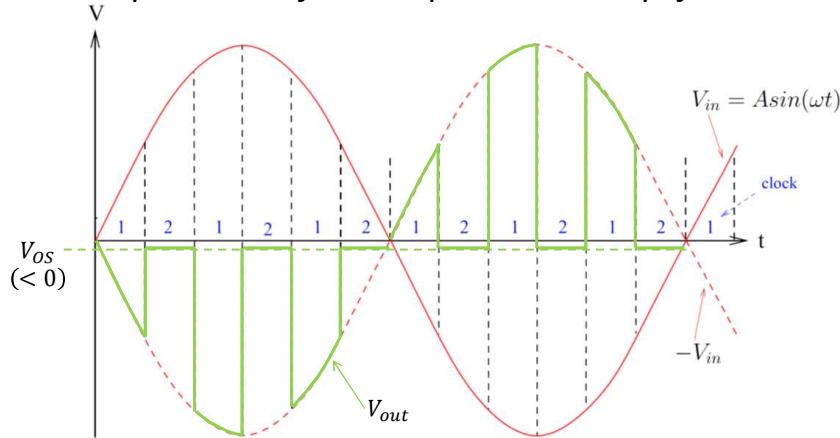


## Exercise 5 – Solution

$$\Phi_1: V_{out} = -(C_1/C_2)V_{in} = -V_{in}$$

$$\Phi_2: V_{out} = V_{os}$$

*High slew rate requirements for the operational amplifier.*



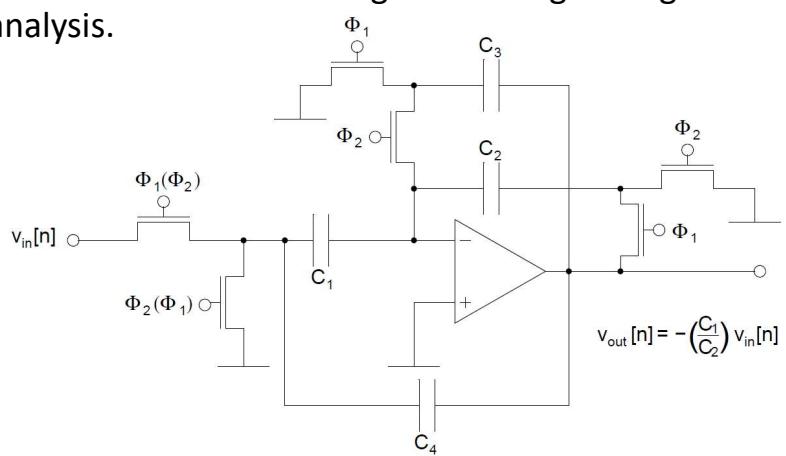
243



## Exercise 6

In the following, a switched-capacitor amplifier with capacitive reset and (optional) deglitching capacitance is considered. Neglect the deglitching capacitance  $C_4$  during the analysis.

- a) Analyze the circuit.
- b) What is the role of  $C_3$ ?



244



## Exercise 6 – Solution

- $\Phi_1: t = (n - 1)T$

$$Q_1[n - 1] = -C_1 V_{in}[n - 1]$$

$$Q_2[n - 1] = -C_2 V_{out}[n - 1]$$

$$Q_3[n - 1] = -C_3 V_{out}[n - 1]$$

- $\Phi_2: t = (n - 1/2)T$

$$Q_1[n - 1/2] = Q_2[n - 1/2] = 0$$

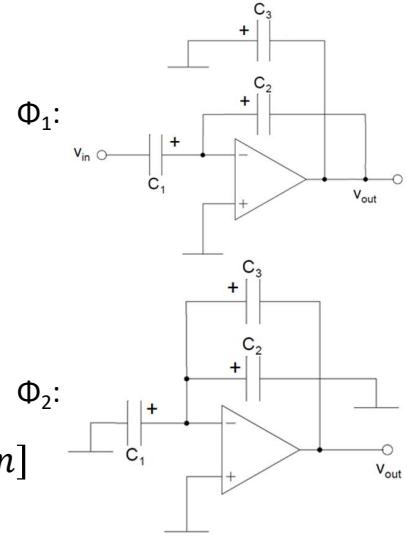
$$Q_3[n - 1/2] = -C_3 V_{out}[n - 1/2]$$

- $\Phi_1: t = nT$

$$Q_1[n] = -C_1 V_{in}[n]$$

$$Q_2[n] = -C_2 V_{out}[n]$$

$$Q_{1+2}[n] = Q_{1+2}[n - 1/2] \rightarrow V_{out}[n] = -\frac{C_1}{C_2} V_{in}[n]$$



245

## Exercise 6 – Solution

- b) What about  $C_3$ ? What is its role?

- $\Phi_2: t = (n - 1/2)T$

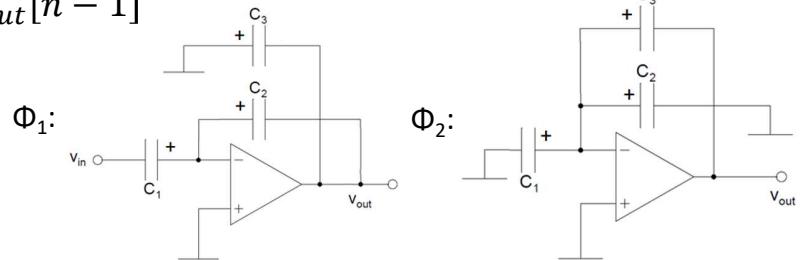
Charge conservation:  $Q_{1+2+3}[n - 1/2] = Q_{1+2+3}[n - 1]$

$$\rightarrow C_3 V_{out}[n - 1/2] = C_3 V_{out}[n - 1] + C_2 V_{out}[n - 1] + C_1 V_{in}[n - 1]$$

From  $t = nT$ :  $C_1 V_{in}[n] + C_2 V_{out}[n] = 0 \rightarrow$  applies for any  $n$

$$\rightarrow C_1 V_{in}[n - 1] + C_2 V_{out}[n - 1] = 0$$

$$\rightarrow V_{out}[n - 1/2] = V_{out}[n - 1]$$



246

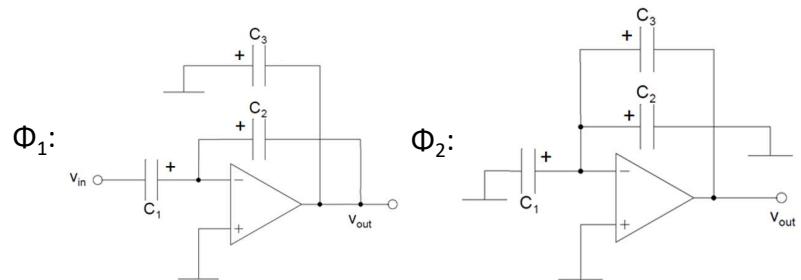
## Exercise 6 – Solution

$C_3 \rightarrow$  capacitive reset

On  $\Phi_2$ ,  $V_{out}$  is no longer reset, but keeps the value from the previous  $\Phi_1 \rightarrow$

- slew rate requirements relaxed

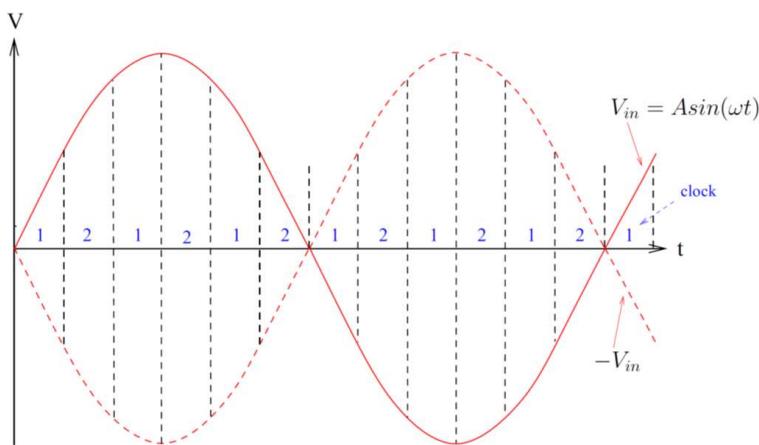
- switching noise and power consumption reduced



247

## Exercise 6

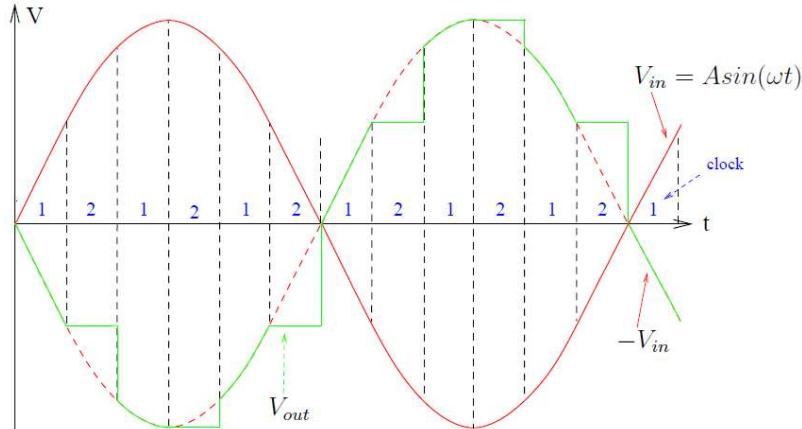
- c) Assume  $C_1=C_2=C$  and  $V_{in}(t)=A \cdot \sin(\omega t)$ , as depicted in the figure. Sketch the output signal  $V_{out}(t)$ . Compare with the circuit without capacitive reset.



248

## Exercise 6 – Solution

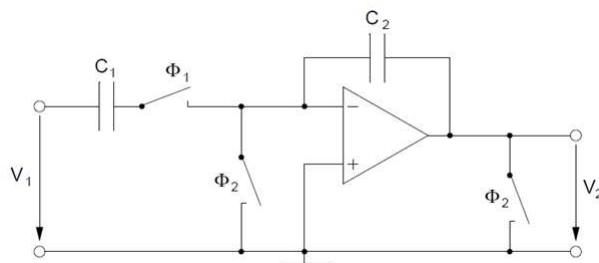
- c)  $\Phi_1: V_{out}[n] = -(C_1/C_2)V_{in}[n] = -V_{in}[n] \rightarrow track$   
 $\Phi_2: V_{out}[n - 1/2] = V_{out}[n - 1] \rightarrow hold$



249

## Exercise 7

- a) Consider the following circuit. Draw the equivalent circuit for the two clock phases. Derive the transfer function of the circuit.



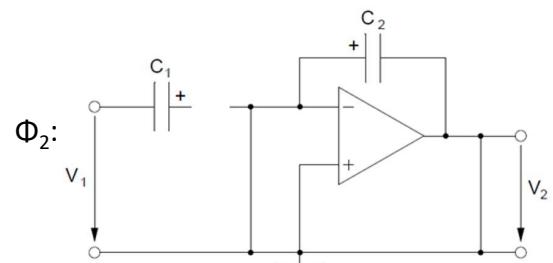
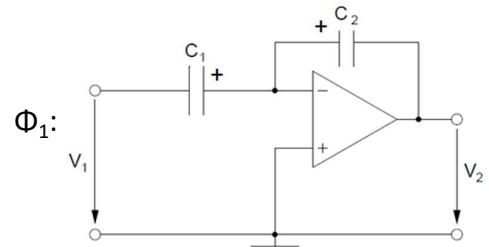
- b) Assume  $C_1=C_2=C$ . What is the functionality of the circuit?  
c) Draw the fully differential version of the circuit.

250

## Exercise 7 – Solution

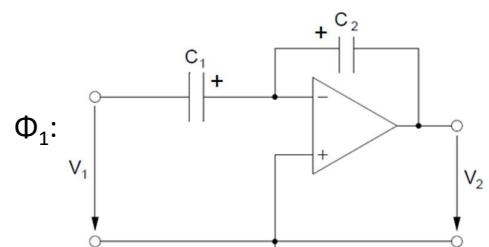
a)

- $\Phi_1: t = (n - 1)T$
- $\Phi_2: t = (n - 1/2)T$

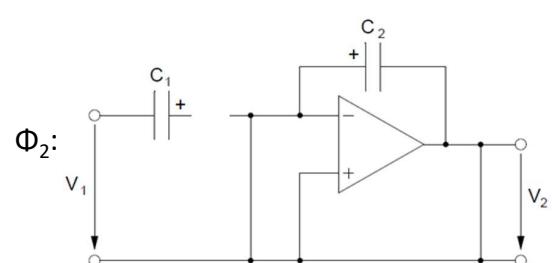


## Exercise 7 – Solution

$$\begin{aligned} \bullet Q_{1+2}[n] &= Q_{1+2}[n - 1/2] \\ \rightarrow V_2[n] &= -\frac{C_1}{C_2}(V_1[n] - V_1[n - 1]) \end{aligned}$$

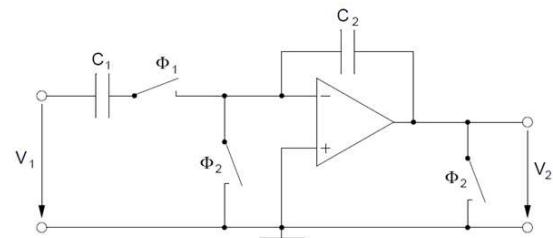


b)



## Exercise 7 – Solution

c)



253



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## Appendix – Common-Mode Feedback

- Fully differential OTA
  - 2 current sources
    - PMOS ( $V_{B1}$ )
    - NMOS ( $V_{B2}$ )
  - conflicting biasing,  
unless currents perfectly matching
  - output CM unstable
- Solution:
  - apply one constant biasing
  - regulate output CM and the other biasing
  - common-mode feedback (CMFB)

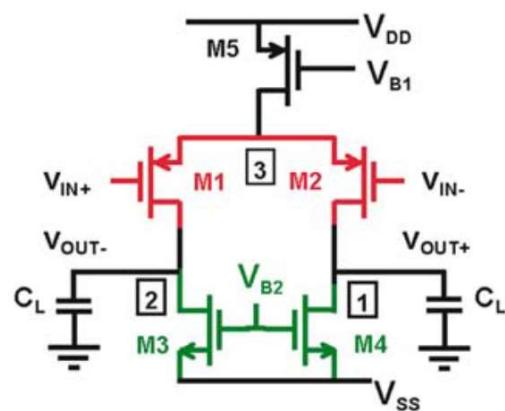
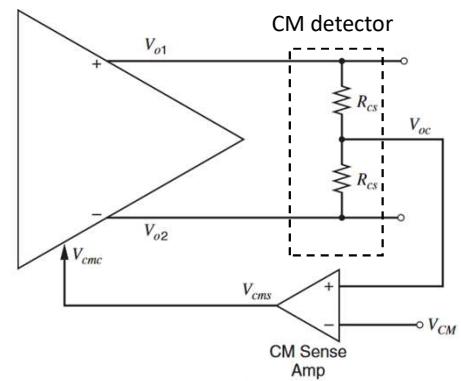
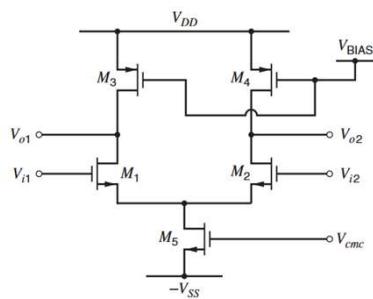


Illustration: W. Sansen, Analog Design Essentials, Springer 2006  
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254

## Appendix – Common-Mode Feedback

- Common-mode feedback:
  - main amplifier
  - CM detector (resistive, switched-capacitor or transistor-based)
  - CM error amplifier (can have gain just 1):  
compares output CM with reference CM



Illustrations: P. Gray et al., Analysis and Design of Analog Integrated Circuits, 5th ed., Wiley 2009

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255

# Chapter 6

## Nyquist-Rate

## Digital-to-Analog Converters

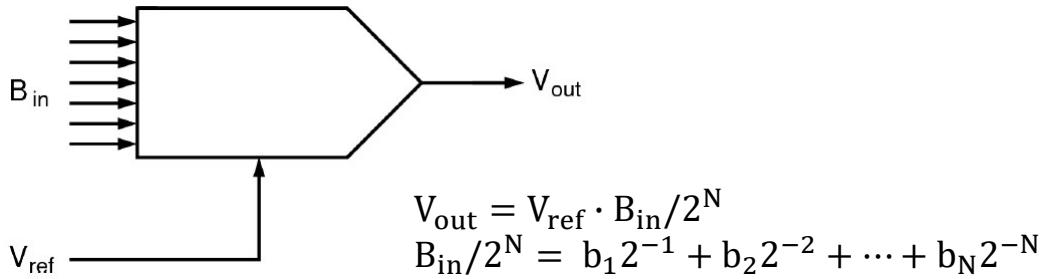
Dr. Florin Burcea (revised by)  
Courtesy of Dr. Stephan Henzler



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256

## Nyquist-Rate DACs

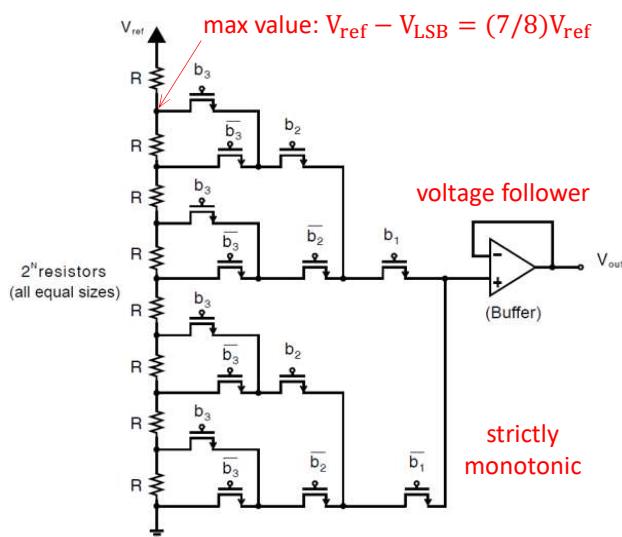


Basic idea:

- Generate all possible voltages according to above equation
- Use switches to connect the voltage selected by  $B_{in}$  to the output



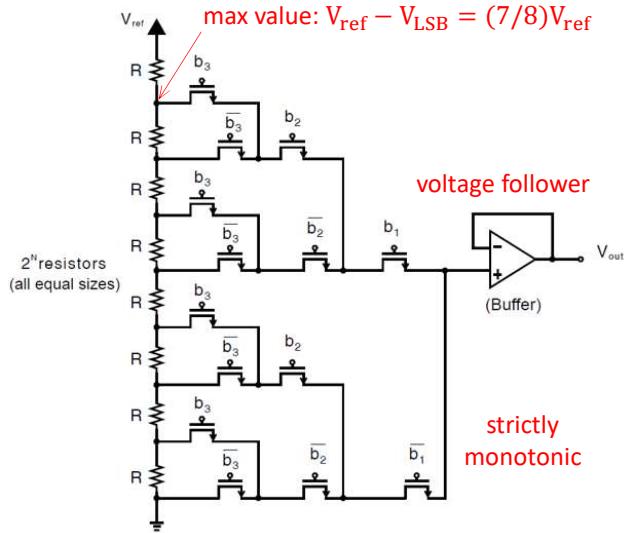
## Resistive String DAC



- Generate all possible voltages with resistive voltage divider.
- Analog multiplexer for voltage selection
- Switches as NMOS transistors:  
 $V_{ref} < \frac{1}{1-2^{-N}}(V_{DD} - V_{th})$
- Transmission gates → higher:
  - voltage range (+)
  - parasitic capacitance, area (-)
- Buffer experiences high input voltage variation.



## Resistive String DAC – Decoding Tree



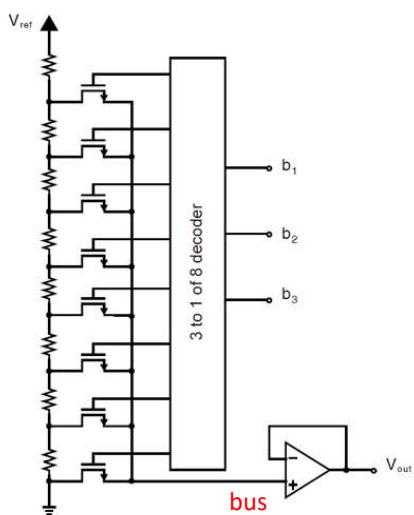
- Analog multiplexer for output selection → decoding tree
- Delay through switch network → main limitation on speed



Illustration: T. Carusone, D. Johns, K. Martin, Analog Integrated Circuit Design, Wiley 2012

259

## Resistive String DAC – Digital Decoder



- Large capacitive loading on single bus
- More area than decoding tree
- Digital decoder can be pipelined → overall faster than decoding tree



Illustration: T. Carusone, D. Johns, K. Martin, Analog Integrated Circuit Design, Wiley 2012

260

## Folded Resistive String DAC

- Advantages:
  - low effort for decoder
  - small load capacitance
- Access scheme as in memories
  - MSBs select row
  - LSBs select column
- $2 \cdot 2^{N/2}$  transistors at output bus
- Disadvantage:
  - all bitlines must be charged

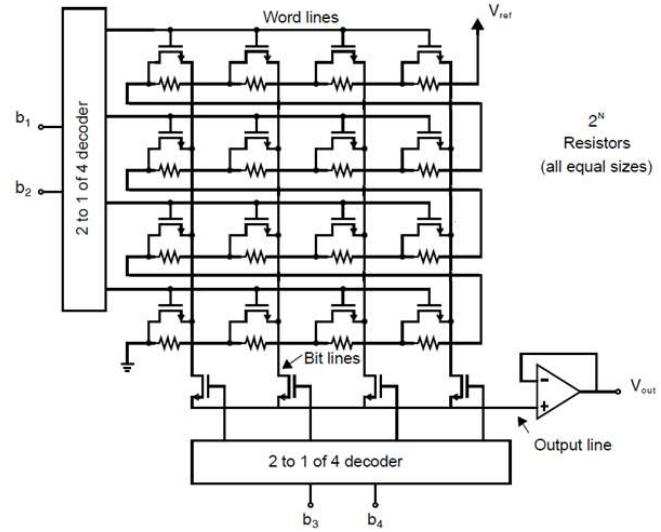


Illustration: T. Carusone, D. Johns, K. Martin, Analog Integrated Circuit Design, Wiley 2012

261

## Binary-Weighted Current-Mode DAC

- Previous: all output voltages generated, 1 out of  $2^N$  copied to the output.
- Here:
  - current-mode  $\rightarrow$  currents are generated, superposed and then converted into the output voltage.
  - binary-weighted  $\rightarrow$  input word already binary; generated binary-weighted currents are superposed into a current that corresponds to the input word.

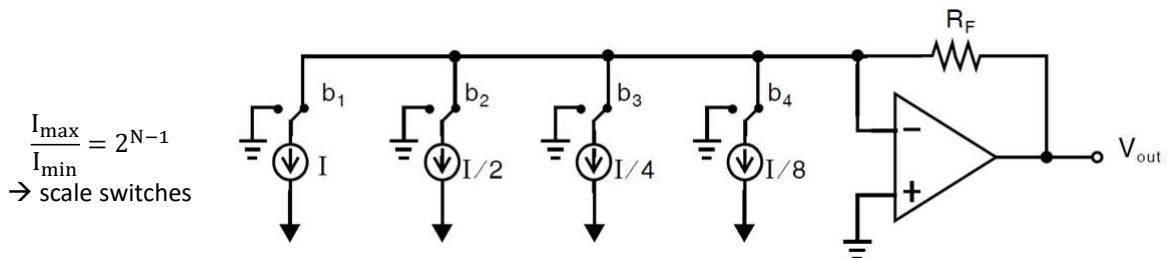


Illustration: T. Carusone, D. Johns, K. Martin, Analog Integrated Circuit Design, Wiley 2012  
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262

## Binary-Weighted DAC - Monotonicity

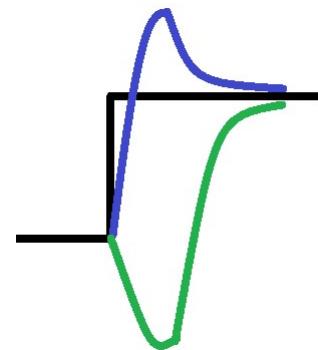
- Binary-weighted DACs → not necessarily monotonic (mismatch)
- Example

$1$	$\frac{1}{2}$	$\frac{1}{4}$	$\frac{1}{8}$	$\frac{6}{8}$	$\frac{1}{2}$	$\frac{1}{4}$	$\frac{1}{8}$
↓	↓	↓	↓	↓	↓	↓	↓
$0$	$1$	$1$	$1 \rightarrow \frac{7}{8}$	$0$	$1$	$1$	$1 \rightarrow \frac{7}{8}$
$1$	$0$	$0$	$0 \rightarrow 1$	$1$	$0$	$0$	$0 \rightarrow \frac{6}{8}$

## Binary-Weighted DAC - Glitches

- Different delays in the control logic of the switches cause voltage spikes, i.e. glitches

$0\ 1\ 1\ 1 \rightarrow 1\ 0\ 0\ 0$   
 $0\ 1\ 1\ 1 \rightarrow \underline{\ 1\ 1\ 1\ 1} \rightarrow 1\ 0\ 0\ 0$   
 $0\ 1\ 1\ 1 \rightarrow \underline{\ 0\ 0\ 0\ 0} \rightarrow 1\ 0\ 0\ 0$



## Exercise 1

Consider the DAC shown in the figure below. For  $b_i=1$  the switch connects the respective resistor to the VGND node and for  $b_i=0$  to AGND.

- Calculate the currents  $I'_1$  to  $I'_4$ .
- Calculate the currents  $I_1$  to  $I_4$ . Generalize.

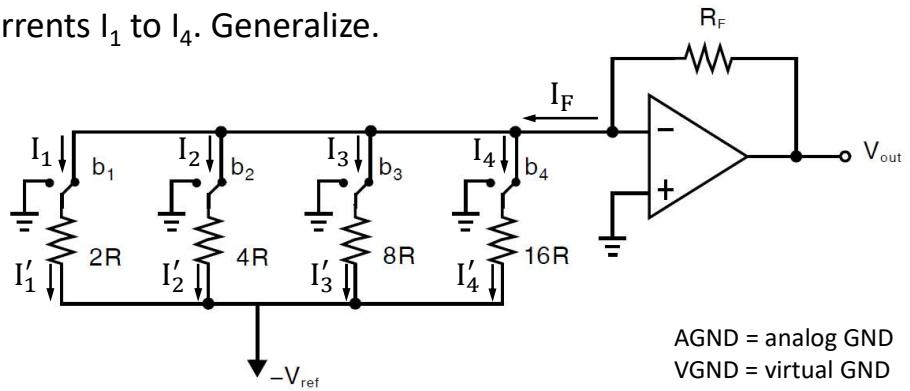


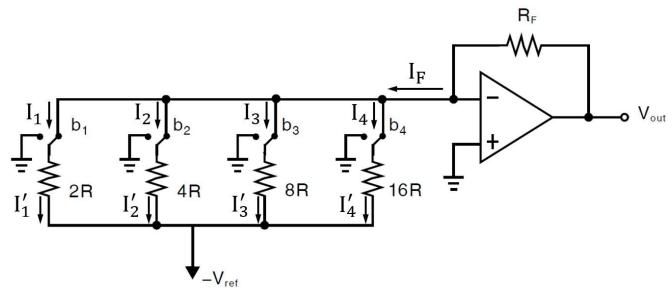
Illustration: T. Carusone, D. Johns, K. Martin, Analog Integrated Circuit Design, Wiley 2012

265

## Exercise 1 – Solution

a)

b)



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266

## Exercise 1

- c) Calculate the current  $I_F$  in dependence of the switch positions  $b_i$  and the reference voltage  $V_{\text{ref}}$ .
- d) Find an expression for the output voltage  $V_{\text{out}}(B, V_{\text{ref}})$ . Generalize.

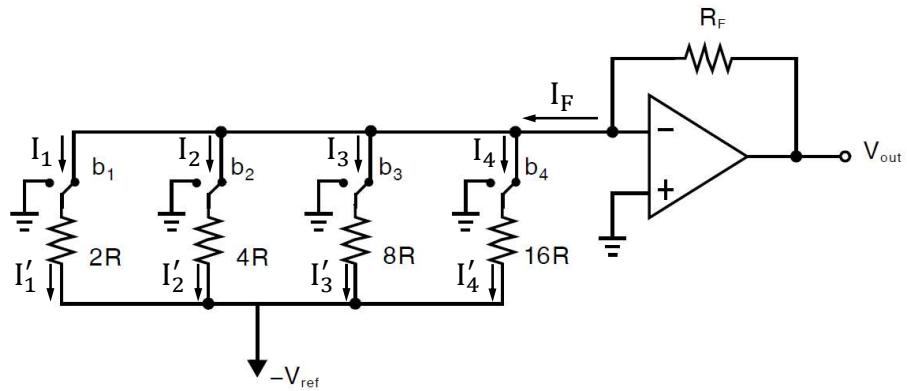


Illustration: T. Carusone, D. Johns, K. Martin, Analog Integrated Circuit Design, Wiley 2012

267

## Exercise 1 – Solution

c)

d)

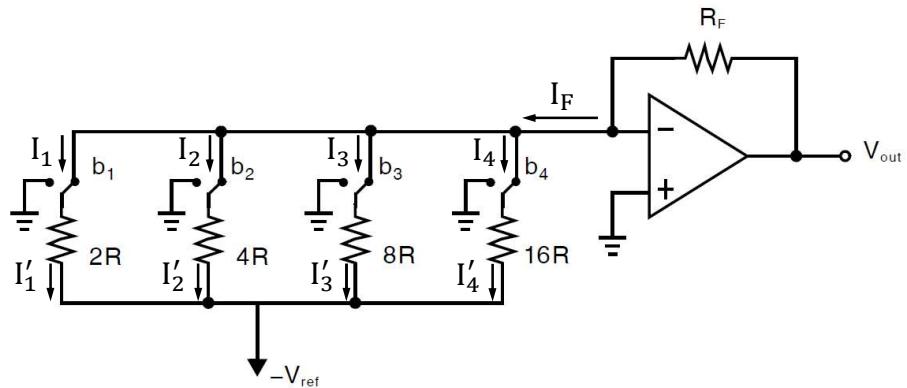


Illustration: T. Carusone, D. Johns, K. Martin, Analog Integrated Circuit Design, Wiley 2012  
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268

## Binary-Weighted Resistive DAC – Summary

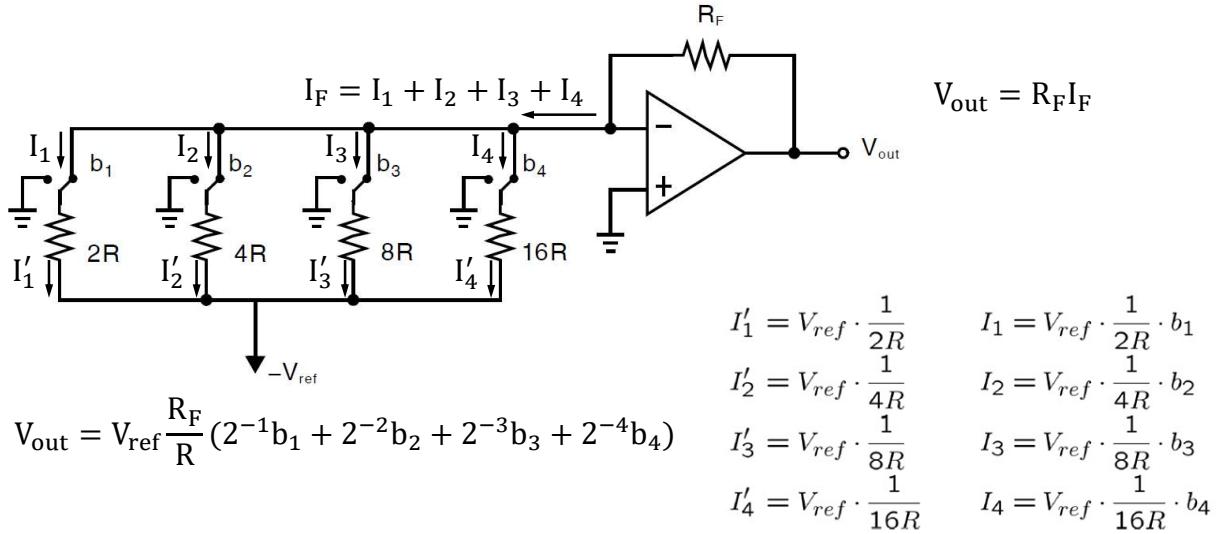


Illustration: T. Carusone, D. Johns, K. Martin, Analog Integrated Circuit Design, Wiley 2012  
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269

## Binary-Weighted Resistive DAC – Summary

- For  $b_i=0$  the same current  $I'_i$  flows, not to VGND but to AGND.
- Not necessarily monotonic (resistor mismatch)
- Glitches, if switches do not switch simultaneously
- $I_{\max}/I_{\min} = R_{\max}/R_{\min} = 8 = 2^{N-1}$
- Resistive network → DC power consumption

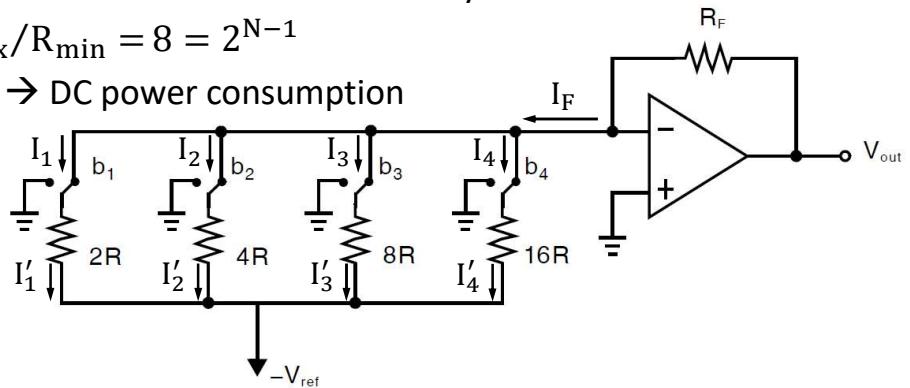


Illustration: T. Carusone, D. Johns, K. Martin, Analog Integrated Circuit Design, Wiley 2012  
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270

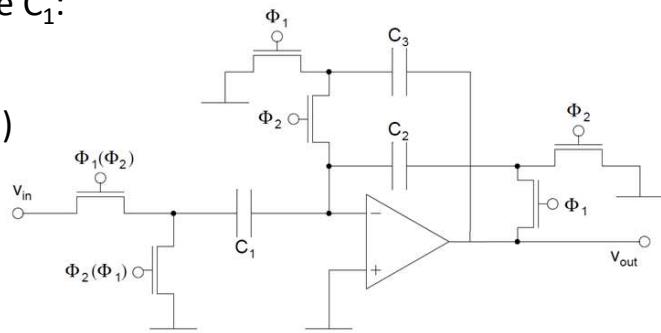
## Exercise 2

Consider a switched-capacitor amplifier with capacitive reset. The gain factor depends linearly on the capacitance  $C_1$ :

$$V_{\text{out}} = \pm(C_1/C_2)V_{\text{in}}$$

( $\pm$  depending on the input clocks,

$V_{\text{in}}$  assumed constant over a period)



Starting from this circuit, design a 4-bit DAC with the following characteristic:

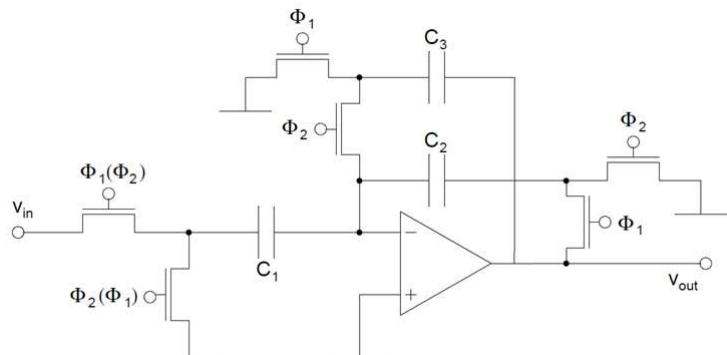
$$V_{\text{out}} = \pm V_{\text{ref}}(2^{-1}b_1 + 2^{-2}b_2 + 2^{-3}b_3 + 2^{-4}b_4)$$

(Extend the circuit and size the capacitances accordingly.)

271

## Exercise 2 – Solution

- SC amplifier:  $V_{\text{out}} = \pm(C_1/C_2)V_{\text{in}} \rightarrow$  gain programmable through  $C_1/C_2$
- DAC:  $V_{\text{out}} = \pm V_{\text{ref}}(2^{-1}b_1 + 2^{-2}b_2 + 2^{-3}b_3 + 2^{-4}b_4)$



272

## Exercise 2 – Solution

$$C_1 = 8Cb_1 + 4Cb_2 + 2Cb_3 + Cb_4$$

$$C_2 = 16C$$

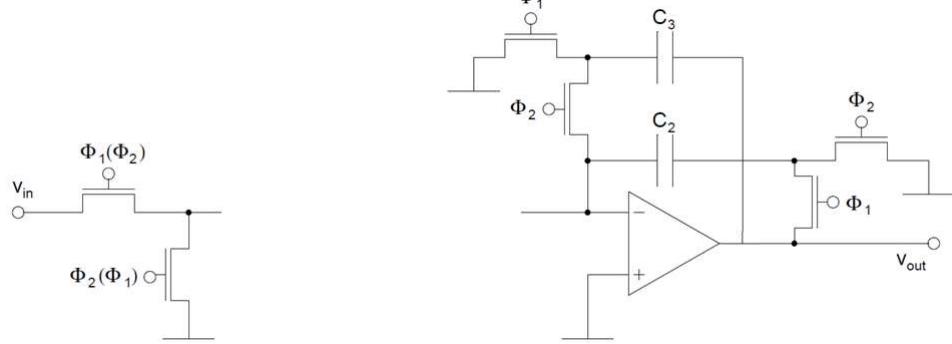


Illustration: T. Carusone, D. Johns, K. Martin, Analog Integrated Circuit Design, Wiley 2012  
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273

## Binary-Weighted Capacitive DAC – Summary

- Capacitors instead of resistors
- No DC current → reduced power consumption
- VGND: floating node → circuit needs reset
- Affected by mismatch

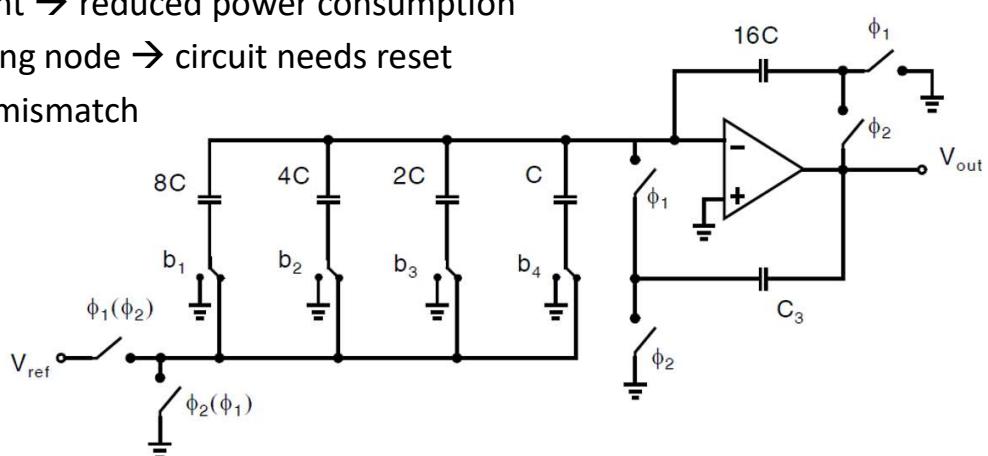


Illustration: T. Carusone, D. Johns, K. Martin, Analog Integrated Circuit Design, Wiley 2012  
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274

## Exercise 3

Consider the following R-2R resistor network.

- Determine  $R_i$  and  $R'_i$  for  $i=1\dots4$ . Generalize.
- Calculate all node voltages. Generalize.
- Calculate the currents  $I_1$  to  $I_4$ . Generalize.

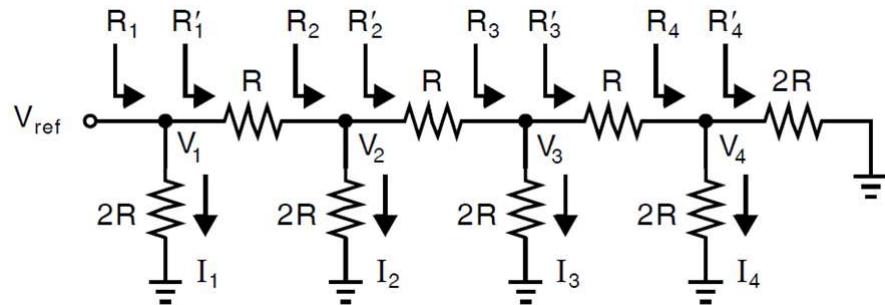
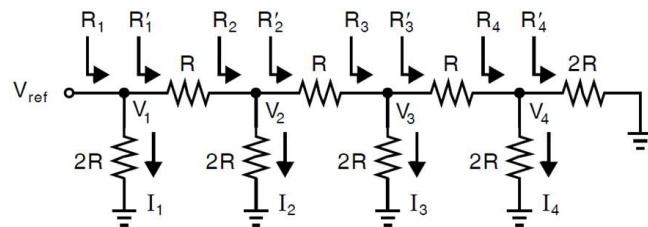


Illustration: T. Carusone, D. Johns, K. Martin, Analog Integrated Circuit Design, Wiley 2012

275

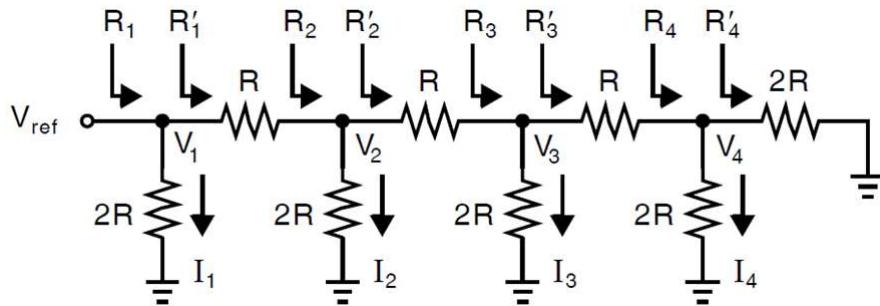
## Exercise 3 – Solution



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276

## R-2R Network – Summary



$$\begin{aligned}
 R'_4 &= 2R \\
 R_4 &= 2R \parallel 2R = R \\
 R'_3 &= 2R \\
 R_3 &= 2R \parallel 2R = R \\
 R'_2 &= 2R \\
 R_2 &= 2R \parallel 2R = R \\
 &\dots
 \end{aligned}$$

$$\begin{aligned}
 R'_i &= 2R & V_i &= V_{\text{ref}} / 2^{i-1} \\
 R_i &= R & I_i &= V_{\text{ref}} / (2^i R)
 \end{aligned}$$



Illustration: T. Carusone, D. Johns, K. Martin, Analog Integrated Circuit Design, Wiley 2012

277

## Exercise 3

- d) Use the R-2R network to build a DAC.

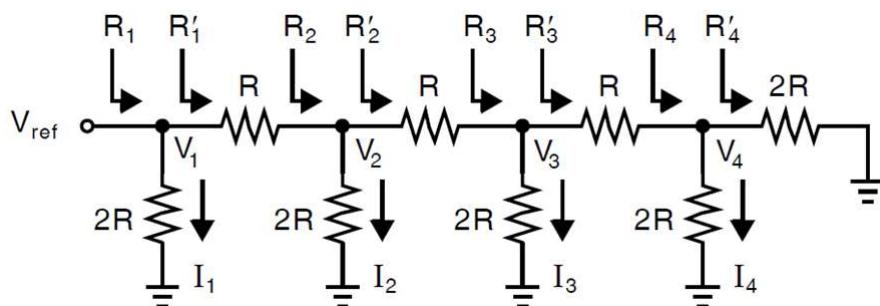


Illustration: T. Carusone, D. Johns, K. Martin, Analog Integrated Circuit Design, Wiley 2012

278

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## Exercise 3

Consider the DAC with R-2R network in the figure below. For  $b_i=1$  the switch connects the respective resistor to the VGND node and for  $b_i=0$  to AGND.

- e) Calculate the currents  $I'_1$  to  $I'_4$  and the nodal voltages  $V_1$  to  $V_4$ .
- f) Calculate the currents  $I_1$  to  $I_4$  in dependence of the switch positions  $b_i$ .

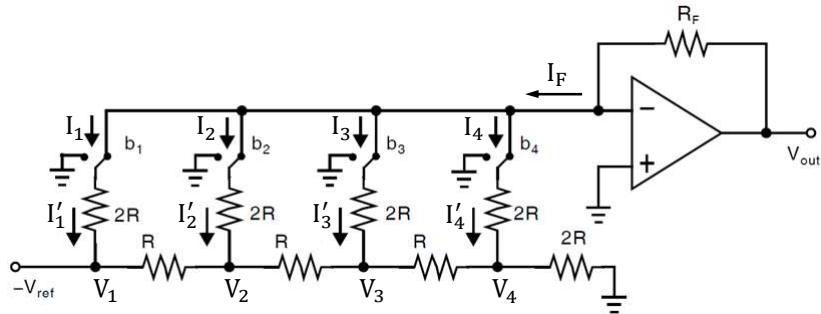


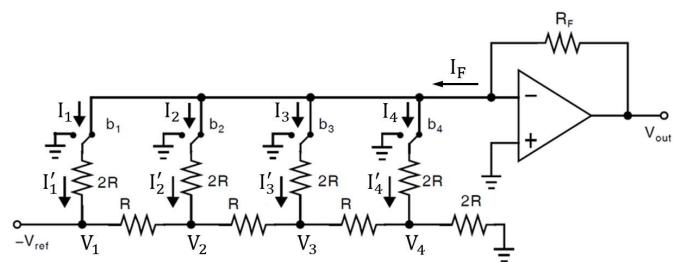
Illustration: T. Carusone, D. Johns, K. Martin, Analog Integrated Circuit Design, Wiley 2012

279

## Exercise 3 – Solution

e)

f)



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280

## Exercise 3

- g) Calculate the current  $I_F$  in dependence of the switch positions  $b_i$  and the reference voltage  $V_{ref}$ .
- h) Find an expression for the output voltage  $V_{out}(B, V_{ref})$ . Generalize.

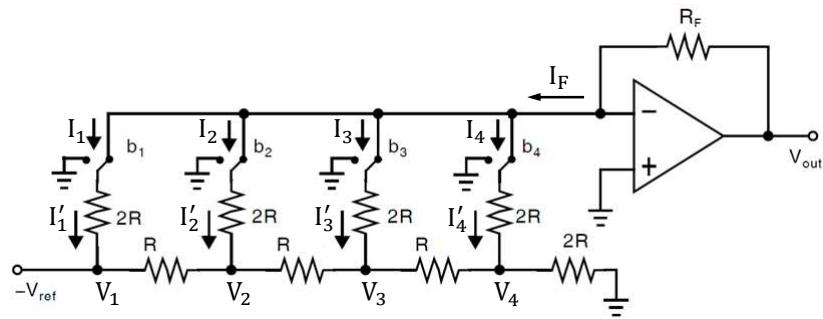


Illustration: T. Carusone, D. Johns, K. Martin, Analog Integrated Circuit Design, Wiley 2012  
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281

## Exercise 3 – Solution

g)

h)

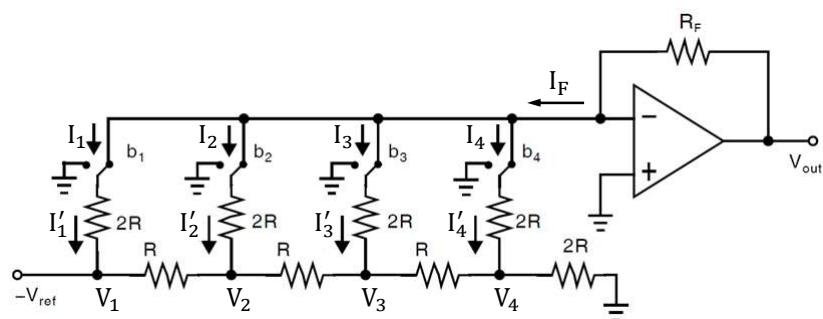
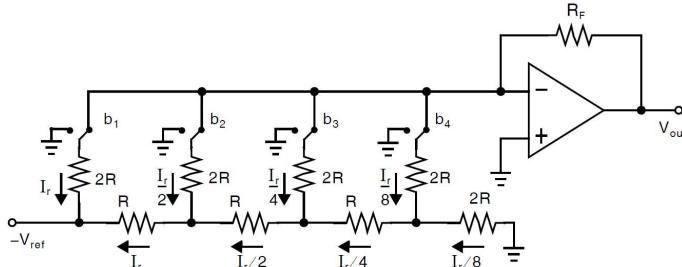


Illustration: T. Carusone, D. Johns, K. Martin, Analog Integrated Circuit Design, Wiley 2012  
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282

## DAC with R-2R Network – Summary



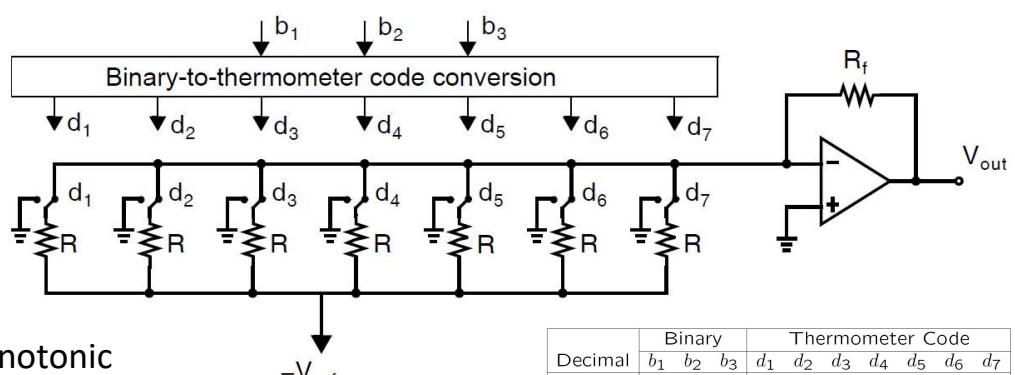
- R-2R network: replace AGND by VGND to collect binary-weighted currents.
- Insert switches, such that the node potential does not change.
- $R_{\max}/R_{\min} = 2$        $I_{\max}/I_{\min} = 8 = 2^{N-1}$
- Not necessarily monotonic; glitches; DC power consumption



Illustration: T. Carusone, D. Johns, K. Martin, Analog Integrated Circuit Design, Wiley 2012

283

## Thermometer Code DAC



- Strictly monotonic
- Minimizes glitches
- Equally-sized switches
- Same analog circuitry size as binary-weighted

Decimal	Binary			Thermometer Code						
	b <sub>1</sub>	b <sub>2</sub>	b <sub>3</sub>	d <sub>1</sub>	d <sub>2</sub>	d <sub>3</sub>	d <sub>4</sub>	d <sub>5</sub>	d <sub>6</sub>	d <sub>7</sub>
0	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	1
2	0	1	0	0	0	0	0	0	1	1
3	0	1	1	0	0	0	0	0	1	1
4	1	0	0	0	0	0	0	1	1	1
5	1	0	1	0	0	0	1	1	1	1
6	1	1	0	0	1	1	1	1	1	1
7	1	1	1	1	1	1	1	1	1	1



Illustration: T. Carusone, D. Johns, K. Martin, Analog Integrated Circuit Design, Wiley 2012

284

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# Tutorial



## Exercise 4

Consider a 4-bit DAC with binary-weighted resistors.

- a) What is the ratio between the maximum resistor  $R_{\max}$  and the minimum resistor  $R_{\min}$  from the resistor network?
- b) What is the ratio between the maximum current  $I'_{\max}$  and the minimum current  $I'_{\min}$  in the resistor network?
- c) Discuss these results with respect to the dimensions of the switches.
- d) What is the total number of unit resistors?
- e) Calculate the static power consumption of the DAC in dependence of the digital input word B. The internal power consumption of the operational amplifier is  $P_{\text{opamp}}$ .



## Exercise 4

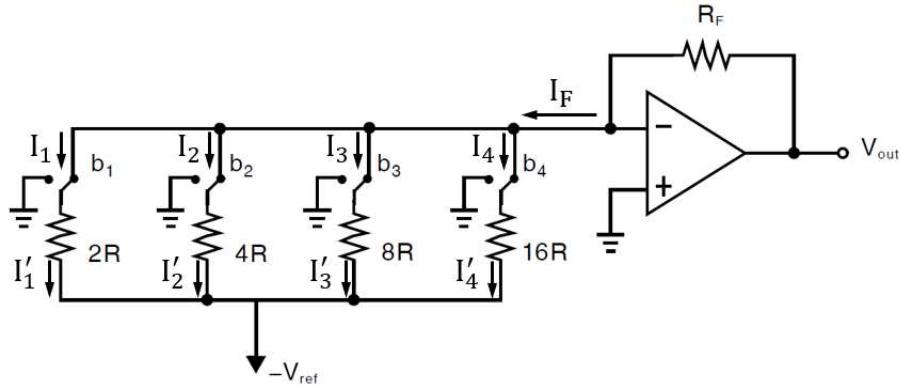


Illustration: T. Carusone, D. Johns, K. Martin, Analog Integrated Circuit Design, Wiley 2012  
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287

## Exercise 4 – Solution

- $R_{max}/R_{min} = 8$
- $I'_{max}/I'_{min} = 8$   
*In general (N bits):  $I'_{max}/I'_{min} = R_{max}/R_{min} = 2^{N-1}$*
- Switches have:*
  - parasitic gate capacitance
  - on resistance*Sizing of switches:*
  - equally sized for same switching time → different voltage drops
  - differently sized for same voltage drop → different switching times
- $2+4+8+16=30=2(2^N-1)$  unit resistors → exponential increase with bit size N



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288

## Exercise 4 – Solution

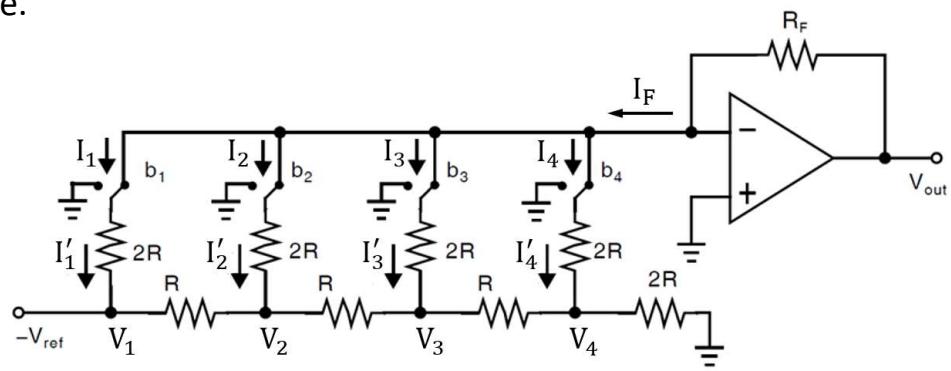
e) resistive network:

*feedback resistor:*

*total power:*

## Exercise 5

Consider a 4-bit DAC with R-2R resistor network. Repeat a)-e) from exercise 4. Compare.



## Exercise 5 – Solution

- a)  $R_{max}/R_{min} = 2$ , independent of bit size  $N \rightarrow$  matching easier to achieve
- b)  $I'_{max}/I'_{min} = 8$ , in general ( $N$  bits):  $I'_{max}/I'_{min} = 2^{N-1} \rightarrow$  same
- c) Switches have different currents  $\rightarrow$  same issues regarding switch sizing
- d)  $13=3N+1$  unit resistors  $\rightarrow$  linear increase with bit size  $N$
- e) resistive network:  $P_R = 2I'_1 \cdot V_{ref} = \frac{V_{ref}^2}{R} \rightarrow \approx$  same  
 -  $P_R$  constant with  $B$  and  $N$   
 feedback resistor:  $P_{RF} = R_F I_F^2 = \frac{R_F}{R} \frac{V_{ref}^2}{R} \left(\frac{B}{16}\right)^2 \rightarrow$  same  
 -  $P_{RF}$  depends on the digital input word  $B$   
 total power:  $P = P_R + P_{RF} + P_{opamp}$

## Exercise 6

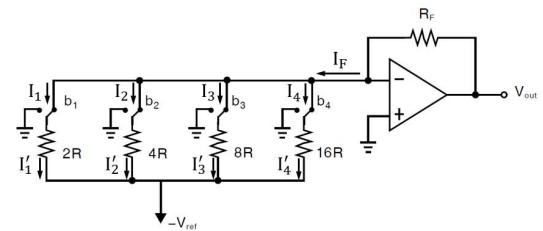
Consider a 4-bit DAC with binary-weighted resistors. The DAC is manufactured in a CMOS technology and all resistors are built from unity resistors which have a relative accuracy of up to +/-10%. Assume uncorrelated resistive variations.

- a) Calculate the nominal, minimal and maximal value for the currents  $I'_1$  to  $I'_4$  through the switches.
- b) The input digital word changes from 0111 to 1000. Which problems might arise because of the switches and the resistors?
- c) Calculate the maximum allowed  $\pm\Delta r[\%]$  resistor accuracy for the converter to have monotonic behavior.

## Exercise 6 – Solution

a)

Current	Nominal	Minimal	Maximal
$I'_i$			
$I'_1$			
$I'_2$			
$I'_3$			
$I'_4$			



## Exercise 6 – Solution

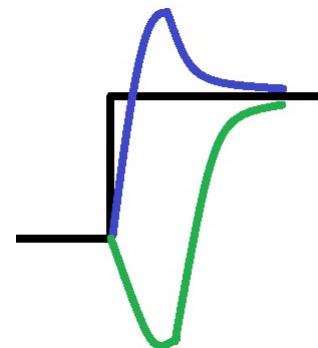
b)

$0111 \rightarrow 1111 \rightarrow 1000$  or

$0111 \rightarrow 0000 \rightarrow 1000$

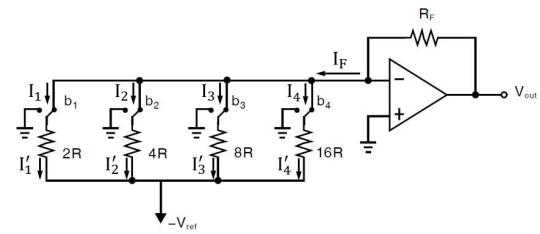
→ different switching times might lead to glitches:

- increased power consumption
- increased switching time



## Exercise 6 – Solution

c)

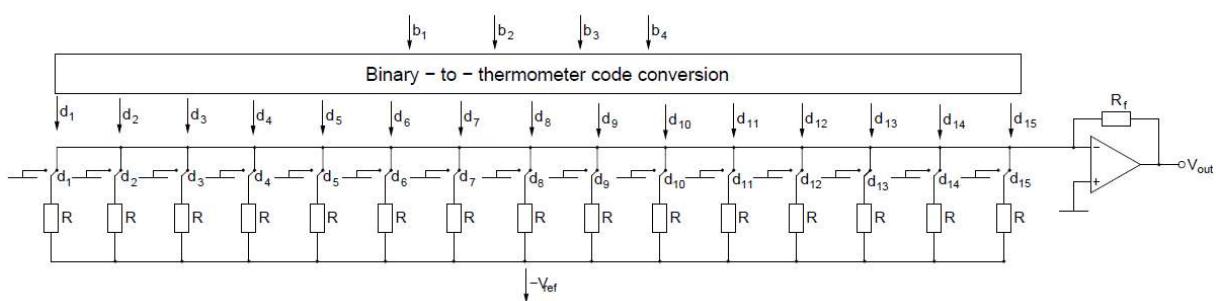


295



## Exercise 7

- Design a digital encoder which converts an unsigned 2-bit input word into a thermometer code.
- Consider the 4-bit thermometer-code DAC below. Compare with the R-2R and binary-weighted DAC considering power consumption, monotonicity, glitches and area.



296



## Exercise 7 – Solution

a)

i	b <sub>1</sub>	b <sub>2</sub>	d <sub>1</sub>	d <sub>2</sub>	d <sub>3</sub>
0	0	0			
1	0	1			
2	1	0			
3	1	1			

b) resistive network:  $P_R = 15 \frac{V_{ref}^2}{R} = (2^N - 1) \frac{V_{ref}^2}{R}$

-  $P_R$  constant with  $B$ , exponential increase with bit size  $N$

feedback resistor:  $P_{RF} = R_F I_F^2 = \frac{R_F}{R} \frac{V_{ref}^2}{R} B^2 \rightarrow$  exponentially larger

total power:  $P = P_R + P_{RF} + P_{opamp}$

$\rightarrow$  more power consumption than R-2R and binary-weighted resistors



## Exercise 7 – Solution

b) Glitches: equal currents  $\rightarrow$  equal switches  $\rightarrow$  equal switching times

$\rightarrow$  no glitches

Additionally, only one bit from the thermometer code switches at a time

$\rightarrow$  no glitches

Monotonicity: every increasing code increases the output current

$\rightarrow$  monotonicity guaranteed

Area:  $15=2^N-1$  unit resistors  $\rightarrow$  exponential increase with bit size  $N$

(same as DAC with binary-weighted resistors)



## Exercise 7 – Solution

b)

Property	Binary-weighted	R-2R	Thermometer
$R_{\max}/R_{\min}$	:(	:)	:)
$I'_{\max}/I'_{\min}$	:(	:(	:)
Area	:(	:)	:(
Power	:)	:)	:(
Monotonicity	:(	:(	:)
Glitches	:(	:(	:)

# Chapter 7

## Nyquist-Rate

## Analog-to-Digital Converters

Dr. Florin Burcea (revised by)  
Courtesy of Dr. Stephan Henzler

## Outline

- Comparators
- Flash ADCs
- Integrating ADCs
- Successive-approximation ADCs
- Non-binary successive-approximation ADCs



## Outline

- Comparators
- Flash ADCs
- Integrating ADCs
- Successive-approximation ADCs
- Non-binary successive-approximation ADCs

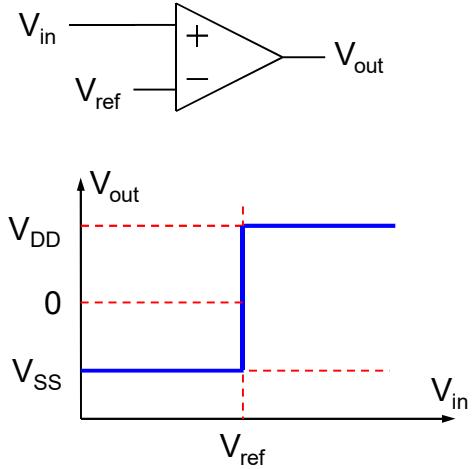


## Comparator

- 1-bit quantizer → simplest ADC

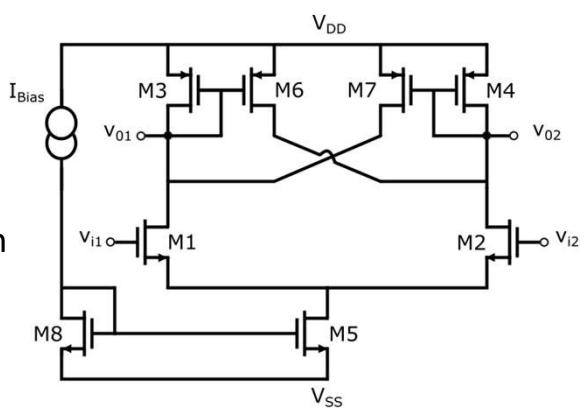
$V_{in} > V_{ref}$	$V_{out} = V_{DD}$	Digital 1
$V_{in} < V_{ref}$	$V_{out} = V_{SS}$	Digital 0

- High-gain amplifier (ideally infinite) → output signal clipped
- Operational amplifier (open-loop) as a comparator:
  - continuous-time
  - not very fast
  - advanced technology nodes: only 20-30 dB gain/stage



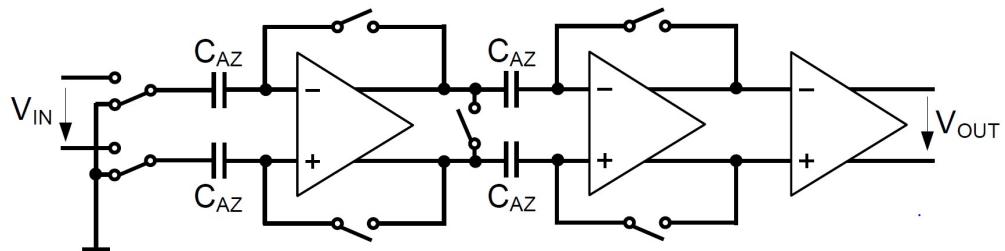
## Comparator Design Considerations

- Needs to be fast in decision
- Needs to trigger at the right point (offset is an issue → auto-zeroing)
- Hysteresis wanted
- Does not need frequency compensation
- High gain and high bandwidth desired → slightly differently optimized version of differential pair



## Comparator Speed Improvement

- Comparator: no feedback requirements
- Cascade several stages (fast, but with limited gain) to obtain a fast comparator result
- Last stage: often a standard CMOS inverter
- Implementation example with auto-zeroing during sampling:



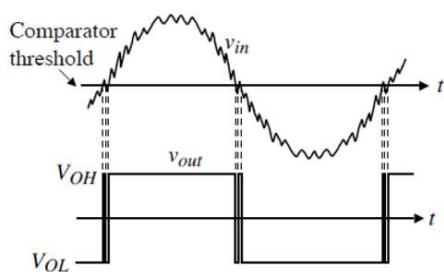
305



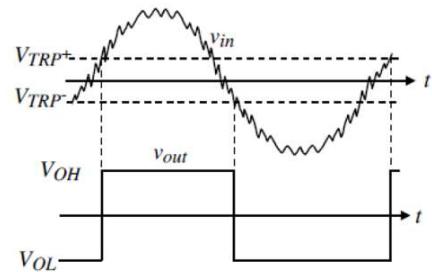
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## Comparator Hysteresis

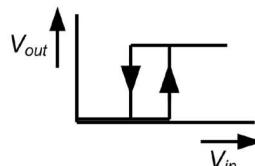
Output without hysteresis



Output with hysteresis



- Transfer function with hysteresis:  
→ delays next decision by setting a time or voltage threshold

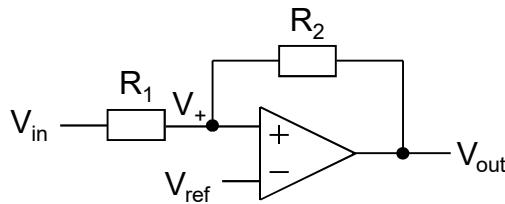


$$V_{HYS} = V_{TRP+} - V_{TRP-}$$

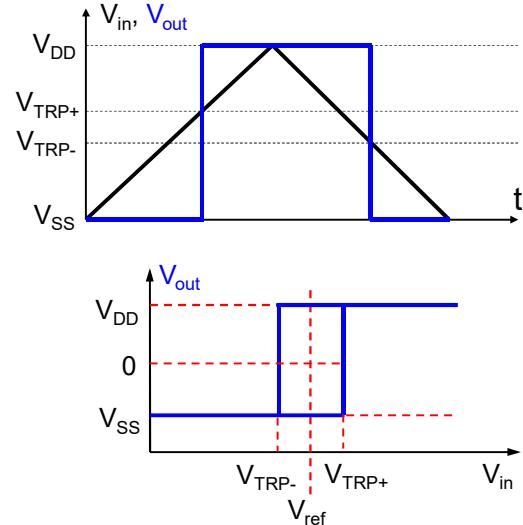
Illustrations: P. Allen, D. Holberg, CMOS Analog Circuit Design, Oxford 2002  
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306

## External Positive Feedback

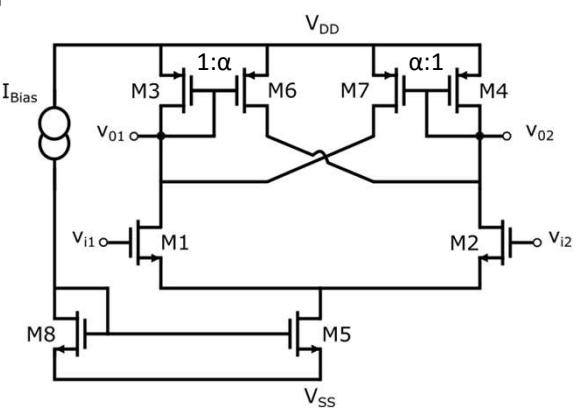


- $V_{out} = V_{SS}$ :  $V_+ = V_{ref}$   
 $\rightarrow V_{in} = V_{ref} + (V_{ref} - V_{SS}) \frac{R_1}{R_2} = V_{TRP^+}$
- $V_{out} = V_{DD}$ :  $V_+ = V_{ref} \rightarrow$   
 $\rightarrow V_{in} = V_{ref} + (V_{ref} - V_{DD}) \frac{R_1}{R_2} = V_{TRP^-}$
- $V_{HYS} = V_{TRP^+} - V_{TRP^-} = (V_{DD} - V_{SS}) \frac{R_1}{R_2}$



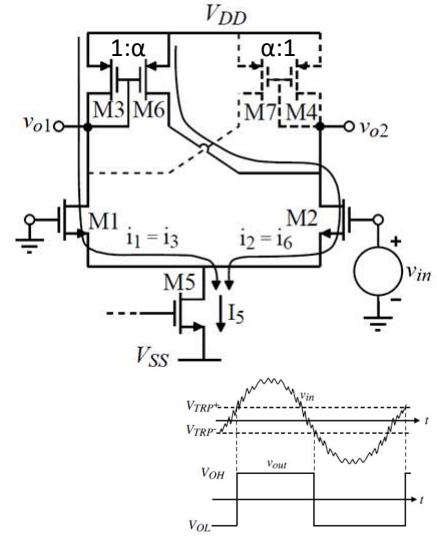
## Internal Positive Feedback

- Hysteresis can be set by a positive feedback
- Positive feedback through M6-M7  
 $\rightarrow$  introduces hysteresis and improves speed
- Hysteresis controlled by current mirror ratio:  
 $\alpha = \frac{(W/L)_6}{(W/L)_3} = \frac{(W/L)_7}{(W/L)_4} > 1$



## Internal Positive Feedback – Upper Trip Point

- Assume  $v_{i1}=0$ ,  $v_{i2} \ll 0$   
 $\rightarrow M1$  on,  $M2$  off  $\rightarrow v_{o2}$  high  
 $\rightarrow M3$  on (sat.),  $M6$  on (triode),  $M4, M7$  off
- As  $v_{in} \nearrow : i_2 \nearrow, v_{o2} \searrow$ ,  
 $M2$  turns on,  $M6$  goes into saturation
- Trip point occurs when  $i_2 = i_6 = \alpha \cdot i_3$   
(boundary where  $M4, M7$  start turning on)  
 $I_5 = i_1 + i_2 = i_3 + i_6 = i_3 + \alpha i_3$   
 $\rightarrow i_1 = i_3 = \frac{I_5}{1+\alpha}$        $i_2 = I_5 - i_1 = \frac{\alpha I_5}{1+\alpha} > i_1$
- Trip point:  $V_{TRP^+} = v_{GS2} - v_{GS1} = \sqrt{\frac{2i_2}{\beta_{1,2}}} - \sqrt{\frac{2i_1}{\beta_{1,2}}}$   
 $\rightarrow V_{TRP^+} = \frac{(\sqrt{\alpha}-1)\sqrt{2I_5}}{\sqrt{\beta_{1,2}(1+\alpha)}}$



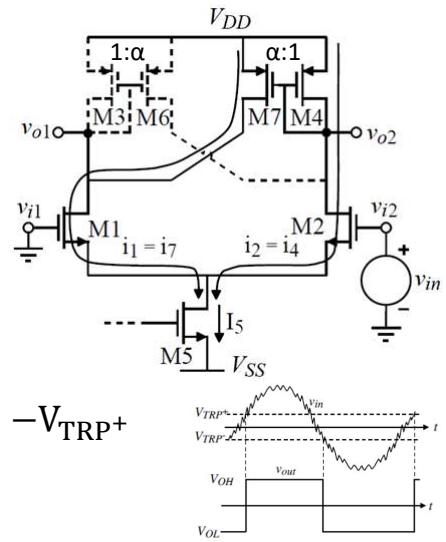
Illustrations: P. Allen, D. Holberg, CMOS Analog Circuit Design, Oxford 2002

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309

## Internal Positive Feedback – Lower Trip Point

- Assume  $v_{i1}=0$ ,  $v_{i2} \gg 0$   
 $\rightarrow M2$  on,  $M1$  off  $\rightarrow v_{o1}$  high  
 $\rightarrow M4$  on (sat.),  $M7$  on (triode),  $M3, M6$  off
- As  $v_{in} \searrow : i_1 \nearrow, v_{o1} \searrow$ ,  
 $M1$  turns on,  $M7$  goes into saturation
- Trip point occurs when  $i_1 = i_7 = \alpha \cdot i_4$   
(boundary where  $M3, M6$  start turning on)  
 $I_5 = i_1 + i_2 = i_4 + i_7 = i_4 + \alpha i_4$   
 $\rightarrow i_2 = i_4 = \frac{I_5}{1+\alpha}$        $i_1 = I_5 - i_2 = \frac{\alpha I_5}{1+\alpha} > i_2$
- Trip point:  $V_{TRP^-} = v_{GS2} - v_{GS1} = \frac{(1-\sqrt{\alpha})\sqrt{2I_5}}{\sqrt{\beta_{1,2}(1+\alpha)}} = -V_{TRP^+}$
- Hysteresis:  $V_{HYS} = V_{TRP^+} - V_{TRP^-} = 2V_{TRP^+}$



Illustrations: P. Allen, D. Holberg, CMOS Analog Circuit Design, Oxford 2002

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310

## Internal Positive Feedback – Two Stages

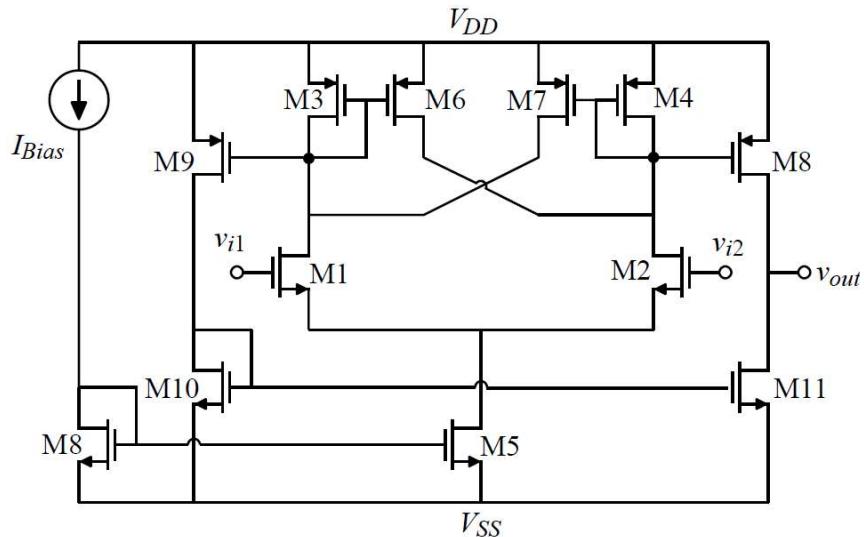


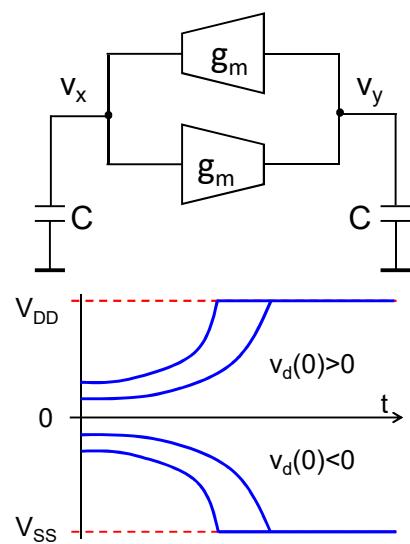
Illustration: P. Allen, D. Holberg, CMOS Analog Circuit Design, Oxford 2002

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311

## Latched Comparator – Concept

- Two transconductance amplifiers ( $g_m$ ) with capacitive load ( $C$ ), cross-coupled
- $-g_m v_x = C \dot{v}_y$   
 $-g_m v_y = C \dot{v}_x$   
 $v_d = v_x - v_y \rightarrow \dot{v}_d = (g_m/C) v_d$   
 $\rightarrow v_d(t) = v_d(0) \exp\left(\frac{g_m}{C} t\right)$
- Positive feedback  
 $\rightarrow$  amplitude increases until saturation (clip)  
 $\rightarrow$  latching operation
- $v_d(0)$  larger  $\rightarrow$  clip reached faster

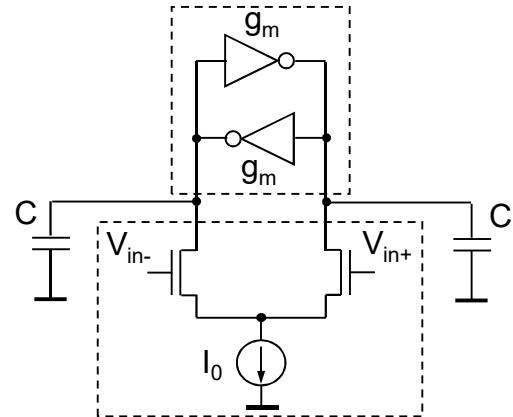


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312

## Latched Comparator – Circuit Realization

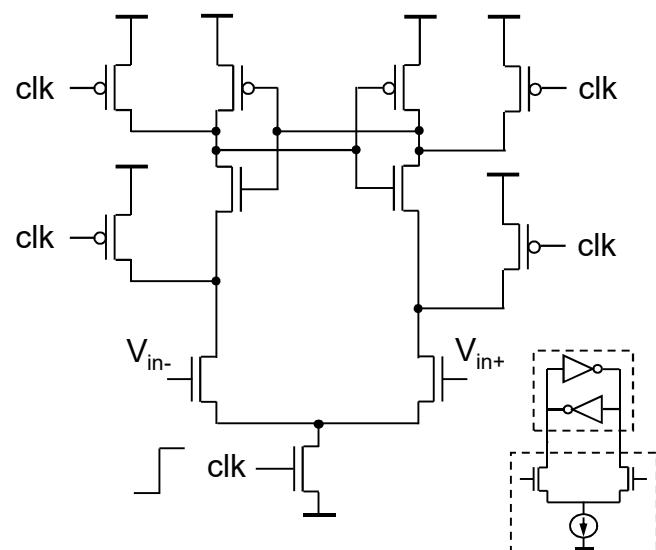
- Differential amplifier: provides input signal for the latch
- Latch: cross-coupled inverters
- Capacitance: load + parasitics



313

## Latched Comparator – Circuit Realization

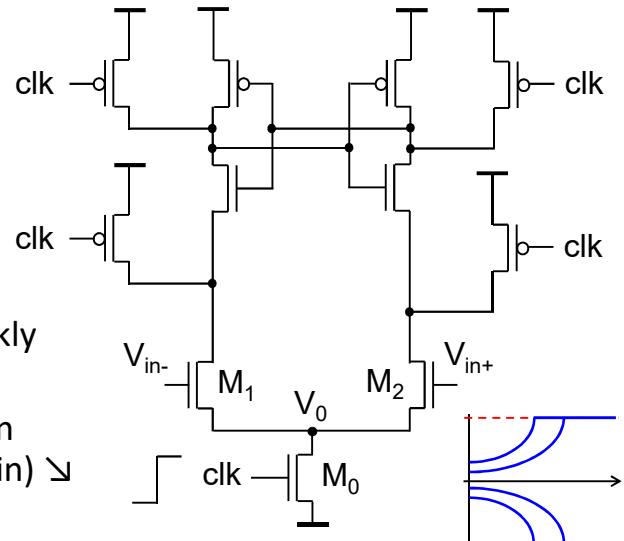
- Bottom transistor:  
acting as a sampling switch  
→ samples when clock goes high
- Clock low: reset phase  
→ one latching operation  
not affected by the previous
- StrongARM latch /  
Sense-amplifier-based latch



314

## Sense-Amplifier Latch

- $v_d(t) \propto v_d(0) \exp\left(\frac{g_m}{C} t\right)$
- High  $g_m \rightarrow$  fast latch regeneration
- Initially (rising clock edge):
  $V_0 = V_{DD}$ ,  $M_0$  in saturation region  
 $\rightarrow$  high current  $\rightarrow g_m$  initially high
- Small initial voltage:  
 high gain needed to regenerate quickly
- During regeneration:  
 $\rightarrow V_0 \downarrow \rightarrow M_0$  moves to linear region  
 $\rightarrow$  current  $\downarrow \rightarrow g_m$  (regeneration gain)  $\downarrow$   
 but high gain no longer needed

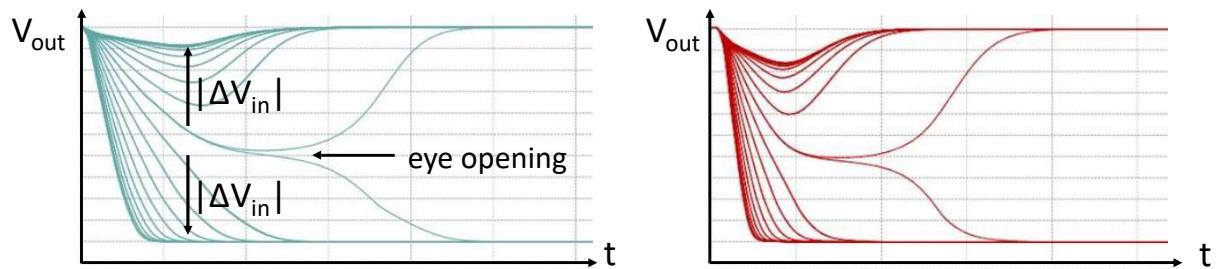


315



## Sense-Amplifier Latch

- Eye diagram  $V_{out}$  vs.  $\Delta V_{in}$ : latch speed  $\nearrow \rightarrow$  eye opening  $\nearrow$



- Dynamic/Clocked/Discrete-time comparator
- 2-bit latch:  $2^2$ -1 comparators with different thresholds  
 (repetition of the same circuit)

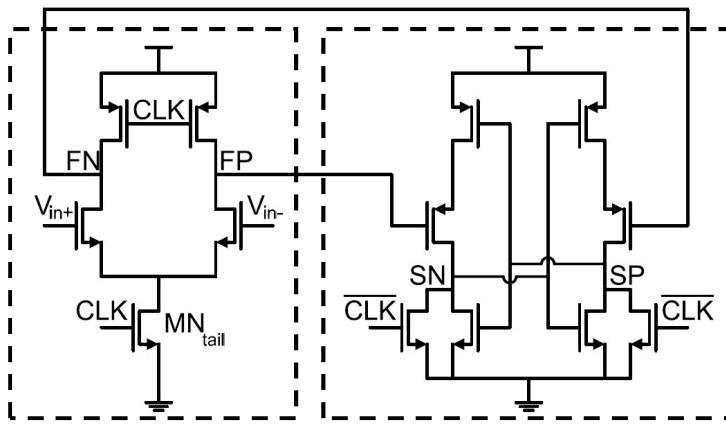
Further reading: B. Razavi, The StrongARM Latch, IEEE SSC Magazine, 2015



316

## Dynamic Two-Stage Comparator

- Pre-amplifier + latch

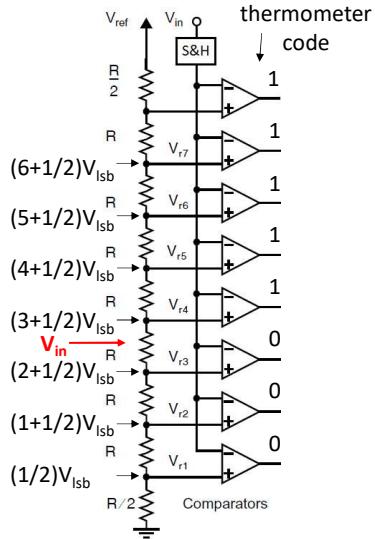


Further reading: M. van Elzakker et al., "A  $1.9\mu\text{W}$   $4.4\text{fJ}/\text{Conversion-step}$  10b 1MS/s Charge-Redistribution ADC", IEEE ISSCC 2008

## Outline

- Comparators
- Flash ADCs
- Integrating ADCs
- Successive-approximation ADCs
- Non-binary successive-approximation ADCs

## Flash ADC



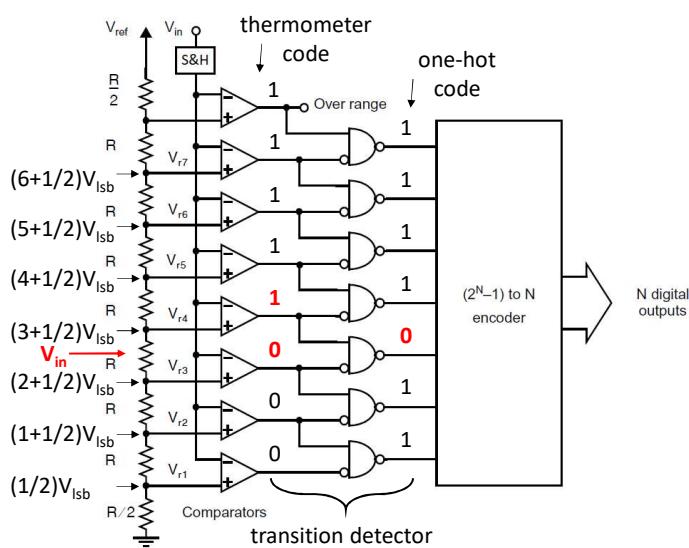
- Generate all switching thresholds in parallel and compare them to the input voltage in parallel.
- Advantages:
  - parallel processing → very fast
  - no analog post-processing
- One comparator per quantization level ( $2^N$ )
- Very high effort in terms of: area, power, noise, synchronous clock distribution, input buffering (high input capacitance)
- Practical in high-speed applications with low resolution → but often used in combinations ...



Illustration: T. Carusone, D. Johns, K. Martin, Analog Integrated Circuit Design, Wiley 2012

319

## Digital Decoding



- Thermometer to binary decoder → often implemented in 2 steps
  - thermometer → one-hot
  - one-hot → binary
- Allows for insertion of bubble correction in between decoders



Illustration: T. Carusone, D. Johns, K. Martin, Analog Integrated Circuit Design, Wiley 2012

320

## Bubble Correction

- Bubbles caused by:
  - noise
  - meta-stability
  - cross-talk
  - mismatch
- Basic bubble correction with 3-input NAND gate: transition only detected if more than one high signal occurs.
- More complex encoders to eliminate long-distance errors

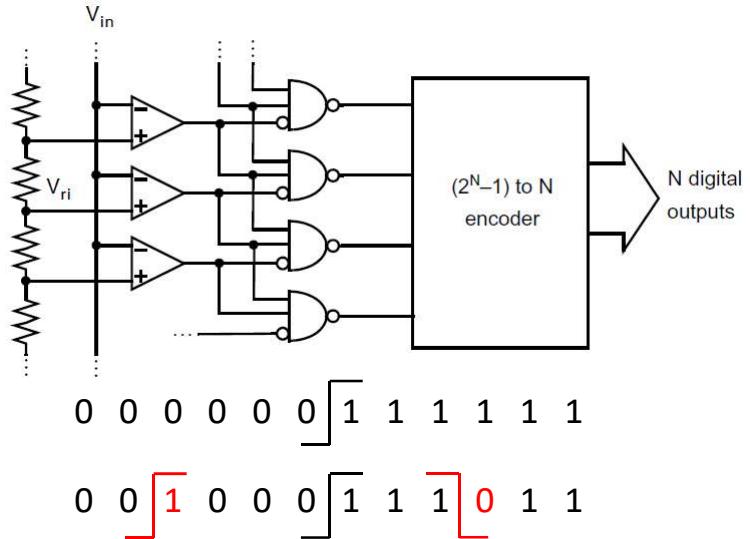
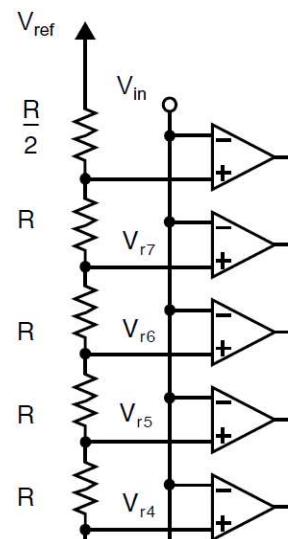


Illustration: T. Carusone, D. Johns, K. Martin, Analog Integrated Circuit Design, Wiley 2012  
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321

## Kickback

- Especially in flash ADCs
- Clocked comparators produce lots of noise at their inputs when toggling from track to latch mode.
- Different impedance seen from the comparator inputs (input drive vs resistor string)  
→ differential error that may corrupt next conversion
- Error decay sets maximum sampling rate



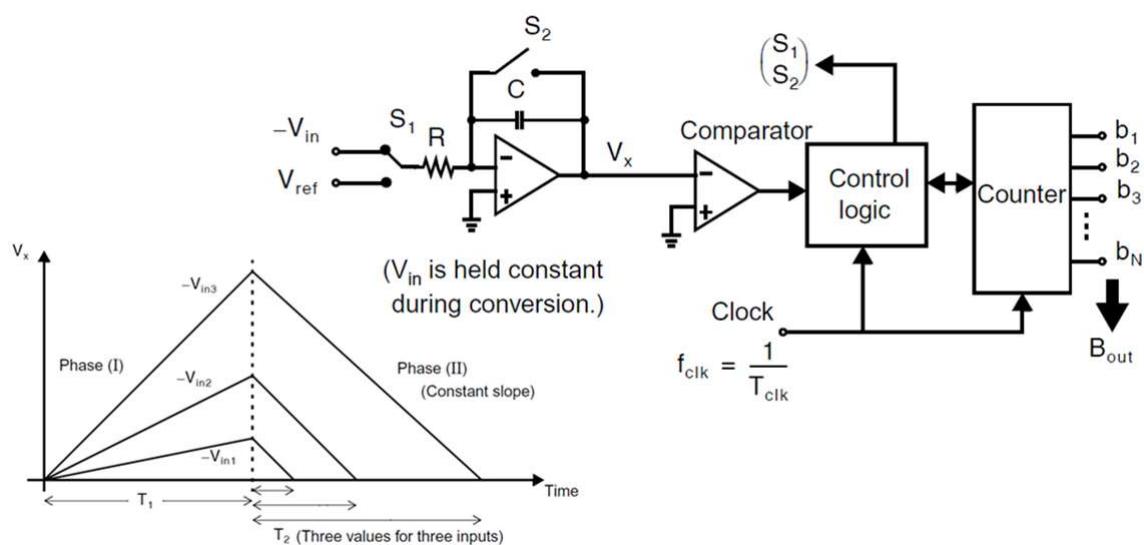
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322

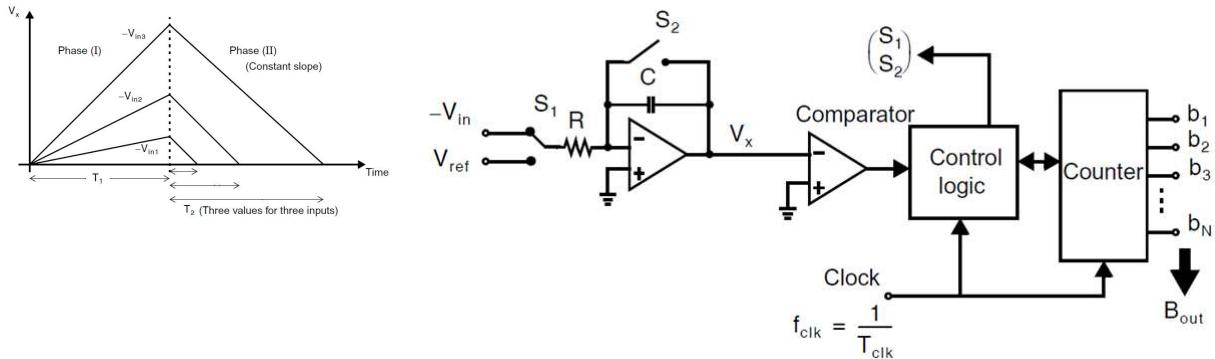
# Outline

- Comparators
- Flash ADCs
- Integrating ADCs
- Successive-approximation ADCs
- Non-binary successive-approximation ADCs

# Dual-Slope ADC



## Dual-Slope ADC



## Dual-Slope ADC

- $\frac{T_2}{T_{clk}} = \frac{V_{in}}{V_{lsb}} = \# \text{ clock cycles}$
- Digital output independent of time constant RC  
→ very robust to manufacturing variations  
→ high accuracy
- Very low offset and gain errors, very linear
- Inherent first-order low-pass filtering of the input signal
- Small amount of circuitry needed
- Disadvantage: low conversion speed
- Traditionally used in measurement instruments (voltage and current meters)

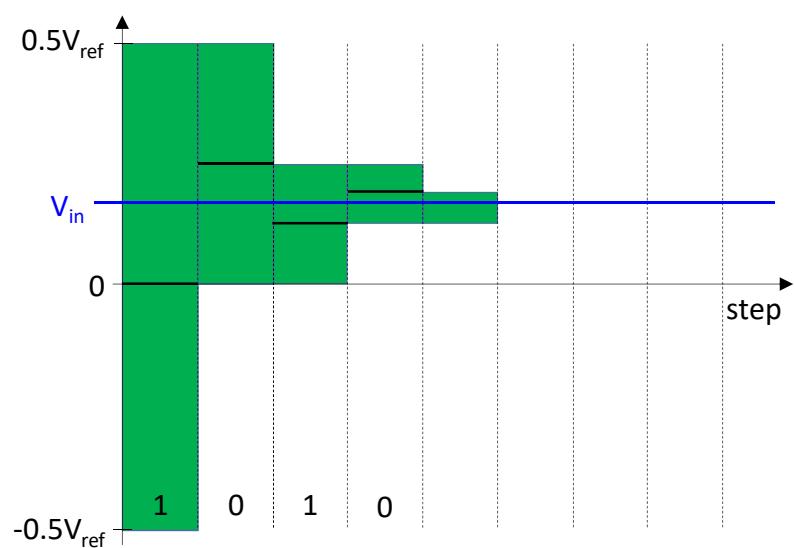
# Outline

- Comparators
- Flash ADCs
- Integrating ADCs
- Successive-approximation ADCs
- Non-binary successive-approximation ADCs

327

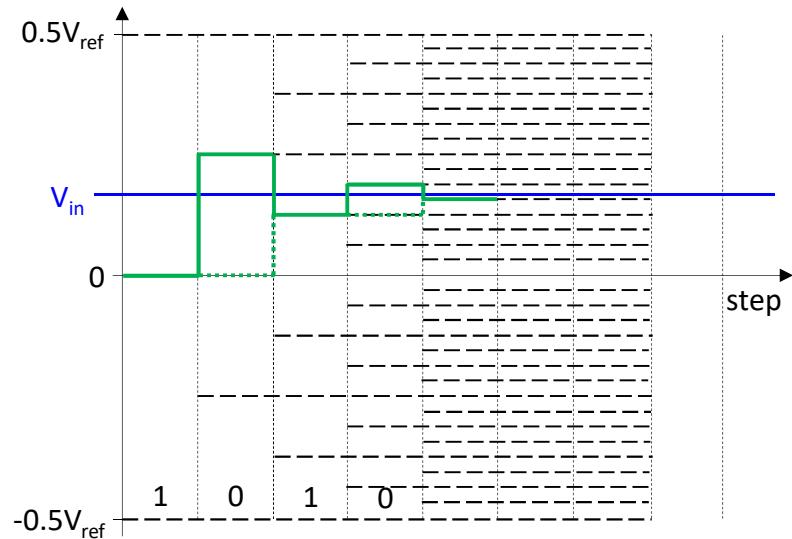
# Binary Search

- Partition the interval where the voltage is located in two equal sub-intervals and check whether the voltage lies in the upper or in the lower part.



328

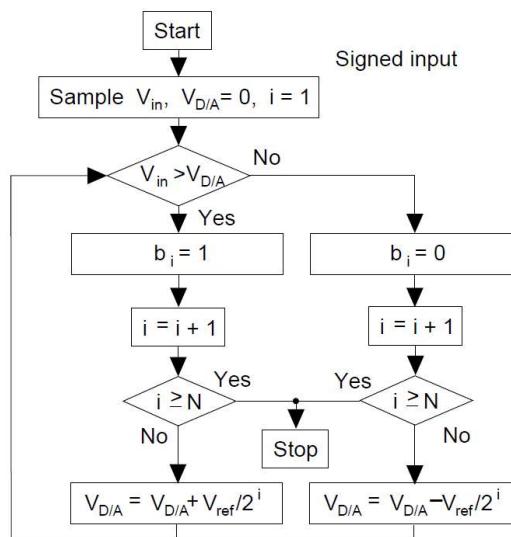
## Successive Approximation



329



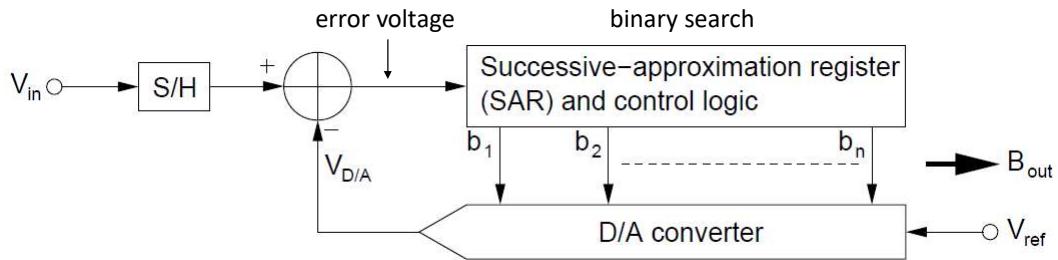
## Successive Approximation Algorithm



330

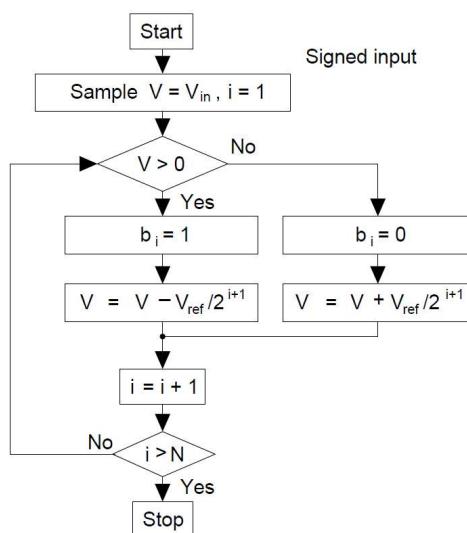


## Successive-Approximation-Register (SAR) ADC



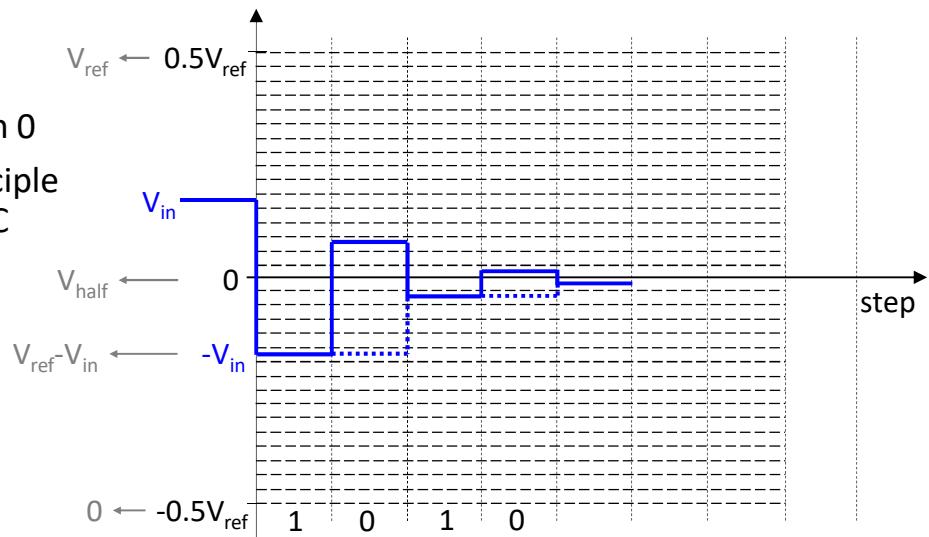
- ADC: mainly a DAC and a comparator
- Conversion principle (goal):
  - make DAC voltage equal to input voltage
  - make error voltage zero

## Modified Successive Approximation Algorithm



## Modified Successive Approximation

- Also based on binary search
- Comparison with 0
- Conversion principle (goal): make DAC voltage zero



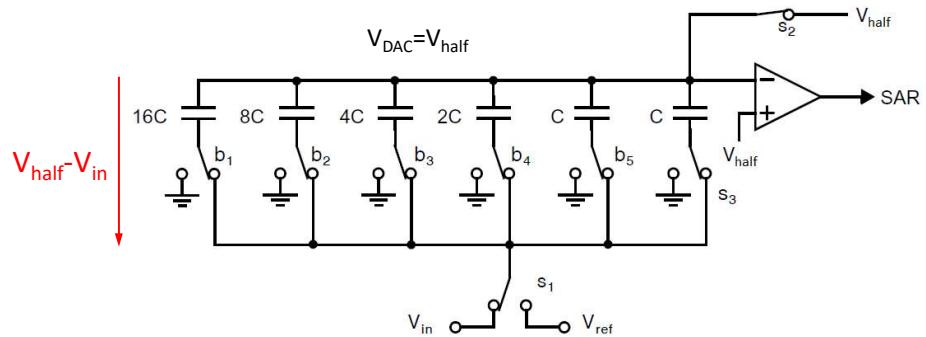
333



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## Charge Redistribution ADC

- Phase I:  
Input tracking  
(Sampling)



- Binary-weighted capacitor array, total capacitance  $C_{tot} = 32C$
- Total charge stored on the capacitor array:  $Q_{tot} = C_{tot}(V_{half} - V_{in})$



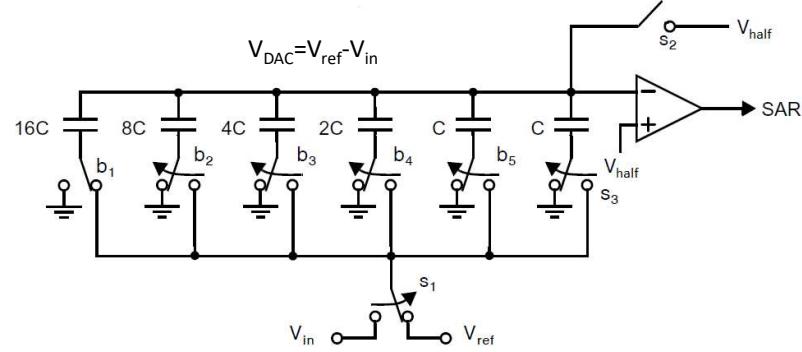
Illustration: T. Carusone, D. Johns, K. Martin, Analog Integrated Circuit Design, Wiley 2012

334

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## Charge Redistribution ADC

Phase II:  
SAR evaluation  
(Bit cycling)



- Top plate floating  
→ charge conservation

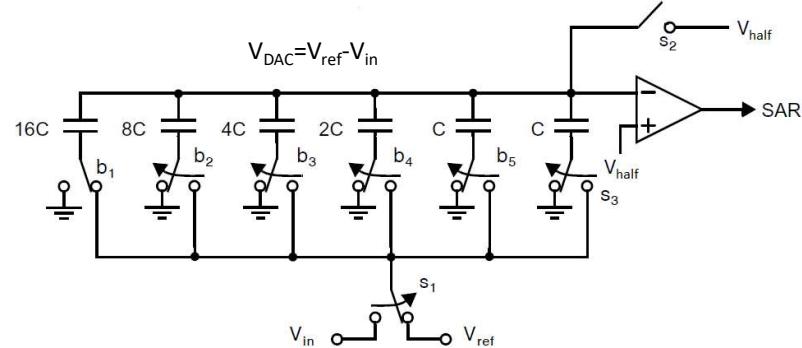


Illustration: T. Carusone, D. Johns, K. Martin, Analog Integrated Circuit Design, Wiley 2012  
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335

## Charge Redistribution ADC

Phase II:  
SAR evaluation  
(Bit cycling)  
Iteration 1



- $V_{DAC} = V_{half} - V_{in} + (1/2)V_{ref} = V_{ref} - V_{in} \rightarrow$  inversion of  $V_{in}$  around  $V_{half}$
- $V_{DAC} - V_{half} = -V_{in} + (1/2)V_{ref}$
- If  $V_{DAC} < V_{half}$  then  $b_1=1$  else  $b_1=0$

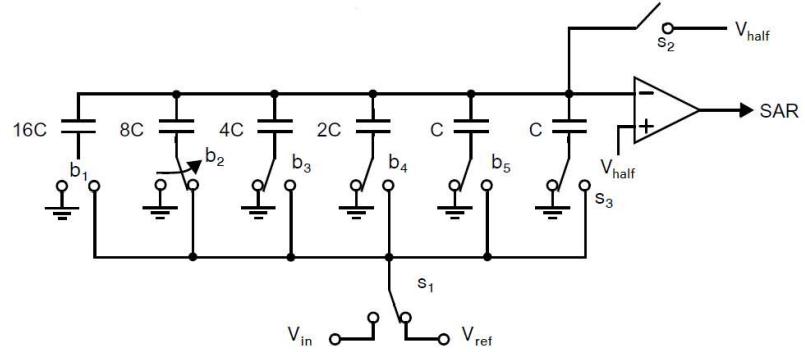


Illustration: T. Carusone, D. Johns, K. Martin, Analog Integrated Circuit Design, Wiley 2012  
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336

## Charge Redistribution ADC

Phase II:  
SAR evaluation  
(Bit cycling)  
Iteration 2



- If  $V_{DAC} - V_{half} < 0$  then  $b_2=1$  else  $b_2=0$

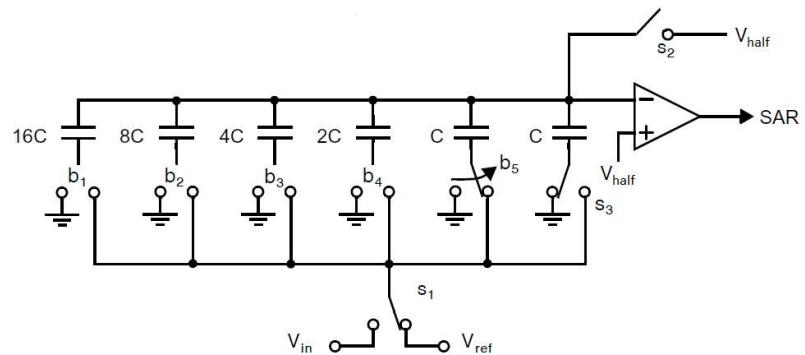


Illustration: T. Carusone, D. Johns, K. Martin, Analog Integrated Circuit Design, Wiley 2012

337

## Charge Redistribution ADC

Phase II:  
SAR evaluation  
(Bit cycling)  
Last iteration



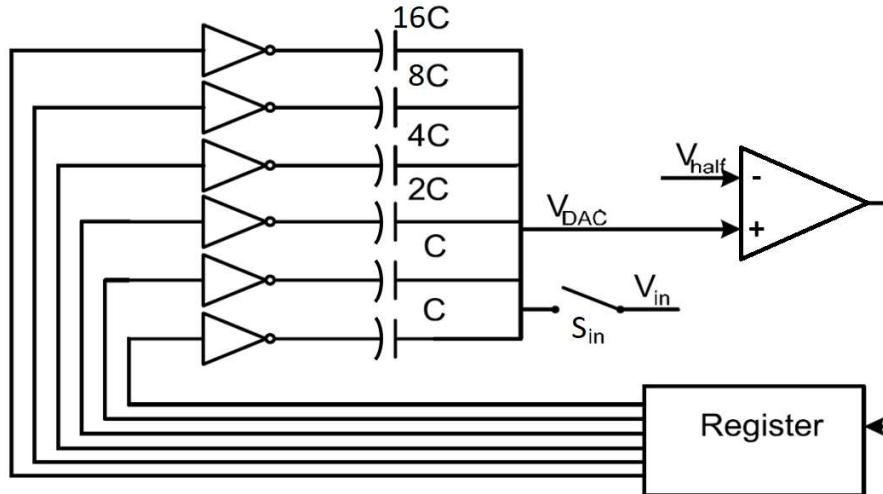
- If  $V_{DAC} - V_{half} < 0$  then  $b_5=1$  else  $b_5=0$



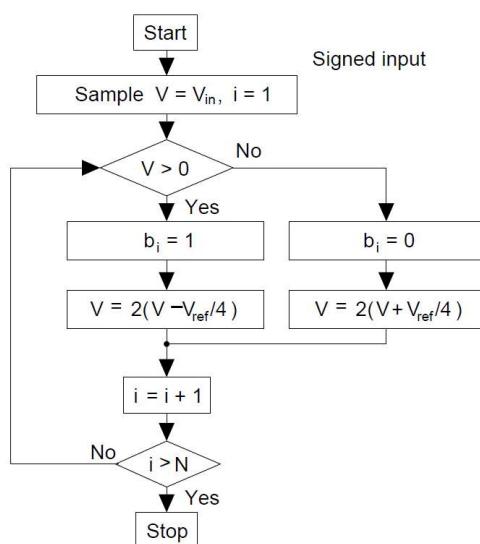
Illustration: T. Carusone, D. Johns, K. Martin, Analog Integrated Circuit Design, Wiley 2012

338

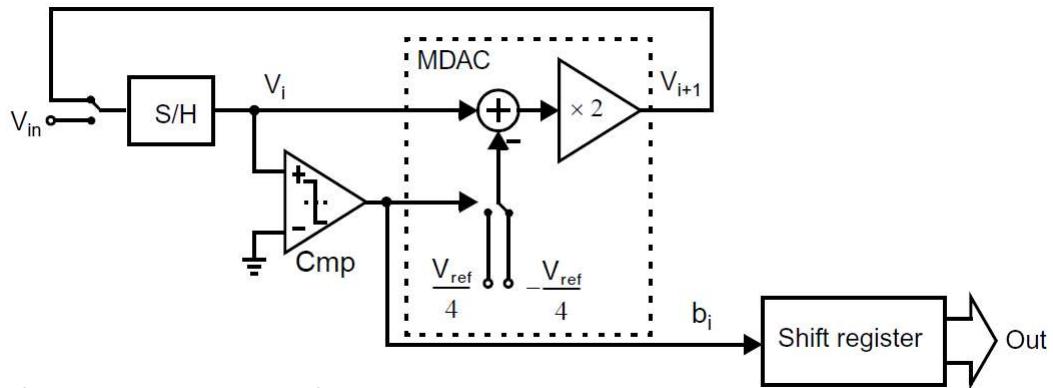
## Alternative Implementation



## Algorithmic (Cyclic) ADC

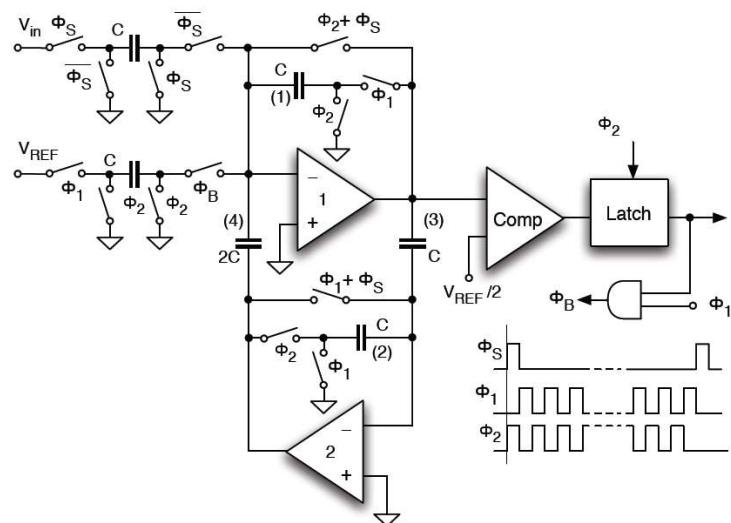


## Algorithmic (Cyclic) ADC



- Similar in operation to the SAR converter
- Instead of scaling  $V_{ref}$  after the comparator decision, the same  $V_{ref}/4$  is subtracted or added and the error (or residue) is doubled.

## Algorithmic (Cyclic) ADC



## Sub-ranging ADC

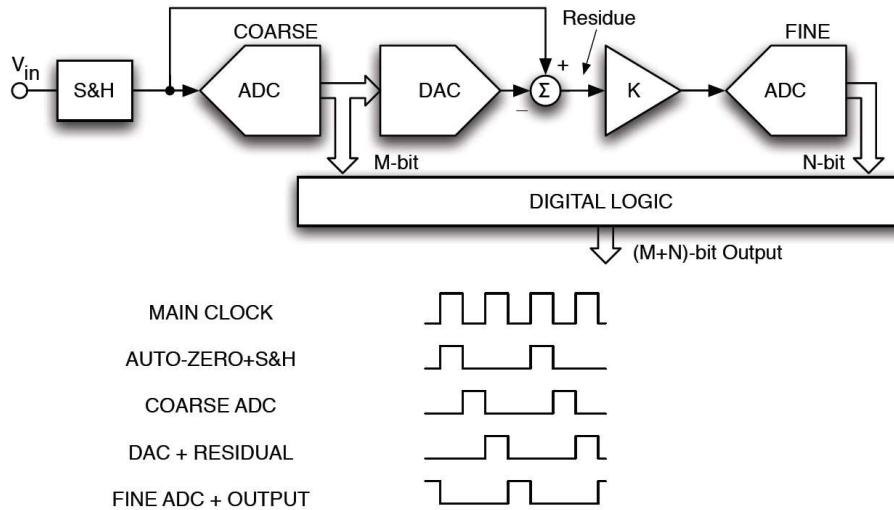
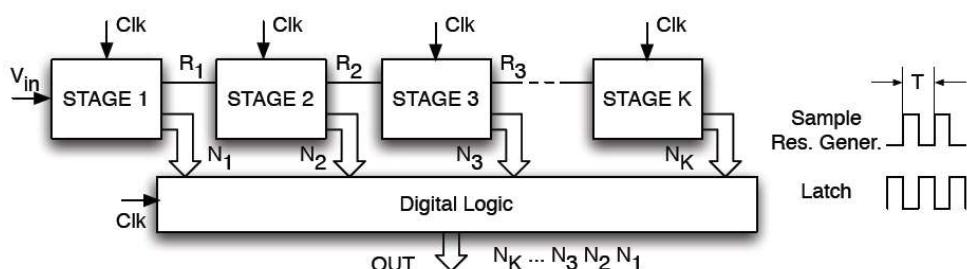


Illustration: F. Maloberti, Data Converters, Springer 2007

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343

## Pipeline ADC



- Sub-ranging ADC concept extended to higher number of stages
- Often uses low-resolution flash sub-ADC in all or some stages.
- Each stage requires one or more clock periods to generate the outputs.
- The pipeline ADC generates the output with a latency time that increases with the number of stages. Be aware of the latency time when using the converter in a feedback loop!

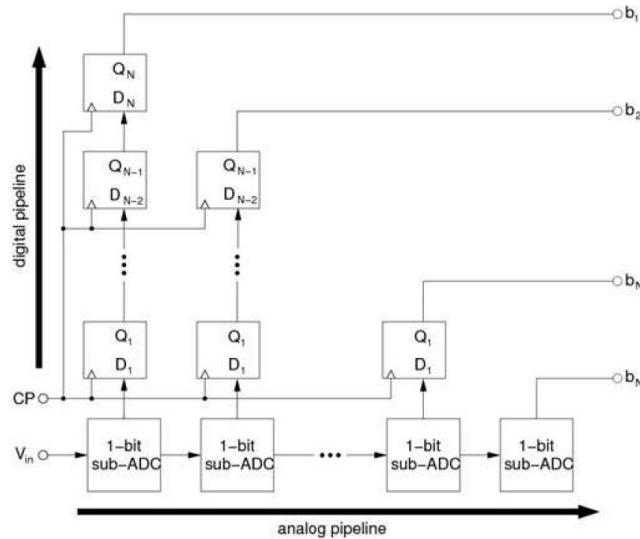


Illustration: F. Maloberti, Data Converters, Springer 2007

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344

## High-speed ADC: Pipeline Processing



345



## Pipeline Timing Diagram

- Example:  
10-bit ADC  
pipeline of 2-bit stages

S&H	S&H n	S&H n+1	S&H n+2				
Stage 1	$b_9-b_8$ $n-1$	$b_9-b_8$ $n$	$b_9-b_8$ $n+1$	$b_9-b_8$ $n+2$			
Stage 2		$b_7-b_6$ $n-1$	$b_7-b_6$ $n$	$b_7-b_6$ $n+1$	$b_7-b_6$ $n+2$		
Stage 3			$b_5-b_4$ $n-1$	$b_5-b_4$ $n$	$b_5-b_4$ $n+1$	$b_5-b_4$ $n+2$	
Stage 4				$b_3-b_2$ $n-1$	$b_3-b_2$ $n$	$b_3-b_2$ $n+1$	$b_3-b_2$ $n+2$
Stage 5					$b_1-b_0$ $n-1$	$b_1-b_0$ $n$	$b_1-b_0$ $n+1$
Digital						OUT $n-1$	OUT $n$

$t$

n n+1 n+2 n+3 n+4 n+5 n+6

346



## Outline

- Comparators
- Flash ADCs
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- Non-binary successive-approximation ADCs



## Binary and Non-Binary Search Algorithms

N-bit, M-step

- Binary search algorithm  $\rightarrow M=N$   
 $D = 8 \cdot b_3 + 4 \cdot b_2 + 2 \cdot b_1 + 1 \cdot b_0 \rightarrow$  4-bit, 4-step
- Non-binary search algorithms  $\rightarrow M>N \rightarrow M-N$  redundant steps  
 $D = 6 \cdot b_4 + 4 \cdot b_3 + 2 \cdot b_2 + 2 \cdot b_1 + 1 \cdot b_0 \rightarrow$  4-bit, 5-step  
 $D = 4 \cdot b_4 + 4 \cdot b_3 + 4 \cdot b_2 + 2 \cdot b_1 + 1 \cdot b_0 \rightarrow$  4-bit, 5-step
- Binary format: unique representation for each number D  
Non-binary format: multiple representations for most numbers D



## Binary and Non-Binary Representation

Binary					Non-binary										
8	4	2	1		6	4	2	2	1	6	4	2	2	1	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	0	0	0	1	1	1	0	0	1	0	1
0	0	1	0	2	0	0	0	1	0	2	0	0	1	0	2
0	0	1	1	3	0	0	0	1	1	3	0	0	1	1	3
0	1	0	0	4	0	0	1	0	0	2	0	1	0	0	8
0	1	0	1	5	0	0	1	0	1	3	0	1	0	1	9
0	1	1	0	6	0	0	1	1	0	4	0	1	0	1	9
0	1	1	1	7	0	0	1	1	1	5	0	1	1	1	10
1	0	0	0	8	0	1	0	0	0	4	1	0	1	1	11
1	0	0	1	9	0	1	0	0	1	5	1	1	0	0	10
1	0	1	0	10	0	1	0	1	0	6	1	1	0	1	12
1	0	1	1	11	0	1	0	1	1	7	1	1	1	0	13
1	1	0	0	12	0	1	1	0	0	6	1	1	1	0	12
1	1	0	1	13	0	1	1	0	1	7	1	1	1	0	13
1	1	1	0	14	0	1	1	1	0	8	1	1	1	1	14
1	1	1	1	15	0	1	1	1	1	9	1	1	1	1	15

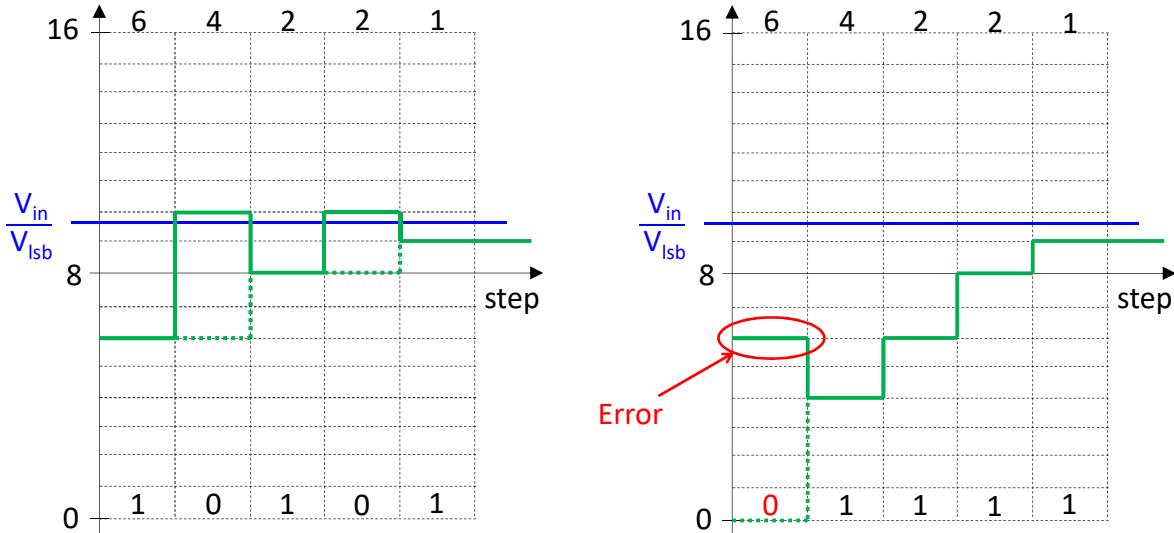
## Binary vs Non-Binary Search

- Algorithmic perspective: redundancy lowers efficiency
- Circuit perspective (dynamic behavior) → high-frequency ADC:
  - Fast, precise (low-offset, low-noise) comparator → power hungry
  - Alternative: slower in decision, less precise comparator
    - lower power
    - erroneous decisions  
(because of e.g. incomplete voltage settling, noise)
    - compensated by algorithmic redundancy!

Further reading:

- T. Ogawa et al., "Non-Binary SAR ADC with Digital Error Correction for Low Power Applications," in IEEE Asia Pacif. Conf. Circuits Syst., 2010.
- A. H. Chang, H. Lee and D. Boning, "A 12b 50MS/s 2.1mW SAR ADC with redundancy and digital background calibration," ESSCIRC, 2013.
- P. Harpe et al., "A 10b/12b 40 kS/s SAR ADC With Data-Driven Noise Reduction Achieving up to 10.1b ENOB at 2.2 fJ/Conversion-Step," IEEE J. Solid-State Circuits, 2013.

## Non-Binary Search Algorithm

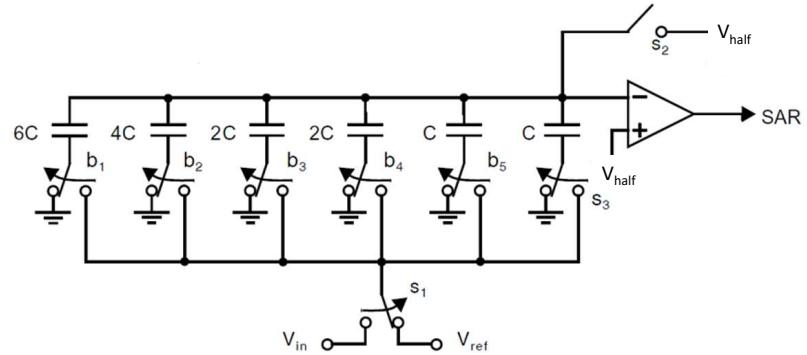


## Non-Binary SAR-ADC

- Bit errors recovered during the conversion process
- Relaxed comparator specifications (speed, power, noise, offset)
- Redundancy reduces non-linearity errors caused by mismatch
- Decoder: converts digital output with redundancy to binary-weighted format
- More conversion cycles than a binary-weighted SAR-ADC, but higher operating frequency → higher speed overall

## Non-Binary Charge-Redistribution ADC

- Example:
  - 4 bits, 5 steps
  - weights [6; 4; 2; 2; 1]



- Industrial example of charge-redistribution SAR-ADC
  - 12 bits, 13 steps
  - weights [1868; 1012; 552; 303; 168; 90; 48; 26; 14; 8; 4; 2; 1]

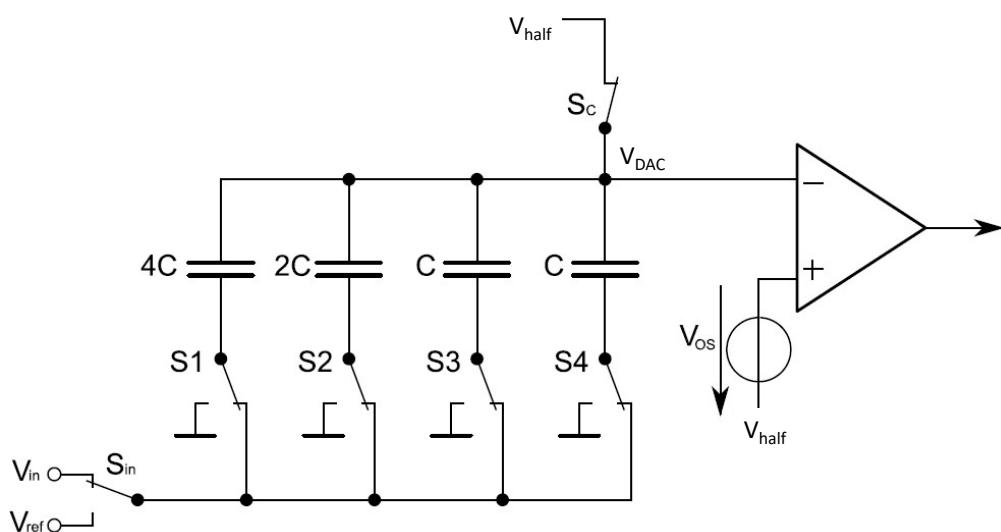
# Tutorial

## Exercise 1

Consider the following ADC. Assume the comparator to have the offset  $V_{os}$ .

- What is the bit size of this ADC?
- Accomplish a conversion for an input signal  $V_{in}=0.68V$  and a reference voltage  $V_{ref}=2V$  and sketch the voltage  $V_{DAC}$ . The offset voltage of the comparator is assumed to be zero.
- Assume an offset voltage  $V_{os}=0.2V$  for the comparator. What is the impact on the resulting bit word?

## Exercise 1



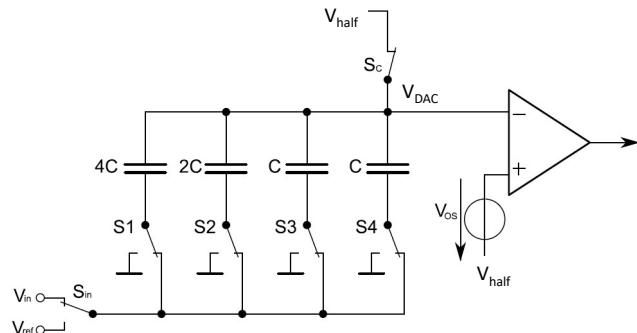
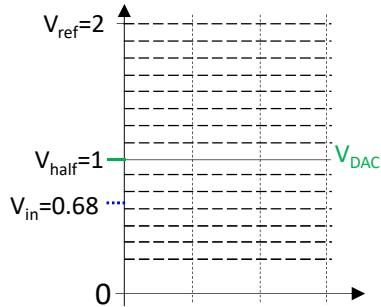
## Exercise 1 - Solution

a) 3 bits

b) Sampling

$$S_{in} \rightarrow V_{in} \quad S_c \text{ on} \quad S1-S4 \rightarrow V_{in}$$

$$V_{DAC} = \quad Q_{tot} =$$



357



## Exercise 1 - Solution

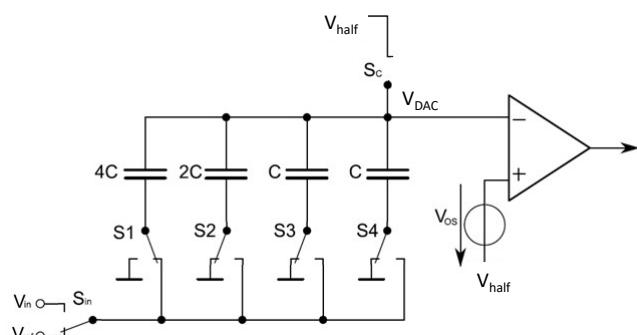
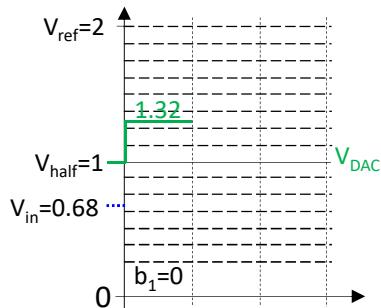
b) Bit cycling –  $b_1$

$$S1 \rightarrow V_{ref} \quad S2-S4 \rightarrow GND \quad S_c \text{ off}$$

$$Q_{tot} =$$

$$\rightarrow V_{DAC} =$$

$$\rightarrow b_1 = 0$$



358

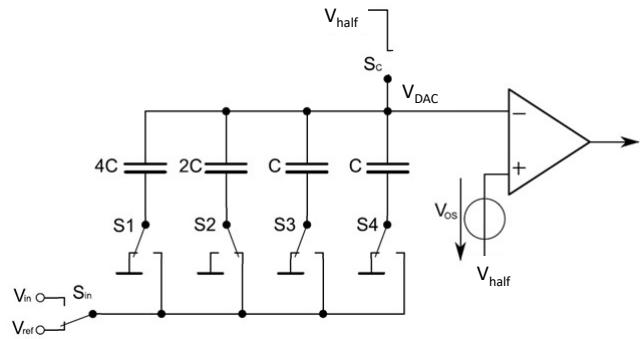
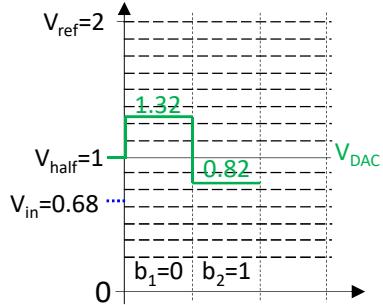


## Exercise 1 - Solution

b) Bit cycling –  $b_2$

$$S1 \rightarrow GND \quad S2 \rightarrow V_{ref} \quad S3-S4 \rightarrow GND \quad S_c \text{ off}$$

$$\begin{aligned} Q_{tot} &= \\ \rightarrow V_{DAC} &= \\ \rightarrow b_2 &= 1 \end{aligned}$$



359

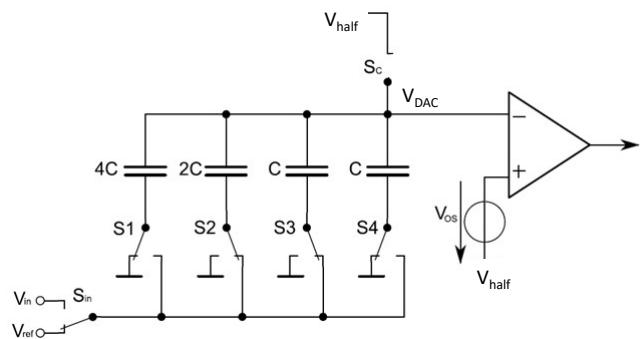
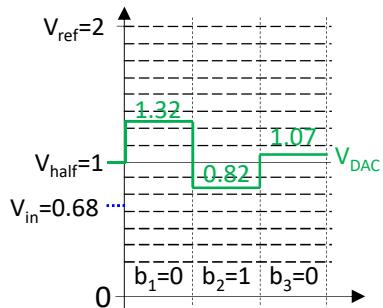


## Exercise 1 - Solution

b) Bit cycling –  $b_3$

$$S1 \rightarrow GND \quad S2 \rightarrow V_{ref} \quad S3 \rightarrow V_{ref} \quad S4 \rightarrow GND \quad S_c \text{ off}$$

$$\begin{aligned} Q_{tot} &= \\ \rightarrow V_{DAC} &= \\ \rightarrow b_3 &= 0 \end{aligned}$$

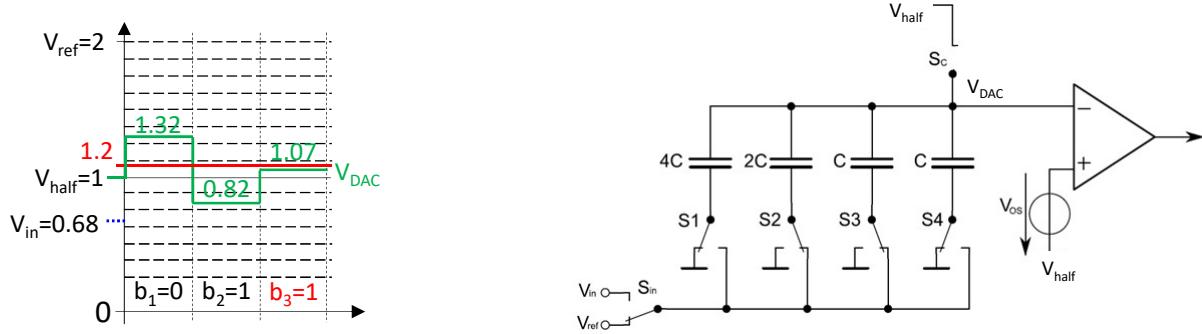


360



## Exercise 1 - Solution

- c) Comparison threshold:  $V_{half} + V_{os} = 1.2V$
- $b_1$ :  $V_{DAC} = 1.32V < 1.2V \rightarrow b_1 = 0$  (same)
  - $b_2$ :  $V_{DAC} = 0.82V > 1.2V \rightarrow b_2 = 1$  (same)
  - $b_3$ :  $V_{DAC} = 1.07V > 1.2V \rightarrow b_3 = 1 \rightarrow \text{wrong decision}$

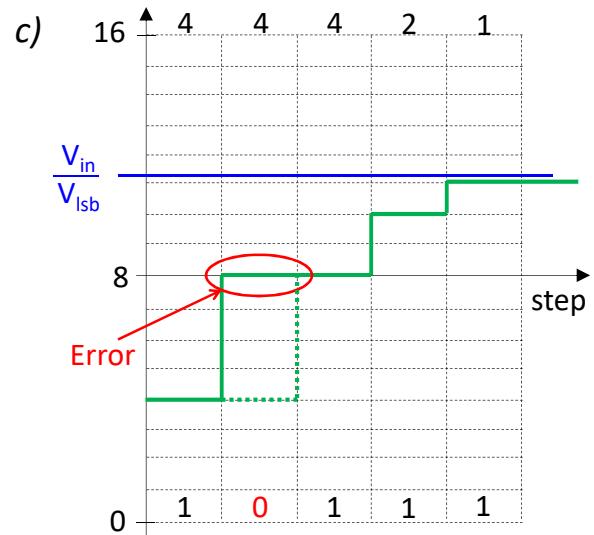
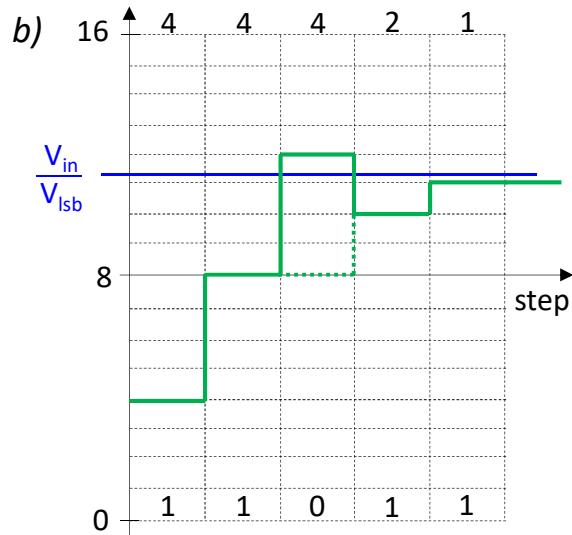


## Exercise 2

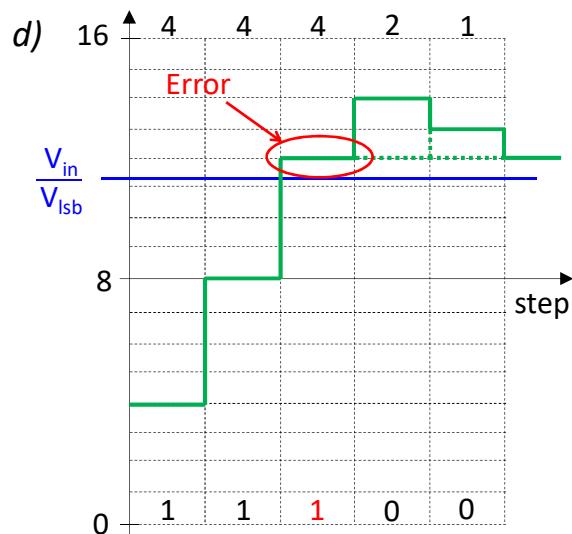
Consider a non-binary search algorithm with weights [4; 4; 4; 2; 1].

- What is the bit size N and what is the step size M?
- Accomplish a conversion for an input signal  $V_{in}=1.4V$  and a reference voltage  $V_{ref}=2V$  and sketch the intermediate voltage. What is the corresponding decimal result? Compare with  $V_{in}/V_{lsb}$ .
- Repeat b), assuming a wrong comparator decision at the second step.
- Repeat b), assuming a wrong comparator decision at the third step.

## Exercise 2 - Solution

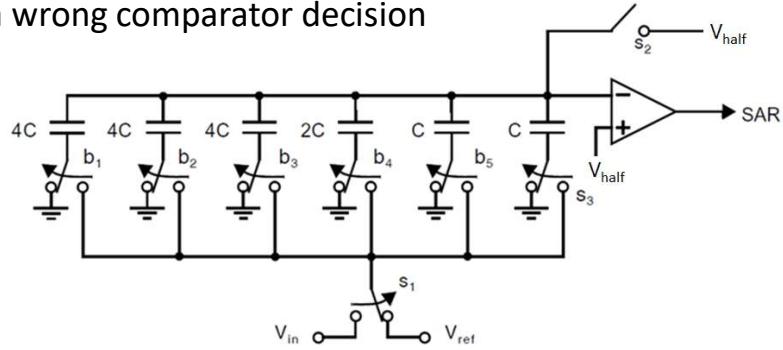


## Exercise 2 - Solution



## Exercise 2

- e) Consider a charge-redistribution ADC corresponding to the previous non-binary search algorithm with weights [4; 4; 4; 2; 1]. Accomplish the first 3 bit cycling steps, for the same input signal  $V_{in}=1.4V$  and reference voltage  $V_{ref}=2V$ , calculating  $V_{DAC}$  and the resulting output bit.
- f) Repeat e), considering a wrong comparator decision at the second step.
- g) Compare e) with b) and f) with c).



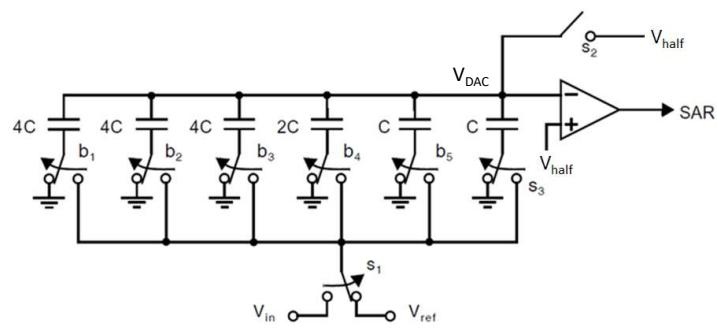
365

## Exercise 2 - Solution

- e) Sampling

$$b_1-b_5, S_3 \rightarrow S_1 \rightarrow V_{in} \quad S_2 \text{ on} \rightarrow V_{DAC}=V_{half}$$

$$Q_{tot} = 16C(V_{half} - V_{in})$$



366

## Exercise 2 - Solution

e) Bit cycling –  $b_1$

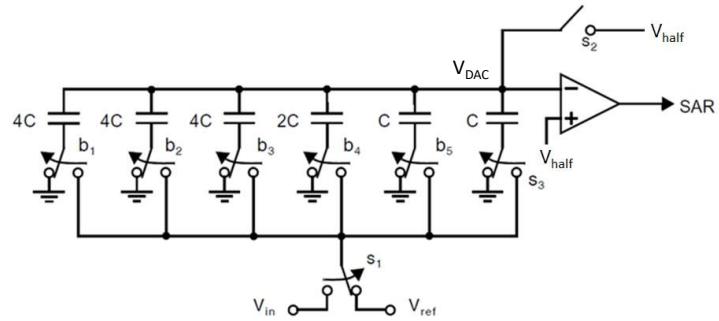
$$b_1 \rightarrow V_{ref} \quad b_2-b_5, S_3 \rightarrow GND \quad S_2 \text{ off}$$

$$Q_{tot} = 4C(V_{DAC} - V_{ref}) + 12CV_{DAC} = 16C(V_{half} - V_{in})$$

$$\rightarrow V_{DAC} = V_{half} - V_{in} + \frac{4}{16}V_{ref} = 0.1V < V_{half}$$

$$\rightarrow b_1 = 1$$

$b_1$	$b_2$	$b_3$	$b_4$	$b_5$
1				



367



## Exercise 2 - Solution

e) Bit cycling –  $b_2$

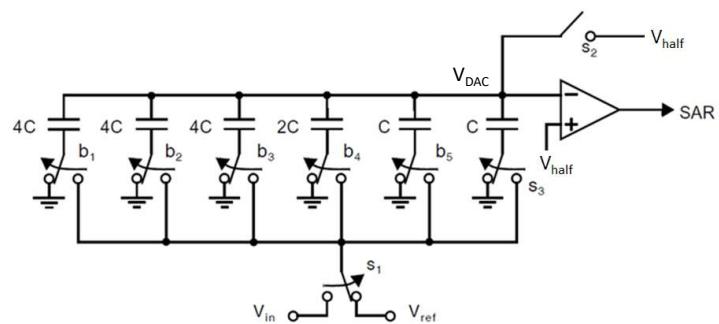
$$b_1 \rightarrow V_{ref} \quad b_2 \rightarrow V_{ref} \quad b_3-b_5, S_3 \rightarrow GND \quad S_2 \text{ off}$$

$$Q_{tot} = 8C(V_{DAC} - V_{ref}) + 8CV_{DAC} = 16C(V_{half} - V_{in})$$

$$\rightarrow V_{DAC} = V_{half} - V_{in} + \frac{8}{16}V_{ref} = 0.6V < V_{half}$$

$$\rightarrow b_2 = 1$$

$b_1$	$b_2$	$b_3$	$b_4$	$b_5$
1	1			



368

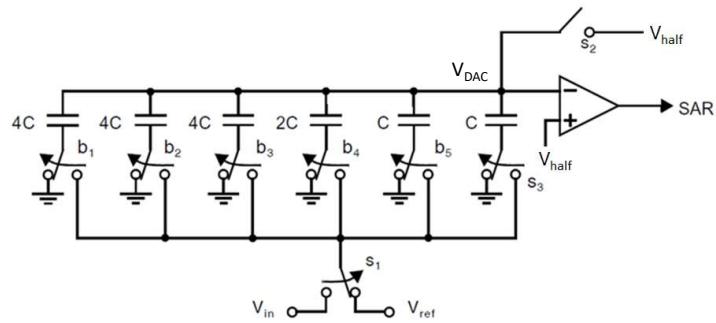


## Exercise 2 - Solution

e) Bit cycling –  $b_3$

$$\begin{aligned} b_1, b_2 &\rightarrow V_{ref} & b_3 &\rightarrow V_{ref} & b_4, b_5, S_3 &\rightarrow GND & S_2 \text{ off} \\ Q_{tot} &= 12C(V_{DAC} - V_{ref}) + 4CV_{DAC} = 16C(V_{half} - V_{in}) \\ \rightarrow V_{DAC} &= V_{half} - V_{in} + \frac{12}{16}V_{ref} = 1.1V > V_{half} \\ \rightarrow b_3 &= 0 \end{aligned}$$

$b_1$	$b_2$	$b_3$	$b_4$	$b_5$
1	1	0		



369



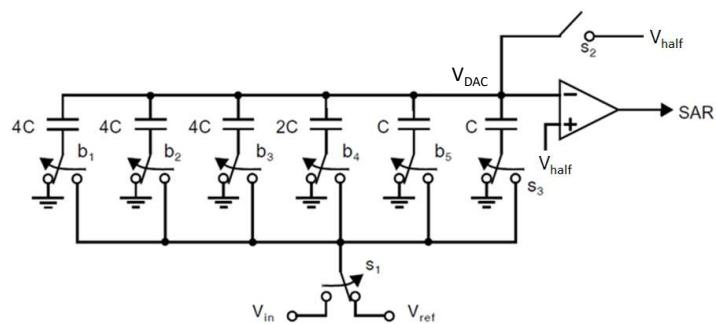
## Exercise 2 - Solution

f) Sampling, bit cycling –  $b_1 \rightarrow$  same as e)

$$\text{Bit cycling } b_2 \rightarrow V_{DAC} = 0.6V < V_{half}$$

wrong comparator decision  $\rightarrow b_2 = 0$

$b_1$	$b_2$	$b_3$	$b_4$	$b_5$
1	0			



370

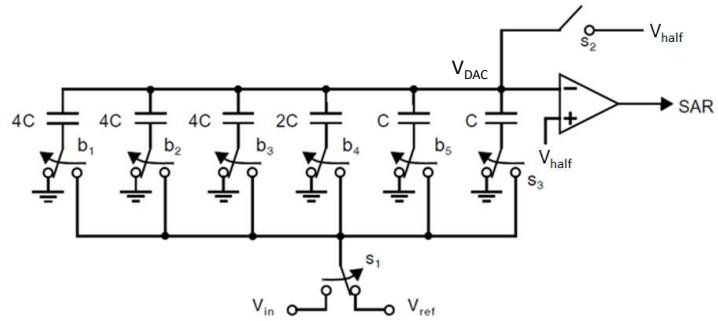


## Exercise 2 - Solution

f) Bit cycling –  $b_3$

$$\begin{aligned} b_1 &\rightarrow V_{ref} & b_2 &\rightarrow GND & b_3 &\rightarrow V_{ref} & b_4, b_5, s_3 &\rightarrow GND & S_2 \text{ off} \\ Q_{tot} &= 8C(V_{DAC} - V_{ref}) + 8CV_{DAC} = 16C(V_{half} - V_{in}) \\ \rightarrow V_{DAC} &= V_{half} - V_{in} + \frac{8}{16}V_{ref} = 0.6V < V_{half} \\ \rightarrow b_3 &= 1 \end{aligned}$$

$b_1$	$b_2$	$b_3$	$b_4$	$b_5$
1	0	1		



371

## Exercise 3

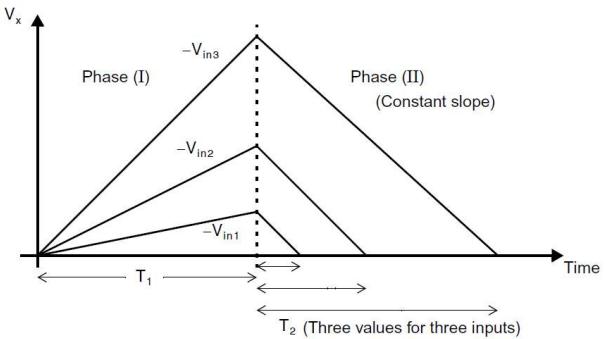
- For which input voltage does the worst-case conversion rate of a dual-slope ADC occur? What is the total number of clock cycles needed to perform a conversion in this case?
- Calculate the worst-case conversion rate of a dual-slope ADC with 16 bits of resolution and a clock frequency of 1MHz.

372

## Exercise 3 - Solution

- a) *Charging time:*  
*Discharging time:*  
*Worst case:*  
 → *Conversion time:*

b)



## Exercise 4

- a) Quantize the following input voltages by rounding and by truncation:  
 $0.2V_{lsb}$ ,  $1.6V_{lsb}$ ,  $2.9V_{lsb}$ ,  $3.3V_{lsb}$ .
- b) Draw the schematic of a 2-bit flash ADC with quantization by rounding.
- c) Calculate the voltages at the nodes of the resistive string.
- d) Sketch the output voltage of the comparators in dependence of the input voltage.
- e) Repeat a), b), c) for a flash ADC with quantization by truncation.

## Exercise 4 – Solution

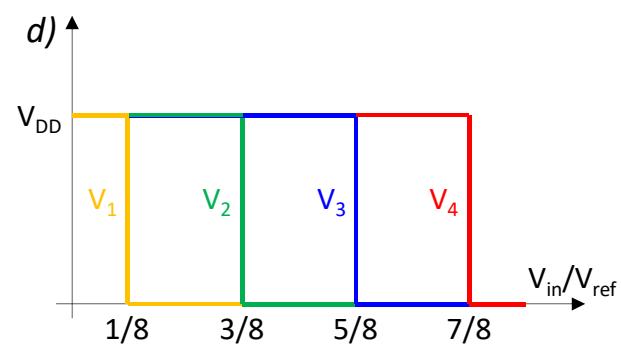
a)

<i>Input voltage</i>	<i>Quantization by rounding</i>	<i>Quantization by truncation</i>
$0.2V_{lsb}$		
$1.6V_{lsb}$		
$2.9V_{lsb}$		
$3.3V_{lsb}$		

375

## Exercise 4 – Solution

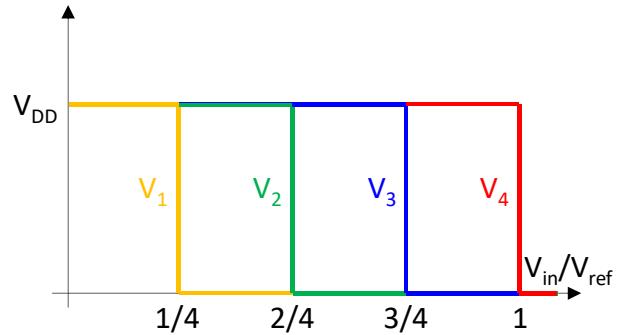
b,c)



376

## Exercise 4 – Solution

e)

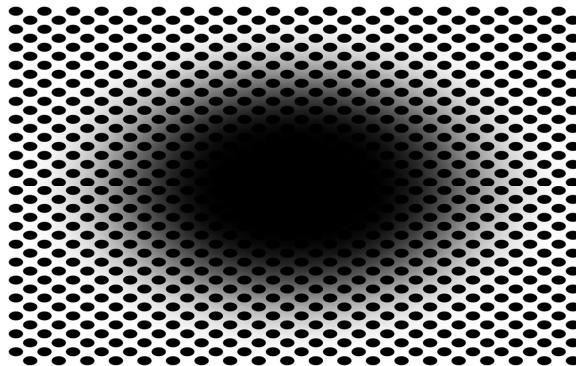


# Chapter 8 Oversampling Analog-to-Digital Converters

Courtesy of Dr. Stephan Henzler

Revised by Maciej Jankowski, Texas Instruments

## Warning



Oversampling converters can be addictive

Image source: <https://www.sueddeutsche.de/wissen/optische-taeuschung-farben-pupillen-augen-1.5601100?reduced=true>



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379

## Outline

- Oversampling
- First-order modulation
- Second-order modulation
- Tones
- Digital filtering
- Sigma-delta DAC
- Circuit design aspects
- Advanced architectures
- Continuous-time sigma-delta ADC



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380

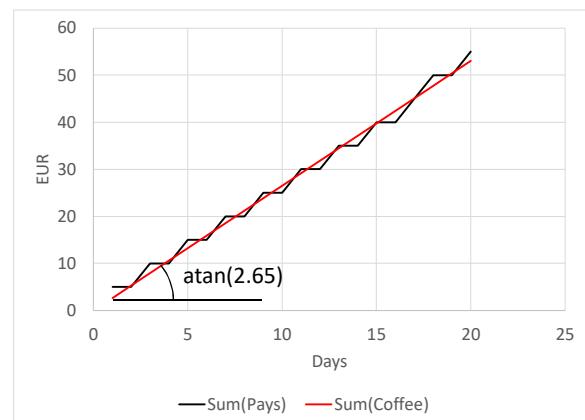
# Outline

- Oversampling
- First-order modulation
- Second-order modulation
- Tones
- Digital filtering
- Sigma-delta DAC
- Circuit design aspects
- Advanced architectures
- Continuous-time sigma-delta ADC

# The Coffee Shop Problem

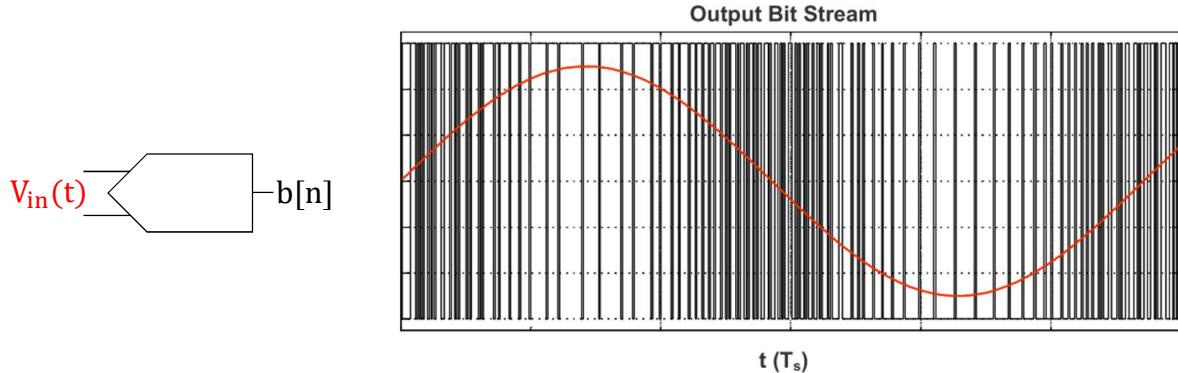
- How to pay for a €2.65 coffee each day using €5 bills/no change?

<b>Day</b>	<b>1</b>	<b>2</b>	<b>3</b>	<b>4</b>
Owes	0	-2.35	0.3	-2.05
Coffee	2.65	2.65	2.65	2.65
€				
Pays	5	0	5	0
€				
<b>Owes</b>	<b>-2.35</b>	<b>0.30</b>	<b>-2.05</b>	<b>0.60</b>
€				



## How to Convert Input Sinewave into Bitstream?

- 1-bit output digital signal
- Bitstream update at a much higher rate than the input signal frequency
- It should be possible to reconstruct the output by some low-pass filtering



383

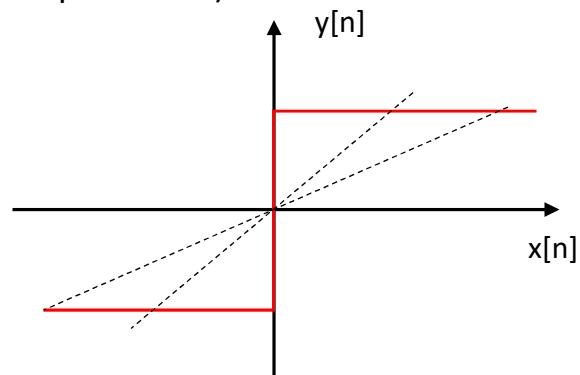
## The Need for Oversampling ADCs

- Resolution of Nyquist-rate ADCs:
  - Flash: limited by prohibitive hardware/power consumption
  - Integrating: can be very high, but conversion speed prohibitively low
  - SAR, algorithmic, pipelined: limited by **matching** accuracy
- **kT/C noise**: fundamental limit on SN(D)R (recall:  $SN(D)R \approx 6 \cdot ENOB$ )  
(large C is bad for power and speed)
- Is it possible to go beyond these limitations? (High-resolution ADC?)  
→ oversampling

384

## Quantizer model

- Voltage in (continuous) → voltage out (discrete)
- No delay
- 1 bit → intrinsically linear (only 2 output values)  
but gain variable



385

## SNR vs. SQNR

### **SNR** – Signal to Noise Ratio

- Perceived in the system containing the ADC (“end user”)
- Thermal noise component  $P_N$  more costly to simulate

$$\text{SNR[dB]} = 10 \log \left( \frac{P_S}{P_N + P_{QN}} \right)$$

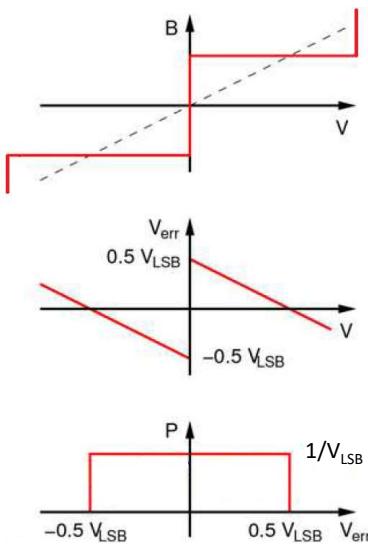
### **SQNR** – Signal to Quantization Noise Ratio

- Can be simulated starting from simple models, checks health of ADC
- In real systems, always coexisting with thermal noise.

$$\text{SQNR[dB]} = 10 \log \left( \frac{P_S}{P_{QN}} \right) > \text{SNR}$$

386

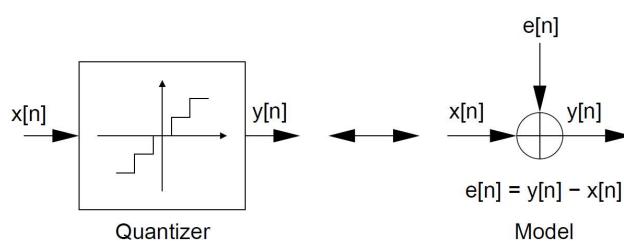
## Recall: Quantization Noise in ADCs



387



## Quantization model



Assuming  $x[n]$  is:



- busy (often and rapidly crosses thresholds)
- random within quantizer intervals
- within quantization range

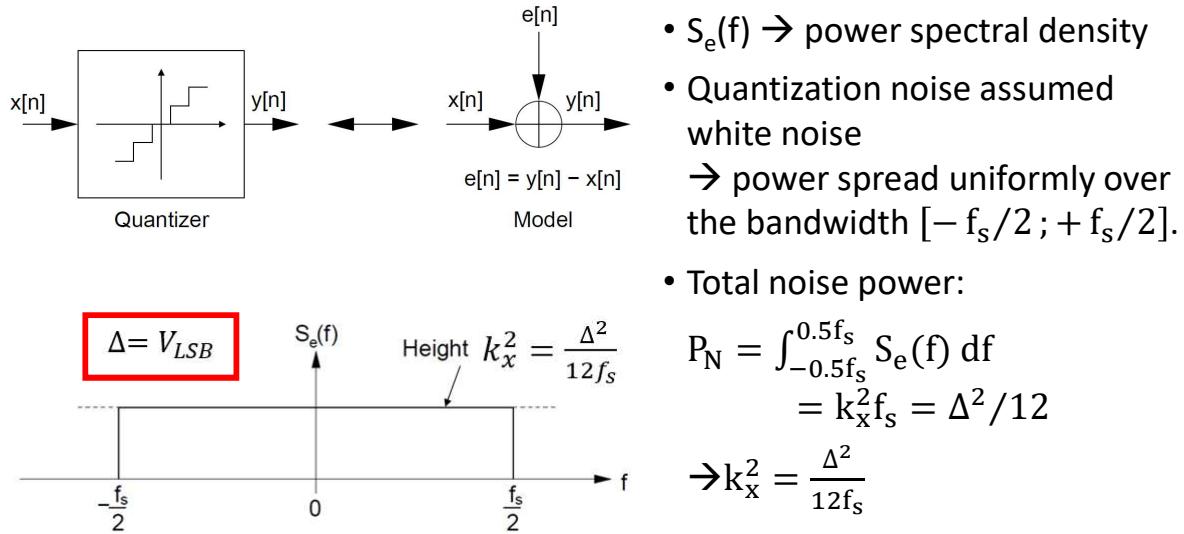
Then  $e[n]$  is:

- an additive noise sequence (always)
- independent of  $x$
- uniformly distributed (if not specified otherwise, within  $[-1, 1]$ )
- spectrally white ("noise")



388

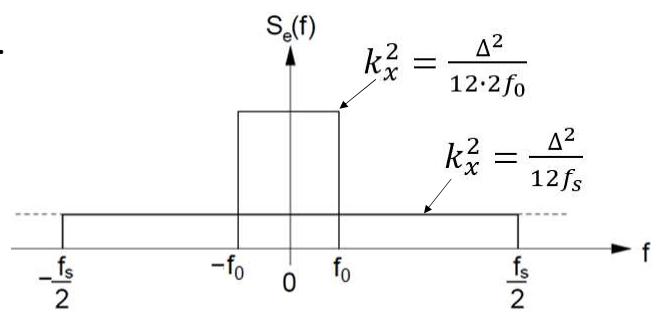
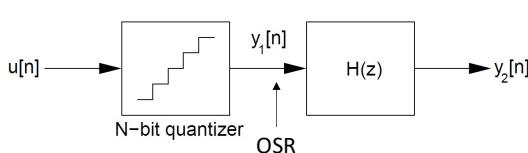
## Linear Model of Quantization Noise



## Quantization Noise and Oversampling

- Oversampling: sampling rate ( $f_s$ ) much higher than required by the Nyquist condition
  - noise power distributed over a wider band
  - total noise power unchanged
  - power spectral density decreases
- Oversampling ratio:

$$OSR = \frac{f_s}{f_{s,Nyquist}} = \frac{f_s}{2f_0} = 8 \dots 1024 \dots$$



## Quantization Noise and Oversampling

- Low-pass filter  $H(f)$ :
  - limit everything to signal bandwidth
  - removes most of quantization noise power

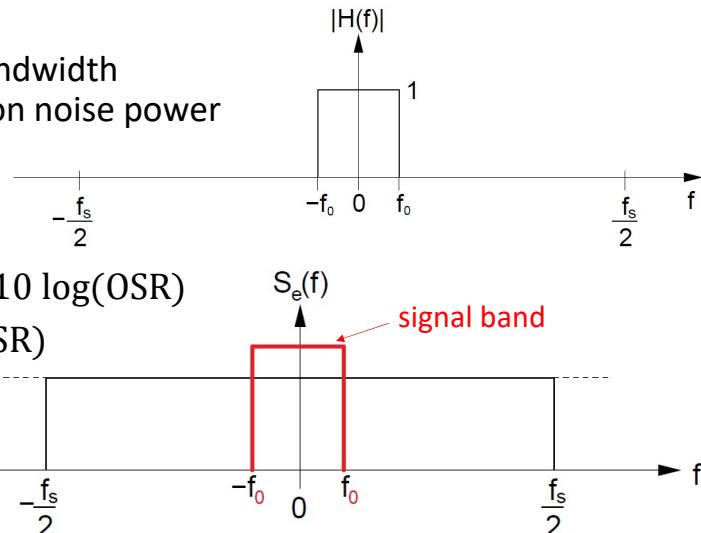
$$\bullet \overline{V_{\text{err}}^2} = \frac{1}{\text{OSR}} \overline{V_{\text{err,Nyquist}}^2}$$

$$\bullet \text{SQNR[dB]} = 6.02N + 1.76 + 10 \log(\text{OSR})$$

$$\bullet \text{SQNR[dB]} = 7.78 + 10 \log(\text{OSR}) \text{ for } N=1 \text{ (common case)}$$

• 2x OSR →

• Works for kT/C noise



391

## Exercise 1

A 12-bit ADC with 22kHz BW should be implemented.

- Calculate the signal-to-quantization-noise ratio SQNR[dB].
- Calculate the oversampling ratio OSR needed to obtain the same SQNR with a 1-bit quantizer.
- Calculate the sampling frequency in this case. Discuss the results.

392

## Exercise 1 – Solution

- a) 12 bits  
 $\rightarrow SQNR[dB] =$
- b)  $SQNR[dB] =$

- c)  $f_s =$

*Conclusion: even medium resolution and low bandwidth lead to unacceptably high sampling frequency.*



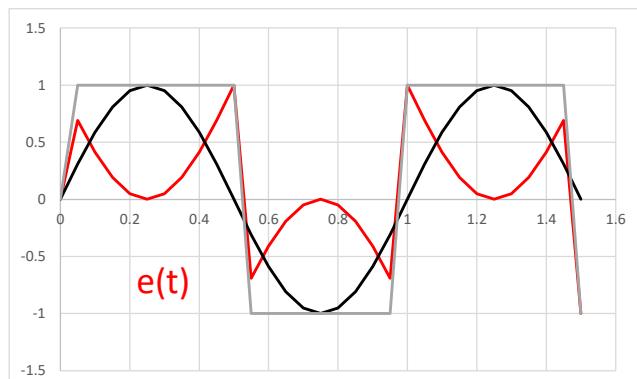
*Q: Do our assumptions on  $Q_{noise}$  even hold here?*

## Sinewave Input to 1-Bit Quantizer

- Quantization error  $e(t)$  = distortion products

$$e(t) = \frac{4}{\pi} \sin(2\pi ft) + \frac{4}{3\pi} \sin(3 \cdot 2\pi ft) + \frac{4}{5\pi} \sin(5 \cdot 2\pi ft) + \dots$$

- Sad truth: Quantization error  $e(t)$  far from spectrally white
- Need to make input busy



## Outline

- Oversampling
- First-order modulation
- Second-order modulation
- Tones
- Digital filtering
- Sigma-delta DAC
- Circuit design aspects
- Advanced architectures
- Continuous-time sigma-delta ADC



It All Started with 50Hz BW and 35dB SNR...

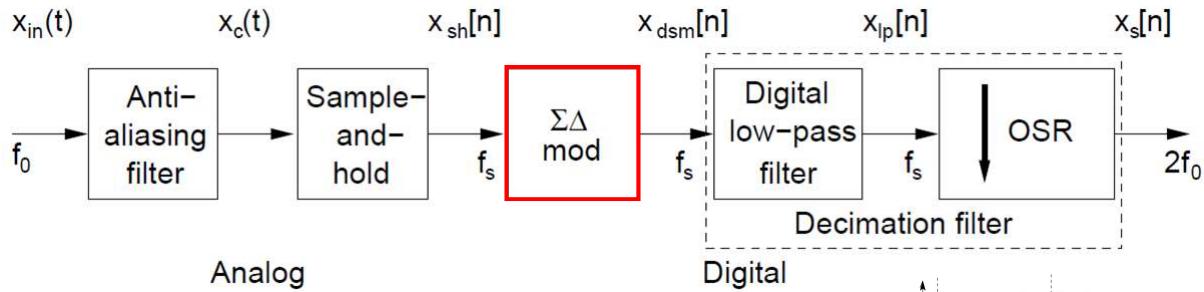
### A Telemetry System by Code Modulation — $\Delta$ - $\Sigma$ Modulation\*

H. INOSE†, MEMBER, IRE, Y. YASUDA†, AND J. MURAKAMI‡

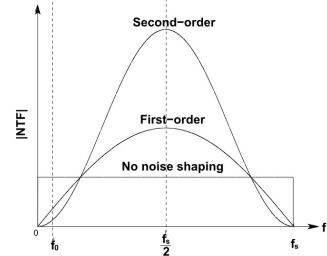
\* Received May 6, 1962.  
 † Faculty of Engineering, University of Tokyo, Japan.  
 ‡ Tokyo Shibaura Electric Co., Japan. Formerly with Faculty of Engineering, University of Tokyo.



## Oversampling with Noise Shaping



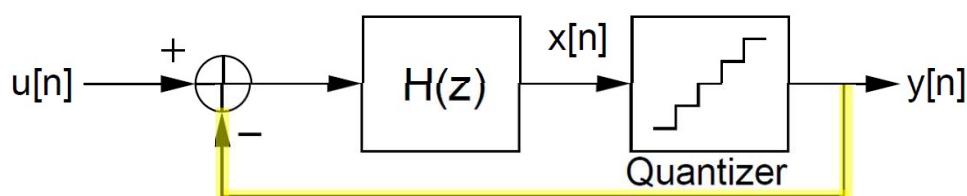
- Concept of  $\Sigma\Delta$  conversion:
    - use a low-bit quantizer → large quantization noise
    - push quantization noise to higher frequencies, then remove it with a digital filter
- SQNR increases more than for pure oversampling



397



## First-Order Noise Shaping

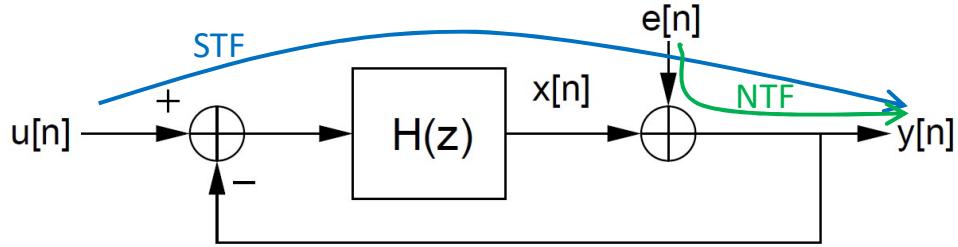


- Feed quantization result back and consider it during next step.
- Quantizer: commonly 1-bit (inherently linear)



398

## Exercise 2



Consider the modulator above with the loop filter transfer function  $H(z)$ .

- Calculate the signal transfer function  $STF(z)$  in terms of  $H(z)$ .
- Calculate the noise transfer function  $NTF(z)$  in terms of  $H(z)$ .
- What requirements should the loop filter transfer function  $H(z)$  fulfill such that, in the signal band (low frequencies), the signal is little affected and the noise is filtered? What type of circuit fulfills these requirements?

## Exercise 2 – Solution

$$Y(z) \triangleq U(z)STF(z) + E(z)NTF(z)$$

$$a) STF(z) = \frac{Y(z)}{U(z)} (E(z) = 0)$$

$$b) NTF(z) = \frac{Y(z)}{E(z)} (U(z) = 0)$$

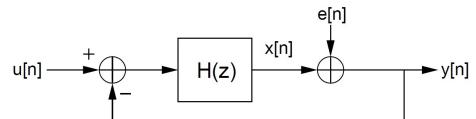
c) *Signal band (low frequency):*

- *signal little affected*

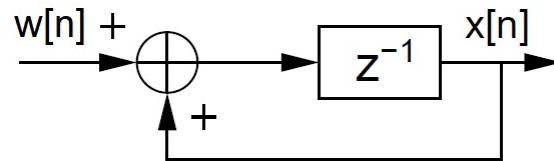
- *noise filtered*

→ *loop gain  $H(z)$  should be as large as possible at low frequency*

→



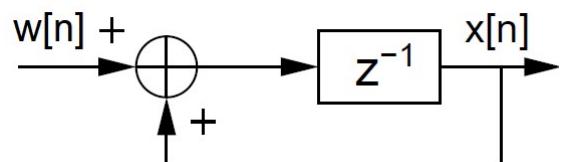
## Exercise 3



- Calculate the transfer function  $H(z)$  of the integrator above.
- Insert into the expressions of  $STF(z)$  and  $NTF(z)$  and calculate them.

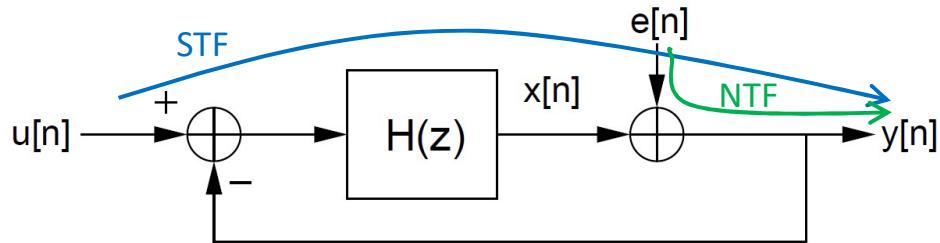
## Exercise 3 – Solution

a)



b)  $STF(z) = \frac{H(z)}{1+H(z)} = z^{-1}$   
 $NTF(z) = \frac{1}{1+H(z)} = 1 - z^{-1}$

## First-Order Noise Shaping – Summary



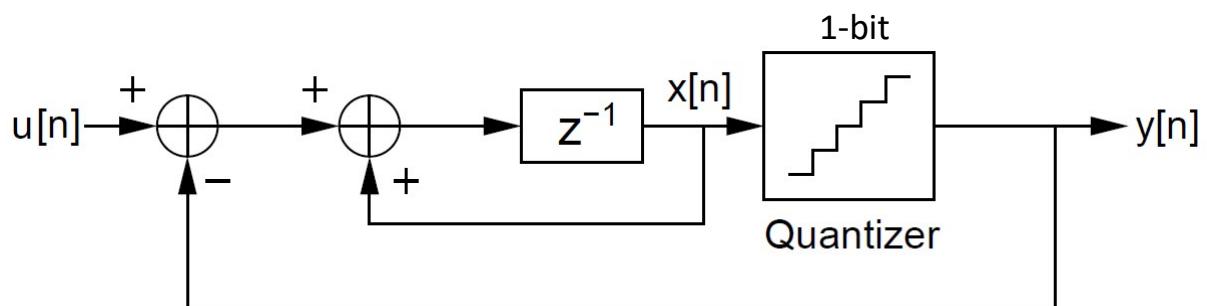
$$Y(z) = U(z)STF(z) + E(z)NTF(z)$$

$H(z) = \frac{z^{-1}}{1-z^{-1}}$  → delaying integrator

$STF(z) = \frac{H(z)}{1+H(z)} = z^{-1}$  → unity in signal band → pure delay

$NTF(z) = \frac{1}{1+H(z)} = 1 - z^{-1}$  → (almost) zero in signal band, high-pass behavior

## First-Order $\Sigma\Delta$ Modulator



## Exercise 4

- a) Calculate STF and NTF in the frequency domain. Calculate the absolute value of these functions.
- b) Calculate the absolute value of NTF for small frequencies,  $f \ll f_s$ .
- c) What is the signal band for a given oversampling ratio OSR?

## Exercise 4 – Solution

*From Z-domain to frequency domain:  $z = e^{j\omega T}$*

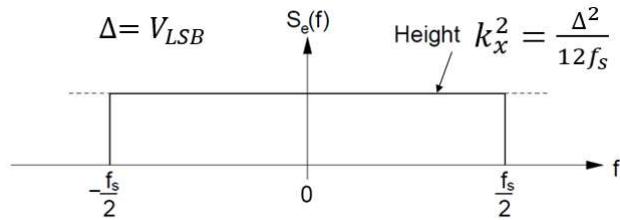
a)  $STF = z^{-1} = e^{-j\omega T} \rightarrow |STF| = 1$   
 $NTF = 1 - z^{-1} = 1 - e^{-j\omega T}$

b)  $f \ll f_s \rightarrow$

c) *signal band:*

## Exercise 4

- d) Calculate the power of the modulated noise in the signal band.  
 Recall the spectrum of the non-modulated noise:



- e) Calculate SQNR[dB] for a sinusoidal input signal of maximum amplitude.  
 f) Calculate the OSR required for an SQNR of 74dB for:  
 - pure oversampling  
 - oversampling with first-order noise shaping  
 Discuss the results.

## Exercise 4 – Solution

$$d) P_N = \int_{-f_s/(2OSR)}^{f_s/(2OSR)} S_e(f) |NTF|^2 df$$

$$P_N = \int_{-f_s/(2OSR)}^{f_s/(2OSR)} \frac{\Delta^2}{12} 4\pi^2 \frac{f^2}{f_s^2} df = \frac{\Delta^2 \pi^2}{36} \frac{1}{OSR^3}$$

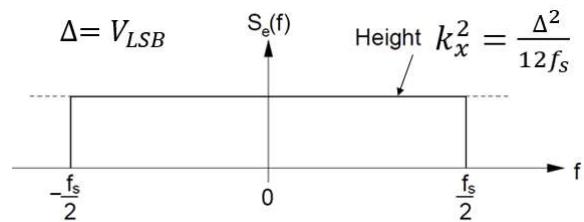
$$e) \text{ signal power: } P_S = \frac{1}{2} \left( \frac{V_{ref}}{2} \right)^2 = \frac{2^{2N} \Delta^2}{8}$$

$$\text{SQNR}[dB] = 10 \log \left( \frac{P_S}{P_N} \right) = 6.02N + 1.76 - 5.17 + 30 \log(OSR)$$

For N=1 (common case)

$$\text{SQNR}[dB] = 2.61 + 30 \log(OSR)$$

$$2x \text{ OSR} \rightarrow$$



## Exercise 4 – Solution

f) - pure oversampling:

$$SQNR[dB] = 6.02N + 1.76 + 10 \log(OSR) = 74$$

1-bit quantizer  $\rightarrow N=1$

$\rightarrow OSR = 4 \cdot 10^6 \rightarrow$  not feasible (while optimistic)

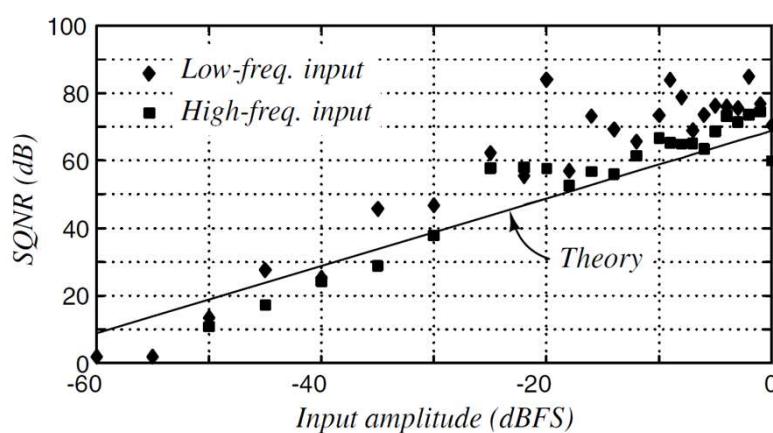
- with noise shaping (first-order):

$$SQNR[dB] = 6.02N + 1.76 - 5.17 + 30 \log(OSR) = 74$$

1-bit quantizer  $\rightarrow N=1$

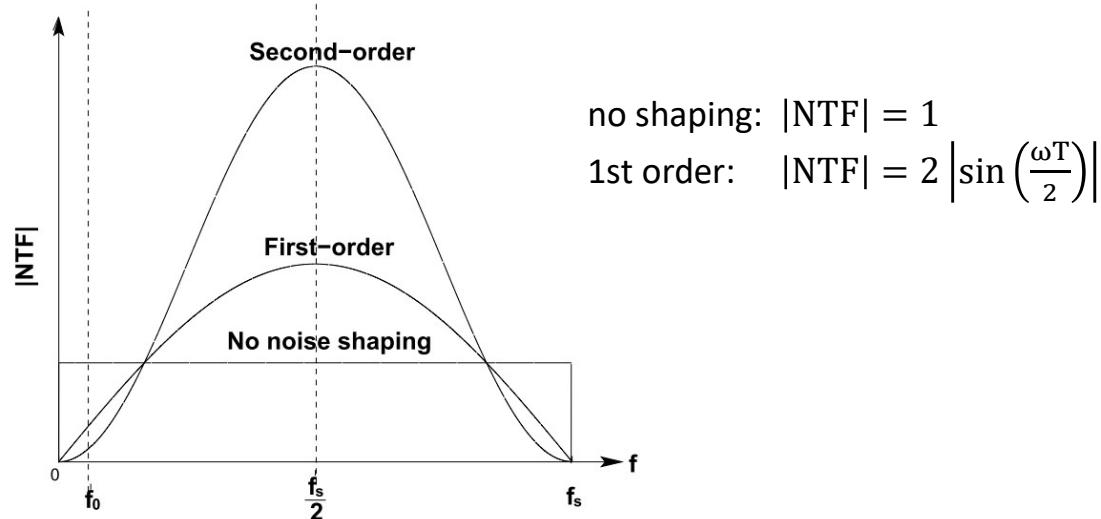
$\rightarrow OSR = 240 \rightarrow$  feasible

## SQNR of 1<sup>st</sup> Order Modulator, OSR 256



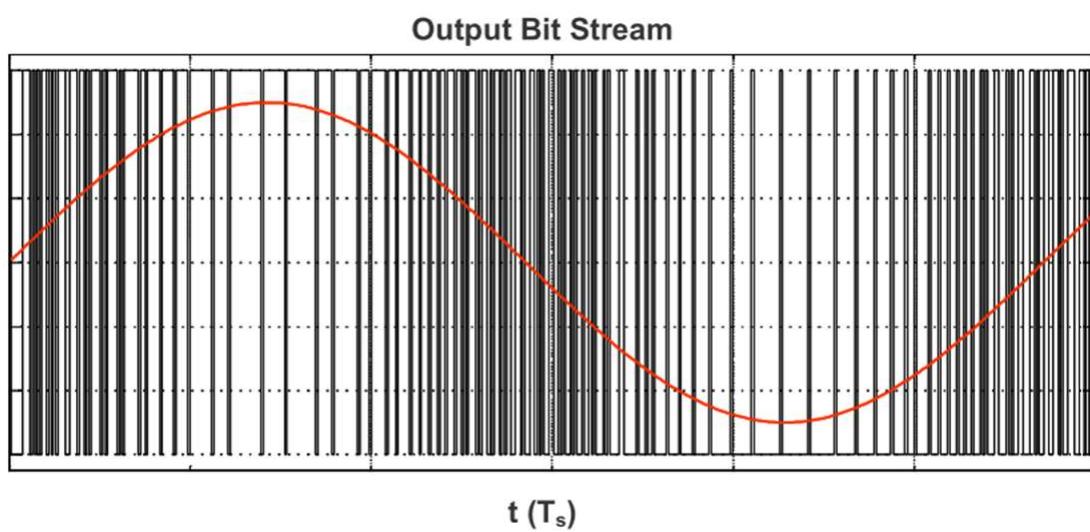
- Simulated SQNR deviates strongly from theory because of the 1-bit quantizer

## Noise Spectrum



411

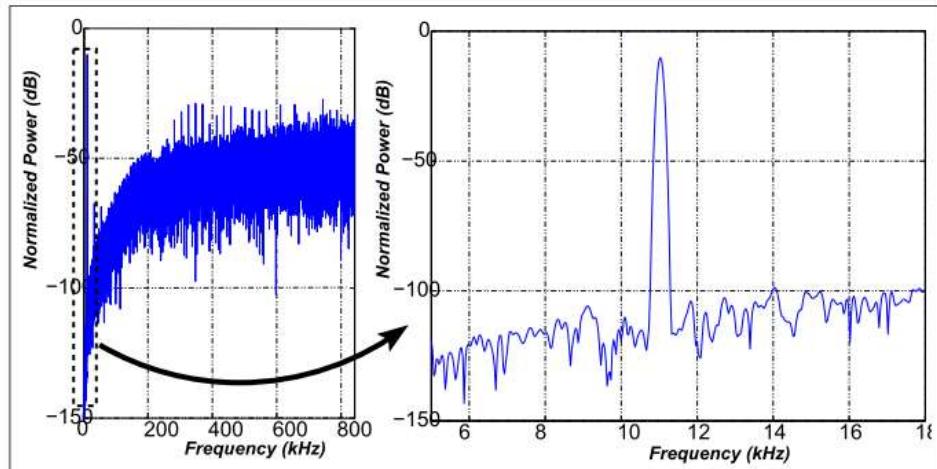
## Output Bit Stream with Sinusoidal Input Signal



412

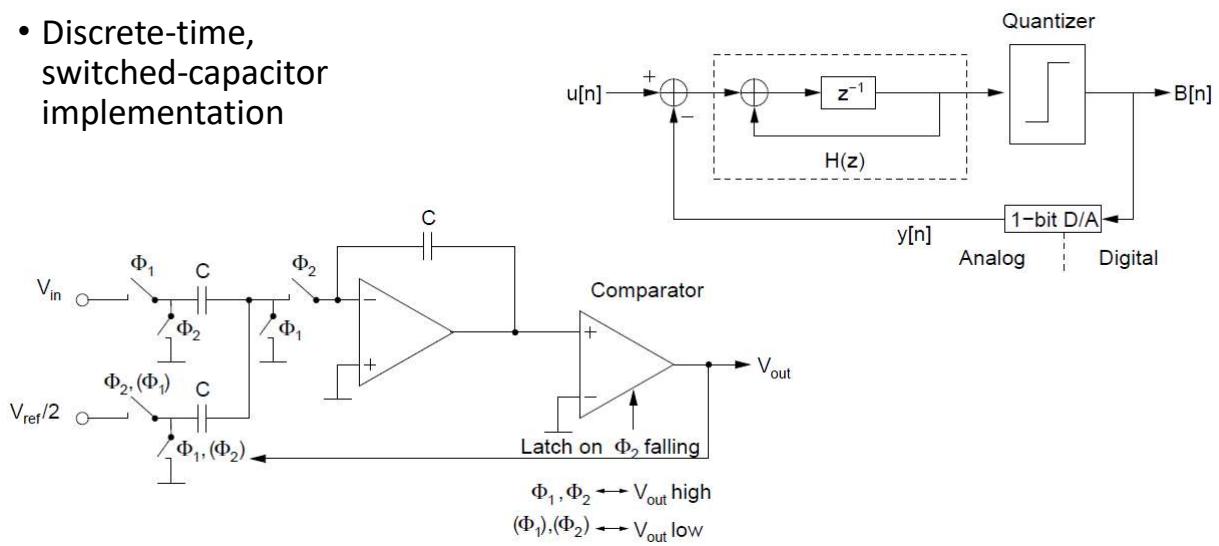
# Output Spectrum

- First-order  $\Sigma\Delta$  modulator, sinusoidal input signal



# First-Order $\Sigma\Delta$ Modulator Example

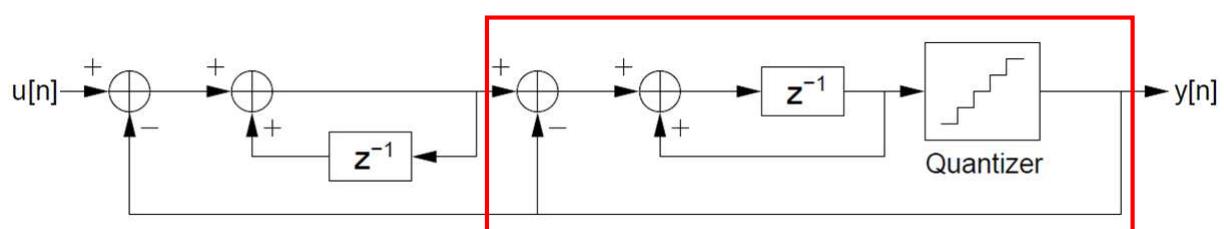
- Discrete-time, switched-capacitor implementation



# Outline

- Oversampling
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- Second-order modulation
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- Digital filtering
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- Circuit design aspects
- Advanced architectures
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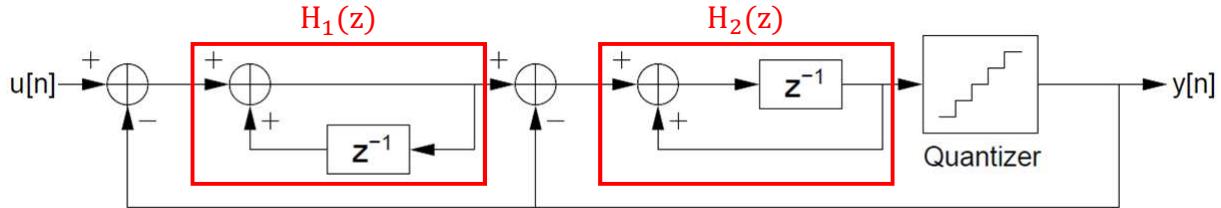
# Second-Order $\Sigma\Delta$ Modulator



- Recall:
  - simple quantizer (pure oversampling) → no shaping
  - 1st-order modulator → 1st-order noise shaping
- Idea of 2nd-order modulator:
 

replace the quantizer of the 1st-order modulator by 1st-order noise shaping  
→ shape the shaped noise.

## Exercise 5



Consider the ideal second-order  $\Sigma\Delta$  modulator above.

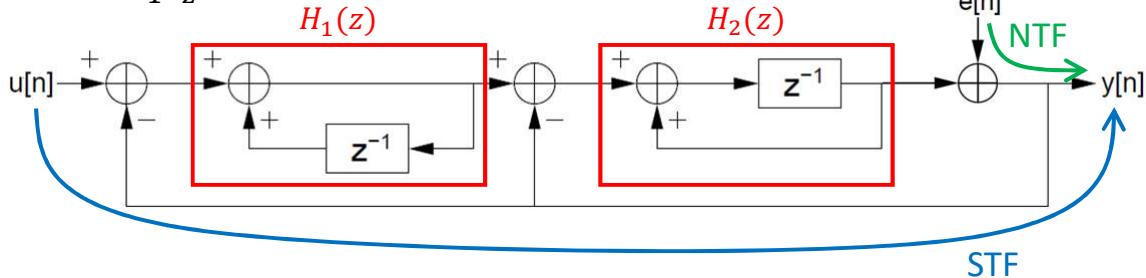
- Calculate the transfer functions  $H_1(z)$  and  $H_2(z)$  of the integrators.
- Sketch the linear equivalent circuit of the modulator.
- Calculate the STF and the NTF (in the Z domain).

## Exercise 5 – Solution

a)

$$H_2(z) = \frac{z^{-1}}{1-z^{-1}} \text{ (see exercise 3)}$$

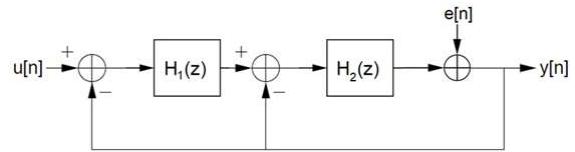
b)



## Exercise 5 – Solution

c)  $Y(z) = U(z)STF(z) + E(z)NTF(z)$

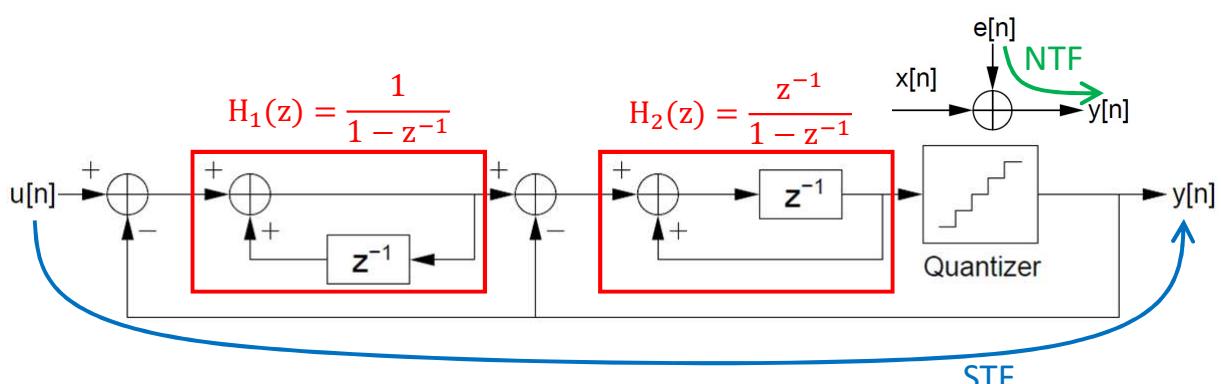
$$STF(z) = \frac{Y(z)}{U(z)} (E(z) = 0)$$



$$NTF(z) = \frac{Y(z)}{E(z)} (U(z) = 0)$$

419

## Second-Order $\Sigma\Delta$ Modulator



$$STF = \frac{Y(z)}{U(z)} (E(z) = 0) = z^{-1} \rightarrow \text{delay}$$

$$NTF = \frac{Y(z)}{E(z)} (U(z) = 0) = (1 - z^{-1})^2 \rightarrow \text{2nd-order high pass}$$

420

## 2nd vs. 1st-Order $\Sigma\Delta$ Modulator

- Intuitive derivation for 2nd-order modulator:

	1st order	2nd order
NTF	$1 - z^{-1}$	
NTF( $j\omega$ )	$\propto \sin(\omega T/2)$	
$ NTF , f \ll f_s$	$\propto f/f_s$	
$P_N$	$\propto OSR^{-3}$	
SQNR[dB]	$\dots + 30 \log(OSR)$	

## Exercise 5

- Calculate STF and NTF in the frequency domain. Calculate their absolute values.
- Calculate the absolute value of NTF for small frequencies,  $f \ll f_s$ .
- Calculate the power of the modulated noise in the signal band.
- Calculate SQNR[dB] for a sinusoidal input signal of maximum amplitude.

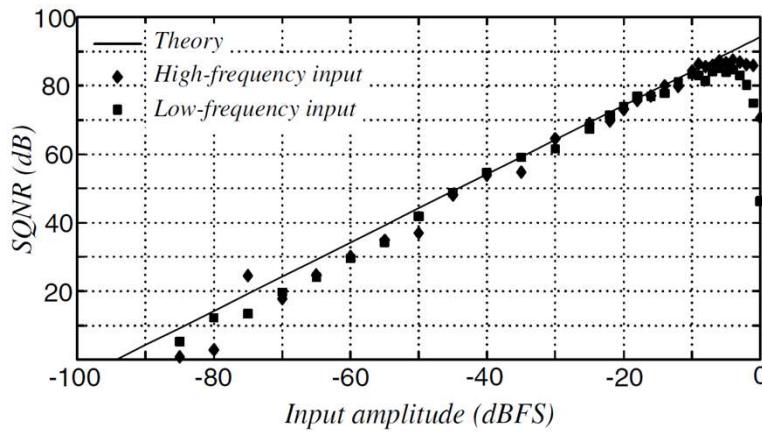
## Exercise 5 – Solution

- d)  $STF = z^{-1} = e^{-j\omega T} \rightarrow |STF| = 1$   
 $NTF = (1 - z^{-1})^2 = (1 - e^{-j\omega T})^2$   
 $\rightarrow NTF = e^{-j\omega T} (e^{j\omega T/2} - e^{-j\omega T/2})^2 \left(\frac{1}{2j}\right)^2 (-4) = -4e^{-j\omega T} \sin^2\left(\frac{\omega T}{2}\right)$   
 $\rightarrow |NTF| = 4 \left|\sin^2\left(\frac{\omega T}{2}\right)\right|$
- e)  $f \ll f_s \rightarrow |NTF| \cong (\omega T)^2 = 4\pi^2(f/f_s)^2$
- f)  $P_N = \int_{-f_s/(2OSR)}^{f_s/(2OSR)} S_e(f) |NTF|^2 df$   
 $P_N = \int_{-f_s/(2OSR)}^{f_s/(2OSR)} \frac{\Delta^2}{12f_s} 16\pi^4 \frac{f^4}{f_s^4} df = \frac{\Delta^2 \pi^4}{60} \frac{1}{OSR^5}$

## Exercise 5 – Solution

- g) signal power:  $P_S = \frac{1}{2} \left( \frac{V_{ref}}{2} \right)^2 = \frac{2^{2N} \Delta^2}{8}$   
noise power:  $P_N = \frac{\Delta^2 \pi^4}{60} \frac{1}{OSR^5}$   
 $SQNR[dB] = 6.02N + 1.76 - 12.9 + 50 \log(OSR)$   
for N=1 (common case):  
 $SQNR[dB] = -5.12 + 50 \log(OSR)$   
2x OSR  $\rightarrow +15\text{dB SQNR.}$

## SQNR of 2<sup>nd</sup> Order Modulator, OSR 128



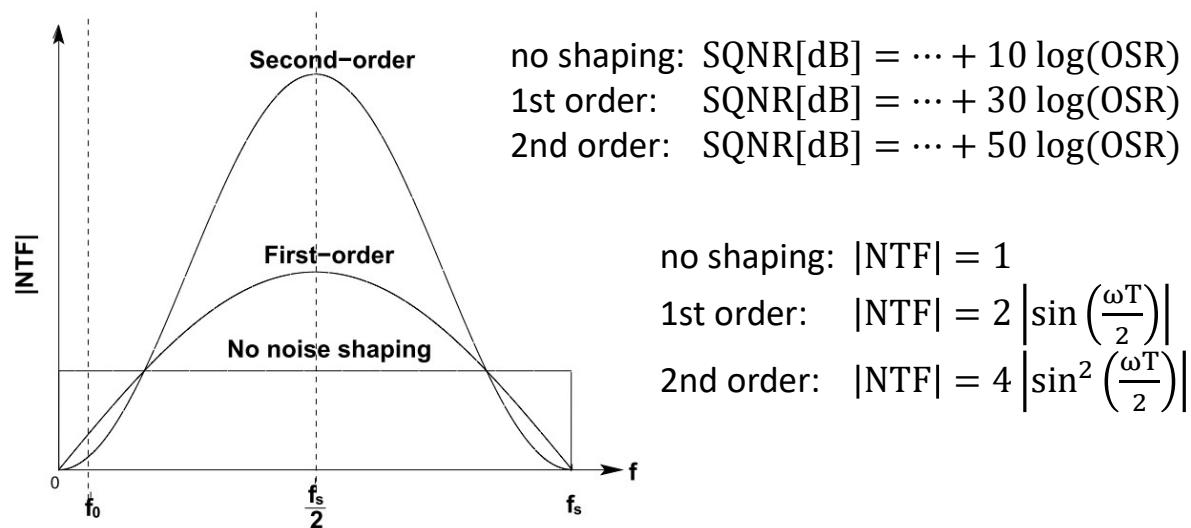
- Simulated SQNR better follows theory thanks to the extra noise shaping.



Illustration: S. Pavan, R. Schreier, G. Temes, Understanding Delta-Sigma Data Converters, Wiley 2017

425

## Noise Spectrum

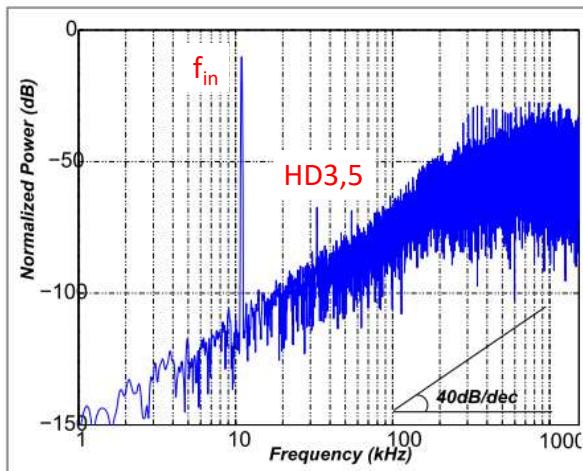


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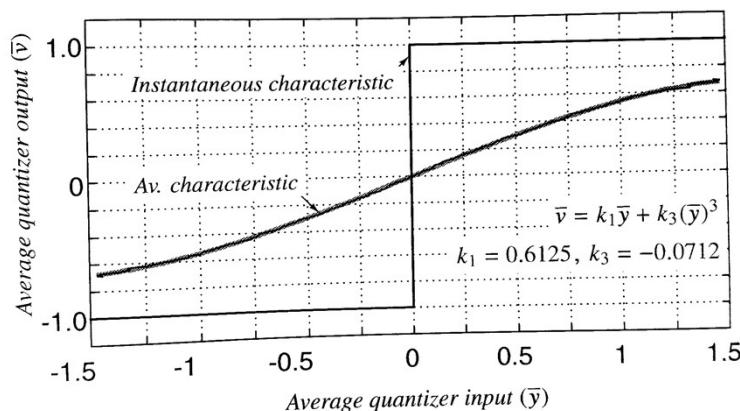
426

## Output Spectrum

- Second-order  $\Sigma\Delta$  modulator, sinusoidal input signal



## Averaged Quantizer Gain with Nonlinearity

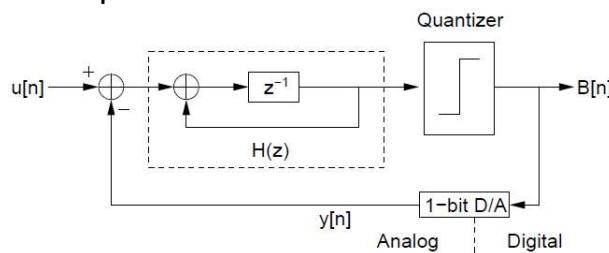


3rd order component of the quantizer characteristic is shaped to limited degree by 2nd order NTF, causes distortion despite ideal components.

# Tutorial

## Exercise 6

Implement a switched-capacitor first-order  $\Sigma\Delta$  modulator.

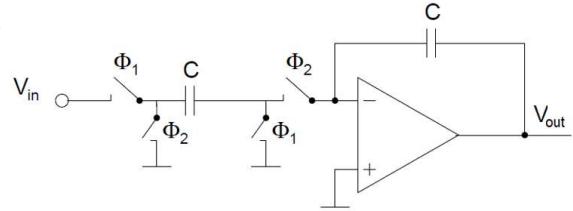


- Draw a switched-capacitor delaying integrator with gain 1. Write its transfer function.
- Extend the circuit to a summing integrator with inputs  $V_{in}$  and  $V_{ref}/2$ .
- Modify the circuit to a subtracting integrator with inputs  $V_{in}$  and  $V_{ref}/2$ . For each circuit, write the time-domain dependence of  $V_{out}$  on the input(s).

## Exercise 6 – Solution

a) Recall switched-capacitor integrators.

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{z^{-1}}{1-z^{-1}}$$

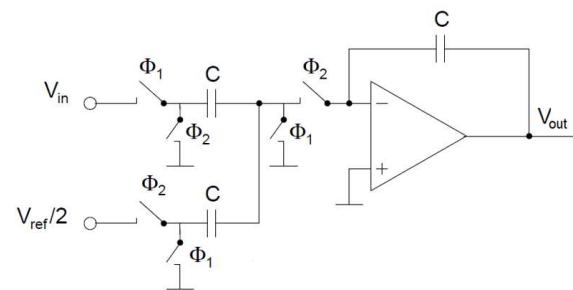
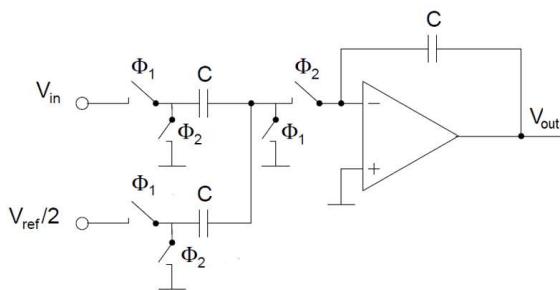


b) Recall superposition in switched-capacitor circuits.

c) Recall that changing the input clock phases changes the sign of the input.

## Exercise 6 – Solution

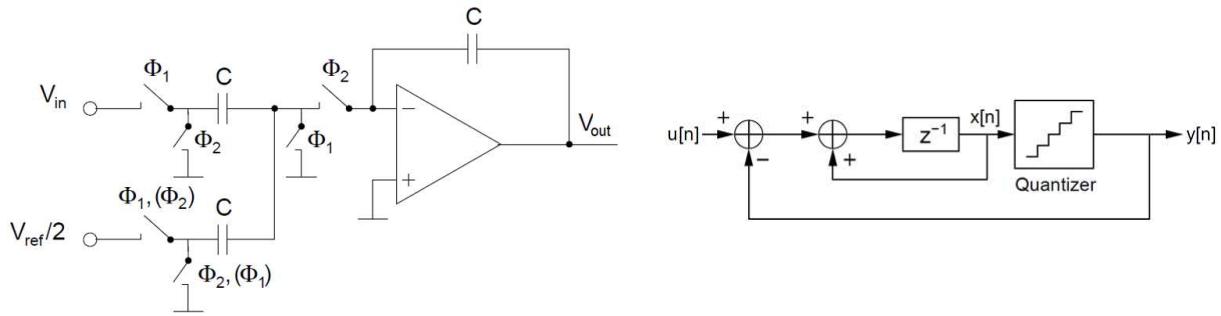
$$V_{out}[n] = V_{out}[n - 1] + V_{in}[n - 1] \pm V_{ref}/2$$



## Exercise 6

Consider the following switched-capacitor circuit, which combines the circuits from b) and c).

- d) Implement a first-order  $\Sigma\Delta$  modulator with this switched-capacitor circuit.  
Design also the circuit block controlling the switches.



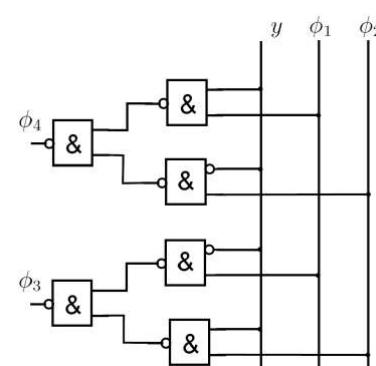
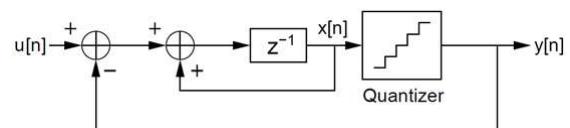
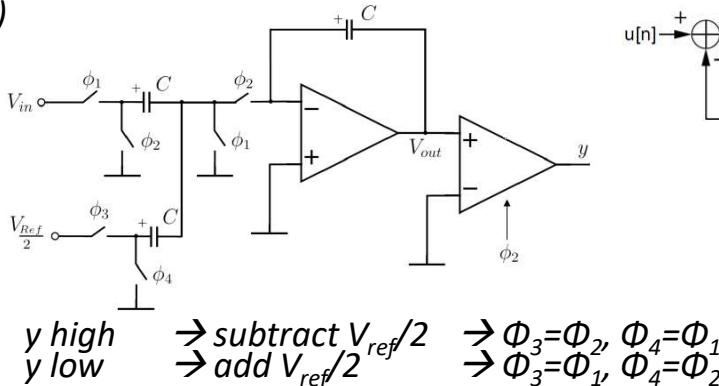
433



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## Exercise 6 – Solution

d)



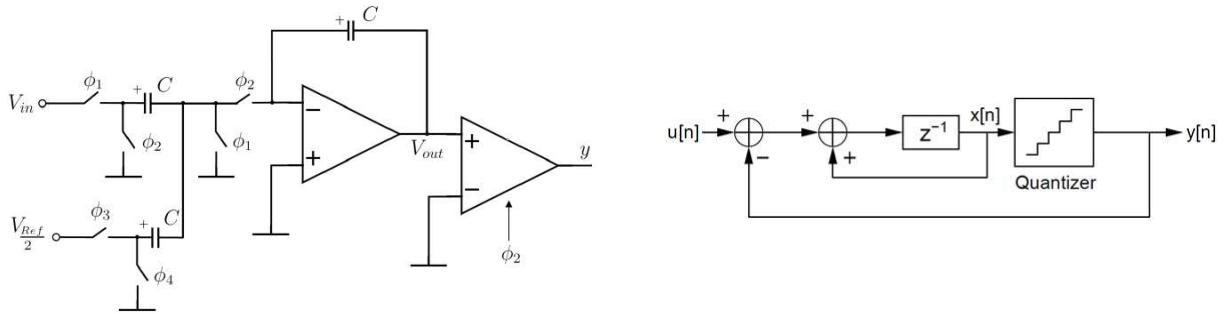
434



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## Exercise 6

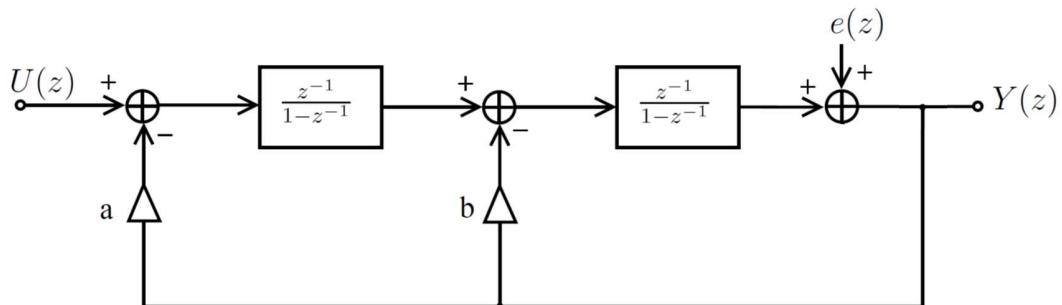
- e) Can a continuous-time comparator be used? Reason why.
- f) Associate, if possible, each element in the block diagram to the corresponding element in the circuit.



## Exercise 7

Consider a second-order  $\Sigma\Delta$  modulator. For implementation reasons, the first integrator stage shall be realized with the same transfer function as the second one. To achieve the behavior of the ideal modulator, two scaling factors  $a$  and  $b$  are introduced in the feedback paths.

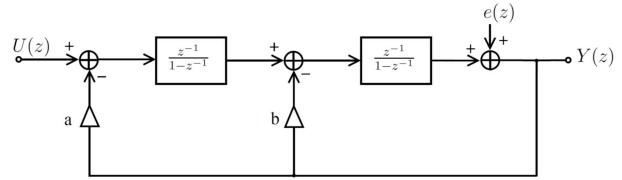
- a) Calculate the values of these scaling factors.



## Exercise 7 – Solution

$$a) \quad STF(z) = \frac{Y(z)}{U(z)} (E(z) = 0)$$

$$NTF(z) = \frac{Y(z)}{E(z)} (U(z) = 0)$$



437

## Exercise 7 – Solution

a)

$$STF(z) = \frac{z^{-2}}{(1+a-b)z^{-2} + (b-2)z^{-1} + 1}$$

$$NTF(z) = \frac{(1-z^{-1})^2}{(1+a-b)z^{-2} + (b-2)z^{-1} + 1}$$

$$|STF(z)| = 1 \rightarrow STF(z) = z^{-2}$$

$$NTF(z) = (1 - z^{-1})^2$$

$$\begin{aligned} \rightarrow b - 2 &= 0, 1 + a - b = 0 \\ \rightarrow b &= 2, a = 1 \end{aligned}$$

438

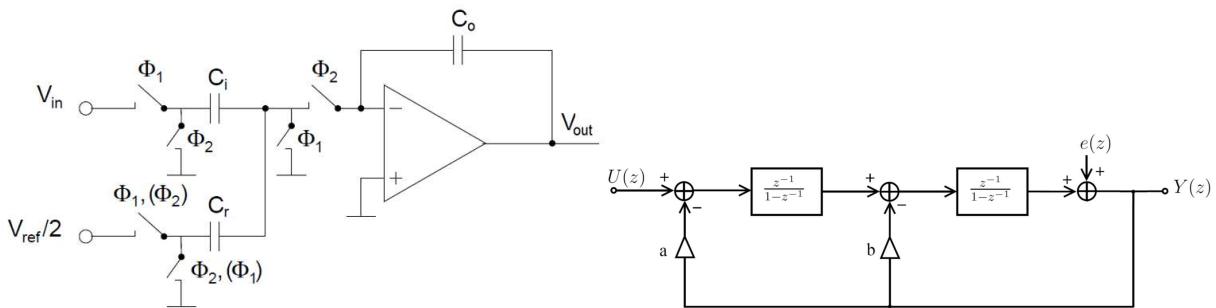
## Exercise 7

- b) The switched capacitor integrator given below has the following behavior:

$$V_{out}[n+1] = V_{out}[n] + (C_i/C_o) \cdot V_{in}[n] \pm (C_r/C_o) \cdot V_{ref}/2$$

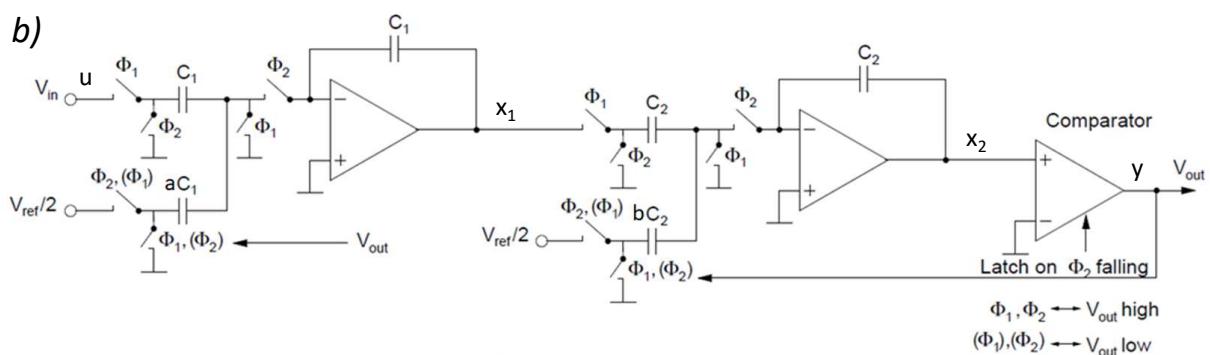
+ :  $\Phi_1, \Phi_2$       - :  $(\Phi_1), (\Phi_2)$

Draw a switched-capacitor implementation of a second-order  $\Sigma\Delta$  modulator with the feedback coefficients calculated previously.



## Exercise 7 – Solution

b)



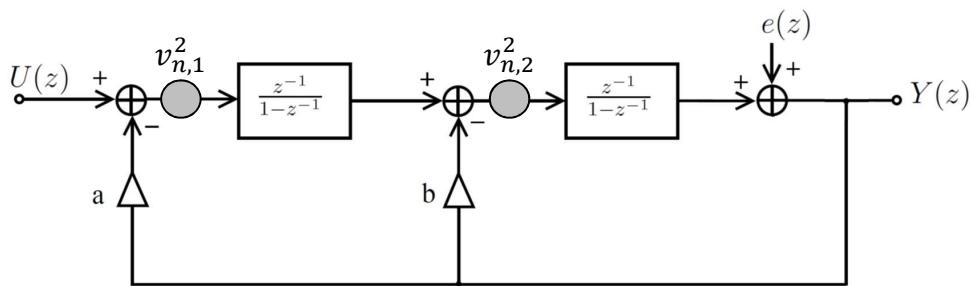
$$V_{out}[n+1] = V_{out}[n] + (C_i/C_o) \cdot V_{in}[n] \pm (C_r/C_o) \cdot V_{ref}/2$$

## Exercise 7

- c) What is the effect of the input noise of the first integrator referred to the input signal?
- d) What is the effect of the input noise of the second integrator referred to the input signal?

## Exercise 7 – Solution

- c)  $v_{n,1}$  : directly added to the input signal  
 $|STF| = 1 \rightarrow$  no shaping
- d)  $v_{n,2}$  : divided by the gain of the first integrator  
 $\rightarrow$  first-order shaped, then added to the input signal  
 $\rightarrow$  negligible effect compared to  $v_{n,1}$



# Exercise 7

- e) Calculate the in-band input-referred sampling noise of the modulator with respect to the capacitance  $C_1$  and the oversampling ratio OSR.
  - f) Size the capacitances  $C_1$  of the first integrator such that the sampling noise RMS voltage is less than half of the resolution  $\Delta$  of a 16-bit ADC with  $V_{ref}=2.4V$ . Consider OSR=128.
  - g) Calculate the total SNR for the OSR and the calculated  $C_1$ .
  - h) Calculate the ENOB for the calculated SNR value.  
Neglect harmonic distortion.

## Exercise 7 – Solution

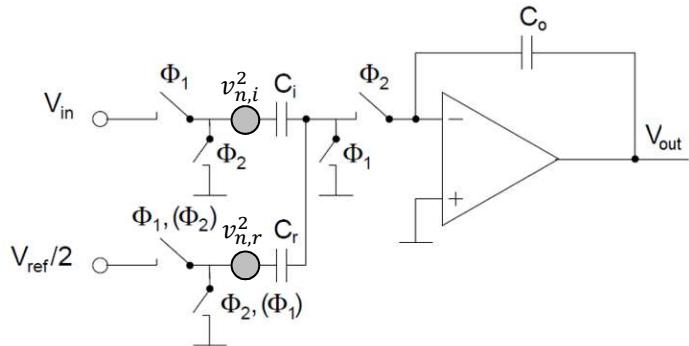
- e) Total input sampling noise:

### *In-band input sampling noise:*

$$f) \quad \text{Resolution: } \Delta = \frac{V_{ref}}{2^n}, \quad n=16$$

$$v_n < \frac{\Delta}{2} \rightarrow$$

$$kT \approx 4 \cdot 10^{-21} \text{ J} \quad (T = 300K)$$



## Exercise 7 – Solution

$$g) \quad SNR = 10 \log \left( \frac{P_S}{P_N} \right) \quad P_N = P_{QN} + P_{SN} \quad P_S = \frac{V_{ref}^2}{8}$$

$$P_{SN} = 2 \frac{kT}{C_1} \frac{1}{OSR} \quad \text{from capacitance sizing: } P_{SN} = \frac{V_{ref}^2}{4 \cdot 2^{2n}}$$

$$SQNR = -5.12 + 50 \log(OSR) = 100 \text{ dB}$$

h)

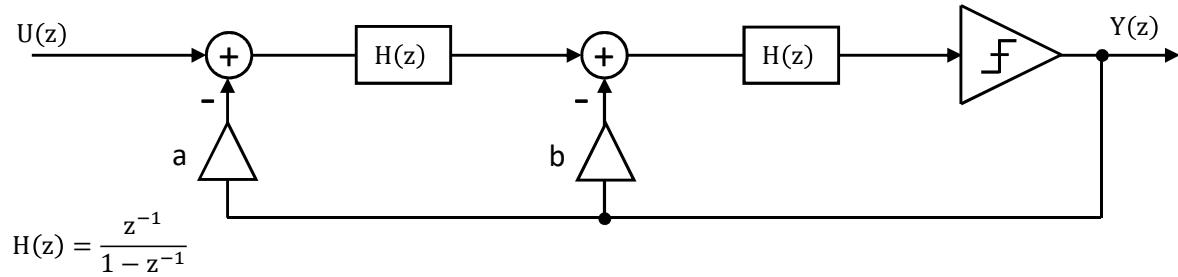
445



## Exercise 8

The amplifiers used in the integrators have a linear behavior within the specified output range  $\pm kV_{ref}$  ( $k=0.3$ ). System-level simulation (with ideal circuits) shows output values up to  $\pm lV_{ref}$  ( $l=0.5$ ) for the first integrator and  $\pm mV_{ref}$  ( $m=0.4$ ) for the second integrator.

Calculate the scaling factors of the modulator, such that its transfer function remains unchanged.

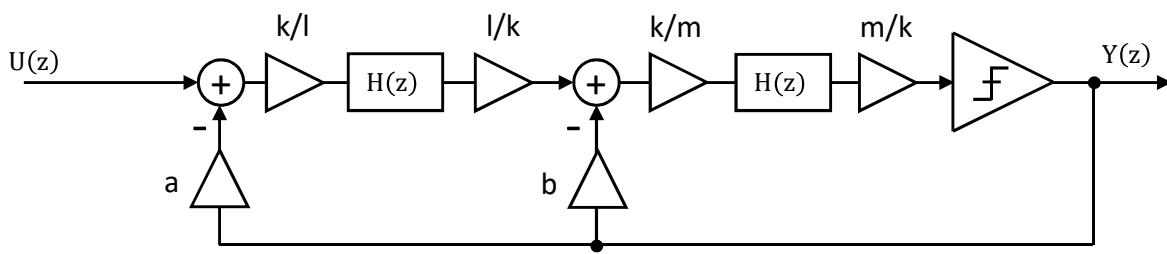


446



## Exercise 8 – Solution

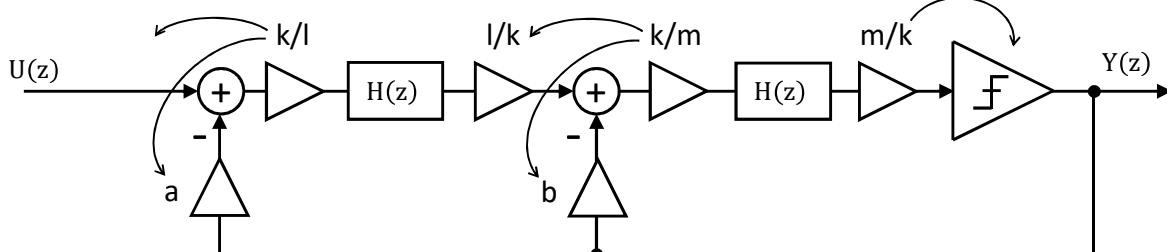
- *Integrator output:*
  - up to  $\pm l(m)V_{ref}$
  - needs to be scaled to  $kV_{ref}$ 
    - scale input by  $(k/l(m))V_{ref}$
    - amplify the output to compensate input scaling



447

## Exercise 8 – Solution

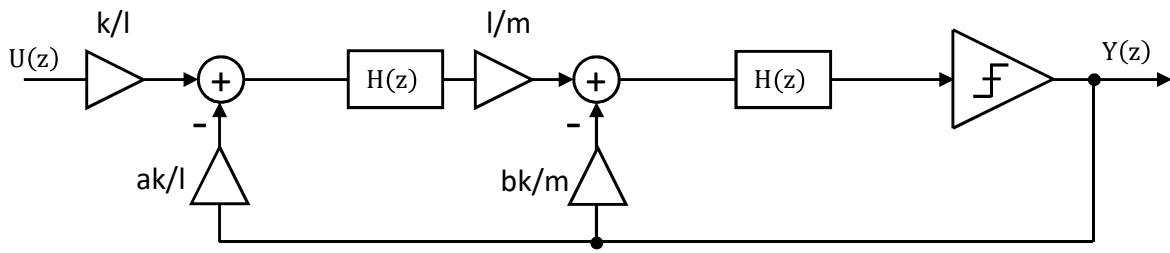
- *Scale switching level of quantizer*  
(for 1-bit quantizer, no scaling, because switching level is 0)
- *Merge coefficients before integrators*



448

## Exercise 8 – Solution

- $a=1, b=2$   
 $k=0.3, l=0.5, m=0.4$
- Coefficients implemented by capacitor ratios (see previous exercise)



449



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# Chapter 8

## Oversampling

### Analog-to-Digital Converters

Courtesy of Dr. Stephan Henzler

Revised by Maciej Jankowski, Texas Instruments



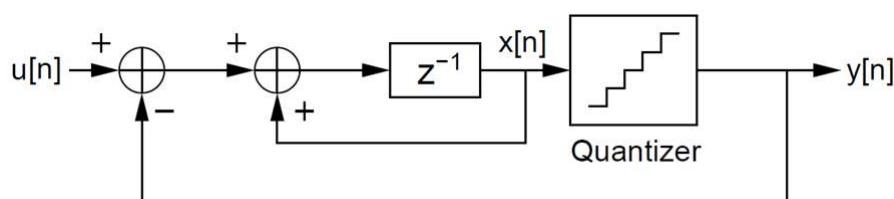
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450

## Outline

- Oversampling
- First-order modulation
- Second-order modulation
- Tones
- Digital filtering
- Sigma-delta DAC
- Circuit design aspects
- Advanced architectures
- Continuous-time sigma-delta ADC

## Exercise 9

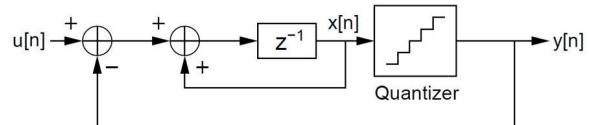


Assume the first-order  $\Sigma\Delta$  modulator to have a constant input signal  $u[n]=1/3$ . Calculate the output signal and all internal signals for the next 3 time steps. The initial condition of the integrator is assumed to be  $x[0]=0.1$ . The output of the quantizer can take the values  $\pm 1$ . Discuss the result. Which assumption of an ideal  $\Sigma\Delta$  modulator is violated?

## Exercise 9 – Solution

- Output  $y[n]$  periodic  
 $\rightarrow$  quantization noise  $e[n]$  not random  
 $\rightarrow$  model not linear!

- $y[n]$  periodic pattern is 3 cycles long  
 $\rightarrow$  power concentrated at DC and  $f_s/3 \rightarrow$  tone at  $f_s/3$ !  
 $\rightarrow$  by low-pass filtering only DC level remains



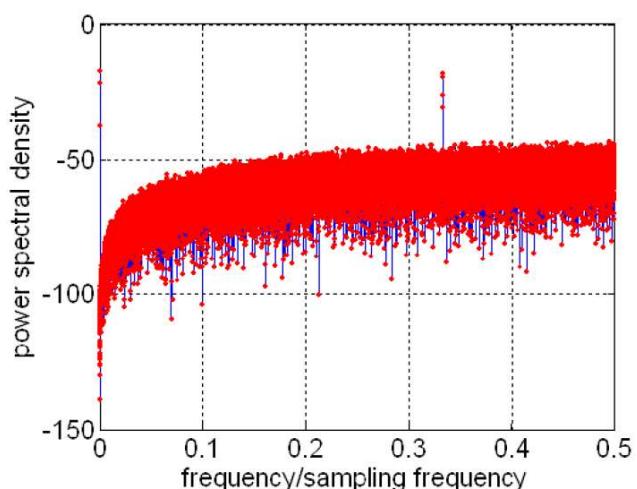
$$(u[n]-y[n])+x[n]=x[n+1]$$

n	u[n]	x[n]	e[n]	y[n]
0	1/3			
1	1/3			
2	1/3			
3	1/3			

453

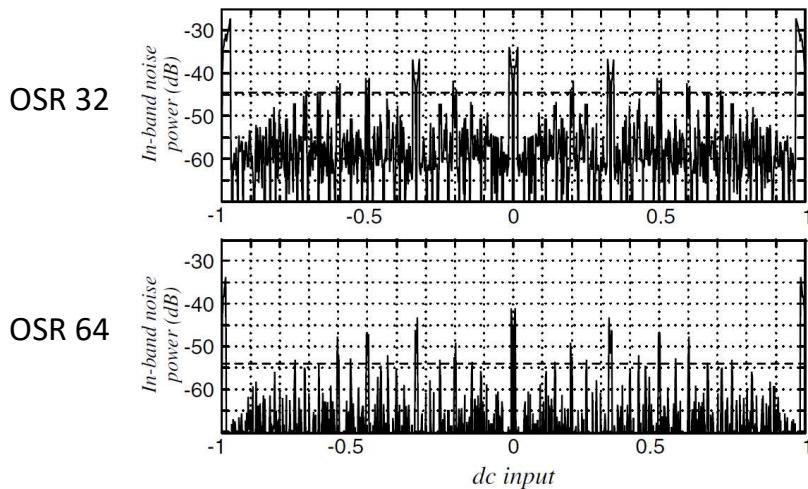
## Tones in Frequency Domain

- $u[n] = 1/3 \rightarrow y[n]$  3 cycles period  
 $\rightarrow$  tone at  $f_s/3$   
 $f_s/3$  outside signal band  
 $\rightarrow$  tone removed through low-pass filtering
- $u[n] = 1/M \rightarrow y[n]$  M cycles period  
 $\rightarrow$  tone at  $f_s/M$   
if  $M > 2 \cdot \text{OSR}$   
 $\rightarrow$  tone within signal band  
 $\rightarrow$  tone remains after low-pass filtering!



454

## 1<sup>st</sup> Order Modulator, In-Band Noise vs. DC



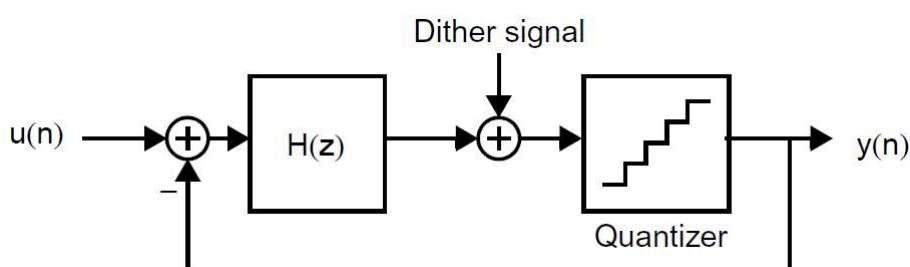
- Spikes indicates conditions for idle tones, degrading SQNR.



Illustration: S. Pavan, R. Schreier, G. Temes, Understanding Delta-Sigma Data Converters, Wiley 2017

455

## Dithering



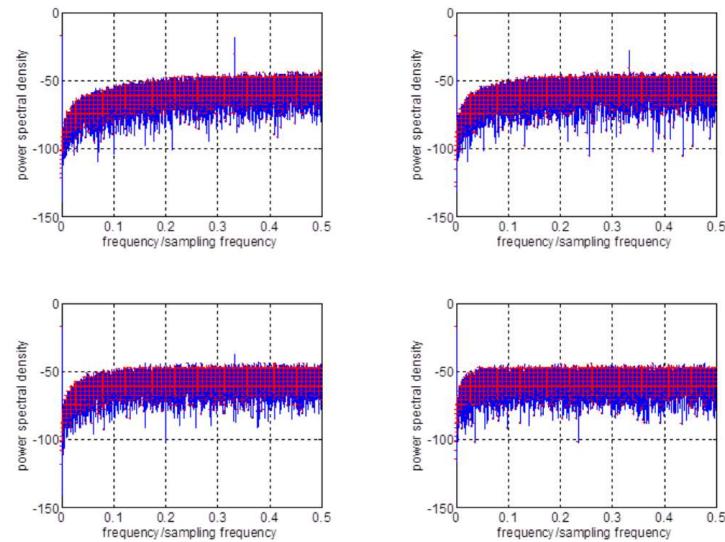
- Reduce the risk of tones by randomizing (artificially) the comparator input signal: dithering
  - typically a bipolar signal  $\pm V_{\text{dith}}$  with constant amplitude and sign controlled by a (pseudo-)random number generator.
  - input dither signal distributed over  $f_s/2$
  - dither noise power comparable to quantization noise power  
→ ~3dB extra in-band noise



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456

## Dithering



457

## Outline

- Oversampling
- First-order modulation
- Second-order modulation
- Tones
- **Digital filtering**
- Sigma-delta DAC
- Circuit design aspects
- Advanced architectures
- Continuous-time sigma-delta ADC

458

## System Architecture of $\Sigma\Delta$ ADC

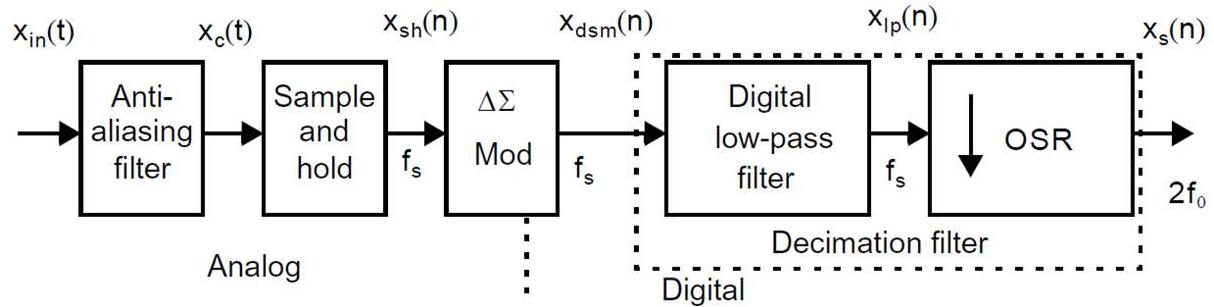


Illustration: T. Carusone, D. Johns, K. Martin, Analog Integrated Circuit Design, Wiley 2012  
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459

## $\Sigma\Delta$ Analog to Digital Conversion

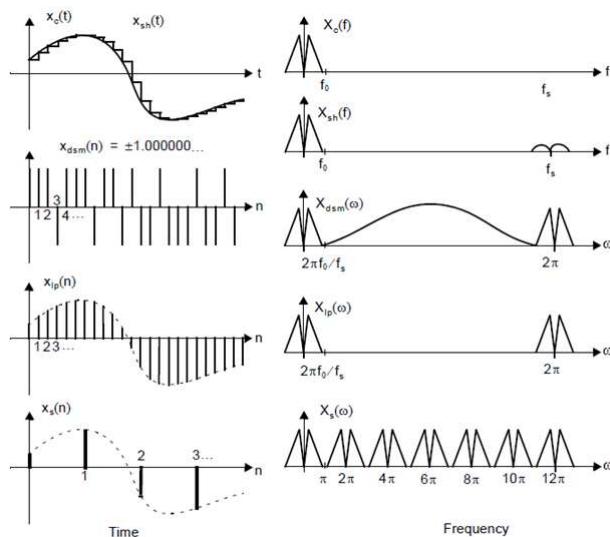


Illustration: T. Carusone, D. Johns, K. Martin, Analog Integrated Circuit Design, Wiley 2012  
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460

## Digital Decimation Filtering (1)

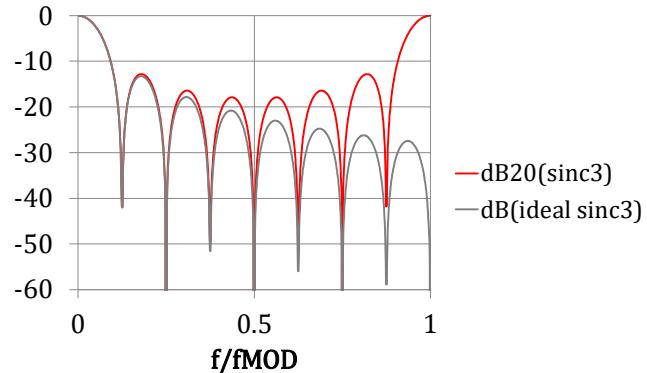
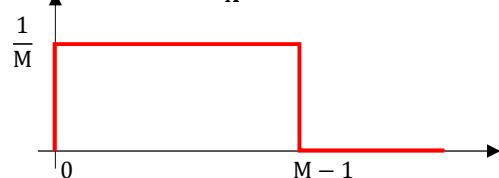
- Sinc filter: basic low-pass filter that averages M subsequent samples

$$\Rightarrow T(z) = \frac{1}{M} \sum_{i=0}^{M-1} z^{-i} = \frac{1}{M} \cdot \frac{1-z^{-M}}{1-z^{-1}}$$

$$\Rightarrow |T(e^{j\omega})| = \left| \frac{\text{sinc}(\omega M/2)}{\text{sinc}(\omega/2)} \right|$$

- Zeros at multiples of  $f_s/M$

$$\text{sinc}(x) = \frac{\sin(x)}{x}$$

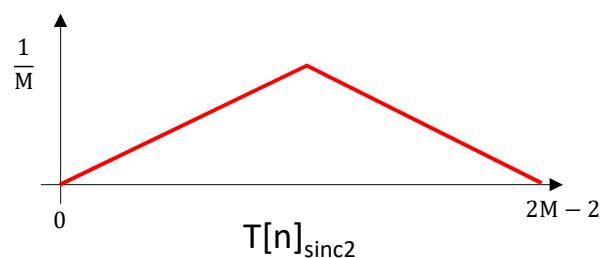


## Digital Decimation Filtering (2)

- Cascade of L+1 averaging filters:  $\text{sinc}^{L+1}$  filter

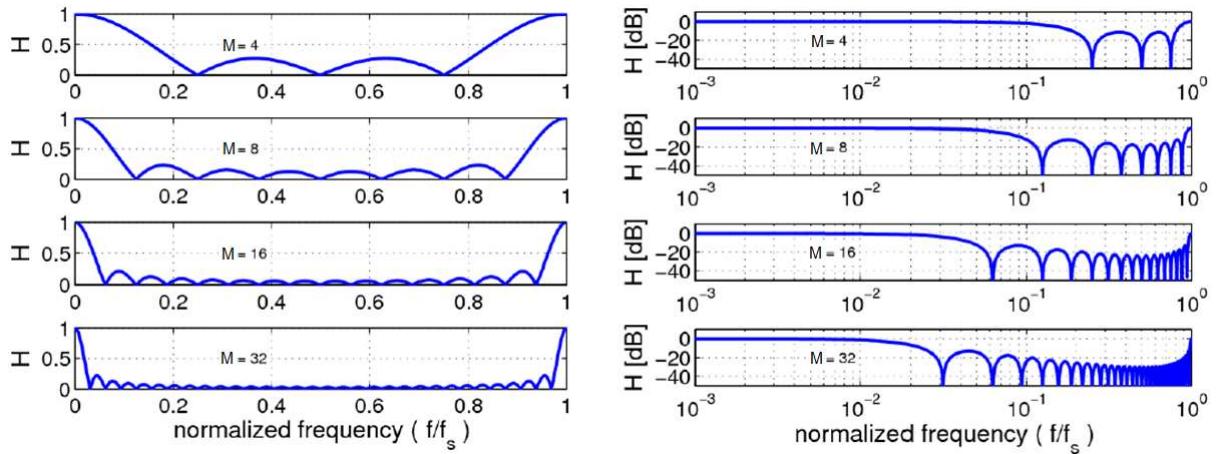
$$\Rightarrow T_{L+1}(z) = \left(\frac{1}{M}\right)^{L+1} \left(\frac{1-z^{-M}}{1-z^{-1}}\right)^{L+1}$$

- Pulse response (convolution):



- The low-pass filter order should be the  $\Sigma\Delta$  modulator order +1  
 → the filter attenuation slope greater than the rising quantization noise  
 → resulting noise falls off at a relatively low frequency

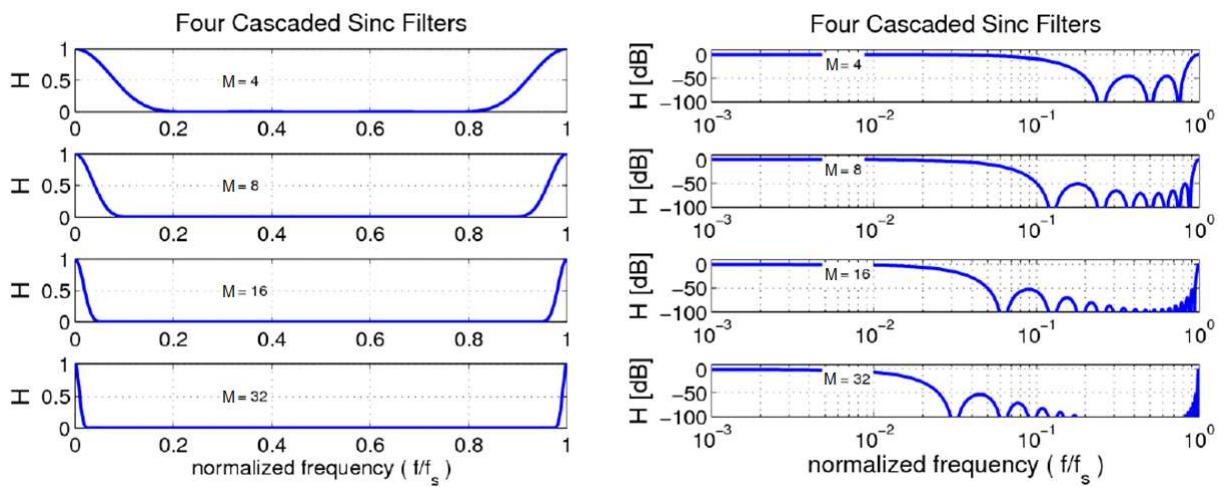
## Sinc Filter Transfer Functions



463



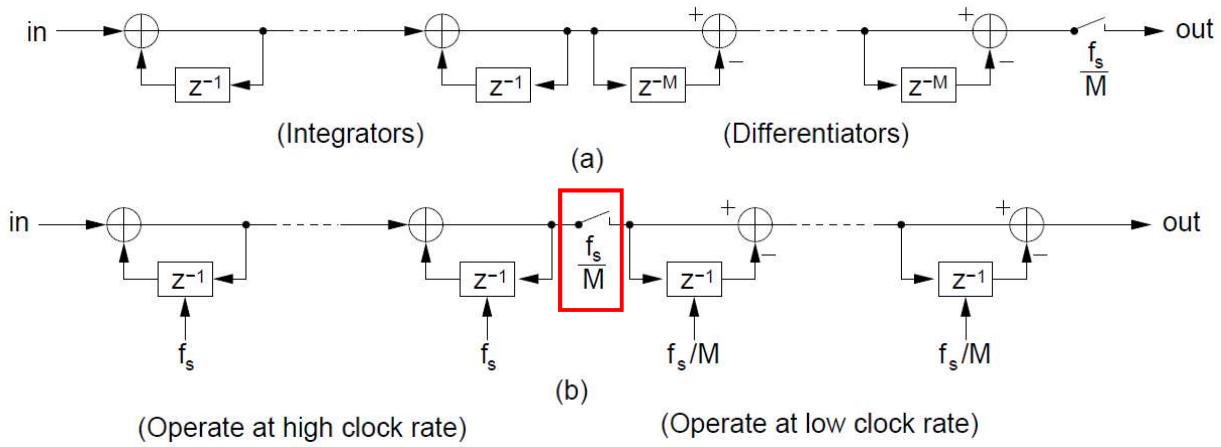
## Sinc Filter Transfer Functions



464



## Sinc Filter Implementation



- Option b) (downsampling before the differentiators) more efficient (Hogenauer structure)

## Nyquist-Rate vs. Oversampling ADCs

Nyquist-rate	Oversampling
High voltage domain resolution	Low voltage domain resolution, down to 1 bit
Low time domain resolution $f_s \approx f_{\text{Nyquist}} (\times 2-10)$	High time domain resolution $f_s >> f_{\text{Nyquist}} (\times 8-1024)$
Low to high resolution (18 bit)	Very high resolution (up to 32 bit)
Result can be directly used	Large decimation filter required
One output symbol = one sample	One sample distributed over many output symbols
"Medium" speed requirements for all circuit blocks	Very high speed requirements for opamps, DAC, etc.

## Outline

- Oversampling
- First-order modulation
- Second-order modulation
- Tones
- Digital filtering
- Sigma-delta DAC
- Circuit design aspects
- Advanced architectures
- Continuous-time sigma-delta ADC



## The Need for $\Sigma\Delta$ Digital-to-Analog Conversion

- Limited resolution of Nyquist-rate DACs:
  - Unary architectures
    - Resistive ladder: by exponential growth of decoding logic
    - Thermometric: by prohibitive area and/or power consumption
  - Binary architectures (binary-weighted, R-2R): by matching accuracy
- High-resolution DAC?
  - oversampling →  $\Sigma\Delta$  DAC



## System Architecture of $\Sigma\Delta$ DAC

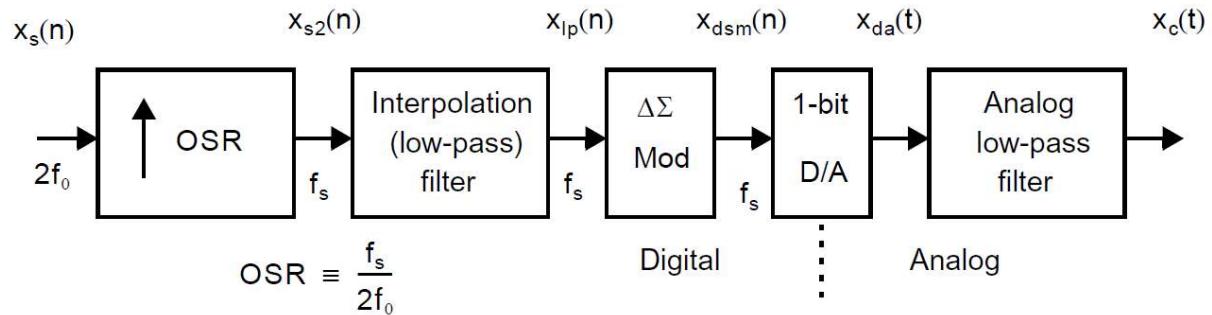


Illustration: T. Carusone, D. Johns, K. Martin, Analog Integrated Circuit Design, Wiley 2012  
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469

## $\Sigma\Delta$ Digital to Analog Conversion

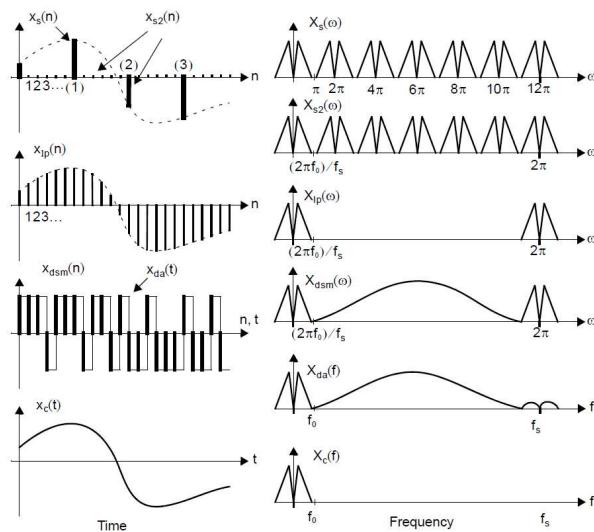


Illustration: T. Carusone, D. Johns, K. Martin, Analog Integrated Circuit Design, Wiley 2012  
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470

# Outline

- Oversampling
- First-order modulation
- Second-order modulation
- Tones
- Digital filtering
- Sigma-delta DAC
- **Circuit design aspects**
- Advanced architectures
- Continuous-time sigma-delta ADC



# Circuit Design Aspects

- Opamp (or OTA) offset
- Noise
- Finite opamp gain
- Finite opamp bandwidth
- Finite opamp slew-rate
- Non-ideal operation of the ADC
- Non-ideal operation of the DAC



## Offset

- First integrator: added to the input signal  
→ equal offset at the digital output → critical
- Second integrator: referred to the input divided by the transfer function of the first block (very high DC gain!)
- Quantizer/ADC: referred to the input divided by the transfer function of one or more integrators  
→ does not limit the DC operation  
→ flexibility of the quantizer design
- DAC: added to the input  
→ output offset, similar to the  $V_{os}$  of the first integrator.

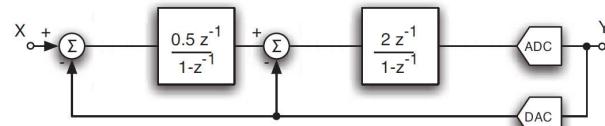


Illustration: F. Maloberti, Data Converters, Springer 2007  
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473

## Offset Reduction: Dynamic Element Matching

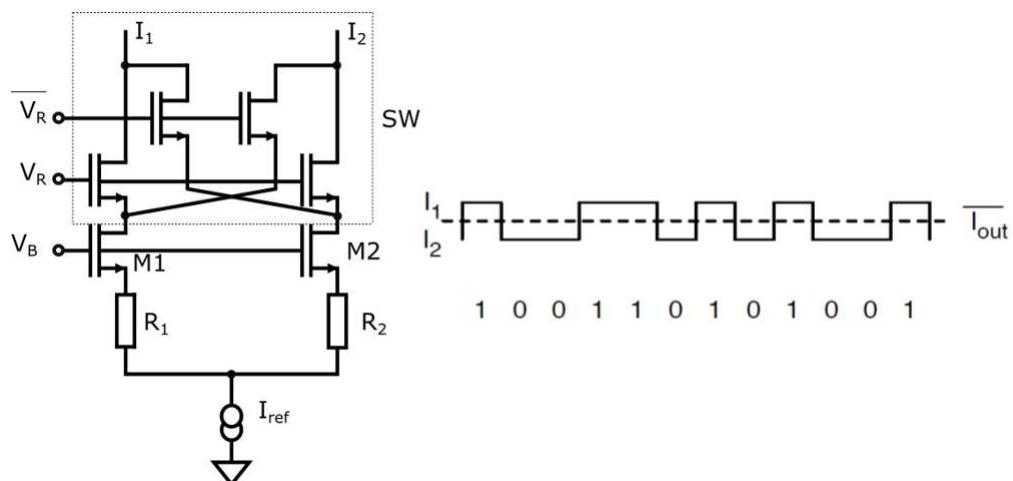


Illustration: F. Maloberti, Data Converters, Springer 2007  
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474

## Noise

- Same considerations as for offset
- $kT/C$  noise at the input of the first integrator (= modulator input): limits the minimum usable input capacitance

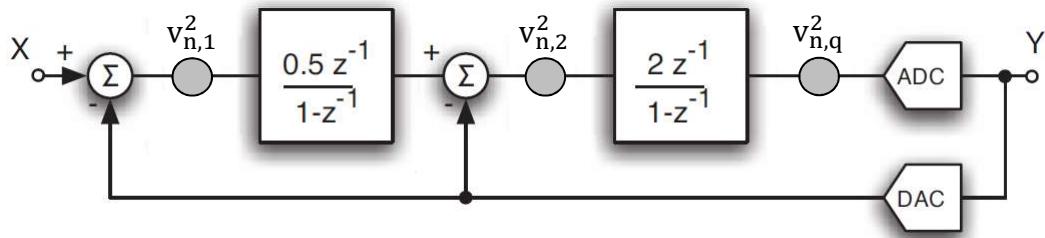
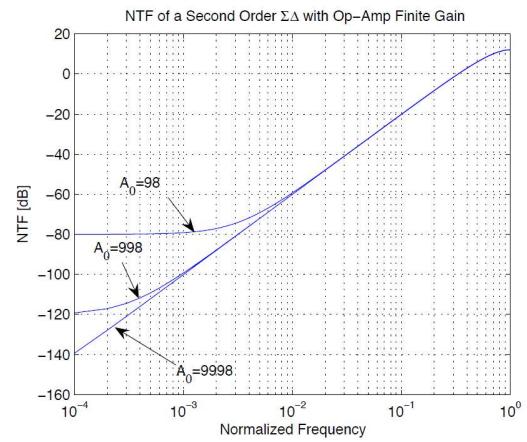
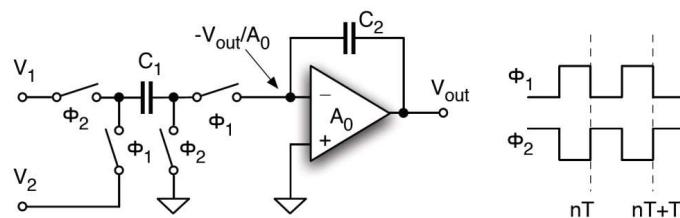


Illustration: F. Maloberti, Data Converters, Springer 2007  
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475

## OTA/Opamp Open-Loop Gain

- If the opamp does not have enough open-loop gain, the virtual ground node does not fully settle to zero.  
→ charge left on  $C_1$ , proportional to  $V_{out}$   
→ degradation in ADC SQNR and linearity
- Requirement:  $A_{ol} \gg \frac{OSR}{\pi}$



Illustrations: F. Maloberti, Data Converters, Springer 2007  
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476

## OTA Open-Loop Gain: Deadzone

- In a deadzone, the output does not respond to changes at the input: increased code width (DNL).
- Caused by finite open-loop gain.
- Non-linear effect.
- Ends of deadzone marked by tones.
- AC inputs can disperse the DZ.

$$1^{\text{st}} \text{ order: } |x| < \frac{2}{A_{\text{ol}}}$$

$$2^{\text{nd}} \text{ order: } |x| < \frac{1.5}{A_{\text{ol}}^2}$$

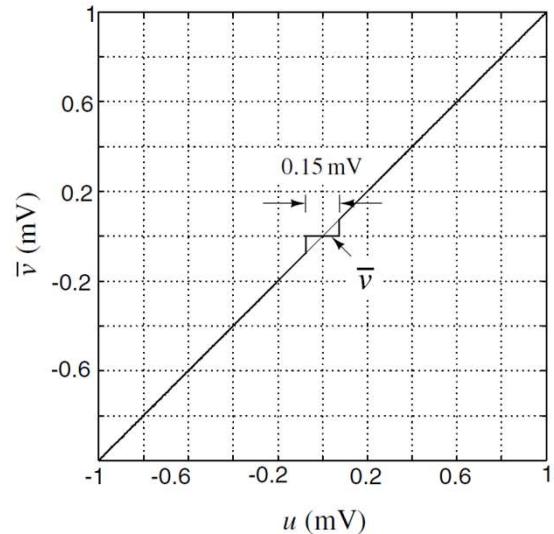


Illustration: S. Pavan, R. Schreier, G. Temes, Understanding Delta-Sigma Data Converters, Wiley 2017

477

## OTA/Opamp Bandwidth and Slew-Rate

- Incomplete settling of the opamp output  
→ error added to the integrator output  
→ shaped by the transfer function from injection point to the output  
→ first integrator more critical than the second
- Opamp → trade-off speed vs. power

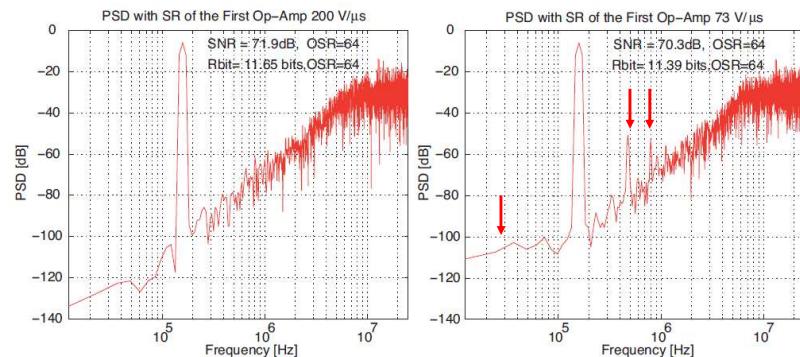


Illustration: F. Maloberti, Data Converters, Springer 2007

478

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## Amplifier Choice

- The integrators only need to drive capacitors
- At the end of settling, no output current – high  $R_{out}$  OK
- OTA (Operational Transconductance Amplifier) well suited
  - No frequency compensation (power, PSRR, SR)
  - Telescopic or folded-cascode (shown)

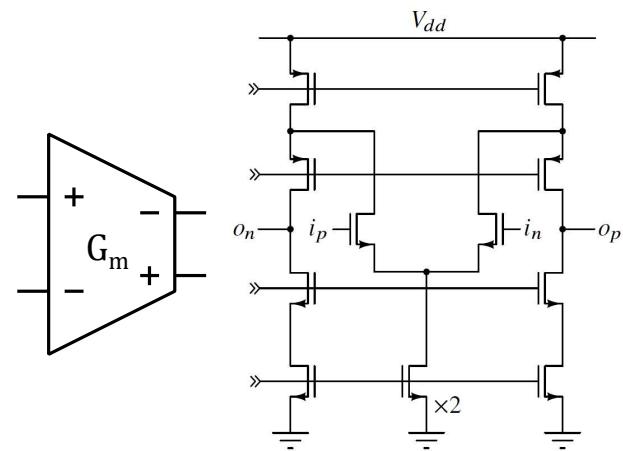


Illustration: S. Pavan, R. Schreier, G. Temes, Understanding Delta-Sigma Data Converters, Wiley 2017  
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479

## ADC and DAC Errors

- ADC (quantizer) output error:
  - added to the quantization noise → noise-shaped
  - usually much smaller than quantization noise
  - does not hamper circuit performance
- DAC output error (noise, offset, non-linearity):
  - added to the input of the modulator
  - transferred to the output through the STF
  - noise at the modulator input → limits the minimum usable input capacitance

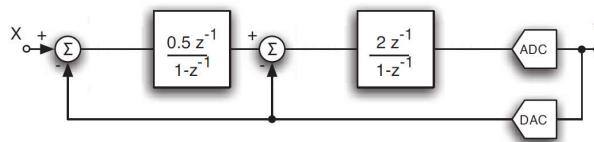
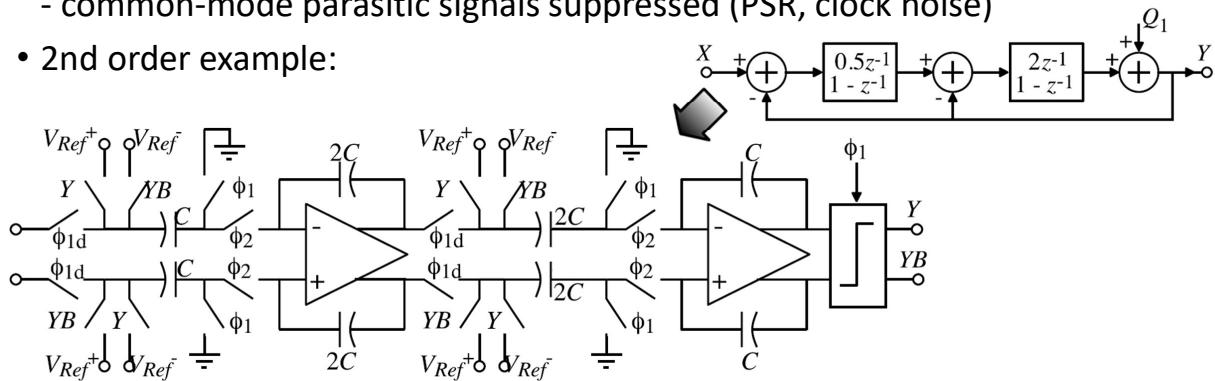


Illustration: F. Maloberti, Data Converters, Springer 2007  
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480

## Fully Differential $\Sigma\Delta$ ADCs

- Most common implementation of practical  $\Sigma\Delta$  modulators
- Advantages:
  - double signal swing  $\rightarrow$  6dB increase of dynamic range
  - common-mode parasitic signals suppressed (PSR, clock noise)
- 2nd order example:



Illustrations: P. Allen, D. Holberg, CMOS Analog Circuit Design, Oxford 2002

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481

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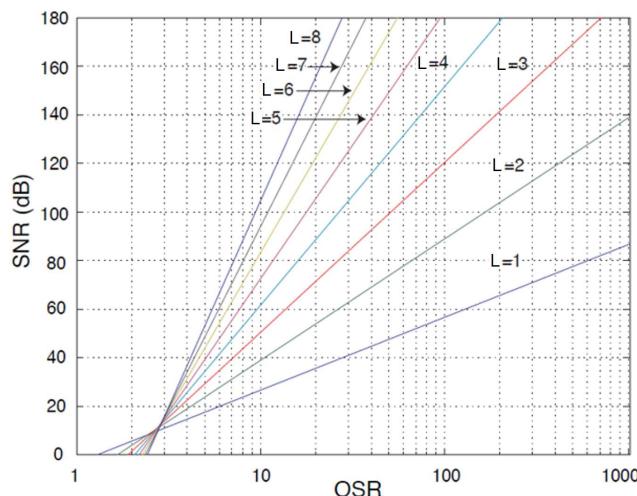


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482

## SQNR vs. Modulator Order

SNR versus the OSR for different Modulator Order



- Main advantage of high-order  $\Sigma\Delta$  modulators is wider band with low quantization noise – allows lower OSR.
- Multi-bit modulators achieve similar advantages.
- SQNR increases with:
  - modulator order L
  - oversampling ratio OSR
  - quantizer number of bits N

$$\text{SQNR} \approx 6N + 10(2L + 1)\log(\text{OSR})$$



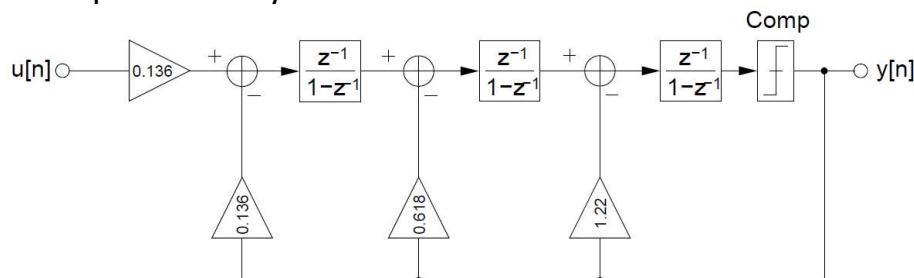
Illustration: F. Maloberti, Data Converters, Springer 2007

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483

## 3rd Order Single-Stage $\Sigma\Delta$ Modulator

- 3rd order loop → stability difficult to achieve



$$\text{STF}(z) = \frac{0.136}{1 - 1.78z^{-1} + 1.178z^{-2} - 0.262z^{-3}}$$

$$\text{NTF}(z) = \frac{(1 - z^{-1})^3}{1 - 1.78z^{-1} + 1.178z^{-2} - 0.262z^{-3}}$$

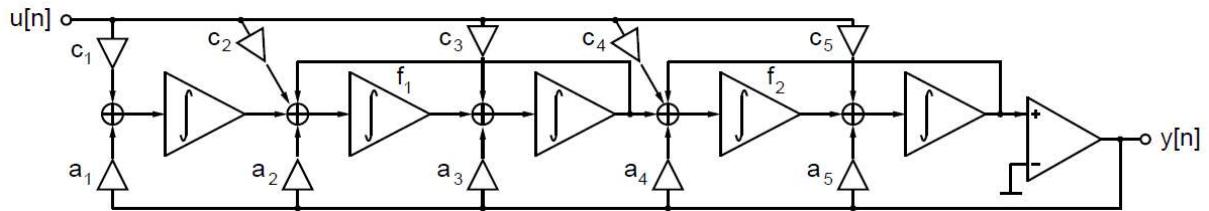


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484

## Higher-Order Single-Stage $\Sigma\Delta$ Modulator

- Stable only for some coefficients (difficult to find, with complex math)
- Very sensitive to variation of these coefficients → low robustness
- Maximum Stable Amplitude reduces with order



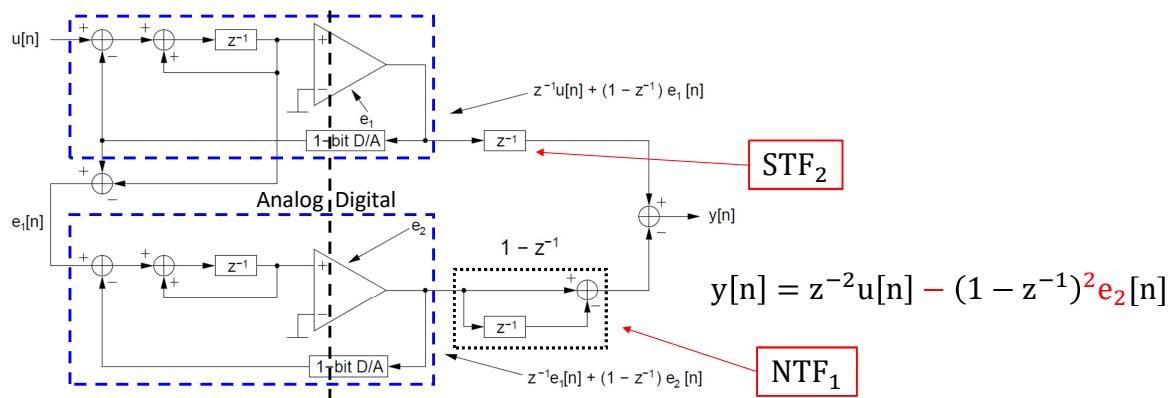
485



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## Cascaded $\Sigma\Delta$ Modulators (1)

- MASH (Multi-stAge noise SHaping)
- Example: 2 cascaded 1st-order modulators → 2nd-order MASH  $\Sigma\Delta$  modulator



486

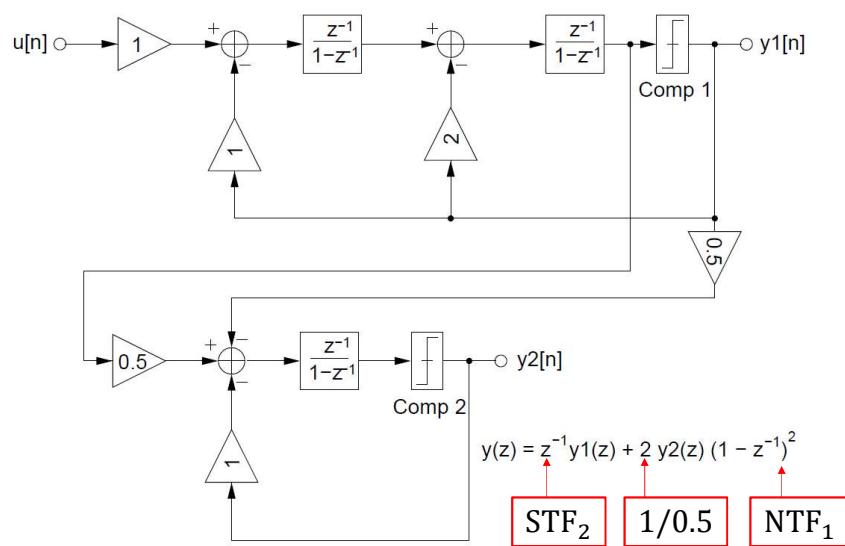


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## Cascaded $\Sigma\Delta$ Modulators (2)

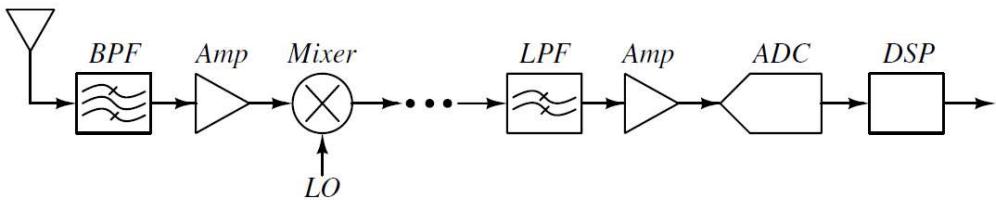
- Consist of 1st and 2nd order modulators  
→ Stability easy to achieve, unlike for single-stage high-order modulators
- Challenge: matching of coefficients critical for cancelation of  $e_1[n]$  (or noise leakage)  
→ Fortunately, capacitor matching in CMOS technologies is very good

## 3rd-Order (2-1) MASH Structure

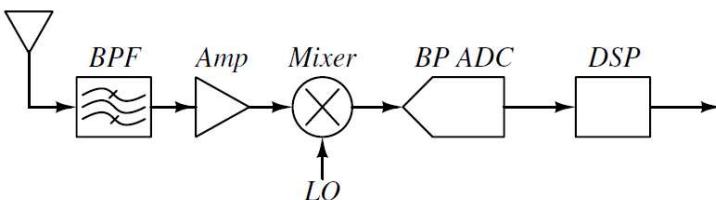


# The Need for a Bandpass $\Sigma\Delta$ Modulator

*Superheterodyne Receiver*



*Receiver using a Bandpass ADC at the first IF*



Illustrations: S. Pavan, R. Schreier, G. Temes, Understanding Delta-Sigma Data Converters, Wiley 2017

489

## Bandpass $\Sigma\Delta$ Modulator (1)

- Loop filter:  $H(z) = \frac{X(z)}{W(z)} = \frac{z^{-1}}{1+z^{-2}}$
- STF(z) =  $\frac{H(z)}{1+H(z)} = \frac{z^{-1}}{1+z^{-1}+z^{-2}}$
- NTF(z) =  $\frac{1}{1+H(z)} = \frac{1+z^{-2}}{1+z^{-1}+z^{-2}}$
- Zero in NTF(z)  $\leftrightarrow$  pole in H(z)
- $1 + z^{-2} = 0 \leftrightarrow z = \pm j = e^{\pm j\pi/2}$   
 $\rightarrow \omega T = \pm j \pi/2 \leftrightarrow f = \pm f_s/4$
- H(z): resonator with resonance frequency  $f_s/4$

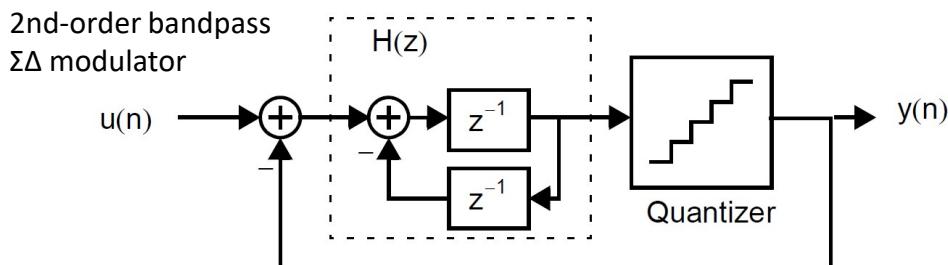


Illustration: T. Carusone, D. Johns, K. Martin, Analog Integrated Circuit Design, Wiley 2012

490

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## Bandpass ΣΔ Modulator (2)

- $H(z)$ : pole at  $f_s/4$
- NTF(z): zero at  $f_s/4$  (center frequency), bandwidth  $BW = f_\Delta = f_s/\text{OSR}$
- Bandpass ΣΔ ADC: applicable for systems with narrowband signals (IF frequencies)
- Sampling frequency must be 4x carrier frequency

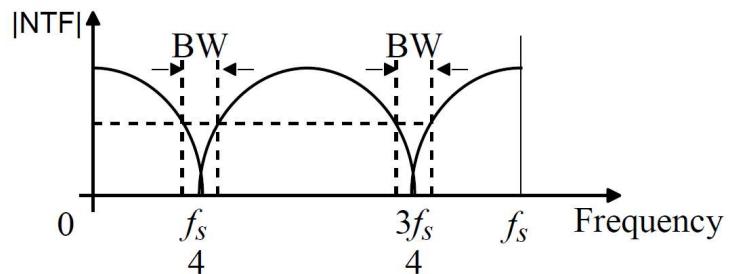


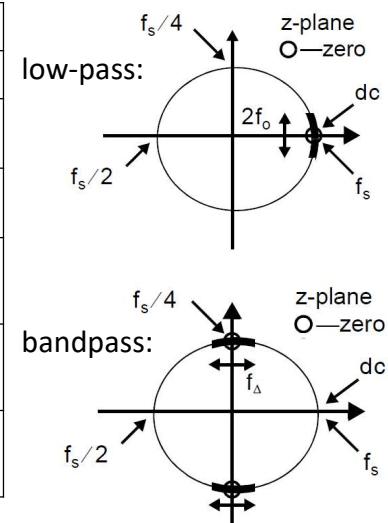
Illustration: P. Allen, D. Holberg, CMOS Analog Circuit Design, Oxford 2002

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491

## Bandpass vs. Low-Pass ΣΔ Modulator

	1st-order low-pass	2nd-order bandpass
Loop filter	Integrator	Resonator
$H(z)$	$H(z) = \frac{z^{-1}}{1-z^{-1}}$	$H(z) = \frac{z^{-1}}{1+z^{-2}}$
NTF(z)	$1 - z^{-1}$	$\frac{1+z^{-2}}{1+z^{-1}+z^{-2}}$
$H(z)$ pole / NTF(z) zero	DC	$f_s/4$
ΣΔ modulator input/output	Not modulated (baseband, no carrier)	Modulated with carrier $f_s/4$
Carrier demodulation	Analog, before ΣΔ modulator	Digital, after ΣΔ modulator



Illustrations: T. Carusone, D. Johns, K. Martin, Analog Integrated Circuit Design, Wiley 2012

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492

## Advanced $\Sigma\Delta$ Architectures

Significantly more complex  $\Sigma\Delta$  loop filters have been created for:

- High SNR: 130dB+
- Improved THD: -120dB or less
- Low oversampling ratios: 8x, 16x
- Band-pass conversion of high-speed narrow-band signals: RF, DSL communications
- Utilizing deep sub- $\mu$ m digital processes with high leakage and poor component quality
- 3<sup>rd</sup>, 4<sup>th</sup> and higher order of loop filters  
→ complex stability solutions
- Multiple loops (e.g., MASH)  
→ matching problems
- Continuous-time integrators instead of switched-capacitor  
→ clock jitter sensitivity



# Chapter 8

## Oversampling

### Analog-to-Digital Converters

Dr. Florin Burcea

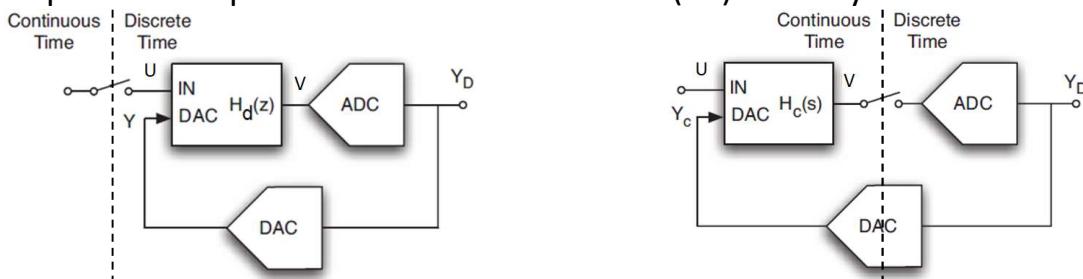


## Outline

- Oversampling
- First-order modulation
- Second-order modulation
- Tones
- Digital filtering
- Sigma-delta DAC
- Circuit design aspects
- Advanced architectures
- Continuous-time sigma-delta ADC

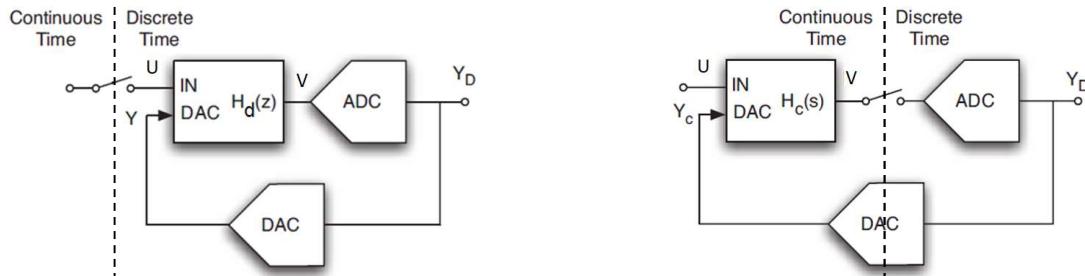
## The Need for Continuous-Time $\Sigma\Delta$ Modulation

- Oversampling discrete-time (DT) ADC :
  - All transients must settle within half of clock cycle
  - Very high speed/wide bandwidth requirements for opamps, DAC, etc.
  - Limitation on maximum frequency
- What could be done?
  - implement loop filter with continuous-time (CT) circuitry



## Continuous-Time ΣΔ Architectures (1)

- If the sampler is moved after the loop filter/before the quantizer input:
  - Loop filter can be realized in continuous time  
→ settling not a basic requirement → increased speed of operation
  - Loop filter also acts as anti-aliasing filter  
→ no need for explicit anti-aliasing filter

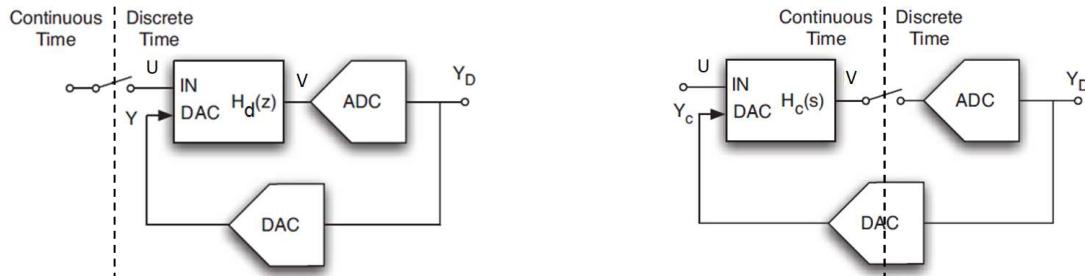


Illustrations: F. Maloberti, Data Converters, Springer 2007  
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497

## Continuous-Time ΣΔ Architectures (2)

- DT ΣΔ: jitter at input sampler affects SNR  $\left(\frac{du}{dt} \cdot \Delta t\right)$
- CT ΣΔ: sampling error due to clock jitter at quantizer gets noise shaped  
But: DAC output processed continuously
  - Effect of clock jitter in DAC is observed directly
  - Error in DAC output directly added → seen at modulator output with STF=1

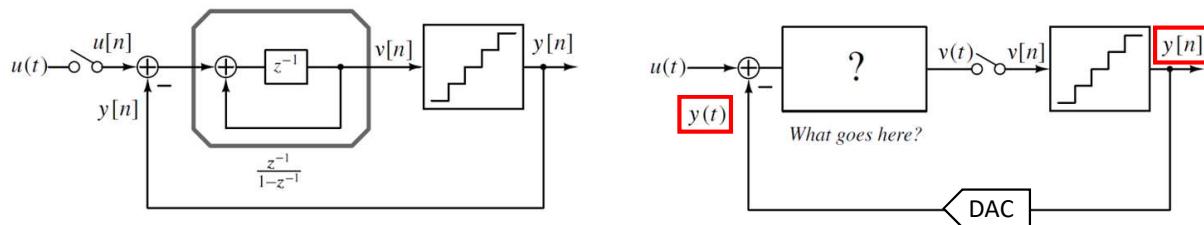


Illustrations: F. Maloberti, Data Converters, Springer 2007  
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498

## CT $\Sigma\Delta$ Modulator Design from DT Equivalent (1)

- CT modulator design: usually starts from an already designed DT prototype
- Quantization noise  $E(z)$ : discrete-time signal (for both DT and CT modulator)
- Quantizer/Modulator output  $Y(z)$ : also discrete-time signal in both cases  
→ Discrete-time noise transfer function:  $NTF(z)$
- CT modulator:  $y[n]$  output and  $y[t]$  at input?  
→ pulse-shaping (hold) DAC between CT modulator output and input

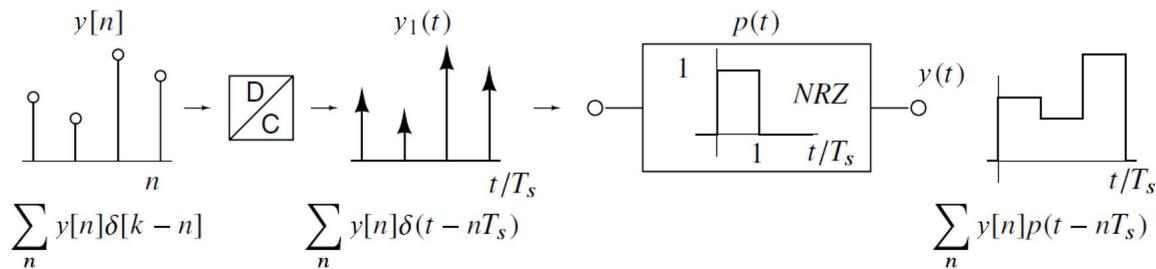
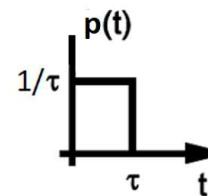


Illustrations: S. Pavan, R. Schreier, G. Temes, Understanding Delta-Sigma Data Converters, Wiley 2017

499

## DAC Pulse Shaping/Hold

- DAC: converts DT sequence to CT sequence by shaping it with an appropriate pulse
- DAC impulse response:  $p(t) \rightarrow H_{DAC}(s) = \frac{1-e^{-st\tau}}{s\tau}$
- Return-to-zero (RTZ) DAC:  $\tau < T$
- Non-return-to-zero (NRZ) DAC:  $\tau = T$

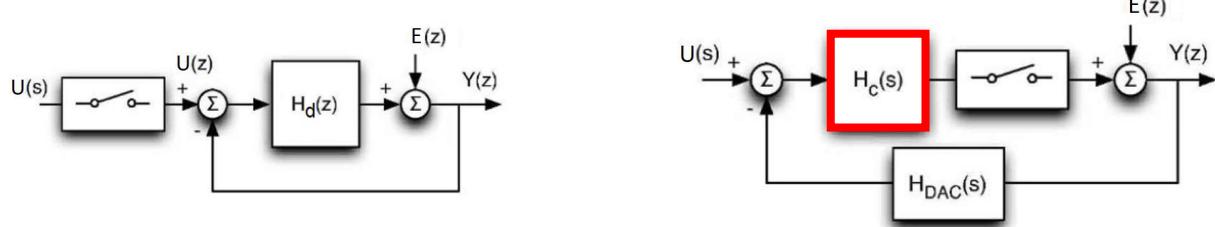


Illustrations: S. Pavan, R. Schreier, G. Temes, Understanding Delta-Sigma Data Converters, Wiley 2017

500

## CT $\Sigma\Delta$ Modulator Design from DT Equivalent (2)

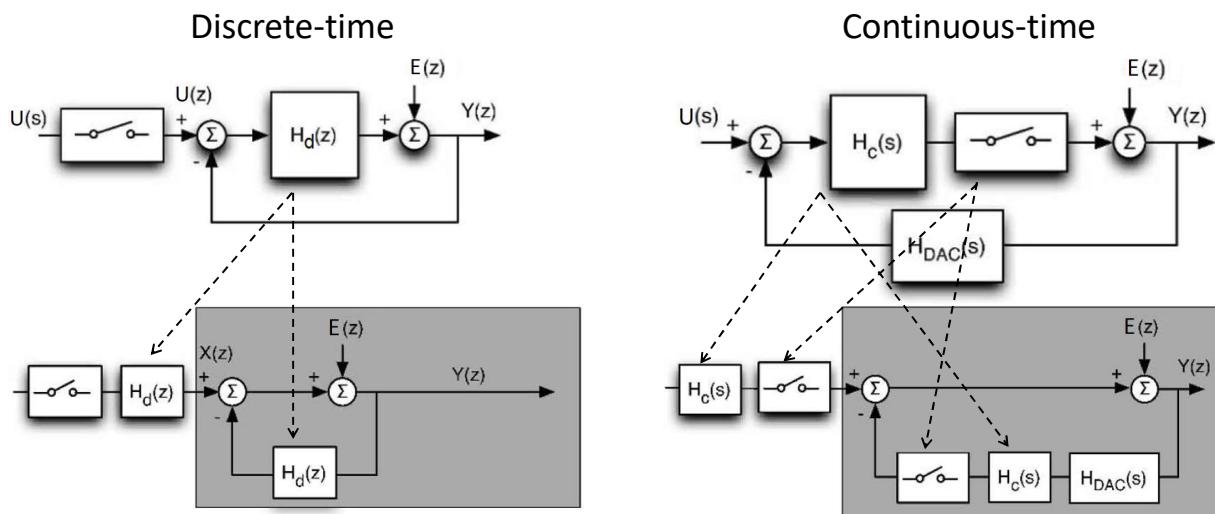
- Design task: identify corresponding CT architecture with equal or very close noise transfer function ( $NTF(z)$ ) to the initial DT modulator  
→ identify CT loop filter transfer function,  $H_c(s)$
- DT modulator:  $NTF_d(z) = \frac{1}{1+H_d(z)}$
- CT modulator: how to express  $NTF_c(z)$  in terms of  $H_c(s)$ ?  
→ draw equivalent linear model of modulator



Illustrations: S. Pavan, R. Schreier, G. Temes, Understanding Delta-Sigma Data Converters, Wiley 2017  
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501

## Linear Equivalent Model of $\Sigma\Delta$ Modulator

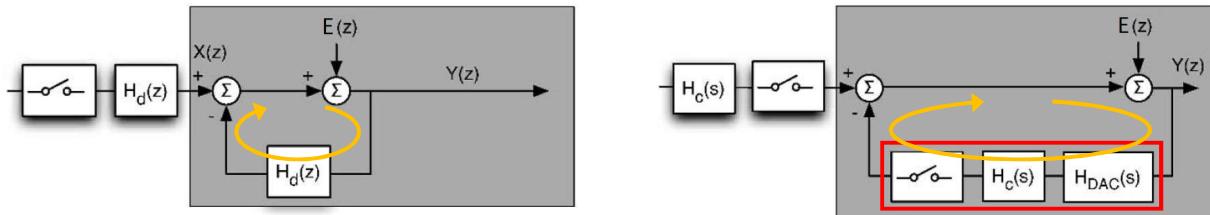


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502

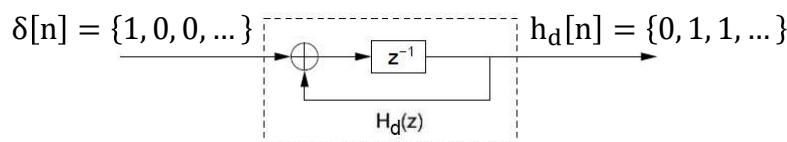
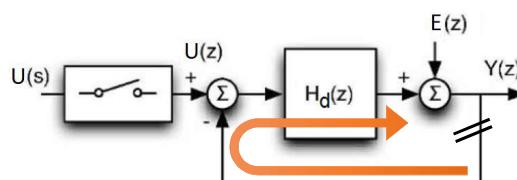
## Equivalent Noise Transfer Function

- $\text{NTF}(z) = \frac{Y(z)}{E(z)} (U = 0) \rightarrow \text{discrete-time for both DT and CT modulator}$
- DT modulator:  $\text{NTF}_d(z) = \frac{1}{1+H_d(z)}$        $H_d(z)$ : loop transfer function
- Equivalent NTF  $\rightarrow$  equivalent loop transfer function:  $H_d(z) = H_c^*(z)$
- CT modulator:  $\text{NTF}_c(z) = \frac{1}{1+H_c^*(z)}$        $H_c^*(z) \neq H_c(e^{sT})$  !



## 1st Order DT $\Sigma\Delta$ – Loop Impulse Response

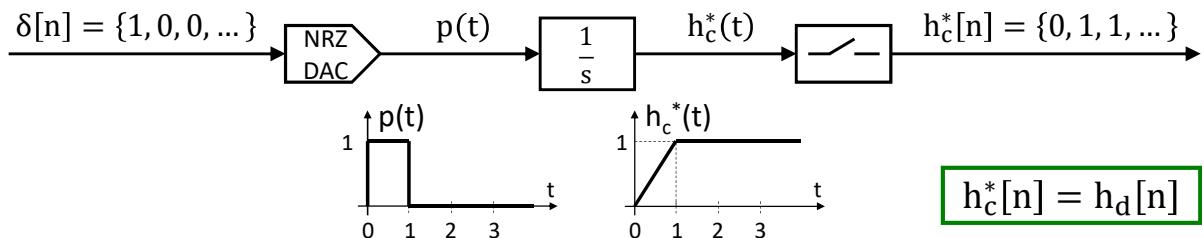
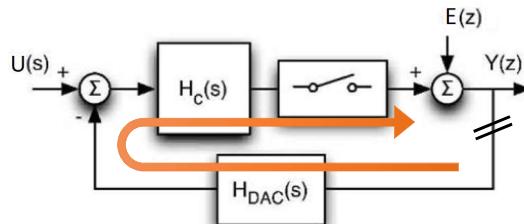
- Discrete-time  $\Sigma\Delta$



## 1st Order CT $\Sigma\Delta$ – Loop Impulse Response

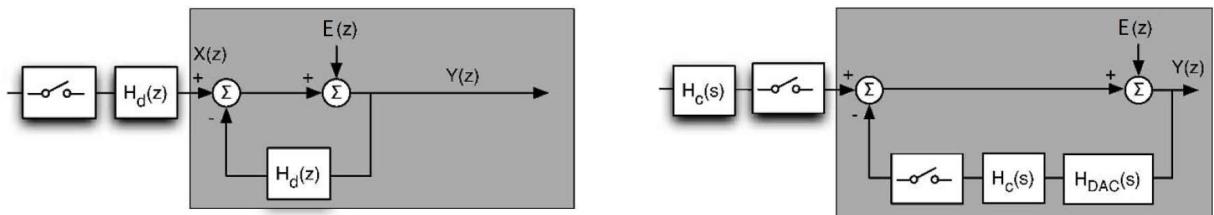
- Continuous-time  $\Sigma\Delta$

Normalization:  
t to T =  $1/f_s$



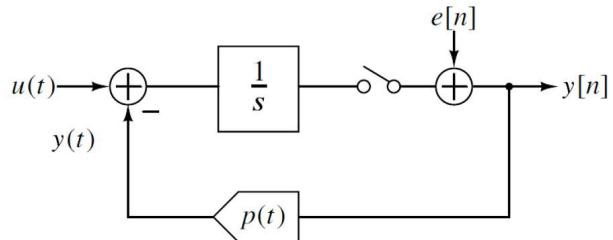
## Equivalent Signal Transfer Function

- $STF_d(z) = \frac{Y(z)}{U(z)}$  ( $E(z) = 0$ ) =  $\frac{H_d(z)}{1+H_d(z)}$  → input and output both DT
- STF for CT modulator: output DT, input CT → mixed  
→ has to be considered in CT domain →  $STF_c(s)$
- Mapping from DT to CT domain (for the DT part):  $z \rightarrow e^{sT}$   
(Normalization: t to T)

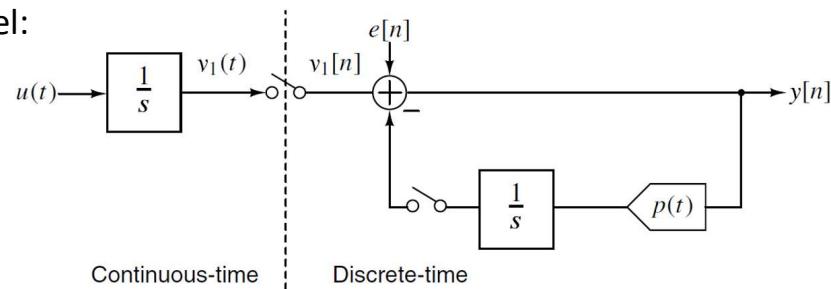


## CT $\Sigma\Delta$ Modulator – STF (1)

- Linear model:
  - DT/CT interface inside FB loop



- Equivalent linear model:
  - DT/CT interface outside FB loop



Illustrations: S. Pavan, R. Schreier, G. Temes, Understanding Delta-Sigma Data Converters, Wiley 2017  
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507

## CT $\Sigma\Delta$ Modulator – STF (2)

- $\text{STF}_c(s) = \frac{Y(s)}{U(s)}$  ( $E = 0$ )  $\rightarrow \text{STF}_c(s) = \frac{Y(s)}{V_1(s)} \cdot \frac{V_1(s)}{U(s)}$  ( $E = 0$ )
- $\frac{Y(z)}{V_1(z)}$  ( $E(z) = 0$ )  $= \frac{Y(z)}{E(z)}$  ( $V_1(z) = 0$ )  $= \text{NTF}_c(z) = 1 - z^{-1}$
- Mapping from DT to CT domain:  $z \rightarrow e^{sT}$       Normalization:  $t$  to  $T$   
 $\rightarrow \frac{Y(s)}{V_1(s)} (E(s) = 0) = \text{NTF}_c(s) = 1 - e^{-s} = 1 - e^{-s/T}$
- $\frac{V_1(s)}{U(s)} = H_c(s) = \frac{1}{s}$

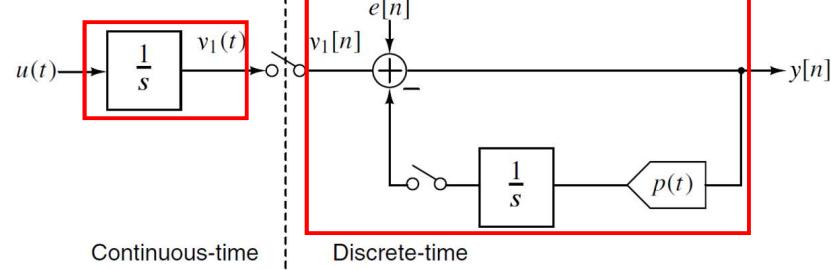


Illustration: S. Pavan, R. Schreier, G. Temes, Understanding Delta-Sigma Data Converters, Wiley 2017  
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508

## CT $\Sigma\Delta$ Modulator – STF (3)

- $\frac{Y(s)}{V_1(s)}(E(s) = 0) = NTF_c(s) = 1 - e^{-s}$        $\frac{V_1(s)}{U(s)} = H_c(s) = \frac{1}{s}$
- $STF_c(s) = \frac{Y(s)}{U(s)}(E(s) = 0) \rightarrow STF_c(s) = H_c(s) \cdot NTF_c(s) = \frac{1-e^{-s}}{s}$
- $\rightarrow STF_c(f) = \frac{1-e^{-j2\pi f/f_s}}{j2\pi f/f_s} = e^{-j\pi f/f_s} \text{sinc}(\pi f/f_s)$

Normalization:  
t to T  $\leftrightarrow$  f to  $f_s$

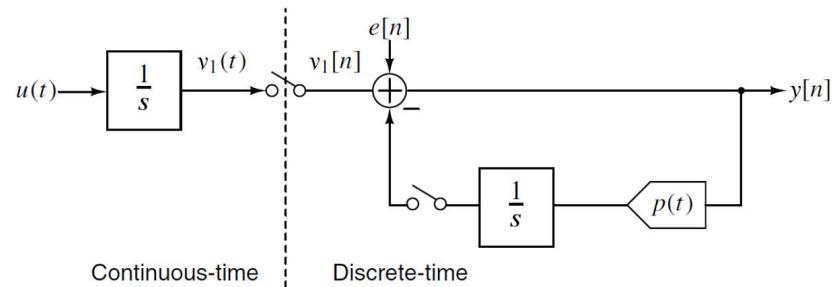


Illustration: S. Pavan, R. Schreier, G. Temes, Understanding Delta-Sigma Data Converters, Wiley 2017  
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509

## Magnitude Response of STF (1)

- $STF_c(f) = e^{-j\pi f/f_s} \text{sinc}(\pi f/f_s) \rightarrow |STF_c(f)| = |\text{sinc}(\pi f/f_s)|$ 
  - unity at low frequency
  - zero at integer multiples of sampling frequency  $\rightarrow$  tones eliminated

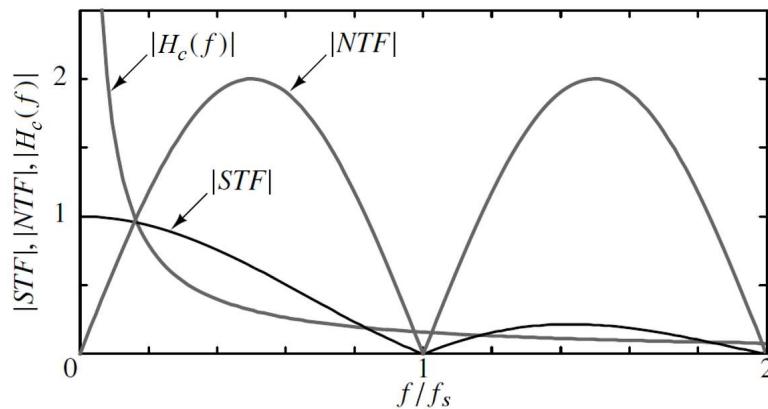


Illustration: S. Pavan, R. Schreier, G. Temes, Understanding Delta-Sigma Data Converters, Wiley 2017  
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510

## Magnitude Response of STF (2)

- STF response in alias band: small → inherent anti-aliasing in CT  $\Sigma\Delta$   
→ explicit anti-aliasing filter before quantizer not necessary
- Intuitively: loop filter (low-pass behavior) before quantizer

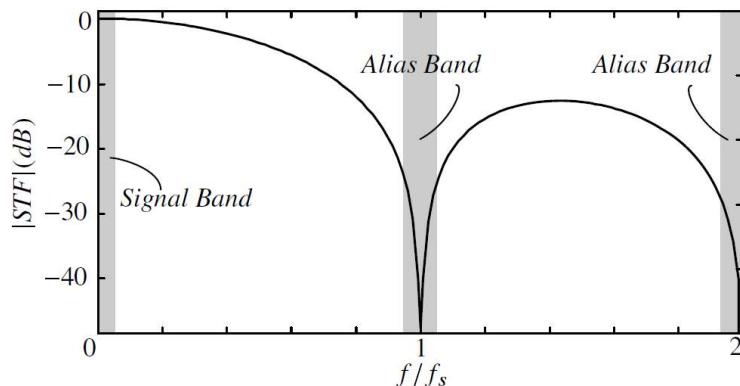
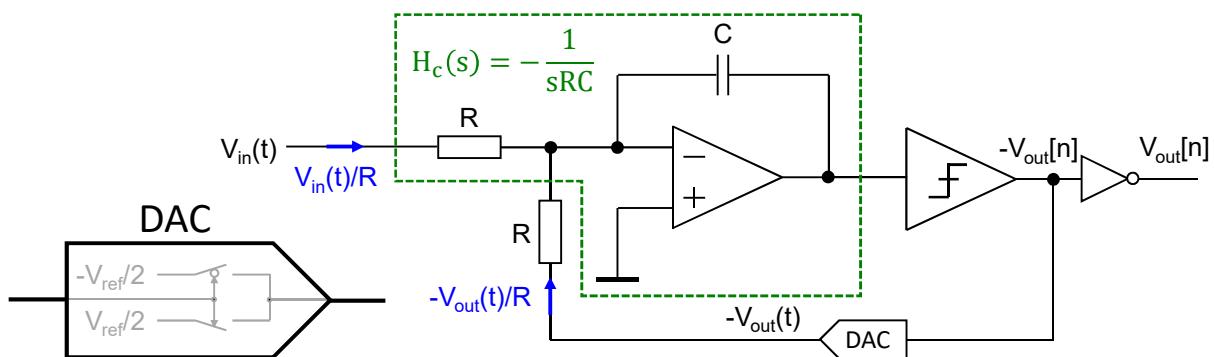


Illustration: S. Pavan, R. Schreier, G. Temes, Understanding Delta-Sigma Data Converters, Wiley 2017

511

## 1st Order CT $\Sigma\Delta$ Modulator – Circuit Example (1)

- Integrator: inverting  
→ modulator output  $V_{out}[n]$ : inverted comparator output  
→ negative feedback  $-V_{out}[n]$ : direct comparator output
- Clocked comparator (e.g. sense-amplifier latch) → no explicit S/H circuit



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512

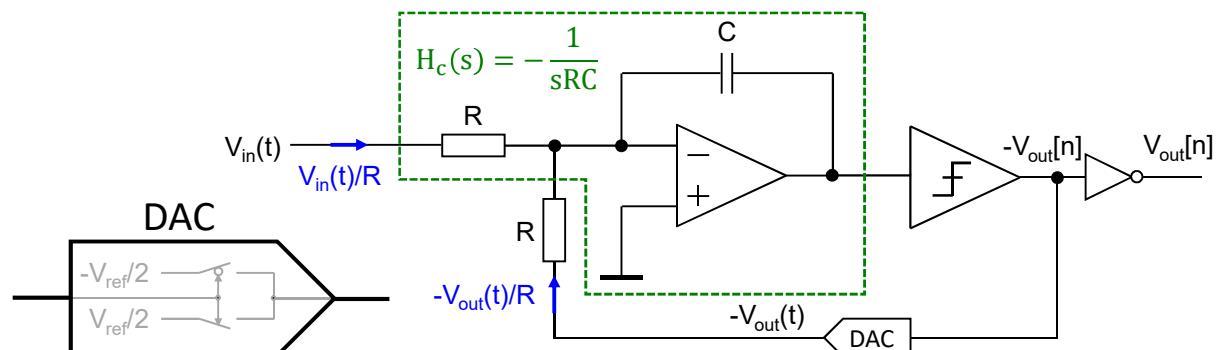
## 1st Order CT $\Sigma\Delta$ Modulator – Circuit Example (2)

- RC constant:

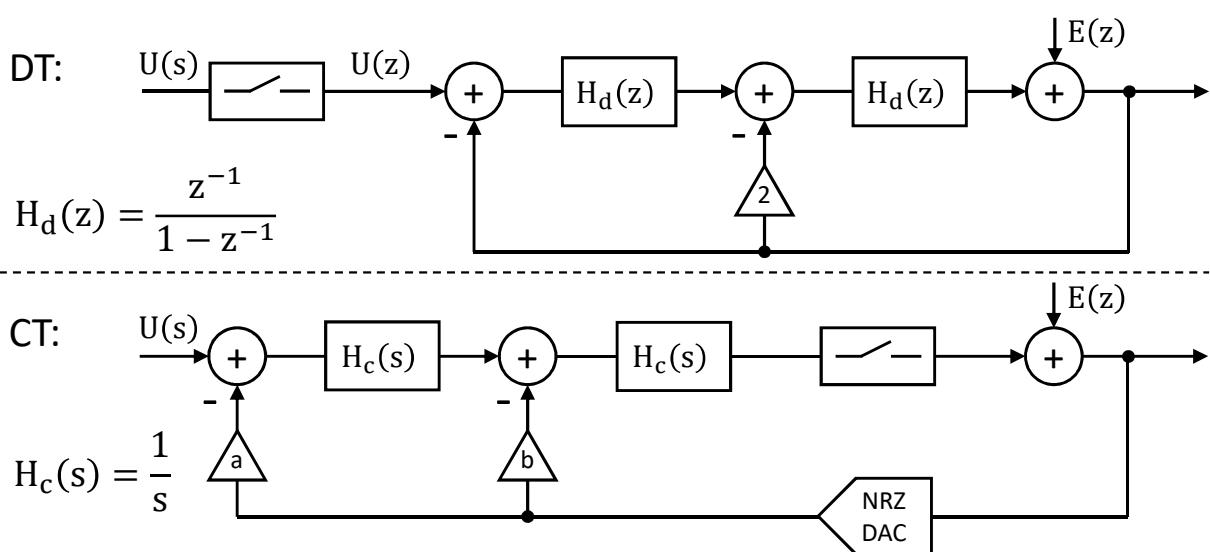
normalized integrator transfer function:  $H_c(s) = (-)\frac{1}{sRC}$

→ normalized RC constant (to T, because t was normalized to T):  $RC = 1$

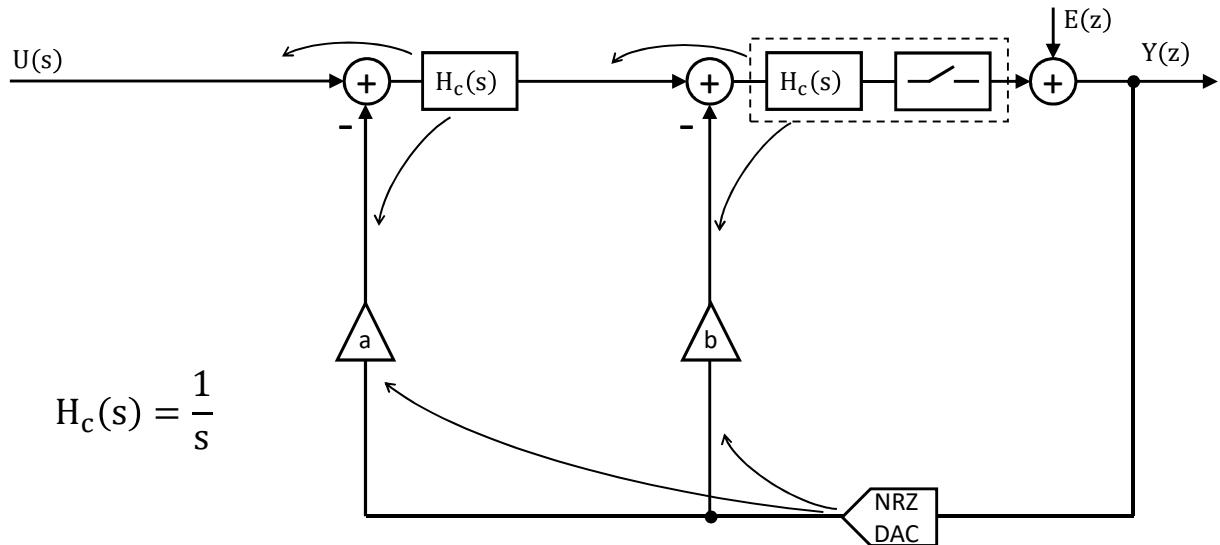
→  $RC = T = 1/f_s \rightarrow$  needs a fixed  $f_s$ , unlike DT  $\Sigma\Delta$



## 2nd Order CT $\Sigma\Delta$ Modulator



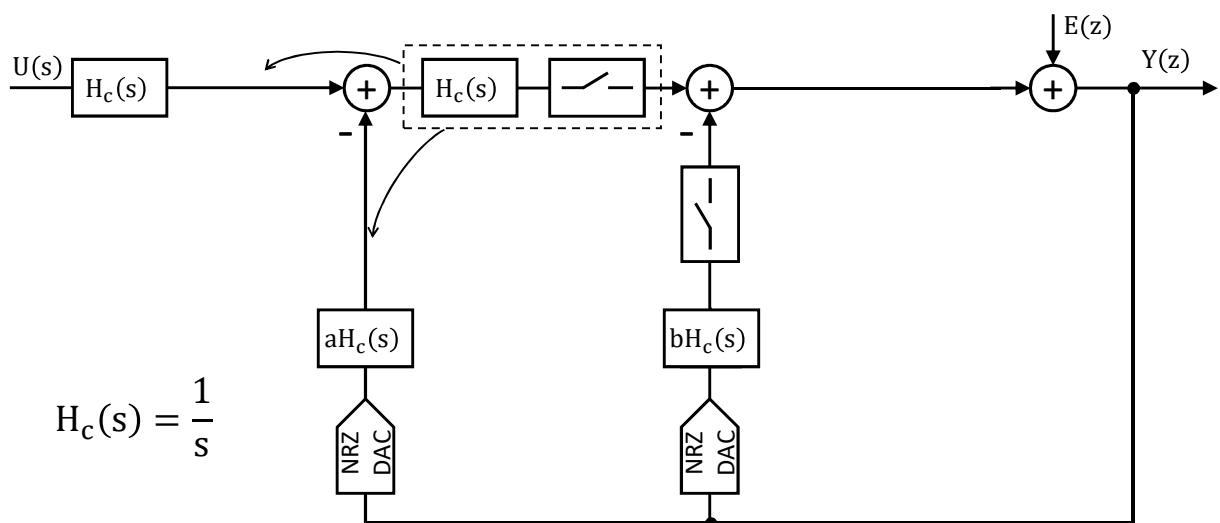
## 2nd Order CT $\Sigma\Delta$ – Equivalent Model (1)



515



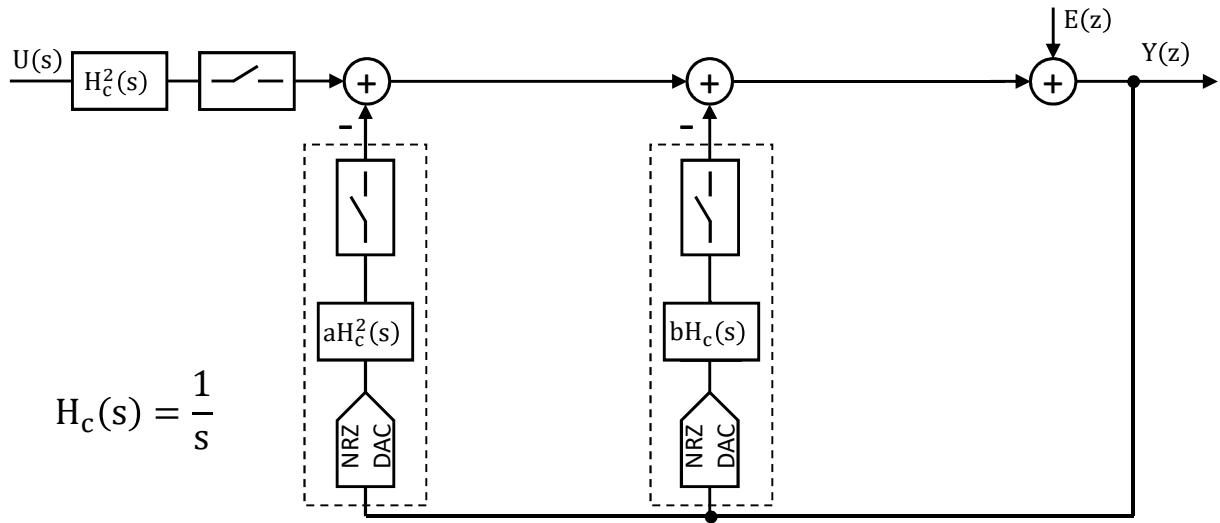
## 2nd Order CT $\Sigma\Delta$ – Equivalent Model (2)



516



## 2nd Order CT $\Sigma\Delta$ – Equivalent Model (3)

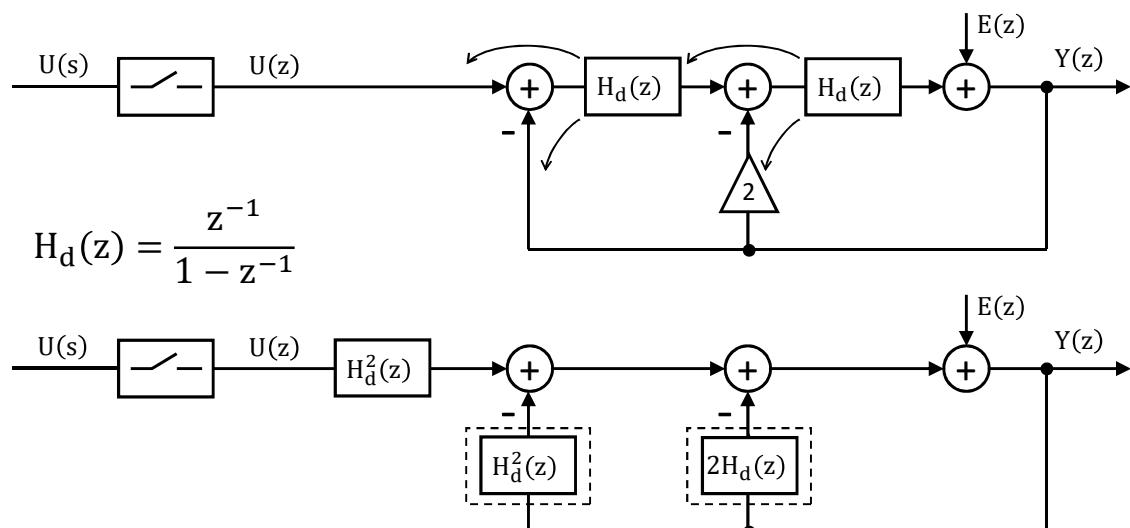


$$H_c(s) = \frac{1}{s}$$

517



## 2nd Order DT $\Sigma\Delta$ – Equivalent Model



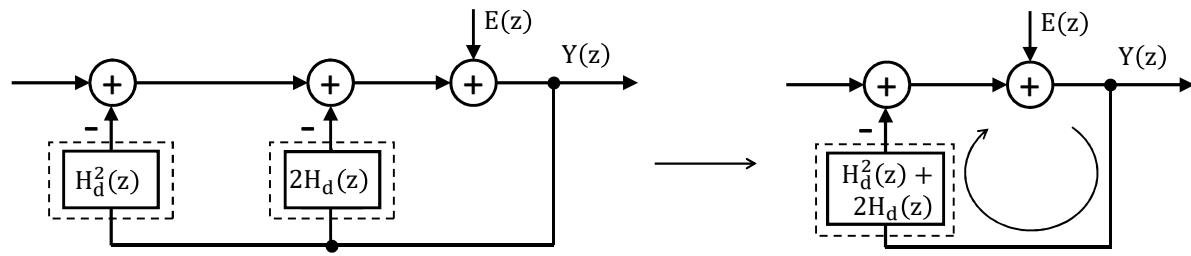
$$H_d(z) = \frac{z^{-1}}{1 - z^{-1}}$$

518



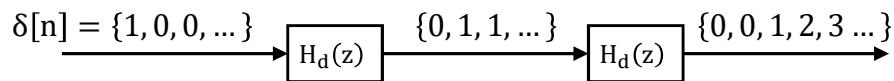
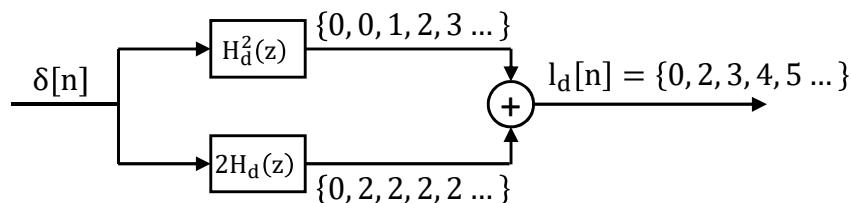
## 2nd Order DT $\Sigma\Delta$ – Loop Transfer Function

- NTF(z) =  $\frac{Y(z)}{E(z)}$  ( $U(z) = 0$ ) =  $\frac{1}{1+L(z)}$   
 $L(z)$  : loop transfer function
- 2nd order DT  $\Sigma\Delta$ :  $L_d(z) = H_d^2(z) + 2H_d(z)$



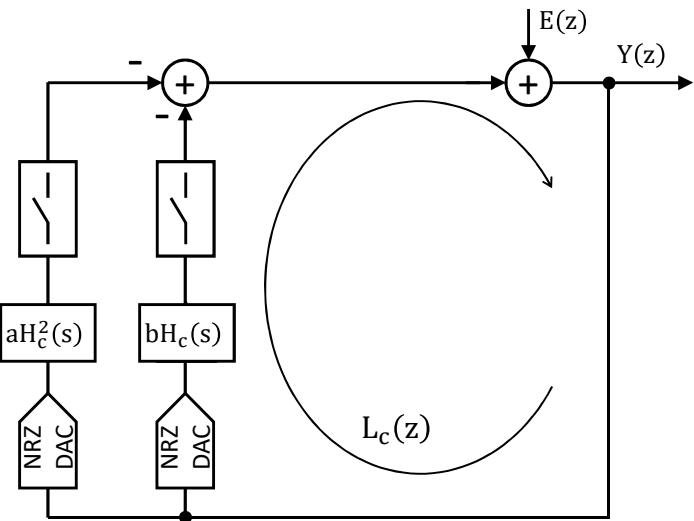
## 2nd Order DT $\Sigma\Delta$ – Loop Impulse Response

- Loop transfer function:  $L_d(z) = H_d^2(z) + 2H_d(z)$   $H_d(z) = \frac{z^{-1}}{1-z^{-1}}$



## 2nd Order CT $\Sigma\Delta$ – Loop Transfer Function

- 2nd order CT  $\Sigma\Delta$
- Loop transfer function:  $L_c(z)$   
(discrete-time function)
- Goal: find coefficients  $a, b$   
such that:  
 $L_c(z) = L_d(z)$   
(same loop transfer function)  
 $\Leftrightarrow l_c[n] = l_d[n]$   
(same loop impulse response)

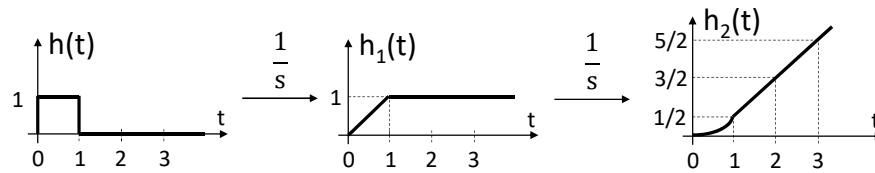


521

## 2nd Order CT $\Sigma\Delta$ – Loop Impulse Response

$$\delta[n] = \{1, 0, 0, \dots\} \rightarrow \text{NRZ DAC} \rightarrow h(t) \rightarrow \frac{a}{s^2} \rightarrow a \cdot h_2(t) \rightarrow \left\{0, \frac{1}{2}, \frac{3}{2}, \frac{5}{2}, \dots\right\}$$

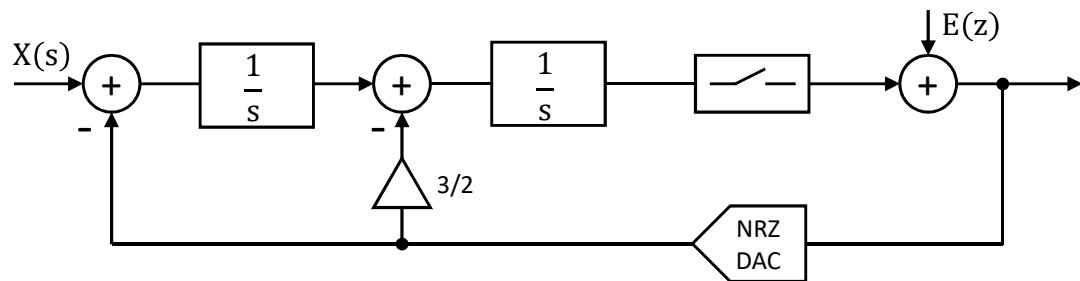
$$\delta[n] = \{1, 0, 0, \dots\} \rightarrow \text{NRZ DAC} \rightarrow h(t) \rightarrow \frac{b}{s} \rightarrow b \cdot h_1(t) \rightarrow \{0, 1, 1, 1, \dots\}$$



522

## 2nd Order CT $\Sigma\Delta$ – Loop Coefficients

- $l_c(z) = \left\{ 0, \frac{a}{2} + b, \frac{3a}{2} + b, \frac{5a}{2} + b, \dots \right\}$
- $l_d(z) = \{0, 2, 3, 4, \dots\}$
- $l_c(z) = l_d(z) \rightarrow \frac{a}{2} + b = 2, \frac{3a}{2} + b = 3$   
 $\rightarrow a = 1, b = \frac{3}{2}$

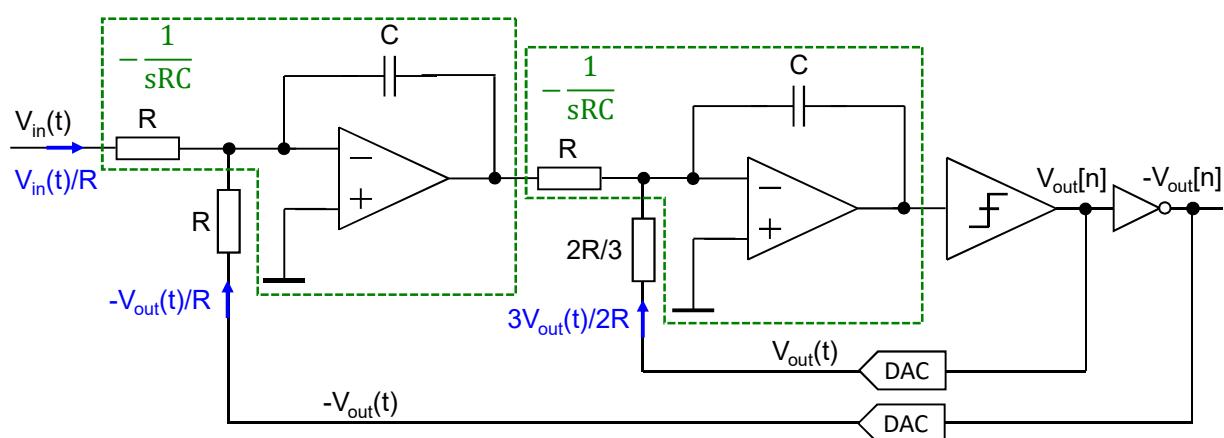


523



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## 2nd Order CT $\Sigma\Delta$ Modulator – Circuit Example



524



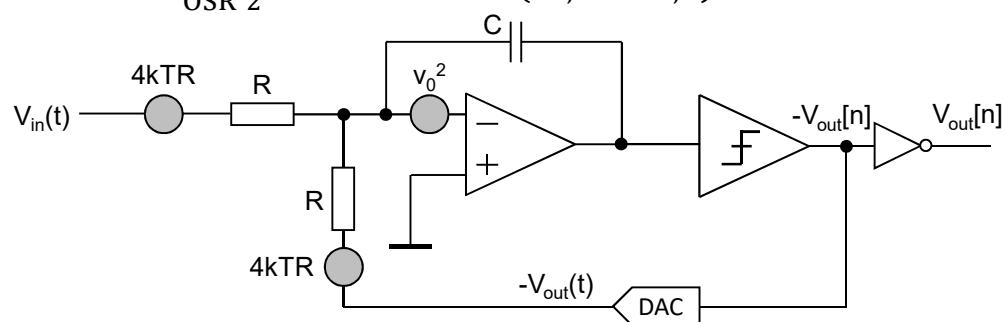
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## CT ΣΔ Modulator – Noise

- Thermal noise: usually most difficult to reduce  
(would increase power consumption significantly)  
→ often gets most of the noise budget (design decision)
- Thermal noise from:
  - resistors →  $v_{n,R}^2 \propto R \propto \frac{1}{I}$
  - amplifier → MOSFET →  $v_{n,A}^2 \propto \frac{1}{g_m} \propto \frac{1}{\sqrt{I}}$
- Noise vs. power trade-off
  - power  $\propto I$
  - noise:  $v_{n,R}^2 + v_{n,A}^2 \rightarrow I$  decrease increases  $v_{n,R}^2$  more than  $v_{n,A}^2$   
→ often more thermal noise budget for resistors than for amplifier
  - Example:  $v_{n,R}^2$  80%,  $v_{n,A}^2$  20%

## CT ΣΔ Modulator – Thermal Noise

- Thermal noise from resistors: adds to the input signal
  - power spectral density:  $v_{n,R}^2 = 4kTR + 4kTR$
- Thermal noise from amplifier:  $v_{n,A}^2 = 4v_0^2$  at the output (see appendix)
- Signal bandwidth  $f_0 = \frac{1}{OSR} \frac{f_s}{2}$  → noise power  $(v_{n,R}^2 + v_{n,A}^2)f_0$



## CT $\Sigma\Delta$ Modulator – SNR

- Signal power:  $P_S = \frac{1}{2} \left( \frac{V_{ref}}{2} \right)^2 = \frac{V_{ref}^2}{8}$
- Noise: quantization + thermal (+ other noise sources)  $\rightarrow P_N \approx P_{QN} + P_{TN}$   

$$P_{QN} = \int_{-f_0}^{f_0} S_e(f) |NTF|^2 df$$

$$P_{TN} = (v_{n,R}^2 + v_{n,A}^2) f_0 \quad f_0 = \frac{f_s}{2 \cdot OSR} \rightarrow \text{signal bandwidth}$$
- Signal-to-quantization-noise ratio:  

$$SQNR[dB] = 10 \log \left( \frac{P_S}{P_{QN}} \right) \rightarrow N_{ADC} = \frac{SQNR[dB] - 1.76}{6.02}$$
- Signal-to-noise (and distortion) ratio, effective number of bits:  

$$SN(D)R[dB] = 10 \log \left( \frac{P_S}{P_N + (P_{harmonics})} \right) \rightarrow ENOB = \frac{SN(D)R[dB] - 1.76}{6.02}$$

## Exercise 10

A second-order continuous-time  $\Sigma\Delta$  is given with OSR=96 and sampling frequency  $f_s=1\text{MHz}$ . The modulator uses a 1-bit quantizer. The reference voltage is  $V_{ref}=1.6\text{V}$  and the supply rails are  $V_{ref}/2$  and  $-V_{ref}/2$ .

- Calculate the number of bits  $N_{ADC}$  achieved with the given OSR.
- Calculate the maximum input resistor value such that  $ENOB=N_{ADC}-1$ , assuming that the thermal noise of the resistors is 80% of the total thermal noise.  
Neglect other noise sources (e.g. flicker noise) and harmonic distortion.
- Size the feedback capacitor of the integrator.

## Exercise 10 – Solution



## Exercise 10 – Solution



## Continuous-Time vs. Discrete-Time $\Sigma\Delta$ ADC

	Discrete-time	Continuous-time
Anti-aliasing filter (AAF)	Explicit AAF required	Implicit filtering by the integrator
Sampling	At input → low jitter and full linearity required for sampler	At comparator, i.e. within $\Sigma\Delta$ loop → sampling error: noise-shaped
Sampling circuit	Switched-capacitor integrator → implicit sampling	Clocked comparator → implicit sampling
Maximum frequency and opamp bandwidth	All transients must settle within half of clock cycle, quickly changing pulses everywhere in the circuit → high bandwidth requirements limit maximum frequency	Continuous-time waveforms → 5-10x relaxed bandwidth requirements → higher clock frequency or lower power possible

## Continuous-Time vs. Discrete-Time $\Sigma\Delta$ ADC

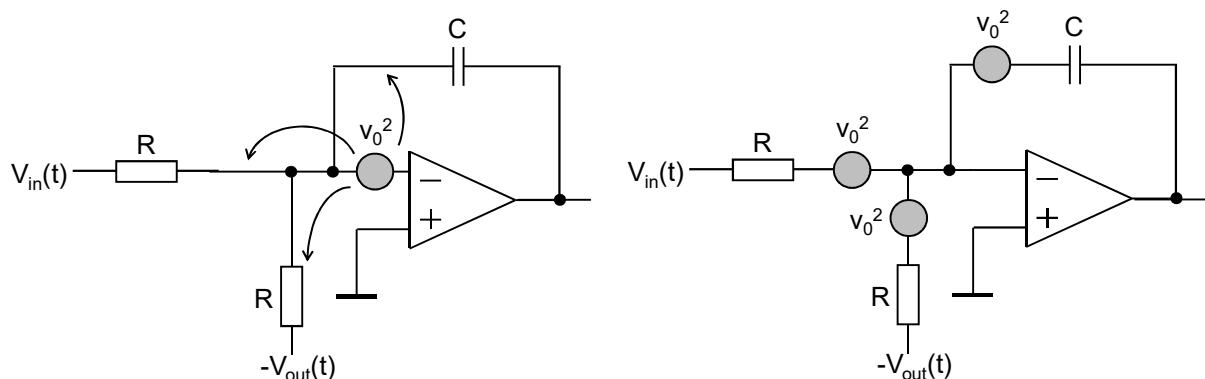
	Discrete-time	Continuous-time
Jitter	Only critical for sampler, but not for the rest of the $\Sigma\Delta$ modulator	Very sensitive to timing variations of clock
Sampling error	Added directly to the modulator input	Noise-shaped
Process variation	Filter transfer function based on capacitor ratio → very robust; works when changing clock frequency	Filter transfer function depends on RC constant → very sensitive to variations, requires trimming; doesn't work when changing clock frequency
Noise	Switching generates noise	Few switches (DACs), reduced supply and ground noise
Loop delay	Not an issue	Very sensitive to loop delay

## CT vs. DT $\Sigma\Delta$ – Common Applications

- Discrete-time  $\Sigma\Delta$ : more robust  
Higher resolution (can reach 16-20, up to 32 bits)
- Continuous-time  $\Sigma\Delta$ : can operate faster  
Higher bandwidth (typically 10-100 MHz)  
Lower resolution attainable (typically 10-14 bits)
- Application requirements:  
Critical accuracy → choose discrete-time  
High bandwidth or low power requirement → choose continuous-time

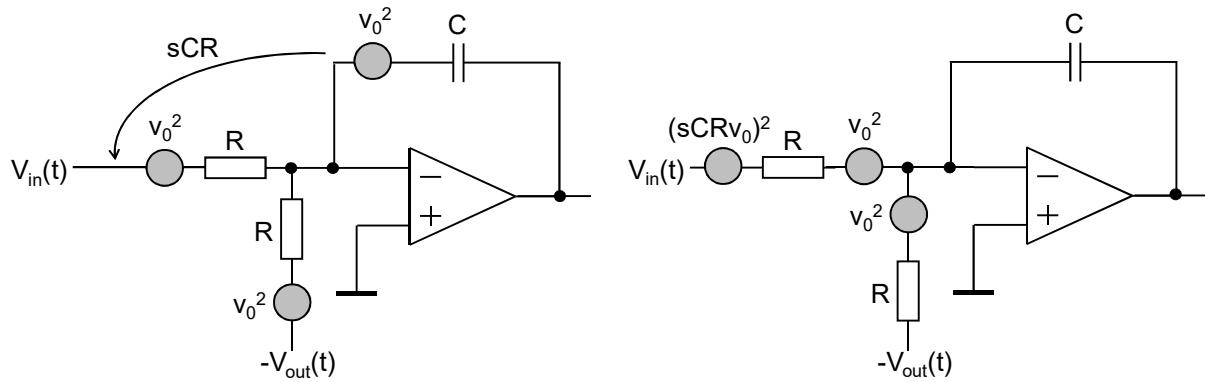
## Appendix – CT $\Sigma\Delta$ Amplifier Thermal Noise

- Thermal noise at amplifier input:  $v_0^2$   
→ linear transformation: distribute the source to the input branches



## Appendix – CT $\Sigma\Delta$ Amplifier Thermal Noise

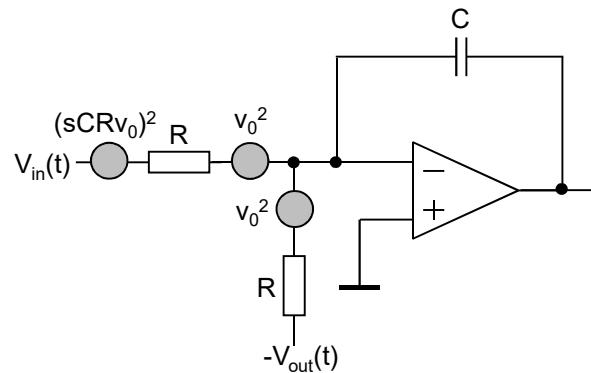
- Source on feedback: directly adds to the output  
→ linear transformation: refer it to the input divided by the closed-loop integrator gain,  $1/(sCR)$



## Appendix – CT $\Sigma\Delta$ Amplifier Thermal Noise

- Total input-referred noise: superposition of input noise sources
- Input sources: 100% correlated (derived from the same original source)
  - superpose noise voltage, not power
  - $v_{n,A} = v_0 + v_0 + sCRv_0$
  - $v_{n,A}^2 = \left(2v_0 + \frac{j\omega}{f_s}v_0\right)^2$

$$RC = T = \frac{1}{f_s}$$



## Appendix – CT $\Sigma\Delta$ Amplifier Thermal Noise

- Input-referred noise:  $v_{n,A}^2 = v_0^2 \left( 2 + \frac{j\omega}{f_s} \right)^2$   
 → appears at modulator output:  
 - with STF=1  
 - limited to signal band  $f_0 = f_s / (2 \cdot \text{OSR}) \rightarrow \omega \ll f_s \rightarrow v_{n,A}^2 \cong 4v_0^2$

