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# **Design of a 12-bit 200-MSps SAR Analog-to-Digital converter**

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## **Kungliga Tekniska Högskolan**

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School of Electrical Engineering and Computer Science  
Master of Science – Embedded Systems



# **Design of a 12-bit 200-MSps SAR Analog-to-Digital converter**

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# Abstract

The Successive Approximation (SAR) Analog-to-Digital converter is one of the most energy-efficient A/D converter. In this thesis, the development of a SAR ADC in a 28-nm CMOS technology based on charge redistribution is presented.

The implemented SAR ADC uses a switching procedure based on a modified version of the monotonic switching algorithm to reduce the switching energy and area of the DAC. The DAC is a binary-weighted array of unit capacitors. A unit custom capacitor has been designed with a value of 0.8 fF to reduce the DAC energy consumption. Two comparators have been implemented, a dynamic comparator and a static comparator. The dynamic implementation allows to obtain better performance. Therefore, the dynamic comparator is chosen for the SAR ADC. The sampling switches are bootstrapped to reduce the non-linearity introduced when the input signal is sampled. The SAR operations are controlled by an asynchronous logic implemented as a behavioural model in Verilog-A.

The effect of the designed circuits on the linearity of the converter is assessed with the integral non-linearity (INL) and differential non-linearity (DNL). Moreover, the performance of the ADC are assessed in terms of signal-to-noise-and-distortion ratio (SNDR). The co-simulation of Verilog-A behavioural models with circuit schematics allowed to evaluate the effect of each block on the overall performance of the ADC. The co-simulations show that the ADC is able to achieve an ENOB of 10.9 at a sampling rate of 200 MSps with a power consumption of 2.83 mW. The resulting FoM is 7.4 fJ/conv-step.

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# Sammanfattning

SAR (Analog-Digital-omvandlaren) är en av de mest energieffektiva omvandlare. I den här avhandlingen är utvecklingen av en SAR ADC i en 28-nm CMOS-teknik baserad på laddning omfördelning presenteras.

Den implementerade SAR ADC använder en omkopplingsprocedur baserad på en modifierad version av den monotoniska omkopplingsalgoritmen för att reducera omkopplingsenergin och DAC-området. DAC är en binärviktad matris med enhetskondensatorer. En anpassad kondensator för enheten har utformats med ett värde av 0,8 fF för att minska DAC-energiförbrukningen. Två komparatorer har implementerats, en dynamisk komparator och en statisk komparator. Den dynamiska implementeringen gör det möjligt att få bättre prestanda. Därför väljs den dynamiska komparatoren SAR ADC. Provtagningsomkopplarna startas upp för att minska icke-lineariteten introduceras när insignalen sampelas. SAR-operationerna styrs av en asynkron logik implementerad som en beteendemodell i Verilog-A.

Effekten av de designade kretsarna på konverterarens linearitet bedöms med integralen icke-linearitet (INL) och differentiell icke-linearitet (DNL). Dessutom är ADC:s prestanda bedömdes i termer av signal-till-brus-och-distorsionsförhållande (SNDR). Samsimulering av Verilog-A beteendemodeller och scheman tillåts utvärdera effekten av varje block på prestandan hos ADC. Omvandlaren kan uppnå en ENOB på 10,9 med en samplingshastighet på 200 MSps, vilket resulterar i en FoM eller 7,4 fJ / konv-steg.

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# Preface

I want to thank prof. Bonfanti and prof. Samori for their guidance during this project. When I first started, I was a little bit lost in the complexities of the circuits presented in this thesis. However, they taught me with great patience how to tackle the challenging problems a designer encounters during the design of ICs. The methods and the mindset needed to design integrated circuits I learned from them will remain with me for the rest of my life and for that I am grateful.

I want to thank the people I met in the laboratory for the fruitful discussions during my brief stay: Simonino, Bucc and Bibo. Last but not least, Luca Bertulessi and Angelo Parisi, which have always found the time to help me and to teach me how to smartly solve apparently unsolvable problems. Among all of the many tasks they had to carry on, they always found the time for helping me and supporting me. Unfortunately, this project was stopped right at the most exciting time. However, it is possible we will work again together, you never know.

This thesis concludes the double degree programme between Politecnico di Milano and the Royal Institute of Technology (KTH), Stockholm. I want to thank prof. Ana Rusu for being my examiner, for pushing me to write a high-quality report and for her support during this project. Moreover, I want to thank KTH for letting me have the possibility to study there and be part of the great community it hosts. It was fun and exciting to study and to live in Stockholm. I met a lot of people from all around the world that enriched me with their life experience.

Also an important thanks goes to all of my friends. Thank you for the beautiful days passed together during the last years. Finally, I want to thank my parents, my sister and the rest of my family. They have always been with me, no matter the difficulties I encountered during my life. I would not be where I am today without them.

Luca Ricci

Milano, 17/08/2020



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# Introduction

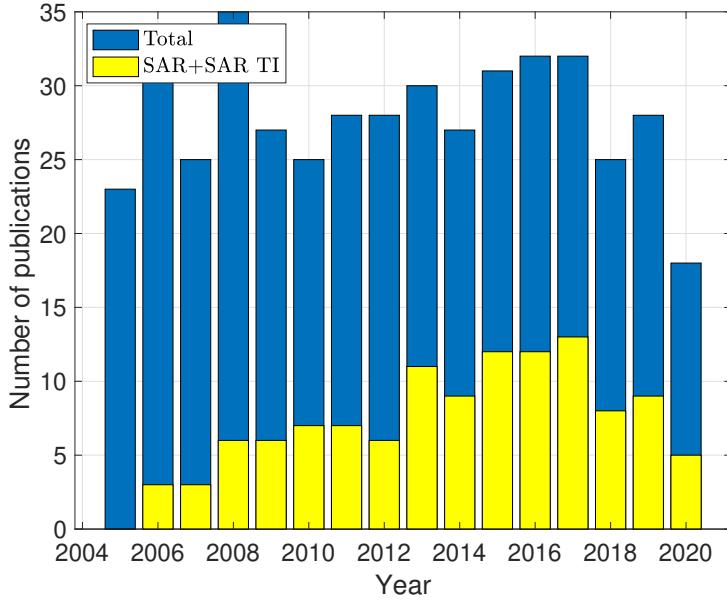
Integrated circuits (IC) are present in almost all the objects we interact with everyday. One of the factors that contributed to the pervasiveness of ICs in our daily lives is the improvement of their fabrication process.

The metal-oxide-silicon field-effect transistor (MOSFET) is one of the devices at the basis of today's circuits. The MOSFET was invented by K. Dawon and J. Atalla in 1959 at the Bell Labs[1] and its working principle was first proposed in 1925 by J. E. Lilienfeld[2]. Then, J. Kilby developed the first integrated circuit in 1958, but the manufacturing process of transistors was still not ready to produce reliable devices. There was a leap forward when F. Faggin developed the self-aligned gate technology, allowing the production of reliable MOSFETs. This achievement paved the way to the development of the microprocessors in the seventies and eighties. These huge efforts behind the advancement of the manufacturing process were led by cost reductions, performance improvements and the possibility to integrate more complex functions in the same area.

In the last twenty years, the performance obtained by aggressively scaling the transistor dimensions and supply voltages slowed down due to the exorbitant costs involved in the construction of foundries and the physical limits of the transistor dimensions. On the one hand, digital circuits benefit from scaling transistor dimensions and supply voltages in terms of power dissipation, speed and area. On the other hand, short-channel effects and the low supply voltage make the design of analog circuits more challenging. Short-channel effects, like drain-induced barrier lowering or leakage currents, affect also digital electronics but the performance improvement brought by new technology nodes more than offset these issues. The flexibility, the development of systematic design procedures and the possibility to develop really complex functions are features of digital electronics not shared by analog circuits. Therefore, circuit designers moved as much functionality as possible to the digital domain. However, some tasks performed by analog circuits cannot be carried out by digital circuits, like signal filtering or amplification on the front-end electronics of a signal acquisition chain. Additionally, there is also the need to move from the analog domain to the digital domain and vice versa. The circuits that perform this function are called data converters. Data converters can be divided in two kinds: digital-to-analog converters (DAC) and analog-to-digital converters (ADC). The former takes a digital word at its input converting it into an analog signal, whereas the latter performs the opposite operation. This work aims to design a 12-bit 200-MSps SAR ADC in a 28-nm CMOS process.

## 1.1 Objectives and motivations

The SAR ADC has been extensively used in the past and in the last decade it has received a renovated interest. More than 20% of the total number of ADCs published at the ISSCC and VLSIC in the last fifteen years are SAR ADCs as it is shown in Figure 1.1. This trend can be understood considering the



**Figure 1.1:** Number of ADC publications between 2005 and 2020 at the ISSCC and VLSIC. Data from [3].

features offered by a SAR ADC. From a system perspective, the structure is simple, namely a DAC, a comparator and a control logic. Furthermore, most of the circuitry is digital. Hence, smaller power consumption and faster conversion in new technology nodes. Therefore, this kind of data converter is convenient when low-power consumption is needed with sampling frequencies up to hundreds of MSps. For larger sampling frequencies, the technique of time-interleaving (TI) is used (see next chapter).

Important performance metrics of an ADC are the effective number of bits (ENOB) and the Figure-of-Merit (FoM). The ENOB is a measure of the dynamic performance of a converter quantifying the effective resolution of the ADC taking into account noise and distortion. It is defined as [4]:

$$ENOB = \frac{SNDR - 1.76}{6.02}, \quad (1.1)$$

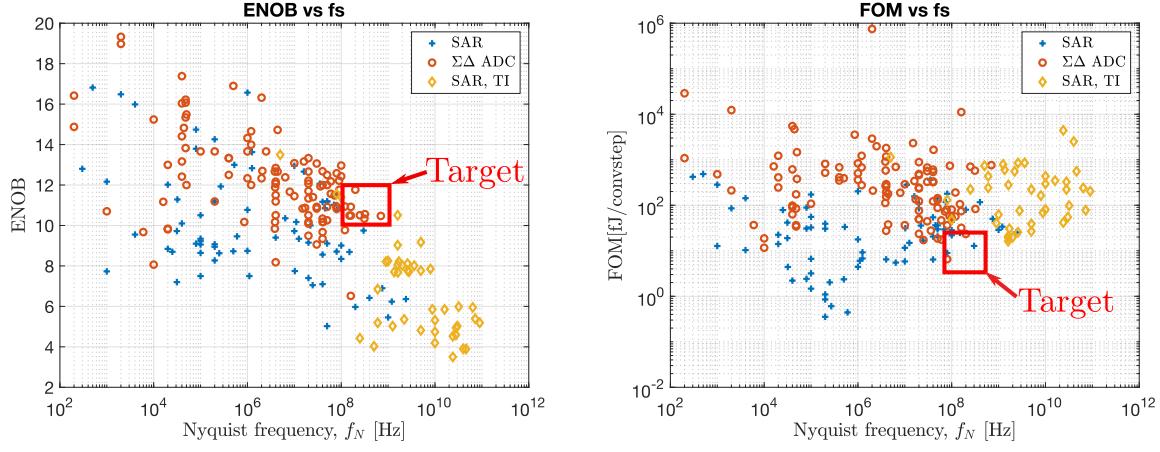
where  $SNDR$  is the signal-to-noise-and-distortion ratio. The  $SNDR$  is typically expressed in decibel and it is computed as the ratio between the signal power and the noise power summed with the power of the harmonics generated by an input sine wave. The FoM is defined as[4]:

$$FoM = \frac{P_{tot}}{2^{ENOB} f_s} \left[ \frac{J}{conv-step} \right], \quad (1.2)$$

where  $P_{tot}$  is the total power of the converter and  $f_s$  its sampling frequency. This parameter gives a measure of the power efficiency of converter.

The goal of this thesis is to design of a 12-bit 200-MSps SAR ADC in a 28-nm CMOS technology node for 5G applications. In the future the converter will be employed as a channel of a 1-GSpss TI ADC employing 5 stages. In Figure 1.2, there is a summary of ADCs presented at the ISSCC and VLSIC between 2005 and 2020. The expected performances are a FoM around tens of fJ/conv-step and an ENOB of approximately 10 as highlighted in the red boxes in Figure 1.2.

The structure of the report is the following. A background about ADCs is given in Chapter 2. In the background section, there is a brief introduction on different kinds of ADCs to let the reader understand the advantages of the SAR ADC with respect to other ADC architectures. Then, the SAR ADC architecture is presented with the description of popular architectures proposed in literature. The implementation of the main blocks (sampling circuit, DAC, comparator and logic) is presented in Chapter 3.



**Figure 1.2:** Reported FoM and ENOB vs Nyquist frequency at the ISSCC and VLSIC. Data from [3].

The sampling circuit, DAC and comparator are implemented at transistor level, whereas the control logic is implemented with a block modelled in Verilog-A. The sampling circuit employs the bootstrap technique to improve the linearity of the circuit. The DAC is implemented with a custom-designed capacitor to reduce its area and power dissipation. Two comparators were implemented. First a static comparator and then a dynamic comparator. The static comparator dissipates more power than the dynamic version, therefore in the end a dynamic comparator was selected. Moreover, the ADC has better performance with the designed dynamic comparator. Finally, the control logic circuit is asynchronous to avoid the design of an internal clock generator and its effects in terms of power consumption. The results and discussions are given in Chapter 4. In the result section, the effects of each implemented block on the linearity of the converter is assessed with the integral non-linearity (INL), differential non-linearity (DNL) and SNDR. Finally, the report concludes in Chapter 5 suggesting future possible developments and summarizing the results presented in this thesis.



# Chapter 2

## Background

In the next sections, there is a brief summary (based on [4, 5, 6]) of the most popular ADC architectures to understand the advantages and limits of the converter presented in this thesis, the successive approximation register (SAR) ADC. Then, the SAR ADC architecture is described in detail with popular implementations found in literature. The reader already familiar with analog-to-digital converters can directly start reading from Section 2.2.

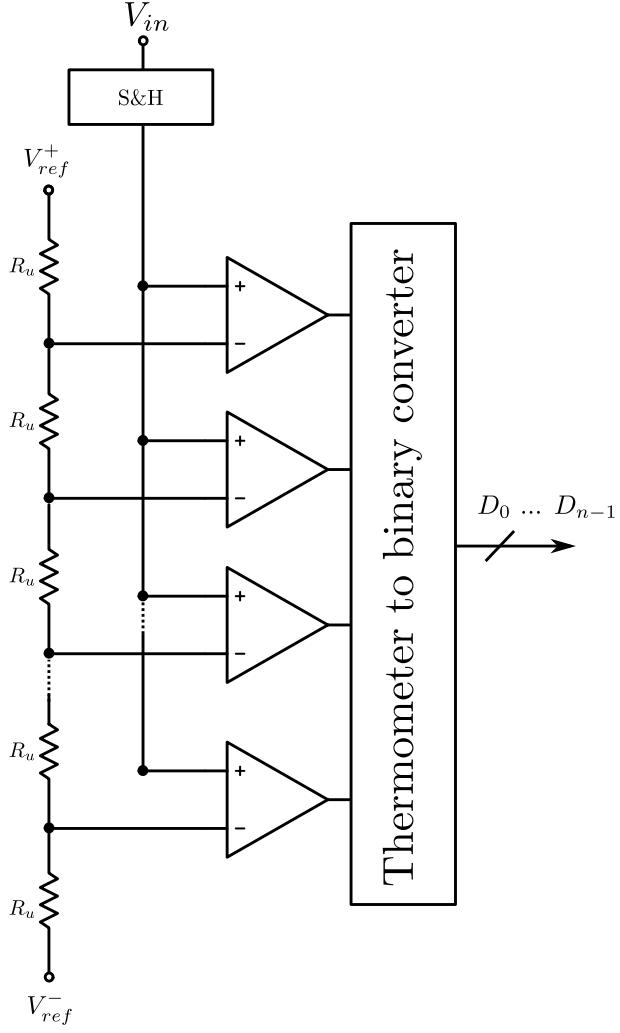
### 2.1 Analog-to-digital converters

Various types of ADCs have been conceived to achieve analog-to-digital conversion. The selection of the ADC for a specific circuit is based on the requirements and application of that design. Important parameters are power, area, resolution and speed. In the following subsections, a small review of the most important architectures of ADCs are discussed to give the reader a quick refresh on the different ways to achieve analog-to-digital conversion. For an exhaustive treatment the interested reader can refer to the references.

#### 2.1.1 Flash ADCs

The conversion of an analog signal into a digital code consists in determining the quantization interval the input signal belongs to. A flash ADC performs this function in a straightforward manner comparing the input signal with reference values corresponding to the edges of each quantization interval[4]. The comparison gives the threshold over which the input is larger. Let us look at Figure 2.1 to understand this concept. Considering an  $n$ -bit ADC, there are  $2^n$  regions dividing the full-scale range of the converter and  $2^n - 1$  transition points. Therefore, it is necessary to have  $2^n - 1$  comparators to perform the comparisons. The name *flash* ADC stems from the way the conversion is carried out. All the comparators are activated in parallel synchronized by a clock signal, thus the output code is generated in one clock cycle. One input of the comparator receives the signal to convert while the other terminal is connected to a reference voltage generated by a resistive divider. The outputs of the comparators form a thermometric code that can be translated into a digital word.

Flash ADCs are mostly employed for high-speed (GHz) converters since the conversion time is equivalent to a clock period. However, they are limited by various issues when the resolution becomes larger than 8 bits. The number of comparators grows exponentially with the number of bits. Area and power consumption are, thus, doubled for each additional bit. Moreover, the resistance value of the unit resistance of the resistive divider is reduced to a very low value. For this reason, the output impedance of the reference voltage driving the divider needs to have a very low value in all the frequencies of operation[4]. Furthermore, the large numbers of comparators adds substantial input capacitance to the



**Figure 2.1:** Architecture of the full-flash ADC, based on [5].

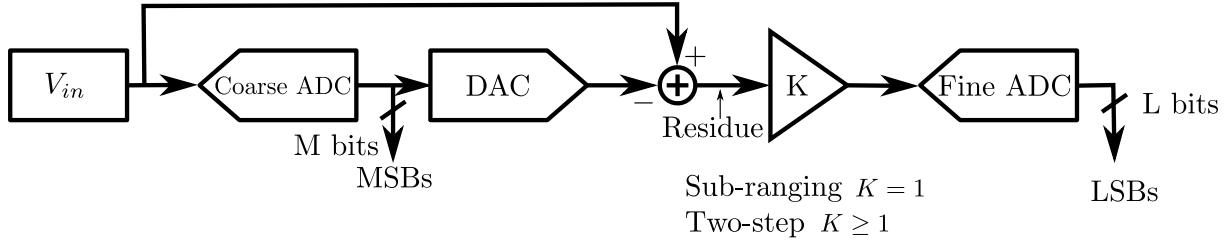
sample and hold (S&H) circuit. These parasitics are also voltage dependent, introducing non-linearity.

In few words, this architecture is a good choice for high-speed (larger than hundreds of MHz) applications and low resolutions (lower than 8 bits).

### 2.1.2 Two-step ADCs

Two-step ADCs (Figure 2.2) have been developed to manage the large power dissipation and area of flash ADCs[5]. The conversion of an  $n$ -bit ADC is divided between two converters of L and M bits, such that the total resolution of the converter is  $n=M+L$ . They work sequentially converting first the MSBs with a coarse ADC and then the remaining LSBs with a fine ADC. After the conversion of the MSBs, the signal is converted back to the analog domain by a DAC and its output is subtracted to the analog input generating the residue. The residue is fed to the fine ADC to obtain the remaining L bits. Finally, a logic circuit takes the MSBs and LSBs and assembles the  $n$ -bit digital word.

Two-step ADCs require about two or three clock periods to convert the input sample, with a smaller number of comparators with respect to the flash architecture. Therefore, the power consumption and silicon area are reduced with respect to a flash ADC at a reduced conversion rate. Additionally, the parasitic capacitive load on the S&H is reduced with respect to a flash ADC. Looking closely to the block diagram in Figure 2.2, it is possible to observe an inherent drawback of this kind of ADC. There is a latency between the MSBs and LSBs since the latter are generated after the residue is available.

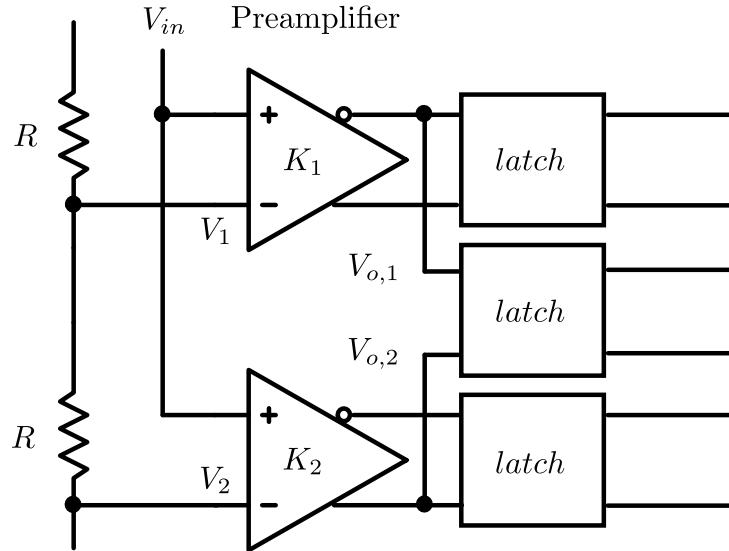


**Figure 2.2:** Block diagram of a two-step ADC, based on [5].

Another important issue is the linearity. The DAC needs to have a resolution larger than  $M$  bits in real designs not to affect linearity of the converter. It is also possible that the residue after the amplification  $K$  will be out of the range of the ADC, thus introducing errors in the conversion[5].

### 2.1.3 Interpolating and folding ADCs

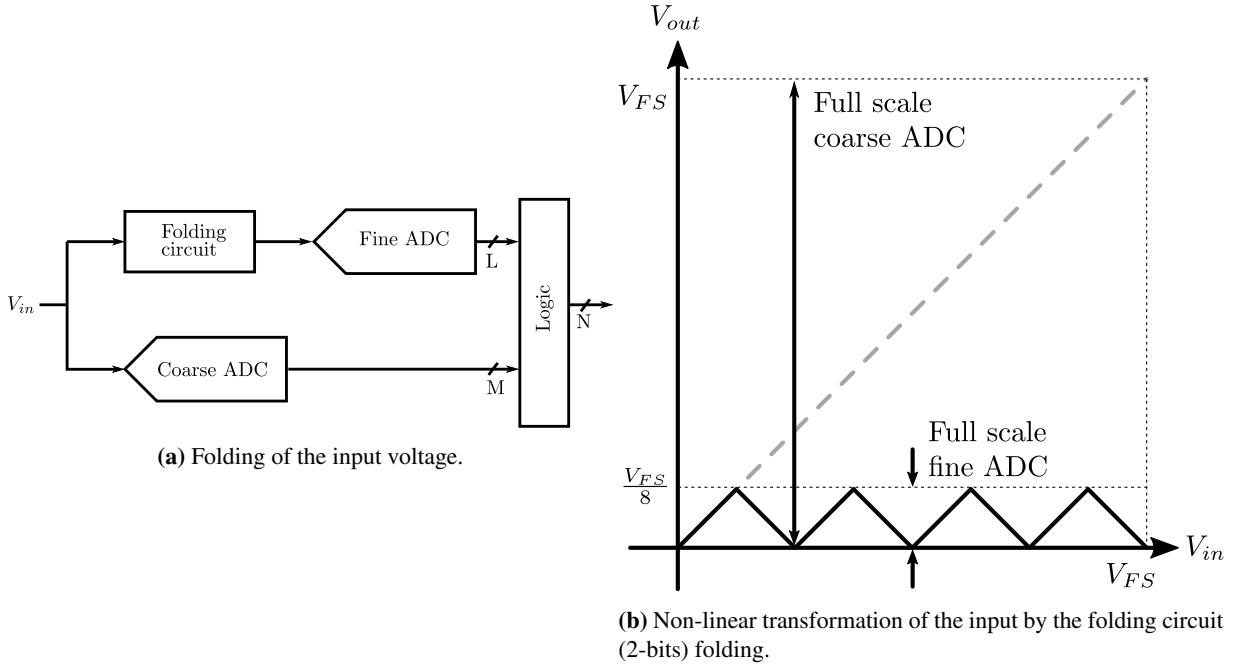
A problem of the flash converter is the large number of comparators that grows exponentially with the number of bits. A possible way to reduce the number of comparators is interpolation. Interpolation consists in generating an intermediate voltage value between two consecutive voltages. An example is shown in Figure 2.3. The outputs of the preamplifiers are connected to an intermediate latch, in such a way that the input signal of the intermediate latch is compared to the average between  $V_1$  and  $V_2$ . Indeed, with a simple analysis of the output voltages of the preamplifiers, it is possible to show that the polarity of  $V_{o,1} - V_{o,2}$  is the same as that of  $V_{in} - \frac{V_1+V_2}{2}$ [6]. This effectively means that the resolution



**Figure 2.3:** Interpolation in a flash ADC[6].

of the converter is doubled, because there is one additional intermediate reference voltage which the input signal can be compared to between two preamplifiers. Interpolation helps reduce the number of preamplifiers with respect to a conventional flash implementation, whereas the number of latches remains the same. The area and power consumption of the comparators is reduced by a factor two. Moreover, having less comparators reduces the capacitive load on the S&H circuit. Therefore, it is possible to design a converter with the same one-clock conversion style as the flash ADC with smaller area and power consumption or smaller area, same power consumption, but higher speed.

The folding ADC exploits the concept of folding and its structure is shown in Figure 2.4a. A folding circuit implements a non-linear transformation of the input voltage as in Figure 2.4b. The output range



**Figure 2.4:** Folding circuit (a) and transformation of the input signal by a 2-bit folding circuit, based on [5].

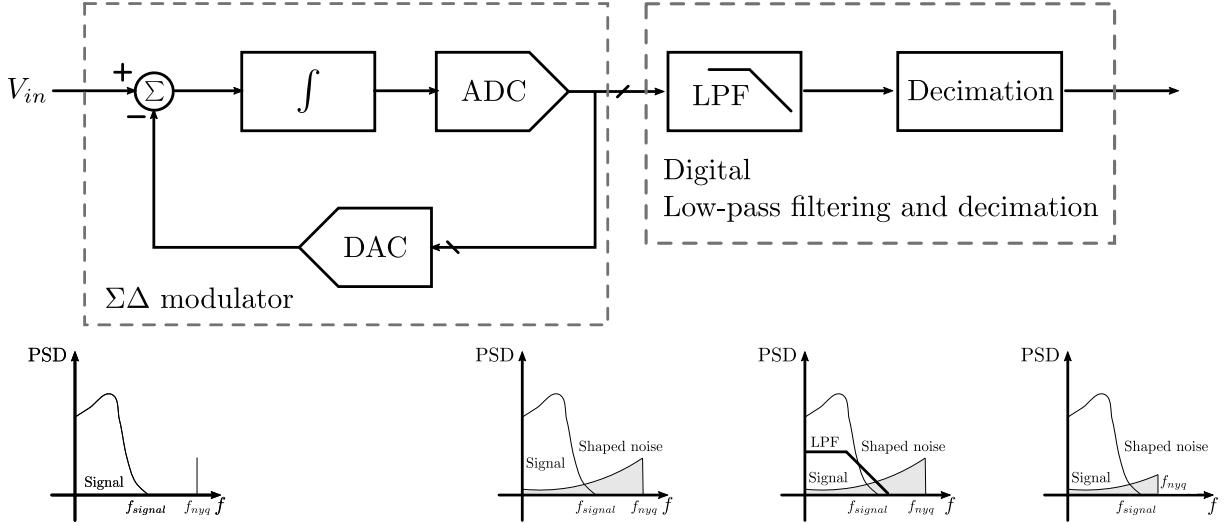
is reduced according to the number of foldings the input signal is subjected to. For example, the peak amplitude is reduced eight times if the folding factor is three. At this point, it is necessary to know in which segment the input is and together with the quantization of the segment we can achieve AD conversion. Practically, a coarse ADC of  $M$  bits determines the region the input is in and a fine ADC resolves the other  $L$  bits, such that the total number of bits is  $N=L+M$ . A problem with folding is to generate sharp transitions and it cannot be achieved by real circuits since the response of MOS or bipolar transistors is not sharp, resulting in non-linearity[4]. Plus, the bandwidth and slew-rate of the folder can limit the performance of the ADC at high conversion rates.

Folding and interpolation can be both used to improve power and area efficiency. However, the non-linearity of folding circuits and limited bandwidth of pre-amplifiers need to be taken into account in the design of high-resolution and high-speed converters.

#### 2.1.4 $\Sigma\Delta$ ADCs

In some applications, such as audio, telecommunication and instrumentation devices, the resolution required by the ADC in the signal acquisition chain can reach up to 24 bits. In these cases, the sampling frequency is usually low-medium from tens of Hz to hundreds of KSps[7].  $\Sigma\Delta$  ADCs are able to meet these requirement in terms of resolution and sampling rates. Conceptually, a  $\Sigma\Delta$  ADC exploits oversampling, noise-shaping and digital filtering to reduce the quantization noise present in the signal bandwidth.

Oversampling means to sample the input signal at a rate much higher than the Nyquist limit, i.e. two times the bandwidth of the input signal. The quantization noise can be considered as a white noise added to the signal by the converter and its power is  $\frac{LSB^2}{\sqrt{12}}$  [4]. The power spectral density (PSD) of the quantization noise extends from DC to half of the sampling frequency. Therefore, the higher the sampling frequency the lower the noise in the band of the signal, since the total noise power must be constant. A smart way to convert the signal is, then, to convert it at a high sampling rate, filter it with a low-pass filter and then change the sampling rate of the output data back to the Nyquist criterion through decimation[9]. The effective result of this conversion will be an output signal with lower quantization noise the more the signal is oversampled. It is possible to further reduce the noise in the bandwidth of interest by manipulating the spectrum of the quantization noise. This process is known as noise-shaping,



**Figure 2.5:** ΣΔ ADC with the spectrum of the signal during the conversion, based on [8].

because the PSD is *shaped*, moving low-frequency noise components to high frequencies. Noise-shaping can be achieved through ΣΔ modulation. The structure of a ΣΔ ADC is shown in Figure 2.5 together with the spectrum of the noise and the signal during the conversion. The ΣΔ modulator is formed by an integrator driven by the difference between the input signal and the output of the DAC. The output of the integrator is converted by an ADC and then reconverted into an analog signal by the DAC. The DAC and the ADC can be 1-bit converters, i.e. a switch and a comparator, respectively, or multi-bit converters. Moreover, it is possible to have more than one integration in the loop. The limitation for the use of multi-bit converters in the modulator is posed by the DAC linearity, whereas the loop stability is difficult to achieve with more than one integration[8]. In the case of a 1-bit DAC and a 1-bit ADC, the output of the modulator will be a stream of zeros and ones. The information about the input signal is in the number of ones and zeros. Without entering the mathematical details, the ΣΔ modulator acts as a low-pass filter for the signal, while as a high-pass filter for the noise[9]. Then, the digital low-pass filter makes an average of the modulator output and the decimator reduces the data rate of the bit stream, resulting in an increased number of bits at a lower rate (typically Nyquist).

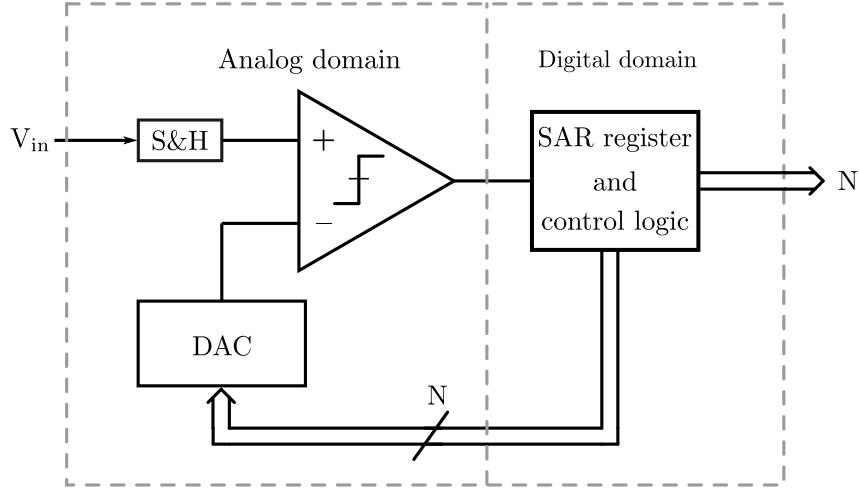
An important advantage of this kind of ADC is that the filtering of the data-stream coming from the ΣΔ modulator is performed by a digital filter. Thus, it is possible to achieve high roll-off and to have more flexibility in the design of the filter. For example, it is possible to have rejection of specific tones, like 50-60 Hz tones coming from electrical power lines[8]. In conclusion, ΣΔ ADCs are the right candidates for high resolution (larger than 12 bits) at low-medium sampling frequency (tens of Hz to hundreds of kHz).

### 2.1.5 SAR ADCs

Another way to convert an analog signal into a digital code can be carried out implementing an algorithm whose first implementations in electronic circuits can be traced back in the late forties at the Bell Labs[10]: the successive approximation (SA) algorithm. The SAR ADC known today as the charge redistribution (CR) SAR ADC was first proposed in 1975 by J.L. McCreary and P.R. Gray at University of California, Berkley in [11].

The basic building blocks of a SAR ADC are a comparator, a sample-and-hold (S&H) circuit, a DAC, a control logic and registers as shown in Figure 2.6.

The SAR ADC working principle is based on a binary-search algorithm. The conversion takes place over the course of multiple clock cycles. At the beginning of the conversion, the input voltage is sampled. The S&H function is integrated in the DAC almost in all kinds of SAR ADCs. Then, the comparator

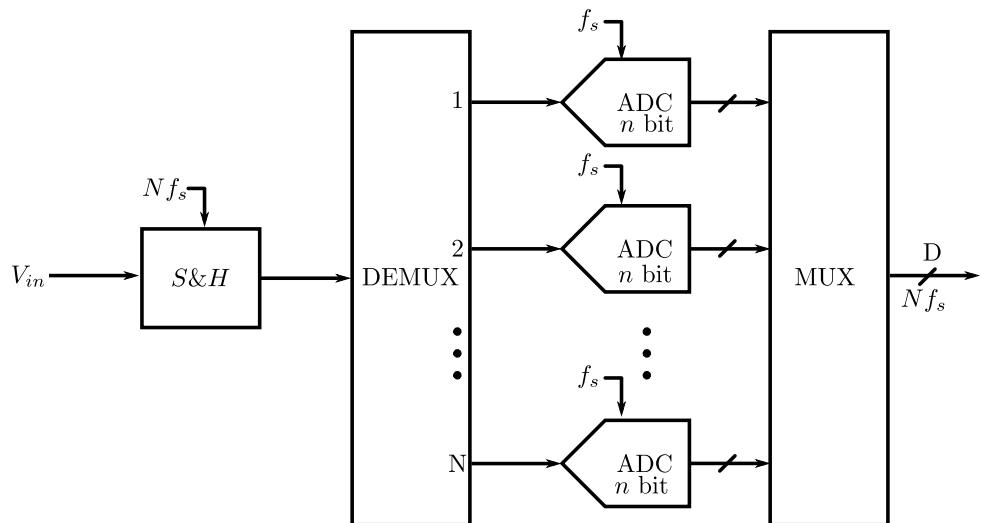


**Figure 2.6:** Basic block diagram of a SAR ADC, based on [4].

compares the sampled voltage and the output voltage of the DAC in order to determine the current bit. The conversion starts from the MSB, then the MSB-1 and so forth until the LSB is determined. As the conversion is performed, the difference between the input voltage and DAC voltages goes toward zero. Therefore, each conversion takes  $N$  steps for an  $N$ -bit SAR ADC. If the SAR converter is controlled by a synchronous logic, the internal clock frequency needs to be at least  $N$  times faster than the sampling frequency. When medium-high conversion rates (about hundreds of MS/s) are needed, an asynchronous logic is preferred because it does not require the same high-speed clock, hence reducing the power consumption[12].

### 2.1.6 Time-interleaving

Converters based on time-interleaving perform the conversion with multiple ADCs working in parallel to achieve high conversion rates as shown in Figure 2.7. Let us consider a converter sampling the input signal at a frequency  $f_s$ . It is possible to implement a converter whose sampling frequency is  $Nf_s$  time-interleaving  $N$  channels. From a system level perspective, the system is composed by a S&H followed



**Figure 2.7:** Architecture of a time-interleaved ADC, based on [4].

by an analog de-multiplexer to feed the sampled signal to one of the channels. Then, the outputs of

the converters are selected with a multiplexer to obtain an ADC effectively working at N times the sampling frequency of a single channel. It is also possible to have a S&H for each channel instead of a single S&H shared among all the channels working at a sampling frequency  $Nf_s$ . Each sampler is driven by equally phase-shifted clocks. An essential requirement is to have an equal phase shift between the clocks to avoid the presence of spurious frequency tones at the output of the converter. Different channels can have different offset, different gain or bandwidth. All these issues make the design of time-interleaved (TI) ADCs particularly challenging. It is worth noting that only theoretically the power consumption of an N-channel TI ADC is N times the power consumption of the single channel. In fact, the calibration techniques to reduce the effect of non-idealities and the control logic that implements the time-interleaving add an overhead, increasing in the power consumption of the converter[13].

## 2.2 SAR ADC architecture

A SAR ADC is composed by three main parts: a digital-to-analog converter and S&H, a comparator and a SAR logic. The majority of modern SAR ADCs is based on a switching-intensive operation where most of the circuitry is digital. In particular, the DAC is a capacitive array where the sampled signal is stored at the beginning of the conversion. Then, the charge is opportunely redistributed among all the capacitors to approximate the sampled voltage. Before delving into the characteristics of the devices that compose the SAR ADC, let us understand how the conversion is carried out with the successive approximation algorithm considering the architecture shown in Figure 2.8.

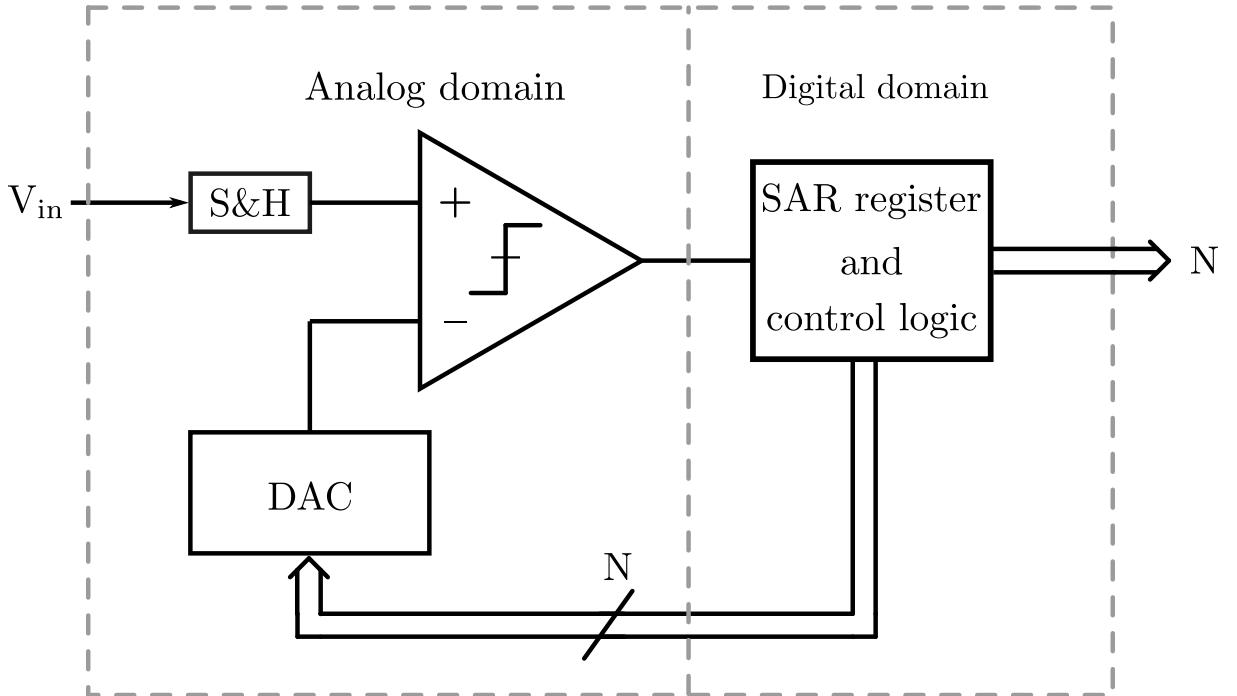


Figure 2.8: Architecture of a SAR ADC.

The conversion is performed over the course of multiple clock cycles starting from the MSB. The information obtained in each clock period is then used to generate the next significant bit. At the beginning of the conversion, the input voltage is sampled by the S&H circuit. In the following step, the MSB is determined comparing the sampled voltage with half of the full scale range, e.g.,  $V_{dd}/2$  if we consider the interval  $[0, V_{dd}]$ , where  $V_{dd}$  is the supply voltage. The reference voltage of the comparator is provided by the DAC, driven by the logic circuit. Based on the output of the comparator, the MSB will be '0' or '1' and it will be stored in a SAR register in the logic circuit. From the MSB evaluation, it

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is possible to determine in which half of the search binary tree the next reference voltage should be set, restricting the search either between 0 and  $V_{dd}/2$  or between  $V_{dd}/2$  and  $V_{dd}$ . In fact, this means that the sampled signal is compared with  $V_{dd}/4$  or  $3V_{dd}/4$ , respectively. This procedure is repeated for each bit up to the LSB.

The following subsections are dedicated to the description of the blocks forming a SAR ADC, based on topologies found in literature. Regarding the DAC, different topologies and switching algorithms are explained together with the effect of the capacitor mismatch on the linearity of the ADC. Then, two different kinds of comparators are treated highlighting the advantages and disadvantages of each topology. Finally, the SAR logic operation is described. The chapter concludes with a brief description on the energy required by the DAC, comparator and logic.

## 2.3 DAC architecture

The DAC has a crucial role in defining the linearity, other than noise and speed, of the SAR ADC. Indeed, a major source of non-linearity is the mismatch between the capacitors that implement the DAC[14]. Moreover, the adopted switching scheme affects the power consumption of the converter. In the next subsections, a background on the most important DAC and switching schemes proposed in literature is presented. It starts from the conventional SAR ADC[11], then the split capacitor array DAC[15] is described and, finally, the monotonic switching algorithm[16] and its modification[17] are presented.

### 2.3.1 Conventional charge-redistribution ADC

The conventional charge-redistribution (CR) ADC was proposed in [11] by P. Gray and J. McCreary. In this SAR ADC, which it will be referred as conventional, the DAC is implemented with an array of binary-weighted capacitors. Therefore, for an  $n$ -bit converter, there are  $n + 1$  capacitive banks and  $2^n$  unit capacitors. The name CR is due to its working principle: after the initial sampling of the signal, the charge is redistributed on the capacitor array until the voltage on the top plates reaches a value close to zero at the end of the conversion. The charge remaining on the top plate when the conversion is finished is not zero because the resolution of the DAC is finite.

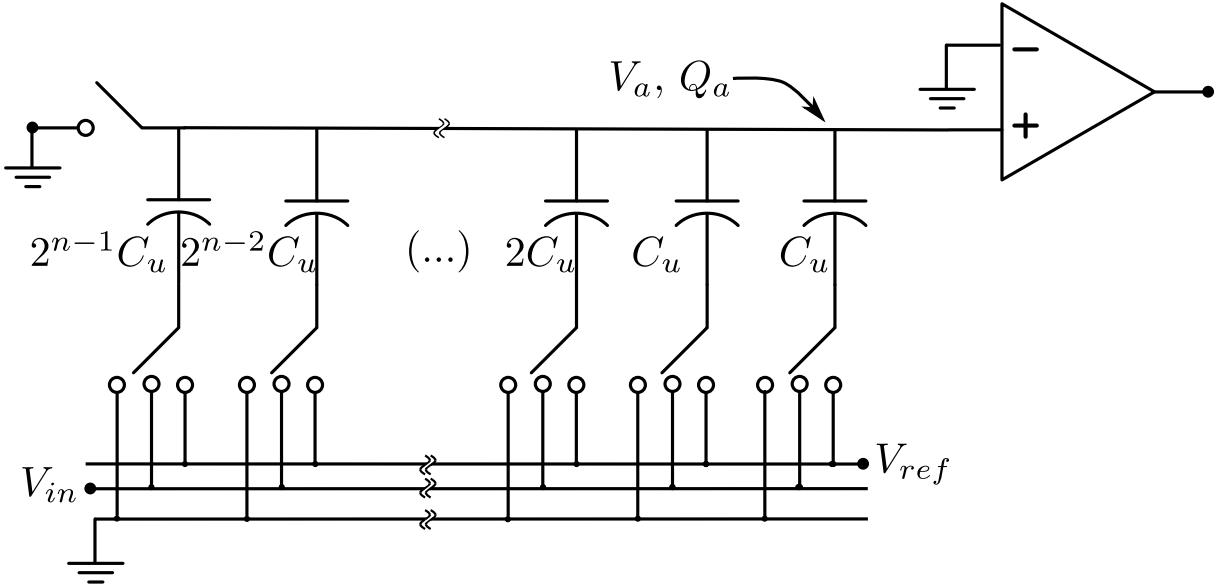
The structure of the DAC with the comparator is shown in Figure 2.9. The capacitor array is a binary-weighted array. Here, a single-ended version is depicted, but it is possible to use also a differential structure, where the DAC networks behave in a complementary way.

A brief summary of the conversion phases is depicted in Figure 2.10. The conversion procedure follows three main steps: sampling phase, hold phase and redistribution mode. During the first phase, the input voltage is sampled on the bottom plates of the capacitors and the top plates are set to ground, thus the charge on the top plate is  $-2^n C_u V_{in}$ . Then, in the hold mode, the top-plates are disconnected from ground while the bottom plates are switched to ground. Since the input terminal of the comparator is a high impedance node, the charge will be conserved and the voltage  $V_a$  will become  $-V_{in}$ . Finally, the redistribution mode starts and the conversion takes place over the course of  $n$  cycles. The following procedure is performed in each cycle.

The bottom plate capacitor corresponding to the bit being evaluated is switched to  $V_{ref}$ , typically equal to the supply voltage  $V_{dd}$ . The variation of the voltage at the input terminal of the comparator can be computed considering a capacitive partition. Therefore, the voltage at the input of the comparator can be written as:

$$V_a = -V_{in} + \frac{C_{MSB}}{C_{tot}} V_{ref} = -V_{in} + \frac{V_{ref}}{2}, \quad (2.1)$$

where  $C_{MSB}$  is the capacitance of the MSB capacitor,  $2^{n-1} C_u$ , and  $C_{tot}$  is the total capacitance of the DAC array,  $2^n C_u$ . Eq. (2.1) represents the difference between the voltage corresponding to the MSB and the sampled voltage. The reference voltage of the comparator is set to ground to determine the sign of the voltage difference between its inputs. The output of the comparator is then used by the SAR logic



**Figure 2.9:** Conventional charge-redistribution DAC array, based on [4].

to set the MSB to 0, if  $V_a > 0$ , i.e.,  $V_{in} < V_{MSB}$ , or 1 in the opposite case. In the former case, the largest capacitor is switched to ground, otherwise it remains connected to the reference voltage. In the next cycle, the capacitor of the MSB-1 bit is switched to  $V_{ref}$ , increasing the voltage  $V_a$  by  $\frac{V_{ref}}{4}$ , and the same procedure is repeated. In this way, if the MSB is 1, the voltage at the input of the comparator becomes:

$$V_a = -V_{in} + \frac{3}{4}V_{ref}, \quad (2.2)$$

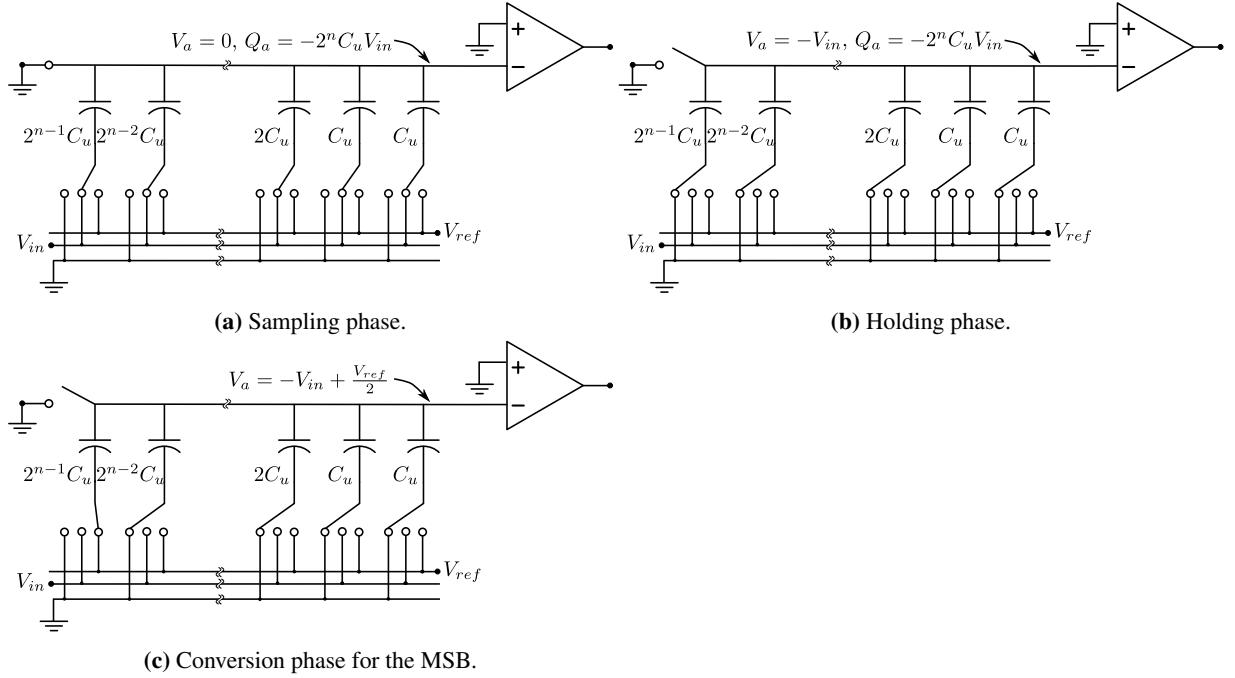
or

$$V_a = -V_{in} + \frac{V_{ref}}{4}, \quad (2.3)$$

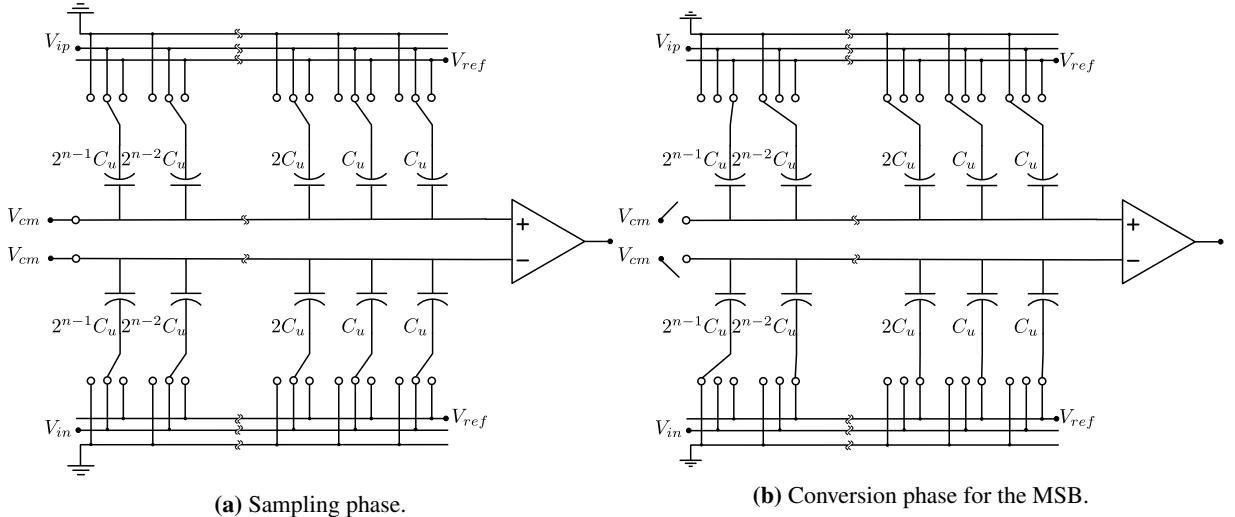
in the opposite case. The conversion finishes when the least-significant bit (LSB) is determined. Even though the procedure explained above is valid for a single-ended structure, it can be easily generalized to a differential SAR with two capacitor networks working in a complementary way. The procedure for the fully differential structure is summarized in Figure 2.11. Note that, for a fully-differential structure, the top plates of the DAC networks are connected to the common mode voltage,  $V_{cm}$  (typically set to half of the supply voltage), whereas the bottom plates sample the positive and negative input voltages,  $V_{ip}$  and  $V_{in}$ , respectively. Then, all the bottom plates are switched to ground except for the largest capacitor of the DAC connected to the positive terminal of the comparator, which is switched to  $V_{ref}$ . The opposite happens in the negative array. In this way, the MSB can be determined. If the result from the comparator is 1 then nothing changes and the conversion proceeds to the next bit, switching the bottom plates of the second largest capacitor of the positive array to the reference voltage. Otherwise, the bottom plate of the capacitor corresponding to the MSB is switched to ground for the positive DAC whereas it is switched to  $V_{ref}$  for the negative DAC. This procedure is repeated until the LSB is determined. An example of the waveforms at the output of the DAC is shown in Figure 2.12.

### 2.3.2 Split capacitor DAC

As already mentioned above, at the beginning of each conversion step, the bottom-plate of the capacitor is connected to  $V_{ref}$  and then the comparison is carried out. Two transitions can take place. If the comparison is successful, i.e., the DAC output voltage lies in the binary path that best approximates the input voltage, the bottom-plate of the capacitor corresponding to the next bit is connected to  $V_{ref}$ . When the current digital estimation of the input voltage is wrong, the bottom-plate of the capacitor



**Figure 2.10:** Summary of the three different phases of a single-ended conventional SAR ADC, based on [11].



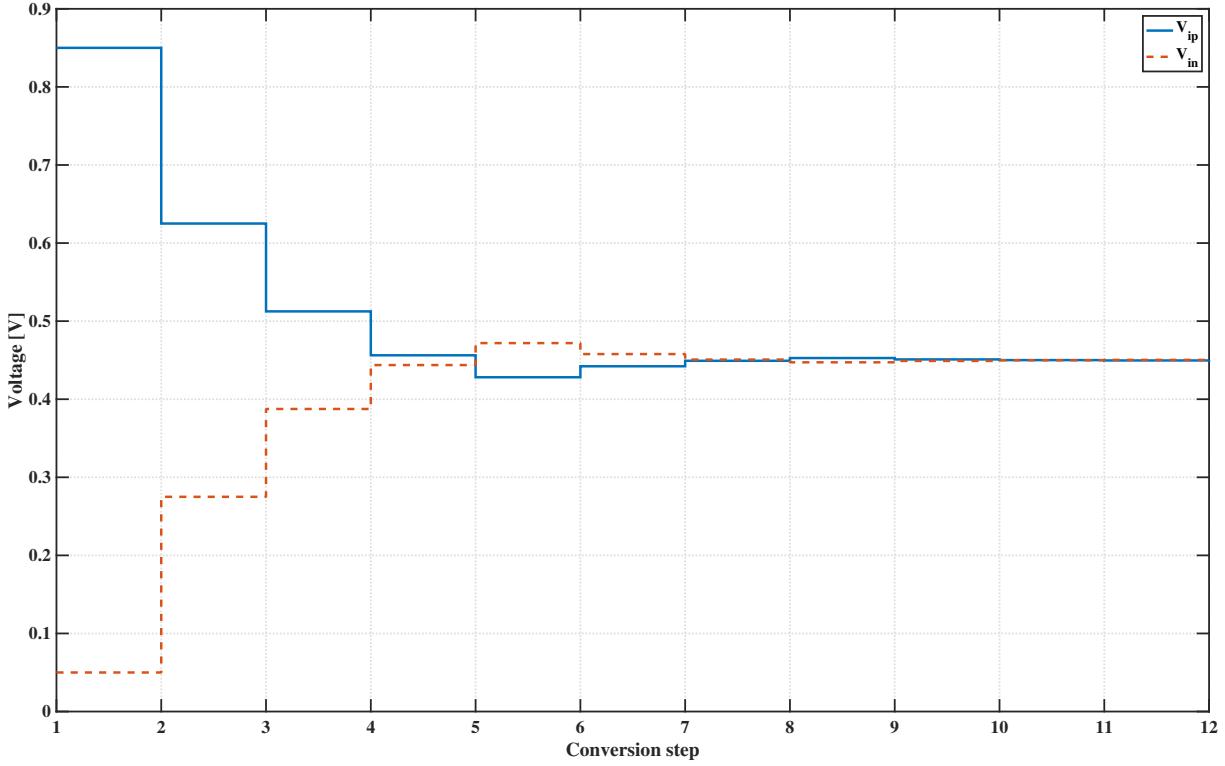
**Figure 2.11:** Summary of the different phases for a conventional fully-differential SAR ADC, based on [18].

corresponding to the bit being evaluated must be switched from  $V_{ref}$  to ground and the next capacitor is switched to  $V_{ref}$ . The first case can be called an “up” transition, while the second one a “down” transition. An example for the MSB evaluation is shown in Figure 2.13.

In [19], Chandrakasan et al. analyzed the energy drawn from the power supply for an “up” transition and a “down” transition as follows. The energy drawn from the power supply when its bottom plate is switched to  $V_{ref}$  at time  $t_1$  and the voltage is settled at time  $t_2$  can be written as:

$$E = \int_{t_1}^{t_2} i(t)V_{ref}dt = V_{ref} \int_{t_1}^{t_2} i(t)dt, \quad (2.4)$$

where  $i$  is the current provided by the reference voltage. Writing the current as the variation of the charge



**Figure 2.12:** Waveforms of the voltage on the positive ( $V_{ip}$ ) and negative ( $V_{in}$ ) input of the comparator for a differential input voltage of 800 mV and a reference voltage of 0.9 V for a conventional SAR ADC.

over time on the capacitor, the energy becomes:

$$E = -V_{ref} \int_{t_1}^{t_2} \frac{dQ}{dt} dt = -V_{ref}[Q(t_2) - Q(t_1)]. \quad (2.5)$$

Let us consider the transition for the capacitor  $C_{MSB}$ , i.e. the capacitor corresponding to the MSB. At the beginning of the transition the voltage  $V_a$  is  $-V_{in}$ , whereas it becomes  $-V_{in} + \frac{V_{ref}}{2}$  at the end. Therefore, Eq. (2.5) becomes:

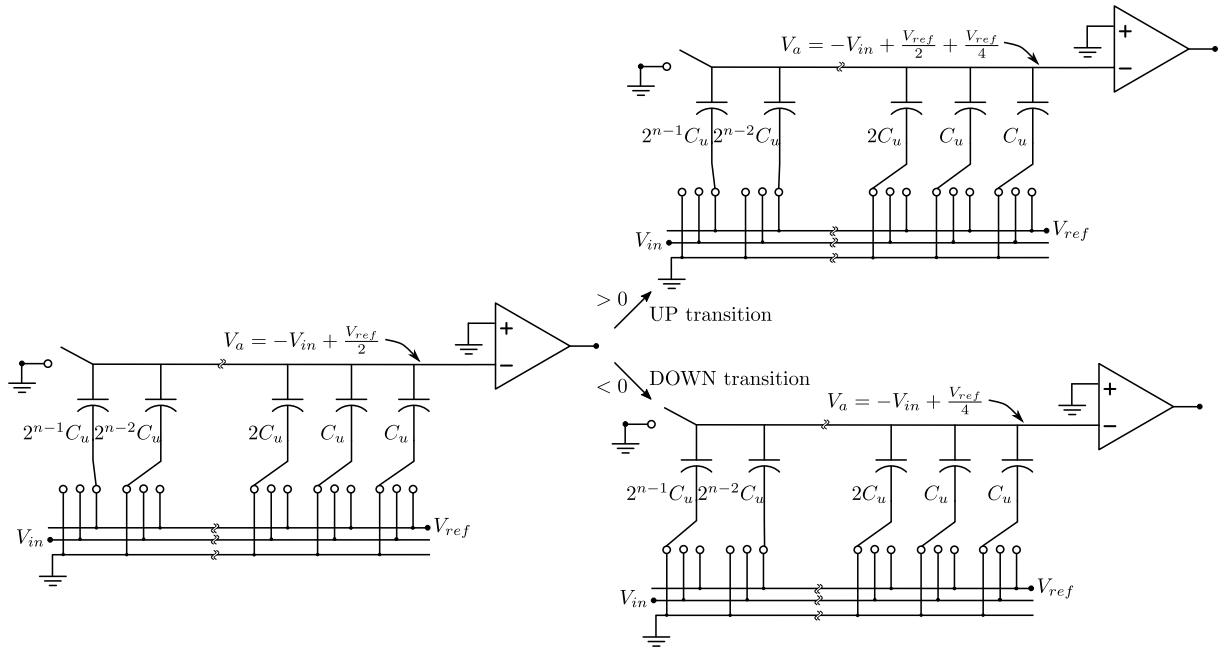
$$E = -V_{ref}C_{MSB}[(-V_{in} + \frac{V_{ref}}{2} - V_{ref}) - (-V_{in})] = \frac{C_{MSB}V_{ref}^2}{2}. \quad (2.6)$$

At this point, if the output of the comparator is the logical state 1, i.e., an “up” transition occurs, the bottom-plate of the next capacitor is switched to  $V_{ref}$  requiring a total energy equal to:

$$\begin{aligned} E_{up} &= -V_{ref}C_{MSB}[(-V_{in} + \frac{V_{ref}}{2} + \frac{V_{ref}}{4} - V_{ref}) - (-V_{in} + \frac{V_{ref}}{2} - V_{ref})] + \\ &\quad - V_{ref}\frac{C_{MSB}}{2}[(-V_{in} + \frac{V_{ref}}{2} + \frac{V_{ref}}{4} - V_{ref}) - (-V_{in} + \frac{V_{ref}}{2})] = \\ &\quad \frac{1}{8}C_{MSB}V_{ref}^2. \end{aligned} \quad (2.7)$$

Note that in the second addend the capacitor  $C_{MSB}$  is divided by 2 because the DAC array is binary-weighted. In the opposite case, the MSB capacitor is switched to ground and the next one to  $V_{ref}$ . Thus, a “down” transition requires an energy equal to:

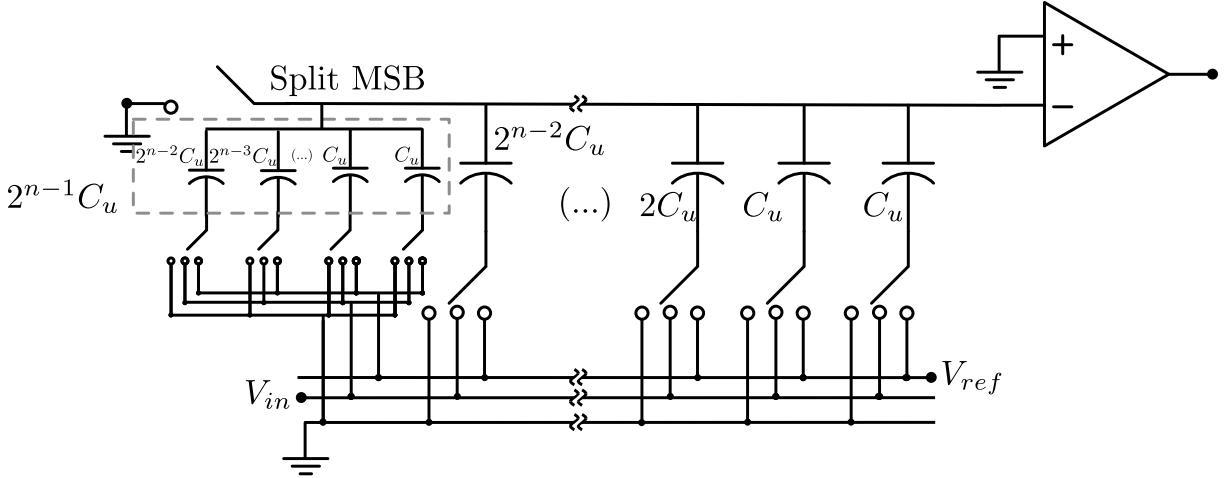
$$\begin{aligned} E_{down} &= -V_{ref}\frac{C_{MSB}}{2}[(-V_{in} + \frac{V_{ref}}{4} - V_{ref}) - (-V_{in} + \frac{V_{ref}}{2})] \\ &= \frac{5}{8}C_{MSB}V_{ref}^2. \end{aligned} \quad (2.8)$$



**Figure 2.13:** "Up" and "down" transitions.

The analysis highlights how the conventional SAR ADC is not efficient since the "down" transition requires five times more energy than an "up" transition. The authors in [19] suggested various methods to perform a "down" transition.

One of the suggested approaches is the capacitor splitting. It consists in splitting the MSB capacitor in an exact replica of the other half of the capacitive DAC (CDAC) as shown in Figure 2.14. The MSB capacitor is formed by  $2^{n-1}$  binary-weighted capacitors for an  $n$ -bit DAC.



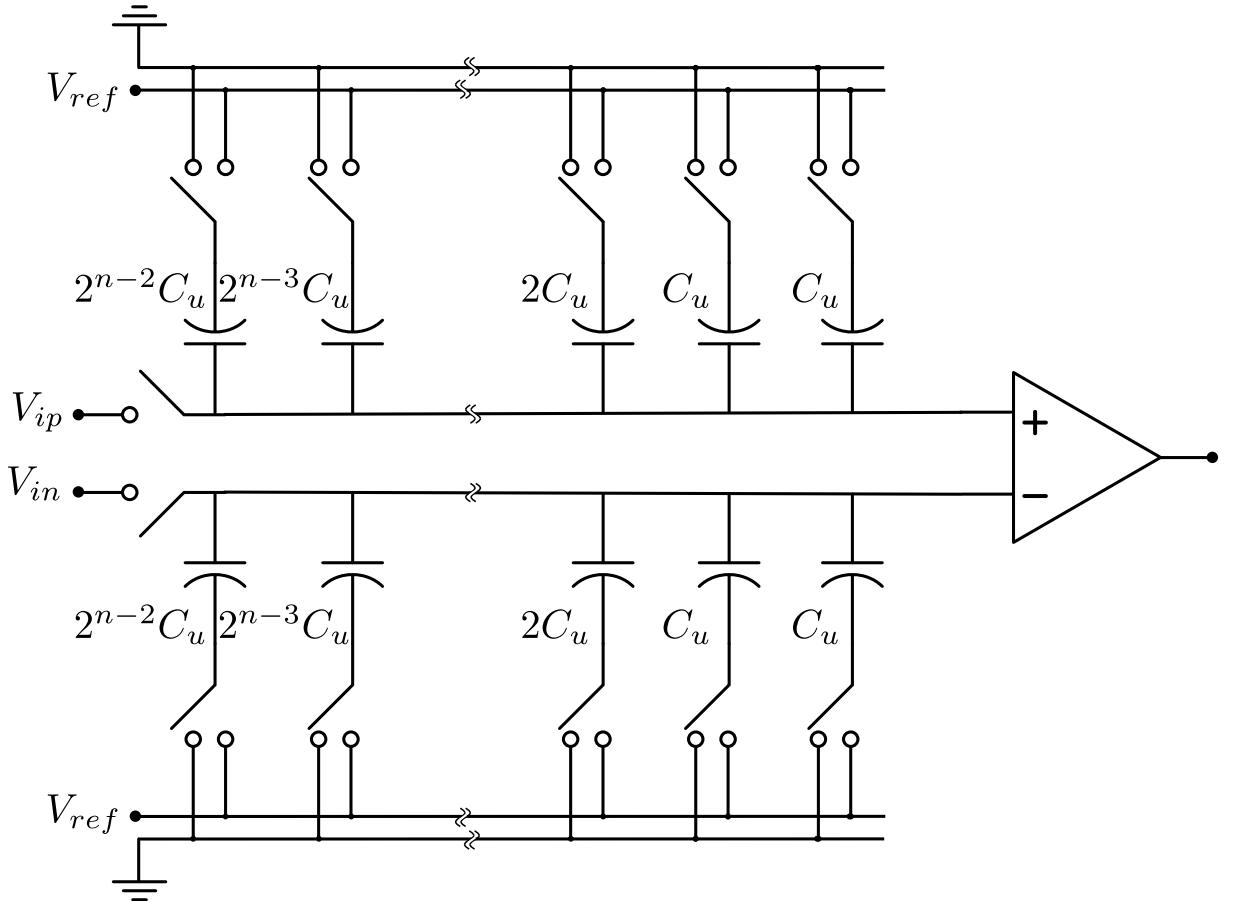
**Figure 2.14:** Single-ended structure of the split capacitor array, based on [15].

At the beginning of the conversion the capacitor corresponding to the MSB is charged to  $V_{ref}$ . In the following cycles, the "up" transition is the same as the conventional switching procedure, that is, the  $i$ -th capacitor of the capacitive array (not of the MSB capacitor), is switched to  $V_{ref}$  for the  $i$ -th decision. For a "down" transition, the only capacitor that is switched to ground is the  $i$ -th capacitor of the MSB. The result is that there is no charging of any capacitor to  $V_{ref}$  during the conversion of the input signal. This method allows to avoid spending energy to charge a capacitor from ground to  $V_{ref}$  in a "down" transition and the same energy is required for a "down" and a "up" transition.

The advantage of using this kind of topology is the reduced energy consumption with respect to the conventional fully-differential SAR ADC. In fact, a SAR ADC based on the capacitor splitting consumes 37% less energy than a conventional SAR ADC[19]. Even though this switching procedure is beneficial in terms of energy with respect to the conventional algorithm, it requires a number of switches that is doubled, because each sub-capacitor of the MSB needs to be controlled. This entails that more area is needed for the switches.

### 2.3.3 Monotonic switching

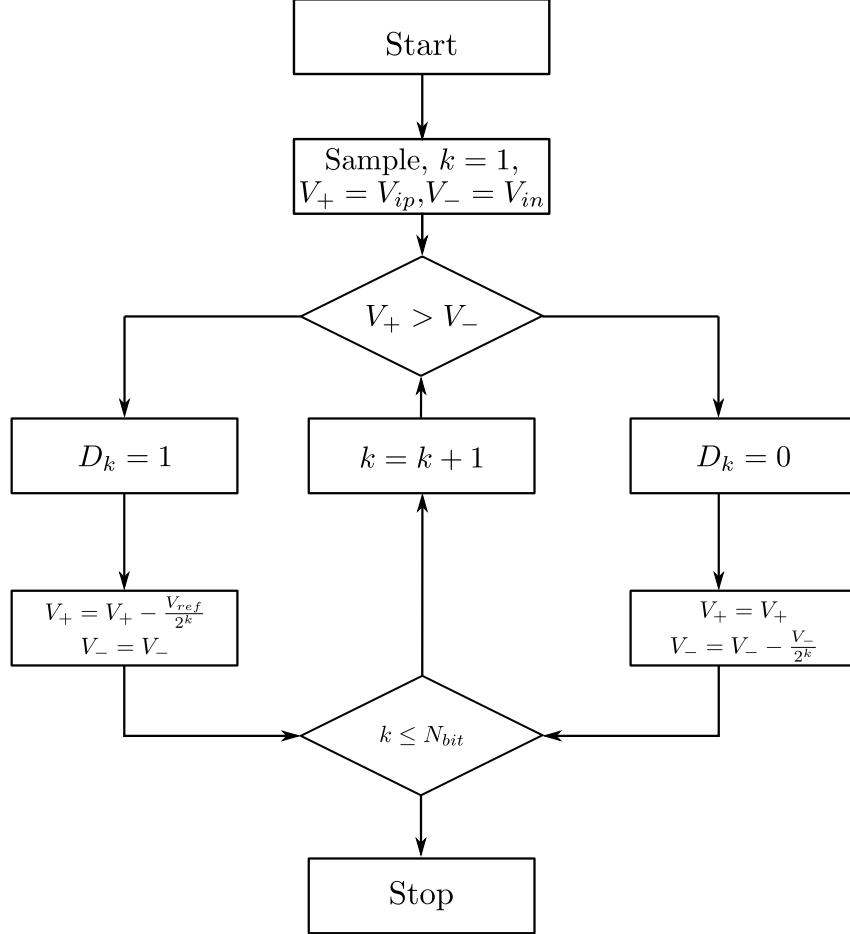
In 2010, Liu et al. at the National Cheng Kung University proposed an algorithm to improve the energy efficiency of the conventional fully-differential (FD) SAR ADC in [16]. The idea at the basis of the proposed algorithm is avoiding to charge any of the capacitor after the sampling phase, that is, only downward transitions happen during conversion after the capacitors are reset to  $V_{ref}$ . The architecture



**Figure 2.15:** Monotonic switching SAR ADC architecture, based on [16].

of the SAR ADC is shown in Figure 2.15. There is only one capacitor switched to ground per each bit cycle, allowing a reduction in power consumption. Moreover, the input signal is sampled on the top-plate of the capacitive DAC. This allows the possibility to perform the MSB decision right after the sampling without switching any capacitors in the DAC. Therefore, only half of the total capacitance present in a conventional SAR ADC is needed. In practice, this means that only  $2^{n-1}$  unit capacitors implement each of the two DACs reducing the area by half with respect to the conventional SAR ADC.

It is not a completely fully-differential structure since only one capacitor array is switched in each cycle of the algorithm. The flow chart of the algorithm is shown in Figure 2.16 and an example of the waveforms of the voltage at the positive ( $V_p$ ) and negative ( $V_n$ ) terminal of the comparator is plotted in

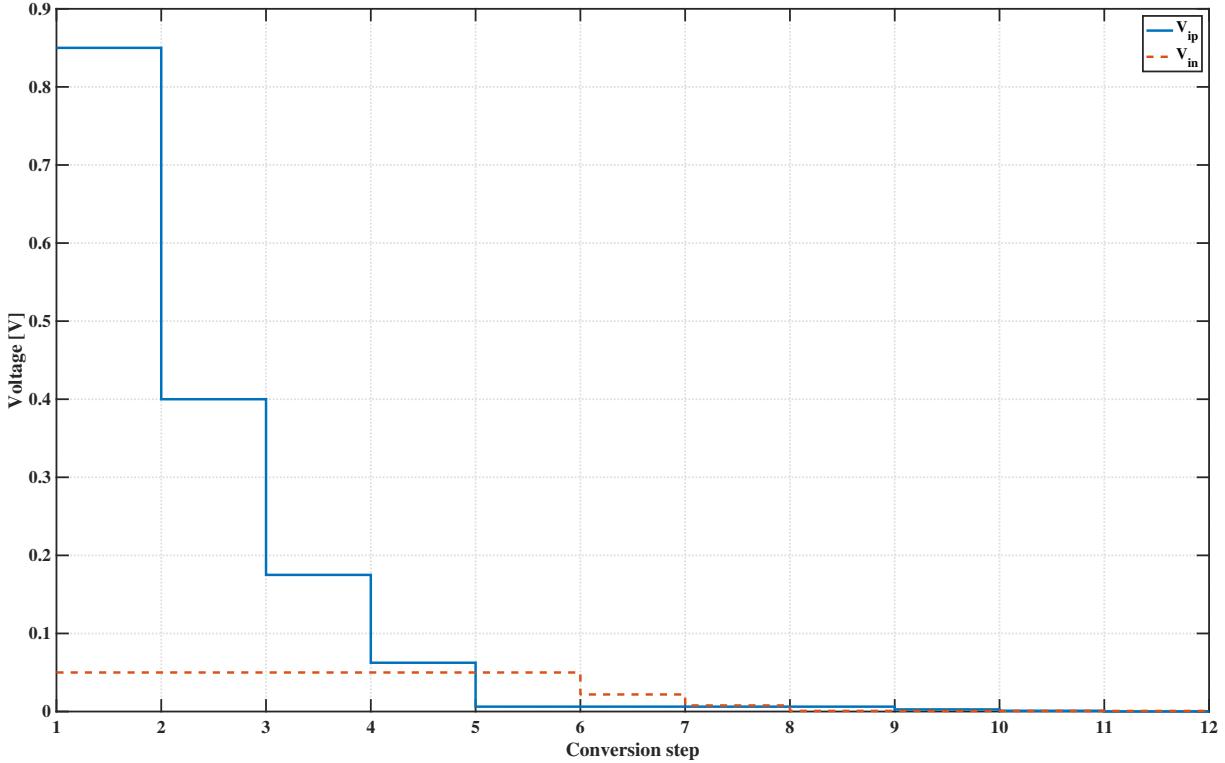


**Figure 2.16:** Flow chart of the monotonic switching algorithm (from [16]).

Figure 2.17. During the sampling phase, the top plates of the capacitor arrays are connected to the input signal, whereas the bottom plates are reset to  $V_{ref}$ . Then, the input switches are opened and the first comparison can be directly performed. At this point, the output of the comparator is used by the SAR logic to set the MSB and, thereafter, to switch the largest capacitor on the array with the larger voltage to ground. The bottom plate of the corresponding capacitor on the other array remains connected to  $V_{ref}$ . This algorithm is repeated until the last significant bit is decided.

Comparing the waveforms plotted in Figure 2.12 and Figure 2.17, it is possible to note an important difference between the conventional and monotonic switching algorithm regarding the variation of the common mode voltage. The conventional SAR ADC has a fully-differential structure where the DACs connected to the positive and negative terminal of the array behave in a complementary way. In the monotonic algorithm, instead, switching takes place only in one of the two sides based on the decision taken by the comparator in the previous cycle and there are only downward transitions. Therefore, the common mode voltage changes during the conversion from  $\frac{V_{ref}}{2}$  to 0 V. This affects the design of the comparator since it has to sustain such a variation of the input common mode voltage.

The switching energy in a SAR ADC implemented with the monotonic switching algorithm is 81% smaller than in the conventional SAR ADC[16]. Moreover, the area required to implement the CDAC is reduced by half. Therefore, it is a good solution to cope with power consumption and area of the CDAC, although the comparator design is more complex for the variation of the common mode voltage.

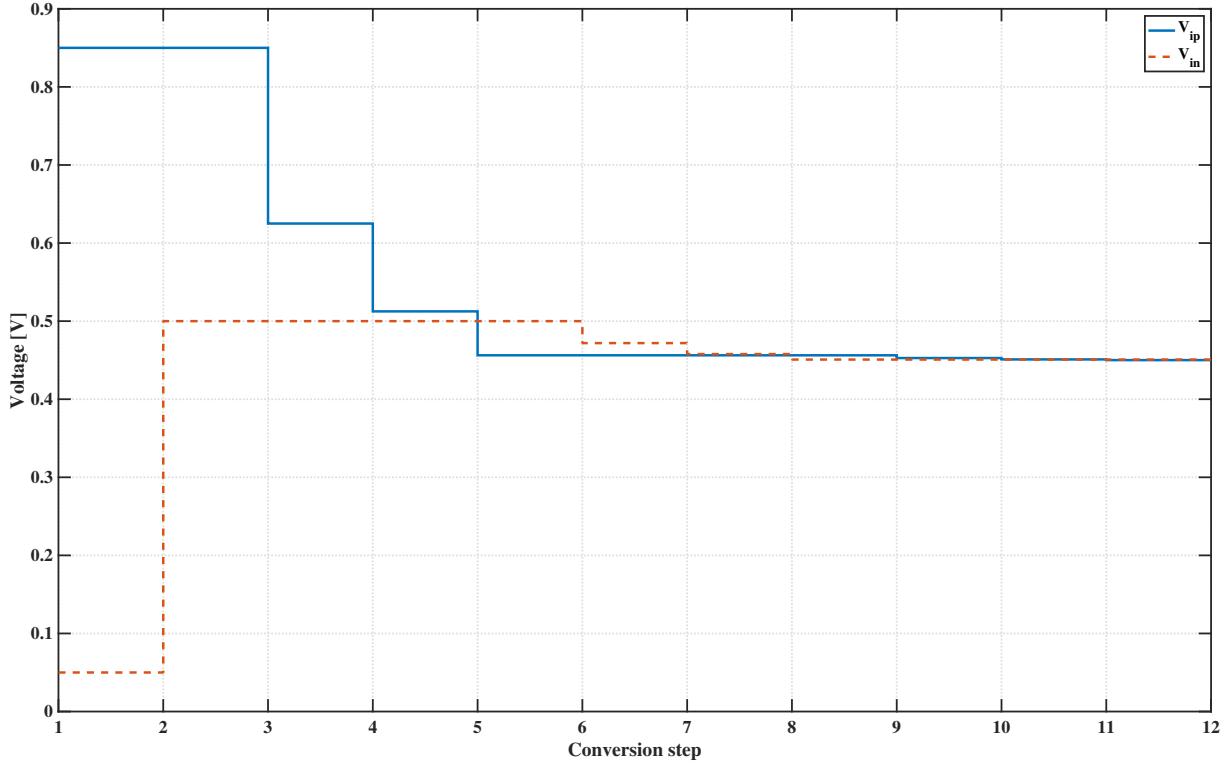


**Figure 2.17:** Waveform of the voltage on the positive ( $V_{ip}$ ) and negative ( $V_{in}$ ) input of the comparator for a differential input voltage of 800 mV and a reference voltage of 0.9 V with the monotonic switching algorithm.

### 2.3.4 Modified monotonic switching

As already mentioned, a distinctive characteristic of the monotonic switching algorithm is that the common mode voltage changes between  $\frac{V_{ref}}{2}$  and ground, and this peculiarity makes the design of the comparator particularly challenging because it has to be able to compare even small voltage differences close to ground. A possible way to solve this problem was proposed in [17]. The difference between the original algorithm and the one proposed by Brenna *et al* is in the first step of the algorithm. From here onward it will be called *modified* monotonic switching algorithm. An example of the voltage waveforms of the positive input and negative input terminal of the comparator is shown in Figure 2.18. When the CDACs are reset, the MSB capacitor is switched to ground, while the others are reset to  $V_{ref}$ . After the first comparison has been performed by the comparator, the MSB capacitor of the DAC corresponding to the negative potential side is switched to  $V_{ref}$ . Therefore, in the first conversion step, there is an upward transition by  $\frac{V_{ref}}{2}$  on one of the input terminals of the comparator. For the remaining steps, the algorithm follows the same procedure as the monotonic switching algorithm.

The slight modification in the switching algorithm results in a variation of the common mode voltage,  $V_{cm}$ , different from the original algorithm. After the MSB decision, there is an upward transition of  $V_{cm}$  by  $\frac{V_{ref}}{4}$  and then a monotonic variation towards  $\frac{V_{ref}}{2}$ . In few words, the common mode voltage varies between  $\frac{3}{4}V_{ref}$  and  $\frac{V_{ref}}{2}$ . The design of the comparator with the use of the modified monotonic switching algorithm is relaxed because the total variation of  $V_{cm}$  is reduced, being  $\frac{V_{dd}}{4}$ , with respect to the original algorithm and it is confined in the voltage interval  $[\frac{3}{4}V_{ref}, \frac{V_{ref}}{2}]$ . This allows the use of NMOS input transistors in the comparator reducing the input non-linear capacitance with respect to PMOS input transistors needed with the monotonic algorithm[17]. In terms of energy efficiency, the switching energy of the modified monotonic switching algorithm is larger than the original algorithm, but this variation is negligible, because only the first step of the algorithm is changed.



**Figure 2.18:** Voltage waveform of the positive input ( $V_{ip}$ ) and negative input ( $V_{in}$ ) of the comparator with the modified monotonic switching algorithm for an initial input voltage difference of 800 mV and reference voltage of 0.9 V.

## 2.4 Linearity

An important requirement for an analog-to-digital converter is the linearity. Two important parameters that quantify the linearity of an ADC are the differential non-linearity (DNL) and the integral non-linearity (INL). Capacitor mismatch is one of the major sources of non-linearity in SAR ADCs[14].

A model to estimate the effect of mismatch in the capacitors of the CDAC was proposed in [15] as follows. The capacitance of the capacitor of the CDAC corresponding to the  $i$ -th bit can be modeled as:

$$C_i = 2^{i-1}C_u + \delta_i, \quad (2.9)$$

where  $C_u$  is the nominal value of the unit capacitance and  $\delta_i$  is an error term considered to be an independent random variable. The error is assumed to have a Gaussian distribution with zero mean value and a variance equal to:

$$E[\delta_i^2] = 2^{i-1}\sigma_u^2, \quad (2.10)$$

where  $\sigma_u$  is the standard deviation of the unit capacitor.  $\sigma_u$  can be expressed in terms of the Pelgrom coefficient,  $k_c$  as:

$$\frac{\sigma_u}{C_u} = \frac{k_c}{\sqrt{2A}}, \quad (2.11)$$

where  $A$  is the area of the capacitor. Considering the digital input  $D = \sum_{j=1}^n S_j 2^{j-1}$ , where  $S_j$  is the decision of the comparator for the  $j$ -th bit, the analog output of the DAC for a conventional  $n$ -bit SAR ADC is:

$$V_a = \frac{\sum_{j=1}^n (2^{j-1}C_0 + \delta_j)S_j}{2^n C_0 + \Delta C} V_{ref}, \quad (2.12)$$

where the sum of all the errors in the denominator is  $\Delta C = \sum_{j=0}^n \delta_j$ , but it can be considered negligible because its average is zero. If we now subtract the ideal value from Eq. (2.12) and consider the variance

---

of the resulting voltage error  $V_\varepsilon$  for an input code  $D$ , we obtain:

$$E[V_\varepsilon^2(D)] = \frac{D}{2^{2n}} \frac{\sigma_u^2}{C_u^2} V_{ref}^2. \quad (2.13)$$

Now, the DNL is the deviation of the interval between consecutive transition points,  $V_a(D)$ , of a real converter from the ideal width and it can be expressed as:

$$DNL(D) = \frac{V_a(D) - V_a(D-1) - LSB}{LSB}. \quad (2.14)$$

If we consider that  $V_a$  can be considered as the sum of the ideal value and an error term  $V_\varepsilon$ , Eq. (2.14) becomes:

$$DNL(D) = \frac{V_\varepsilon(D) - V_\varepsilon(D-1)}{LSB}. \quad (2.15)$$

The maximum value of the variance of the DNL is the one corresponding to the mid-code transition, i.e., between  $D_{MSB} = [1, 0, 0, \dots, 0, 0]$  and  $D_{MSB-1} = [0, 1, 1, \dots, 1, 1]$ , because the errors due to the mismatch of all capacitors add up:

$$\sigma_{DNL,CBW}^2 = E \left[ \left( \frac{V_\varepsilon(D_{MSB}) - V_\varepsilon(D_{MSB-1})}{LSB} \right)^2 \right] = 2^n \frac{\sigma_u^2}{C_u^2}. \quad (2.16)$$

The result in Eq. 2.16 is valid for a single-ended structure. If we consider a fully-differential implementation, we can reduce the standard deviation of the DNL by  $\sqrt{2}$ , because the LSB doubles while the error due to mismatch is increased by  $\sqrt{2}$  times[20].

The effect of mismatches on the linearity changes based on the switching algorithm and DAC architecture. If we apply the same procedure, it is possible to obtain a result similar to (2.16) for the split capacitor array [15]:

$$\sigma_{DNL,SBW} = \frac{2^{\frac{n}{2}}}{\sqrt{2}} \frac{\sigma_u}{C_u}. \quad (2.17)$$

The result is  $\sqrt{2}$  times lower than for the conventional SAR ADC in terms of standard deviation, because there is a partial correlation between the mid code and the previous code[15].

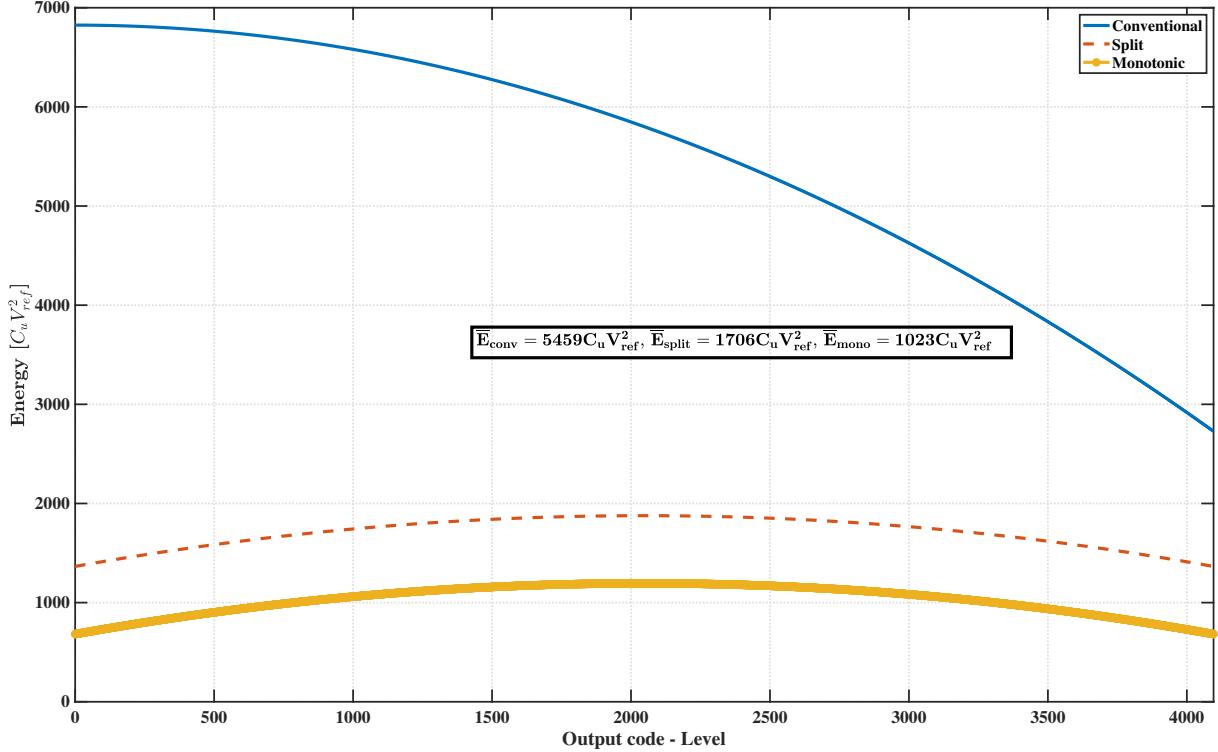
In terms of linearity, there is no difference between the monotonic switching algorithm and its modified version because the output voltages generated by the DAC are the same. Following the analysis explained above, it is possible to obtain the standard deviation of the DNL for the monotonic switching[21]:

$$\sigma_{DNL,MBW} = \frac{2^{\frac{n}{2}}}{\sqrt{2}} \frac{\sigma_u}{C_u}. \quad (2.18)$$

## 2.5 Switching energy

The energy consumption of the CDAC in a SAR ADC is dependent on the switching algorithm and the architecture. Considering the variation of the charge on the capacitors connected to  $V_{ref}$ , it is possible to compute the energy drawn by the supply voltage in each conversion step, as explained in [19]. The energy is, as the intuition suggests, directly proportional to the unit capacitance of the CDAC. It is also worth noting that it depends on the input signal, thus the output digital code. To better explain this point, let us consider a conventional  $n$ -bit SAR ADC. If the sampled signal is in the interval [0 V, 1 LSB], the output digital code will be [0, 0, 0, ..., 0, 0]. This means that during each of the  $n$  conversion steps, the bottom plate of each capacitance of the CDAC is first charged to  $V_{ref}$ , and then, the result of the comparator will be zero. The SAR logic at that point sets the bit currently being evaluated to zero and switches to ground the same capacitance that was charged to  $V_{ref}$ . If, instead, the input signal

corresponds to a digital code [1, 1, 1, ..., 1, 1], each capacitance is charged to  $V_{ref}$  and not switched to ground after the comparator decision, since the result is 1 in each step. Apart from highlighting the inefficiencies present in the conventional SAR ADC, this simple example helps to understand why the energy is a function of the output code. In the first case there is the largest energy consumption, whereas in the second case the smallest one. In order to compute the switching energy, the Matlab tool proposed



**Figure 2.19:** Energy consumption versus output code normalized to  $C_u V_{ref}^2$  for a 12-bit SAR ADC.

| Architecture | $\sigma_{DNL,max}$ [LSB] | Area FD [ $C_u$ ] | $E_{ave}[C_u V_{ref}^2]$ |
|--------------|--------------------------|-------------------|--------------------------|
|              | SE                       | FD                |                          |
| CBW [11]     | 0.64                     | 0.45              | $2 \cdot 4096$ 5459      |
| SBW[15]      | 0.45                     | 0.32              | $2 \cdot 4096$ 1706      |
| MBW[16]      | -                        | 0.45              | $2 \cdot 2048$ 1023      |

**Table 2.1:** Summary of area, maximum value of the standard deviation of the DNL and average switching energy for a 12-bit SAR ADC. Note that the relative mismatch  $\frac{\sigma_u}{C_u}$  is set to 1%.

in [22] was used to estimate the energy as a function of the output code. A graph with the energy versus code is shown in Figure 2.19 for a 12-bit SAR ADC. From the example mentioned above, it is possible to understand the trend of the energy consumption in the plot. Considering the conventional SAR ADC, starting from a code of all 0's the energy drawn from the supply monotonically reduces because there are fewer wrong digital estimations of the input analog signal, i.e., fewer capacitances are switched to ground after the decision of the comparator.

Even though the switching energy is different for different output codes, the average energy is more useful from a design perspective. From the graph, it is possible to see that the split capacitor array and monotonic algorithm reduce the average energy consumption by 37% and 81%, respectively. Therefore, the monotonic switching algorithm is the most efficient among the three. A summary for the area,

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linearity and energy consumption of the algorithms explained above is shown in Table 2.1. In this work, the modified monotonic algorithm was chosen because it reduces the energy consumption and the area of the DAC with respect to the conventional SAR ADCs. The modified monotonic switching algorithm dissipates more energy with respect to its original version. This because there is a certain amount of reset energy, which is the energy spent when the the capacitors are reset. In fact, there is a path between  $V_{dd}$  and ground when the capacitors are reset, since the MSB capacitor is reset to ground, instead to  $V_{dd}$ . This reset energy is a function of the output code. In this work, it has been assumed that the increase of the energy consumption caused by the reset energy can be considered negligible with respect to the total energy.

## 2.6 Comparator

Another important component of the SAR ADC is the comparator. The output value of the comparator represents a logical state corresponding to the sign bit of the voltage difference between its inputs. In a SAR ADC, the logical state is fed to the logic control circuit that sets the value of the bit being evaluated. Comparators are typically formed by two stages. The first stage is a preamplifier that amplifies the differential input signal. Then, the amplified signal is fed to a latch, i.e., a bistable memory element whose binary output states are read by the logic of the SAR ADC. In a latch, positive feedback is exploited to toggle the device from one state to another. The vast majority of comparators can be divided in two classes: static and dynamic comparators. In static implementations, the pre-amplifier is a continuous-time amplifier. The most popular comparators for SAR ADCs belongs to the second category where the preamplifier is clocked, i.e., it is enabled by a signal. They are called dynamic because they draw current from the power supply only when there is a transition, in this case when comparing the inputs, similar to what happens in a digital circuit. There is no DC current in a dynamic comparator. This means that there is an inherent reduction in the power consumption with respect to static topologies.

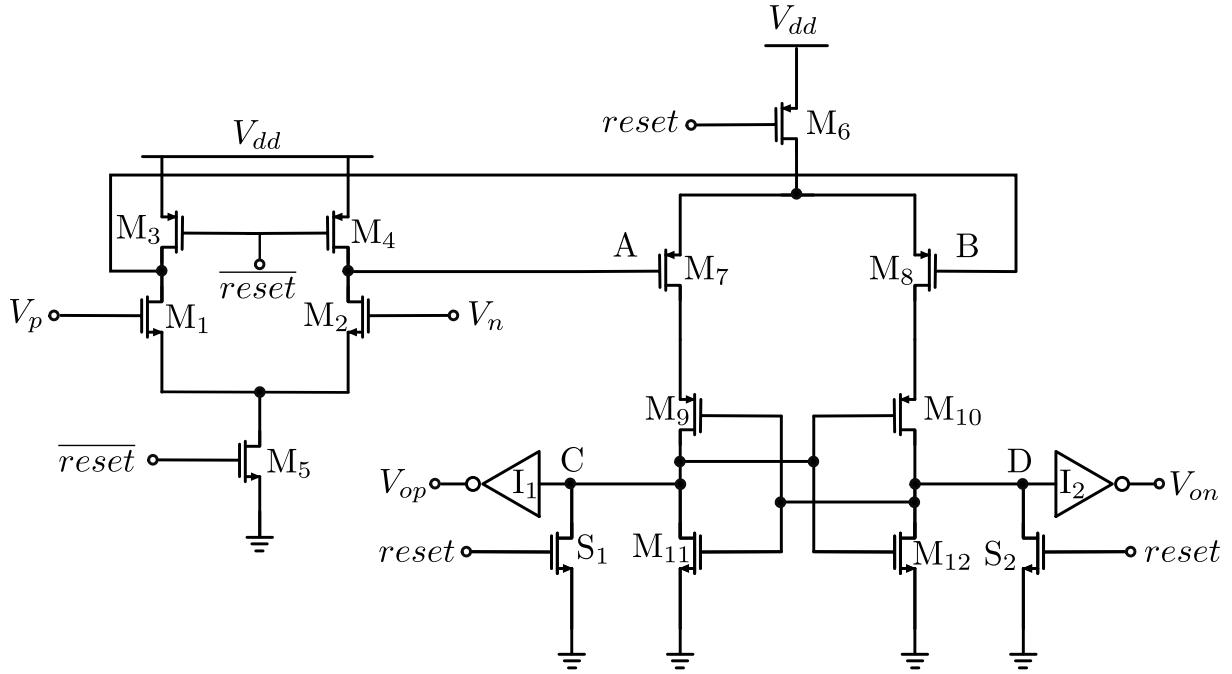
### 2.6.1 Dynamic comparator

Two-stage dynamic comparators are usually composed by two main parts: a clocked preamplifier followed by a latch. A possible choice for a SAR ADC is the dynamic comparator used by Brenna *et al.* in [23], shown in Figure 2.20 with NMOS input transistors, based on the double-tail latch sense amplifier proposed in [24].

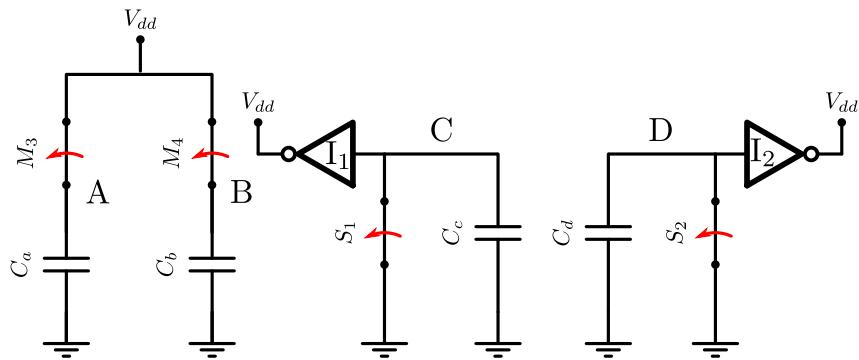
#### Circuit description

There are two stages. The first one is a clocked preamplifier, whereas the second one is a differential latch. Its basic operation has two main phases: the reset and the comparison phase. In the reset phase, the *reset* signal is high. An equivalent circuit for the reset phase is shown in Figure 2.21 with the parasitic capacitors present in each node. Transistors  $M_5$  and  $M_6$  are off, therefore no current flows in  $M_1$ - $M_2$  and  $M_7$ - $M_8$ . Nodes A and B are pre-charged to  $V_{dd}$  by transistors  $M_3$ - $M_4$ , whereas C and D are discharged to ground by  $S_1$ - $S_2$ , setting the output of the comparator to the supply voltage through the inverters  $I_1$ - $I_2$ .

In the next phase, the *reset* signal is pulled down and the comparison phase starts. In the first stage,  $M_5$  is turned on and  $M_3$ - $M_4$  are turned off, whereas in the second stage  $S_1$ - $S_2$  are off and  $M_6$  is turned on. A current flows into the differential pair allowing the discharge of A and B with a different rate depending on the applied signals as shown in Figure 2.22. Once the input differential pair of the second stage is active the signal will be regenerated by the latch. Let us suppose that the current in the branch connected to  $M_7$  is larger than the one in  $M_8$ . The voltage  $V_c$  increases until  $M_{12}$  starts to conduct current. At the same time, the voltage at the node D is raised by the current flowing in the other branch. However,  $M_{12}$  slows down the voltage increase, avoiding that  $M_{11}$  turns on, until its gate-source voltage is large enough to tie D to ground. The cross-coupled inverters  $M_9$ - $M_{11}$  and  $M_{10}$ - $M_{12}$  effectively implement a positive



**Figure 2.20:** Schematic of the dynamic comparator.

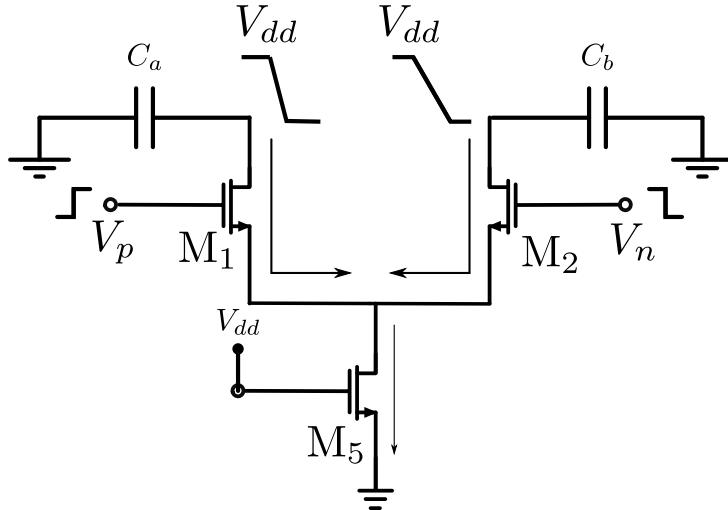


**Figure 2.21:** Equivalent circuit for the reset phase.

feedback loop to regenerate the amplified analog signal to a rail-to-rail digital signal. The inverters  $I_1$ - $I_2$  allow to have sharp transitions to drive the following capacitive load.

During the reset and the comparison phase, there are large voltage transitions as a consequence of the large transient currents drawn during the circuit operation. This voltage variations are then coupled back to the input of the comparator through the parasitic capacitors in the circuit as shown in Figure 2.23. This effect is called *kickback* noise. It can be also caused from the sharp transitions of the *reset* signal. Being the DAC a high-impedance source and the input capacitance of the transistor pair a function of the gate voltage, kickback results in non-linearities during the conversion. Therefore, the dimension of the input pair needs to be as small as possible to reduce the gate-drain and gate-source capacitances while at the same time big enough to drive a large current to satisfy the timing constraints.

In conclusion, the dynamic comparator has a low power consumption and it is a good candidate to be implemented in the design of a SAR ADC. However, kickback noise is problematic because it adds variations of the output voltage of the DAC of the order of the LSB, thus introducing errors during conversion.



**Figure 2.22:** Equivalent circuit of the first stage during the comparison, from [25].

## 2.6.2 Static comparator

Kickback noise is a problem for moderate-high resolution SAR ADCs when the voltage variation due to the kickback is comparable with the value of the LSB. Static comparators experience less abrupt voltage variations during the comparison of the input signal and the drain of the input differential pair is more isolated from the regenerative nodes[26]. A possible topology is shown in Figure 2.24 [17]. The schematic consists of a static preamplifier with a mirrored architecture followed by a fully-differential latch. At the output of the latch, there are two inverters to enhance the driving of the following capacitive load.

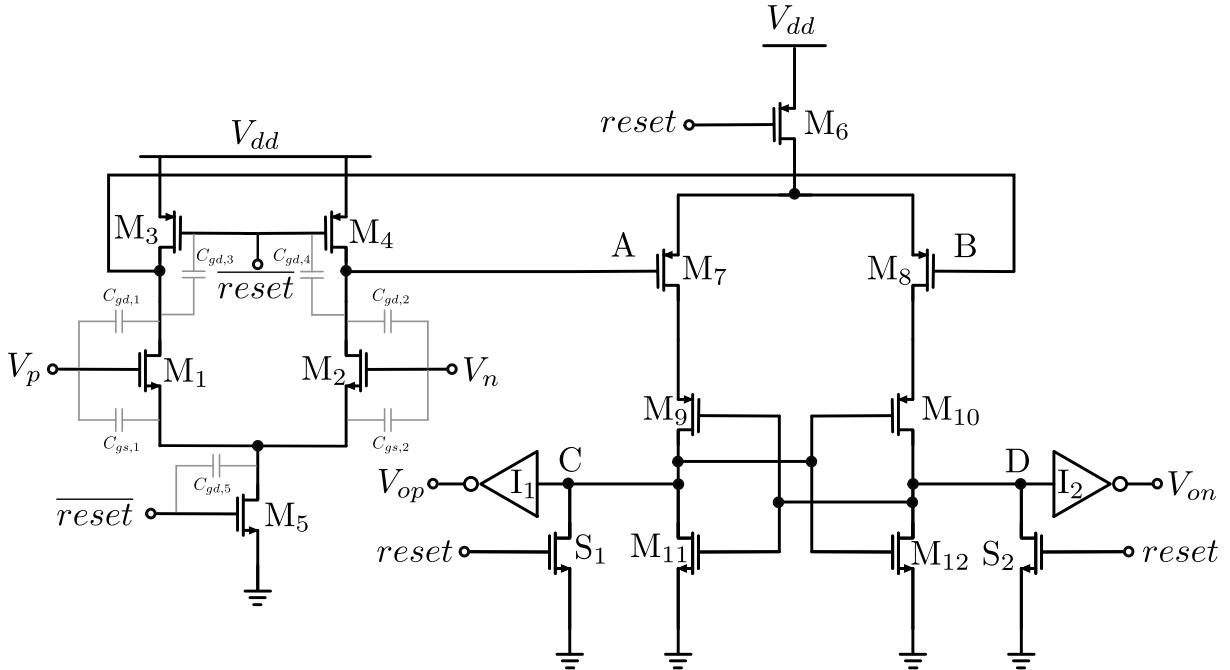
The load of the differential pair,  $M_1$ - $M_2$ , is formed by two transistors in a transdiode configuration. Therefore, the nodes A and B are low-impedance nodes, allowing a reduction of kickback. The input signal is subjected to a low amplification in the first stage of the preamplifier. The differential current in the first stage is mirrored through the couples  $M_3$ - $M_6$  and  $M_4$ - $M_7$ , then, it flows into the resistances  $R_G$  obtaining an amplified differential signal at the input of the latch.

The major difference with respect to a dynamic implementation is the static current in the preamplifier, which results in a larger power consumption. One possible way to reduce the power consumption is to switch on the comparator only during conversion, while switching it off in the sampling phase.

## 2.7 SAR logic

The SAR logic controls the operation of the converter. The digital circuit that implements the SA algorithm in a synchronous ADC is clocked at a frequency  $N+1$  times larger than the sampling frequency. One clock cycle is reserved for the sampling and the remaining ones for the conversion. For instance, in a 12-bit 200-MSps SAR ADC, the clock network is required to distribute a 2.6-GHz clock signal, dissipating a large power consumption. Due to the lack of a high-frequency clock, an asynchronous logic reduces the power consumption, thus it is the preferred solution in SAR ADCs at medium-high sampling frequencies. Another way to further reduce the power consumption of the logic circuit is through dynamic logic gates, which also allow an area reduction with respect to a static implementation[27].

The feedback loop of a SAR ADC is composed by the comparator, the control logic and the DAC. Each conversion cycle in a synchronous system proceeds in three main steps[12], as shown in Figure 2.25. At the beginning of the cycle, the  $i$ -th bit of the DAC is set. Then, when the result of the comparison is available at the output of the comparator, the SAR register corresponding to the bit being evaluated stores the result and the conversion proceeds with the evaluation of the following bit. The lower bound



**Figure 2.23:** Schematic of the comparator with some of the parasitic capacitors present in the circuit.

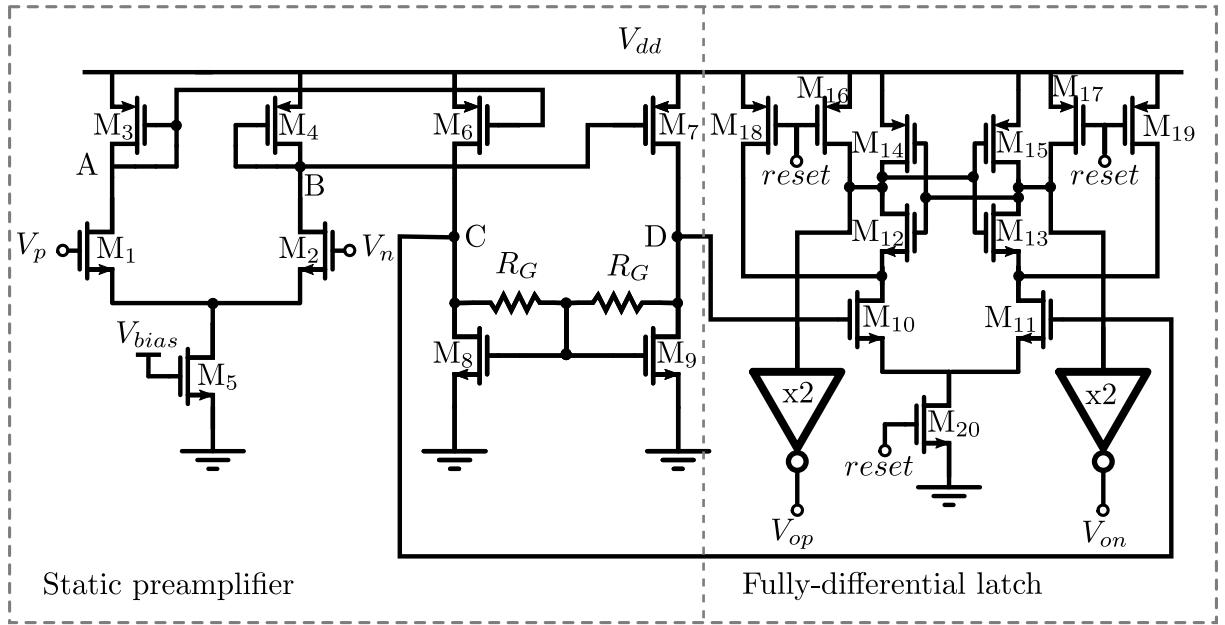
of the length of the clock period is set by the sum of the duration of all the operations performed in each bit evaluation:

- comparison,
- DAC settling,
- bit storing.

In a real implementation, a margin is added to account for non-idealities such as process, voltage and temperature variations. It is possible to assume that DAC settling and bit storing are operations whose duration is fixed, since they last approximately the same in each bit evaluation, whether a 1 or a 0 is stored in the registers. The comparison time is, instead, a function of the voltage difference at the input of the comparator. Indeed, the larger the voltage difference to compare, the smaller is the regeneration time of the latch in the comparator. This means that the clock period for a synchronous SAR ADC is limited by the worst-case scenario, i.e., when the voltage difference at the comparator input falls within  $\pm 0.5$  LSB, and this happens at most one time among the N conversion steps[28]. An asynchronous configuration enables a more efficient way to perform the bit evaluations. Each conversion step is triggered autonomously right after the comparator decision and the subsequent operations have concluded. Therefore, each conversion step lasts differently, based on the input signal, enabling a more efficient management of the time available for conversion. Bit evaluations with large differential voltages at the DAC outputs require less time, whereas more time is needed for small differential voltages. A quantitative treatment of the advantages, in terms of speed, of an asynchronous design over a synchronous one for data converters can be found in [29]. For the advantages mentioned above, the converter presented in this report is controlled by an asynchronous logic.

## 2.8 SAR energy breakdown

The energy dissipated by the SAR ADC can be investigated through the model proposed in [30].



**Figure 2.24:** Schematic of the static comparator[17].

## Comparator

The design of the comparator is guided by noise and speed considerations. The thermal noise introduced by the comparator should not limit the resolution of the converter. Moreover, the comparator must satisfy the speed requirements imposed by the sampling frequency.

Let us consider the static comparator. As it will be shown in the next chapter, the variance of the input-referred voltage thermal noise of the comparator in Figure 2.24 can be expressed as:

$$\sigma_{in,static}^2 = 2 \frac{4kT\gamma}{g_{m,1}} (1 + \alpha) \frac{\pi}{2} BW, \quad (2.19)$$

where  $k$  is the Boltzmann coefficient,  $T$  the temperature,  $\gamma$  a coefficient that depends on the technology (typically 1 for sub-micrometer technology nodes),  $g_{m,1}$  is the transconductance of the input pair transistors,  $\alpha$  is a coefficient to take into account the noise contribution of elements other than the input transistor pair and  $BW$  is the bandwidth of the preamplifier. Based on the noise requirements, it is possible to obtain the bias current,  $I_B$ , of the tail transistor needed in the first stage of the preamplifier. If we assume that the noise is half the LSB for a fully-differential converter, it results:

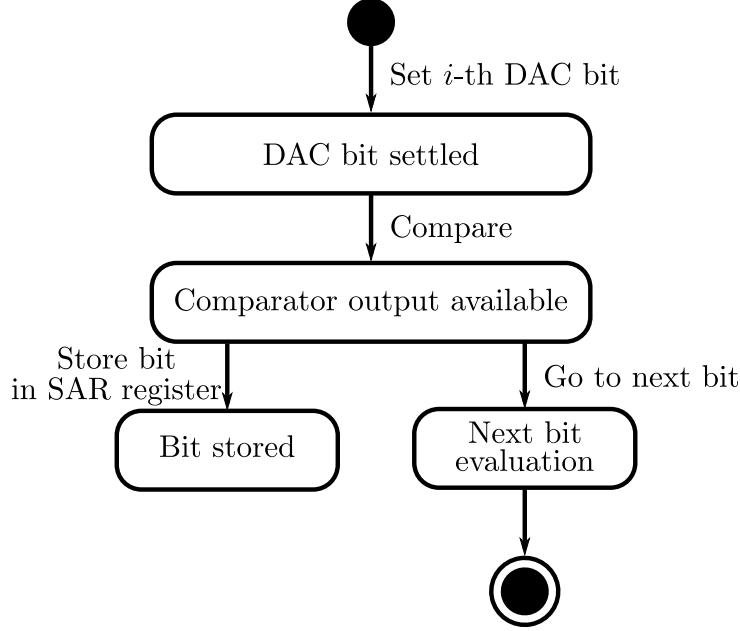
$$\left( \frac{LSB}{2} \right)^2 = \frac{V_{dd}^2}{2^{2n}} = 2 \frac{4kT\gamma}{g_{m,1}} (1 + \alpha) \frac{\pi}{2} BW, \quad (2.20)$$

where  $n$  is the number of bits of the ADC. The transconductance of the transistors in the input pair can be written as  $I_B/V_{ov}$ , where  $I_B$  is the current flowing into the tail transistor and  $V_{ov}$  the overdrive voltage of the differential pair transistors. It is possible to obtain, thus, the bias current of the preamplifier as:

$$I_B = \frac{V_{ov}}{V_{dd}^2} 2^{2n} 4kT\gamma (1 + \alpha) \frac{\pi}{2} BW. \quad (2.21)$$

The bandwidth of the preamplifier is related to the time available for conversion. Indeed, the time for the comparison can be estimated as:

$$T_{comp} = \frac{T_s}{2} \cdot \frac{1}{2} \cdot \frac{1}{n}, \quad (2.22)$$



**Figure 2.25:** State diagram for one bit cycle.

i.e., half the sampling period is available for conversion, in which  $n$  comparisons take place and, in each half of the  $n$  time slots, the comparator performs the evaluation (the other half is allocated for resetting the comparator). In a real implementation, the bandwidth of the preamplifier would be larger than  $1/T_{comp}$ , but, here, for the sake of simplicity, it is possible to consider  $BW = 1/T_{comp}$ . The energy per conversion of the comparator can, thus, be written as:

$$E_{comp} = T_s I_B V_{DD} + n C_{latch} V_{dd}^2 = \frac{V_{ov}}{V_{dd}} n 2^{2n} 4kT\gamma(1+\alpha)2\pi + n C_{latch} V_{dd}^2 \quad (2.23)$$

where  $T_s$  is the sampling period and  $C_{latch}$  is the total capacitance at the output of the latch.

If, instead, a dynamic comparator is considered (see Figure 2.20), the energy dissipated is the one needed to reset the capacitances  $C_a$  and  $C_b$ . Considering that  $n$  comparisons are carried out, the energy dissipated in each conversion can be expressed as:

$$E_{comp,dyn} = 2 \cdot n C_a V_{dd}^2 + n C_{latch} V_{dd}^2, \quad (2.24)$$

where the factor 2 accounts for the reset of two nodes (it was assumed  $C_a = C_b$ ). As it will be shown more in detail in the next chapter, the capacitance is set based on noise considerations and, assuming an input-referred noise equal to  $\frac{LSB}{2}$ , it becomes:

$$C_a = \frac{4kT\gamma}{(\frac{LSB}{2})^2} \frac{V_{cm} - V_{th,n}}{V_{th,p}}, \quad (2.25)$$

where  $V_{th,n}$  and  $V_{th,p}$  are the threshold voltages of an NMOS and a PMOS transistor, respectively. Note that  $V_{cm} - V_{th,n}$  is the overdrive voltage of the input differential pair,  $V_{ov}$ . Combining Eq. (2.24) and Eq. (2.25), we obtain:

$$E_{comp,dyn} = 2 \cdot n 2^{2n} 4kT\gamma \frac{V_{ov}}{V_{th,p}} + n C_{latch} V_{dd}^2. \quad (2.26)$$

## DAC

The energy drawn by the DAC depends on the switching algorithm, the DAC architecture and the input signal. The average energy consumption of the DAC can be written as [30]:

$$E_{ave} \approx 2 \cdot \beta 2^n C_u V_{dd}^2, \quad (2.27)$$

---

where  $\beta$  is a coefficient computed based on the energy reported in Section 2.5. In the conventional SAR ADC,  $\beta$  is 0.66, whereas it reduces to 0.2 and 0.12 for the split CDAC and monotonic switching algorithm, respectively. The factor 2 accounts for the implementation of a fully-differential structure. The unit capacitance can be chosen based on noise constraint, namely the thermal noise when sampling the signal on the DAC, and linearity consideration, caused by mismatch. From the previous section, the variance of the maximum DNL for the monotonic algorithm is:

$$\sigma_{DNL,monotonic}^2 = 2^{n-1} \frac{\sigma_u^2}{C_u^2}. \quad (2.28)$$

The standard deviation can be written in terms of the Pelgrom coefficient,  $k_c$ , and the capacitance per unit area,  $c_{spec}$ , as:

$$\frac{\sigma_u}{C_u} = k_c \sqrt{\frac{c_{spec}}{2C_u}} \quad (2.29)$$

The DNL is set typically smaller than half the LSB, i.e,

$$\sigma_{DNL,monotonic} \leq \frac{1}{2}. \quad (2.30)$$

Thus, the minimum capacitance can be obtained using Eq. (2.28) and Eq. (2.29) in the inequality shown above, resulting in:

$$C_u \geq 2^n k_c^2 c_{spec}. \quad (2.31)$$

Plugging the minimum capacitance into Eq. (2.27) results in:

$$E_{ave} = 2 \cdot \beta 2^{2n} k_c^2 c_{spec} V_{dd}^2. \quad (2.32)$$

For the DAC array, the energy required for sampling depends on the input signal. If we consider the input signal comparable to  $V_{dd}$ , the sampling energy can be written as:

$$E_s \approx 2C_{tot}V_{dd}^2, \quad (2.33)$$

where  $C_{tot}$  is the total capacitance of the DAC and the factor 2 because the signal is sampled on two DACs in a fully-differential SAR ADC. Therefore, the DAC energy consumption per conversion becomes:

$$E_{DAC} = E_{ave} + E_s = 2 \cdot \beta 2^{2n} k_c^2 c_{spec} V_{dd}^2 + 2 \cdot 2^{n-1} C_u V_{dd}^2. \quad (2.34)$$

## SAR logic

Following the same argument in [30], the energy per conversion in the logic can be modeled as:

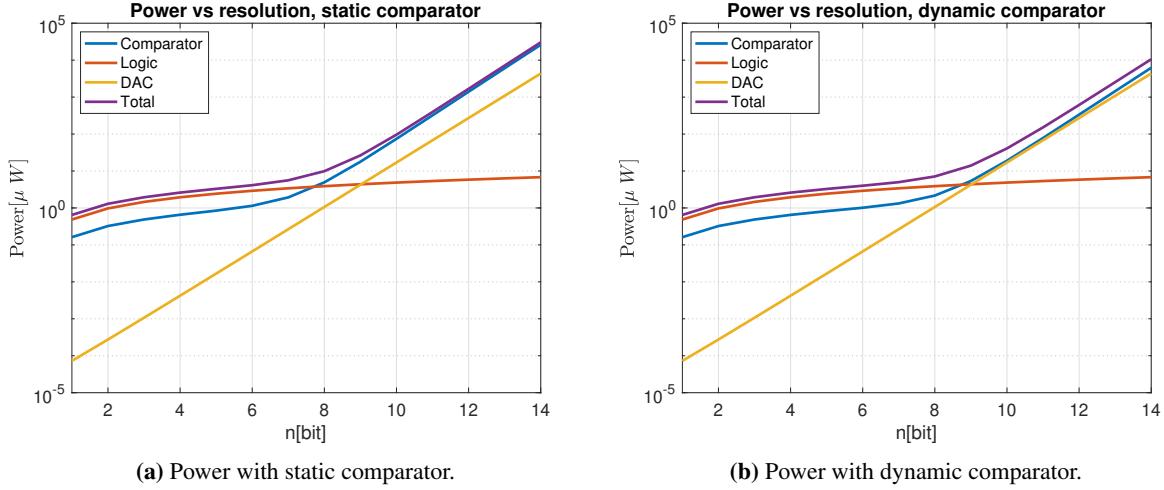
$$E_{logic} = nC_{logic,tot}V_{dd}^2, \quad (2.35)$$

where  $C_{logic,tot}$  is the total capacitance switched in the logic. The energy grows with  $n$  because the SAR logic is typically implemented with an  $n$ -shift registers.

## Total energy

If we sum together Eq. (2.23), Eq. (2.32) and Eq. (2.35), we obtain the energy per conversion with a static comparator

$$E_{tot} = nC_{lach}V_{dd}^2 + nC_{logic,tot}V_{dd}^2 + 2 \cdot \beta 2^{2n} k_c^2 c_{spec} V_{dd}^2 + \frac{V_{ov}}{V_{dd}} n 2^{2n} 4kT\gamma(1 + \alpha)2\pi + 2 \cdot 2^{n-1} C_u V_{dd}^2, \quad (2.36)$$



**Figure 2.26:** SAR power of the comparator, DAC and logic.

whereas the total energy per conversion with a dynamic comparator is

$$E_{tot,dyn} = nC_{latch}V_{dd}^2 + nC_{logic,tot}V_{dd}^2 + 2 \cdot \beta 2^{2n}k_c^2c_{spec}V_{dd}^2 + 2 \cdot n2^{2n}4kT\gamma \frac{V_{ov}}{V_{th,p}} + 2 \cdot 2^{n-1}C_uV_{dd}^2. \quad (2.37)$$

Let us assume, for instance, that the capacitance at the output of the comparator is 1 fF for simplicity and that the logic capacitance is greater due to the larger number of capacitances that are switched in the logic, like 2 fF. Moreover, let us consider that the threshold voltage is 400 mV, the overdrive voltage of the comparator is about 100 mV,  $\alpha$  is about 1 and  $\beta$  is 0.12 (monotonic switching algorithm). From the mismatch characterization reported in [31, 32], we can assume that a Pelgrom coefficient of about  $1\% \times 1 \mu m$  for a metal-oxide-metal (MOM) capacitance (to implement the DAC) and a unit capacitance per unit area around  $1 fF/\mu m^2$  are reasonable approximations. If we plot the power, i.e., the energy times the sampling frequency (200MSps), of each component of the SAR ADC, we obtain a similar result to [30], as shown in Figure 2.26. At low resolution the SAR ADC energy consumption is dominated by the logic. Increasing the resolution makes the dominant contributions of the DAC and comparator grow as  $2^{2n}$  and  $n2^{2n}$ , thus for a 12-bit SAR ADC we expect that the logic is the least energy-consuming block. Albeit the model is rather simple, it can be helpful to the designer to have an idea about the order of magnitude of the expected energy consumption of the SAR ADC blocks. From the model, the power consumption are expected to be  $335 \mu W$  and  $1.4 mW$  employing the dynamic or the static comparator, respectively. The DAC power consumption is expected to be  $271 \mu W$ , whereas approximately  $6 \mu W$  are required by the logic circuit. It is possible to conclude that the DAC and comparator are the most energy-hungry components for a 12-bit SAR ADC and most of the energy is consumed by the comparator, whatever the choice of the topology. Therefore, when designing a SAR ADC with the specifications mentioned in Chapter 1, it is important to reduce the power consumption of DAC and comparator in order to design a low-power converter, based on the assumptions made earlier.

## 2.9 Summary

In this chapter, various DAC architectures and switching schemes were presented. After a brief introduction about AD converters, the monotonic switching algorithm allows to reduce both area and power consumption with a good linearity. The modified version of the monotonic switching algorithm reduces the variation of the common mode voltage at the input of the comparator, thus reducing the complexity

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of the comparator design. For the comparator, a dynamic implementation allows to obtain a smaller power consumption with respect to a static implementation. However, a dynamic comparator suffers from kickback noise that causes errors during the conversion. A static comparator helps reduce the effect of kickback noise at the cost of a larger power consumption. The SAR ADC is controlled by the logic circuit that can operate synchronously or asynchronously. A synchronous implementation requires a high-frequency clock, which implies a large power consumption for medium-high sampling frequency. Thus, an asynchronous logic helps reduce power consumption and area. The cost of this asynchronous implementation is a longer development time, since a synchronous logic can also be synthesized from an HDL model with IPs provided by the foundries, whereas the logic gates needs to be manually implemented at transistor level in an asynchronous design. Furthermore, there is a more efficient management of the time available for conversion in an asynchronous logic because the conversion cycles are self-synchronized. Finally, most of the power consumption in a 12-bit SAR ADC is divided between the comparator and DAC, whereas the logic circuit consumes a negligible energy. In the next chapter, the design of a 12-bit 200-MSps SAR ADC is presented, based on the considerations presented above.



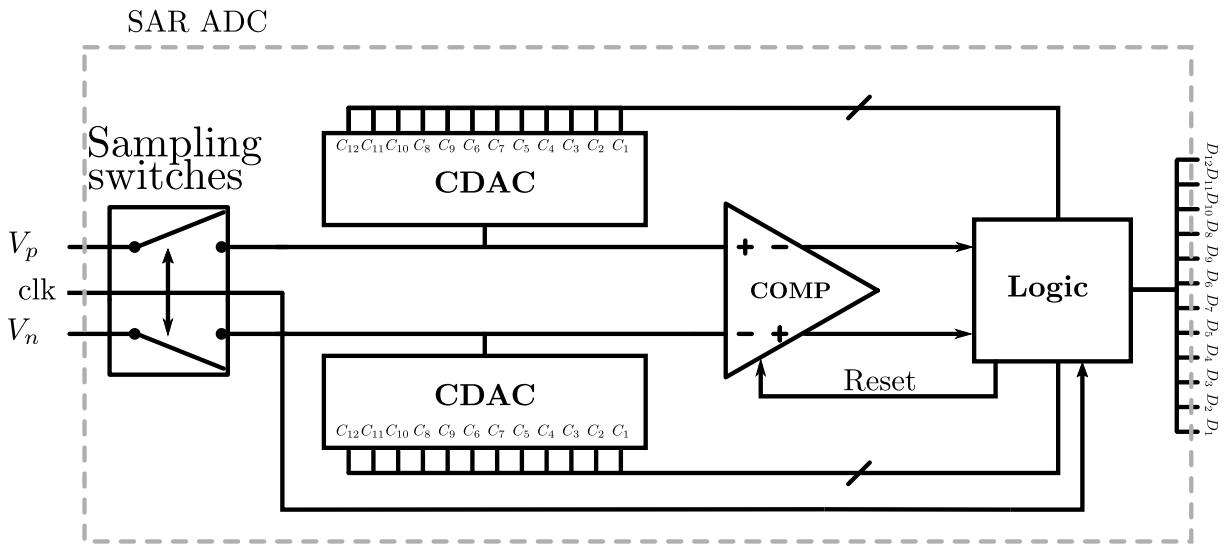
# Chapter 3

## Circuit design

The design of the circuits of the SAR ADC is described in this chapter.

### 3.1 Top level

The schematic of the fully-differential ADC is shown in Figure 3.1. The adopted switching scheme is the modified monotonic switching procedure explained in Section 2.3.4. In this procedure, the input



**Figure 3.1:** Schematic of the the SAR ADC.

signals,  $V_p$  and  $V_n$ , are sampled on the top plates of the DACs. Initially, the sampling switches are activated by the sampling signal,  $clk$  in Figure 3.1. Then, the SA algorithm starts and the conversion of the input signal is carried out. During the conversion, each bit is determined based on the result of the comparison performed by the comparator. In each bit evaluation, the logic control circuit opportunely controls the DAC inputs, which are switched either to the supply voltage,  $V_{dd}$  (0.9 V) or ground. At the same time, the comparator is reset by the asynchronous logic through the *Reset* signal. Each DAC is a 12-bit binary-weighted array of capacitors.

At the beginning of the design, each block of the system was a behavioral model written in Verilog-A. Then, the circuits were designed at transistor level replacing the behavioral models.

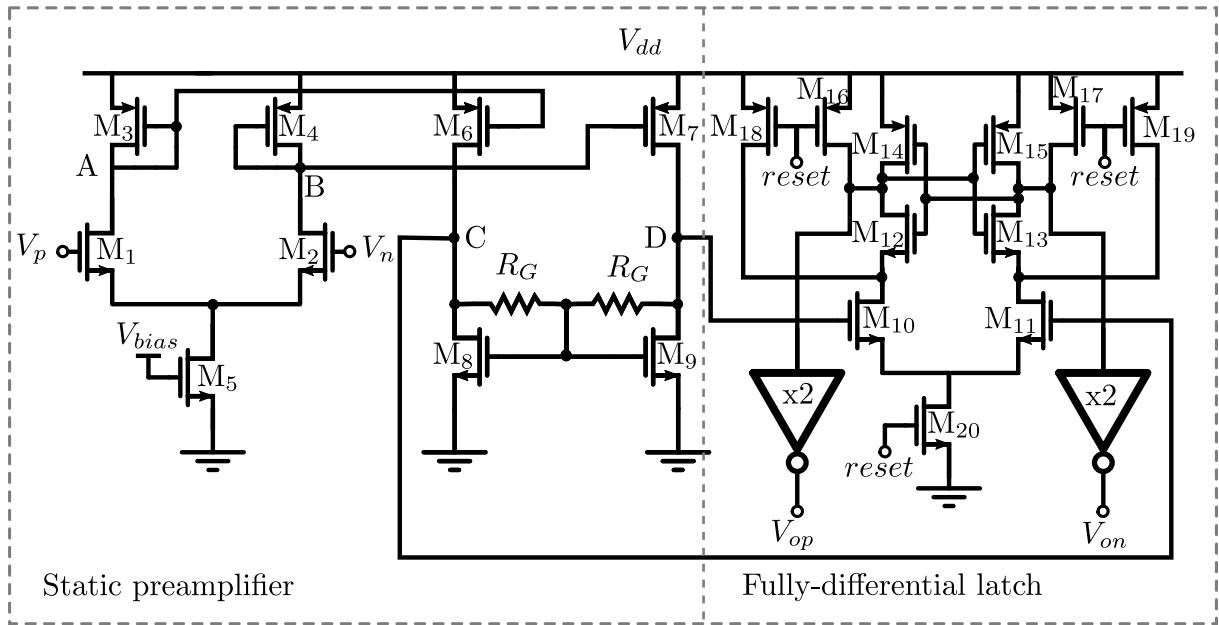
During the design of the converter, a dynamic and static comparator were implemented and simulated. A static comparator and a dynamic comparator. The reason behind this is the kickback noise of the

dynamic comparator. For a 12-bit resolution, the LSB is of the order of few hundreds of  $\mu V$ , therefore the kickback noise can be considered a problem, limiting the resolution of the ADC. After the design of the two comparators, it was found that the performance of the dynamic comparator in the SAR ADC was better than those obtained with the static one. Therefore, the dynamic comparator was chosen in the end. The DAC is based on a custom-designed capacitor. The choice to design a custom capacitor was taken to reduce the energy consumption of the DACs. In this SAR ADC, the sampling switches are bootstrapped in order to not limit the linearity of the ADC. Finally, an asynchronous logic (a behavioral model in Verilog-A) controls the operations of the SAR ADC. The following sections are dedicated to the description of the designed circuits. As a reminder, the ADC is designed to satisfy the following requirements:

- 12-bit resolution,
- 200-MSps sampling frequency,
- ENOB larger than 10 bits and
- a FoM of approximately 10 fJ/conv-step.

### 3.2 Static comparator

The implemented static comparator is shown in Figure 3.2. A brief description of the circuit has been already given in Section 2.6.2. Here, the following analysis is used as a starting point to design the circuit.



**Figure 3.2:** Schematic of the implemented static comparator[17].

In the first stage, the differential current due to an input differential signal is mirrored by the couples M<sub>3</sub>-M<sub>6</sub> and M<sub>4</sub>-M<sub>7</sub> and then amplified through the resistors  $R_G$ . At a first order approximation, the voltage gain of the preamplifier can be expressed as:

$$G \approx g_{m,1} \left( \frac{g_{m,6}}{g_{m,3}} \right) R_G, \quad (3.1)$$

assuming equal transconductance for the transistor pairs M<sub>1</sub>-M<sub>2</sub>, M<sub>3</sub>-M<sub>4</sub>, M<sub>6</sub>-M<sub>7</sub>.

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Regarding the frequency response, there are two poles. The first pole depends on the capacitance at the nodes A and B, whereas the second one is related to the parasitics at the nodes C and D. The frequency of the poles can be expressed as:

$$f_{p,A} \approx \frac{g_{m,3}}{2\pi C_A}, \quad (3.2)$$

$$f_{p,B} \approx \frac{1}{2\pi R_G C_C}, \quad (3.3)$$

where  $C_A$  and  $C_C$  are the total capacitances between node A and ground and between node C and ground, respectively. Since A and B are low-impedance nodes, it was assumed that the dominant pole is  $f_{p,B}$ . The amplifier bandwidth is set based on the time slot allocated to each bit evaluation. Note that the value of the pole can be set acting on the resistance  $R_G$  and the capacitor  $C_C$ . Since the capacitor  $C_C$  is given by the drain capacitance of M<sub>8</sub>, M<sub>6</sub>, M<sub>11</sub>, it is easier to choose the pole frequency setting the value of the resistor.

Considering the noise introduced by the latch negligible with respect to that of the first stage, the power spectral density of the input-referred thermal voltage noise can be expressed, with a first order approximation, as[17]:

$$\begin{aligned} S_{n,in} &= 2 \cdot \frac{4kT\gamma}{g_{m,1}} \left\{ 1 + \underbrace{\frac{g_{m,3}}{g_{m,1}} \left[ 1 + \frac{g_{m,3}}{g_{m,6}} \left( 1 + \frac{g_{m,8} + \gamma/R_g}{g_{m,6}} \right) \right]}_{\alpha} \right\} \\ &= 2 \cdot \frac{4kT\gamma}{g_{m,1}} (1 + \alpha), \end{aligned} \quad (3.4)$$

where  $\alpha$  is a coefficient that takes into account the other noise sources. Therefore, the total input-referred thermal voltage noise is:

$$\sigma_{in}^2 = S_{n,in} \cdot \frac{\pi}{2} BW, \quad (3.5)$$

where BW is the bandwidth of the circuit, set by the dominant pole. If we set that the noise of the comparator should be  $N$  times smaller than the LSB, it is possible to obtain the transconductance of the input differential pair:

$$g_{m,1} = \frac{4kT\gamma}{(\frac{LSB}{N})^2} (1 + \alpha) \cdot \pi BW, \quad (3.6)$$

and consequently, the current  $I_T$  of the tail transistor, M<sub>5</sub>:

$$I_T = \frac{4kT\gamma}{(\frac{LSB}{N})^2} (1 + \alpha) V_{ov} \cdot \pi BW. \quad (3.7)$$

After this brief analysis, the circuit was designed considering the constraint of the system. Since the SAR ADC has a sampling frequency of 200 MSps, the sampling period lasts 5 ns. Half of the sampling period is dedicated to the conversion, i.e. 2.5 ns. Dividing the available conversion time equally for the 12 bits, each conversion should last 208 ps. In each conversion step, the following operations are carried out:

- comparison,
- comparator reset,
- DAC settling.

Let us assume that half of the time in each conversion step is allocated for comparison, whereas the other half for comparator reset and DAC settling. Therefore, the comparator should be designed to compare the input signal in approximately 100 ps.

To summarize, the static comparator should perform an evaluation approximately every 200 ps, i.e., 1/5 GHz. Therefore, let us consider a slightly larger bandwidth of 7 GHz. Assuming:

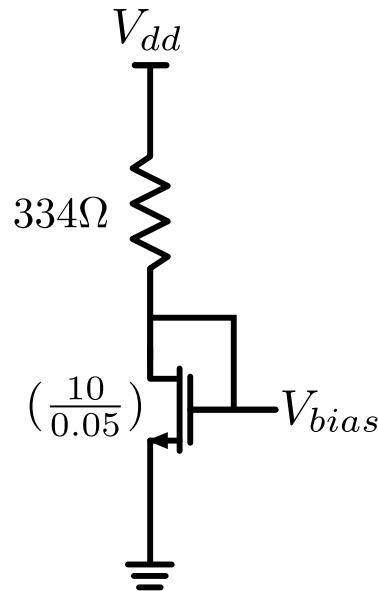
- $N = 2$ , i.e., the comparator noise is equal to half LSB,
- $\alpha = 1$ , that is, the noise introduced by  $M_1$ - $M_2$  is comparable to the other noise sources in the circuit,
- an overdrive voltage of 100 mV for the input differential pair,

the current required by the tail transistor is  $I_T = 1.5 \text{ mA}$ . In the end, a current of 1.6 mA was chosen. The bandwidth was set to 7.1 GHz, which corresponds to a time constant of approximately  $\frac{1}{2\pi 7.1 \text{ GHz}} \approx 22 \text{ ps}$ , with a gain of the preamplifier equal to 9.6. In this case, the bandwidth of the preamplifier was set finding a balance between the noise of the circuit and the amplification of the input signal.

| Transistor    | $\frac{W \text{ [\mu m]}}{L \text{ [\mu m]}}$ | Transistor          | $\frac{W \text{ [\mu m]}}{L \text{ [\mu m]}}$ |
|---------------|---|---------------------|---|
| $M_1$ - $M_2$ | $\frac{58.5}{0.05}$                           | $M_{10}$ - $M_{11}$ | $\frac{2.5}{0.03}$                            |
| $M_3$ - $M_4$ | $\frac{20}{0.1}$                              | $M_{12}$ - $M_{13}$ | $\frac{0.2}{0.03}$                            |
| $M_5$         | $\frac{18}{0.05}$                             | $M_{14}$ - $M_{15}$ | $\frac{0.2}{0.03}$                            |
| $M_6$ - $M_7$ | $\frac{30}{0.1}$                              | $M_{16}$ - $M_{17}$ | $\frac{0.6}{0.03}$                            |
| $M_8$ - $M_9$ | $\frac{10}{0.1}$                              | $M_{18}$ - $M_{19}$ | $\frac{0.3}{0.03}$                            |
| $M_{20}$      |   |                     | $\frac{1}{0.03}$                              |

**Table 3.1:** Dimensions of the transistors in the static comparator.

The dimensions of the transistors in the comparator are shown in Table 3.1. Note that each transistor in the preamplifier consists of 10 unit transistors (in the table there is the total width of the transistor). This allows the possibility to place the differential pairs in a common-centroid structure to increase matching. The resistor  $R_G$  was set to  $1.79 \text{ k}\Omega$ . The tail transistor,  $M_5$ , was biased with the circuit shown

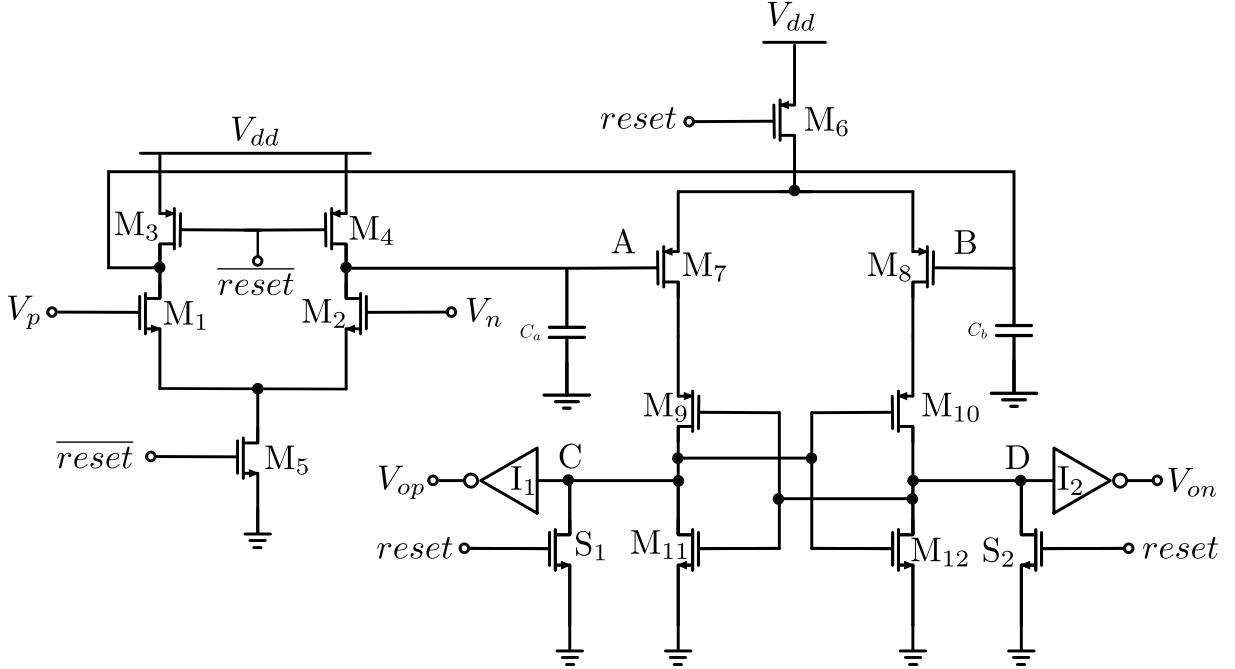


**Figure 3.3:** Biasing circuit of the tail transistor.

in Figure 3.3. The biasing voltage,  $V_{bias}$ , was 450 mV.

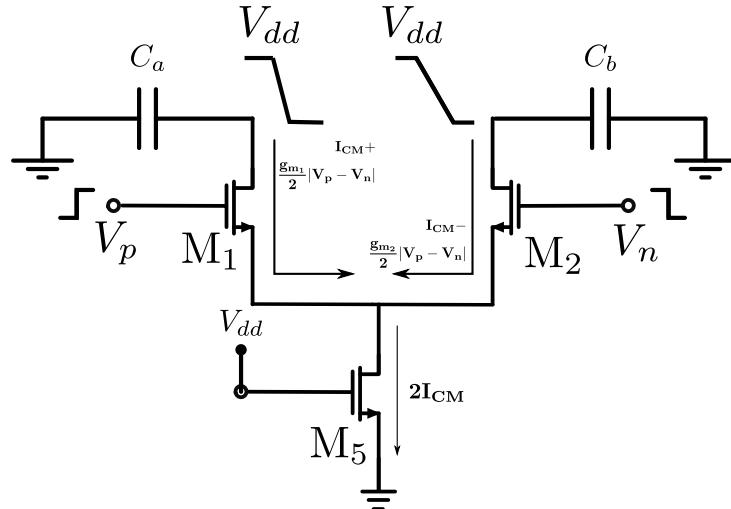
### 3.3 Dynamic comparator

The initial schematic of the designed dynamic comparator is shown in Figure 3.4. The basic circuit op-



**Figure 3.4:** Initial schematic of the implemented dynamic comparator.

eration is already described in Chapter 2. Let us consider more in detail what happens in the comparison phase. The following analysis was the basis for the design of the circuit, similar to the one reported in [25].



**Figure 3.5:** Equivalent circuit of the first stage during the comparison.

The rate of discharge at the output of the first stage is proportional to the differential input signal  $|V_p - V_n|$ . The variation of the voltage as a function of time at nodes A and B can be written at a first

order approximation as:

$$V_a(t) \approx V_{dd} - \frac{I_{CM}}{C_a} t + \frac{g_{m1}}{2} \frac{|V_p - V_n|}{C_a} t, \quad (3.8)$$

$$V_b(t) \approx V_{dd} - \frac{I_{CM}}{C_b} t - \frac{g_{m2}}{2} \frac{|V_p - V_n|}{C_b} t, \quad (3.9)$$

where  $I_{CM}$  is the common mode current and  $g_{m1}$  and  $g_{m2}$  are the transconductance of  $M_1$  and  $M_2$ , respectively. An equivalent circuit can be seen in Figure 3.5. The current flowing in  $M_1$ - $M_2$  will be integrated on the output capacitances building up a differential signal to drive the following stage:

$$|V_a - V_b| \approx g_{m1} \frac{|V_p - V_n|}{C_a} t, \quad (3.10)$$

where  $C_a = C_b$  and  $g_{m1} = g_{m2}$ . Note that the voltage gain  $\frac{g_{m1}}{C_a} t$  of the first stage, i.e., the ratio  $\left| \frac{V_a - V_b}{V_p - V_n} \right|$ , increases with time. Of course, it cannot increase indefinitely because the transistors go in triode region after some time.  $M_7$  and  $M_8$  turn on when their source-gate voltage reaches the threshold voltage,  $V_{th,p}$ . Thus, the integration time of the current can be written as:

$$T_{int} \approx \frac{C_a}{I_{CM}} V_{th,p}. \quad (3.11)$$

The integration time is a parameter that is set by the system constraint, i.e., it is related to the time available for comparison in the converter. Therefore, the current is chosen based on the required comparison speed. The capacitor value is, instead, chosen based on noise requirements.

### Noise and power consumption

The noise of a clocked comparator for a 12-bit SAR ADC plays an important role, because the LSB is of the order of hundreds of  $\mu V$  considering a supply voltage around 1 V. As explained above, the comparator does not compare the input signal continuously, but there are distinct phases. For this reason, the noise analysis is not the same as for a continuous time comparator where the circuit is linearized around the working point. The following analysis is based on [33] and it was used to obtain first order equations about noise and power consumption of the comparator. Note that here only the noise due to the input differential pair is considered. There is also noise caused by  $M_3$ - $M_4$ , which behave as switches, thus kT/C noise, but it was assumed that their contribution is negligible. Moreover, the noise of the second stage has been neglected for simplicity. However, the results show that this is not properly correct (see next chapter).

The power spectral density of the thermal current noise in a MOS transistor working in saturation region is:

$$\overline{i_n^2} = 4kT\gamma g_m, \quad (3.12)$$

where  $k$  is the Boltzmann constant,  $T$  is the temperature in Kelvin and  $\gamma$  is a coefficient typically close to 1 for sub-micrometer technology nodes. When the comparison starts, the noise current is integrated on the parasitic capacitance at nodes A and B. The variance of the output voltage noise of the input pair  $M_1$ - $M_2$  can be shown to be [33]:

$$\sigma_{v_{n,out}}^2 = 2 \cdot \frac{4kT\gamma g_{m1}}{C_a^2} t, \quad (3.13)$$

where the factor 2 accounts for the contributions of  $M_1$  and  $M_2$ . The integration lasts the time needed by the transistors of the following stage to reach the threshold voltage as in Eq. (3.11). Thus, the variance of the noise at the output of the first stage can be written as:

$$\sigma_{v_{n,out}}^2 \approx \frac{8kT\gamma g_m}{C_a} \frac{V_{th,p}}{I_{CM}}. \quad (3.14)$$

---

The input-referred noise can be computed dividing Eq. (3.14) by the square of the voltage gain ( $g_m \frac{T_{int}}{C_a}$ ) from Eq. (3.10) and Eq. (3.11)). Assuming that the input transistors work in saturation region, the transconductance of the MOSFETs is  $\frac{2I_{CM}}{V_{ov}}$ . Thus, Eq. (3.14) becomes:

$$\sigma_{v_{n,in}}^2 = \frac{4kT\gamma}{C_a} \frac{V_{ov}}{V_{th,p}}. \quad (3.15)$$

where  $V_{ov}$  is the overdrive voltage of the input differential pair, approximately  $V_{cm} - V_{th,n}$ . Eq. (3.15) shows that the input-referred noise can be reduced acting on the capacitance at the outputs of the clocked preamplifier, whereas the other parameters depend on the technology and the common-mode of the input signal.

Most of the power consumption of the comparator shown in Figure 3.4 is dissipated in the first stage when the capacitors at nodes A and B are reset to the supply voltage. The power drawn by the supply voltage can be computed as the power needed to charge the capacitor at nodes A and B during the reset phase. Assuming  $C_a = C_b$ , the power consumption in each comparison is:

$$P_{comp} = 2 \cdot \frac{C_a V_{dd}^2}{T_{reset}}, \quad (3.16)$$

where  $T_{reset}$  is the *reset* period and the factor 2 accounts for the two capacitors. From a system design perspective, however, the power consumption of interest is the one spent during the conversion of the input signal. The power consumption of the comparator in the SAR ADC has to be computed on the whole sampling period, accounting also for the sample phase when the comparator is in the reset state. Considering a 12-bit converter with a sampling frequency  $f_s$ , the comparator performs 12 comparisons every  $1/f_s$ , charging two capacitors during the reset phase. Thus, the power consumption of the comparator becomes:

$$P_{dyn} = 2 \cdot C_a V_{dd}^2 12 f_s. \quad (3.17)$$

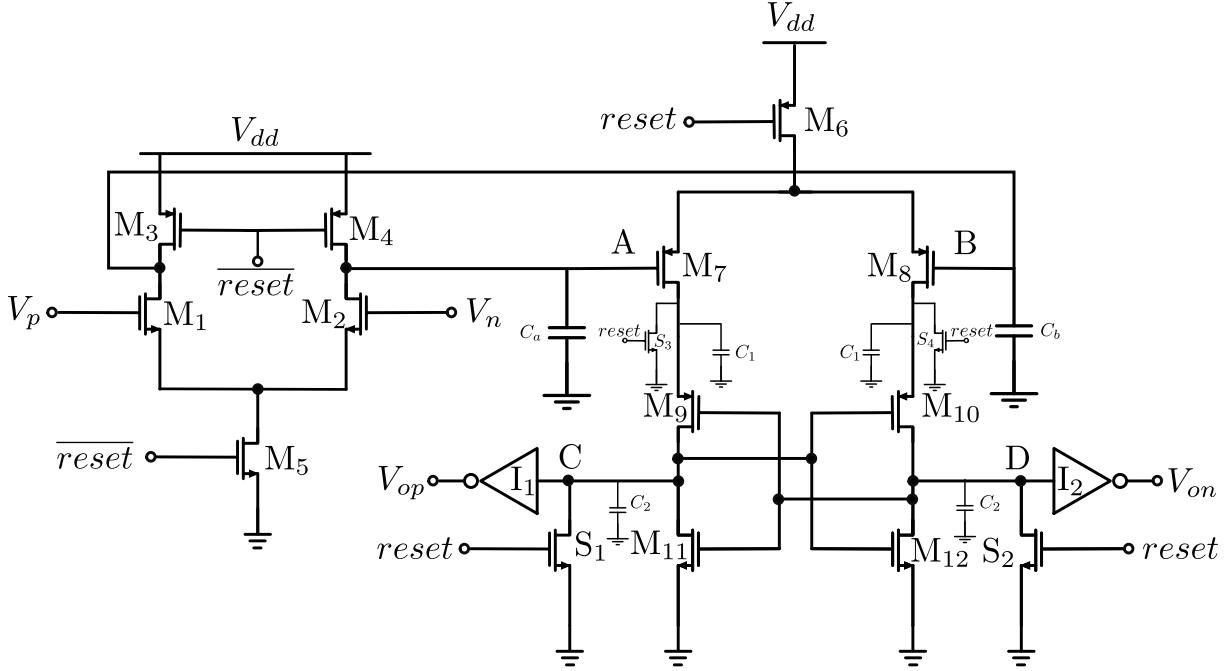
Following the same argument presented in Section 3.2, the comparator should be designed in order to compare the input signal in 100 ps. We can consider that the first half of the comparison time is needed to build up the signal at the input of the latch, whereas the other half is the time needed by the latch to regenerate the differential signal. Therefore, the required integration time is  $T_{int} \approx 50$  ps. Even though there are 100 ps available for the comparison, a smaller comparison time was targeted to account for the effect of the parasitic capacitors added by the layout of the circuit. Finally, let us assume that the input referred noise of the comparator is equal to half LSB and that the threshold voltage of M<sub>7</sub>-M<sub>8</sub> is 350 mV, whereas the overdrive voltage of the input differential pair is approximately 100 mV. Therefore, the capacitance at the nodes A and B can be computed with Eq. (3.15) :

$$C_a \approx \frac{4kT\gamma}{\left(\frac{LSB}{2}\right)^2} \frac{V_{ov}}{V_{th,p}} \approx 98 \text{ fF}. \quad (3.18)$$

At this point, it is possible to compute the minimum common-mode current that is needed to discharge nodes A and B in 50 ps from Eq. (3.11):

$$I_{CM} = C_a \frac{V_{th,p}}{T_{int}} = 686 \mu A. \quad (3.19)$$

The requirement on the current was used to set the aspect ratio of the input differential pair to drive a current large enough to satisfy the timing constraints. The output capacitances of the first stage were set to 120 fF to be conservative, since the noise analysis focused on the noise introduced by the input differential pair, neglecting the other noise sources in the circuit. After an initial design, it was found that the input-referred noise was approximately 300  $\mu V$ , larger than the targeted noise (220  $\mu V$ ). This was due to the noise contribution of the second stage of the comparator and the other noise sources not



**Figure 3.6:** Schematic of the implemented dynamic comparator.

considered during the noise analysis. Considering a noise of  $300 \mu V$ , the resolution of the converter is reduced by more than 1 bit. In fact, let us consider the SNR as:

$$SNR = 10\log \left( \frac{A^2/2}{\sigma_q^2 + \sigma_{comp}^2} \right), \quad (3.20)$$

where  $A$  is the amplitude of the input sinewave,  $\sigma_q^2$  and  $\sigma_{comp}^2$  are the power of the quantization and comparator noise, respectively. The SNR with an amplitude of 0.9 V and a comparator noise of  $300 \mu V$  is 65.8 dB, smaller than the ideal 74 dB. This means that the effective resolution of the converter is reduced by more than 1 bit by the comparator noise. Therefore, the comparator was modified to reduce its noise to a level comparable with the quantization noise. From Eq. (3.15), the noise can be set acting on the overdrive voltage and the capacitor  $C_a$ . Therefore, the aspect ratios of the input pairs of the first and second stage were increased to reduce the overdrive voltage of the transistors. Moreover, the capacitor  $C_a$  was increased to  $300 fF$ . In fact, the capacitance computed with Eq. (3.15) matching the quantization noise ( $\frac{LSB}{\sqrt{12}}$ ) is  $294 fF$ . Finally, the capacitors  $C_1$  and  $C_2$  shown in Figure 3.6 were added to reduce the noise caused by the second stage. The reason behind the addition of the capacitances can be explained considering that the integrated noise is, intuitively, proportional to  $kT/C$ . In other words, they are added to reduce the bandwidth. The trade-off is, therefore, a slower circuit. The value of  $C_1$  and  $C_2$  are  $20 fF$  and  $22 fF$ , respectively.

Finally, another issue of the circuit was that the drains of  $M_7$  and  $M_8$  were not completely reset during the reset phase. Therefore, the latch had memory of the previous state. In case of a large differential voltage at the input of the comparator, this is not a problem since the amplification of the signal is able to overcome the initial unbalance of the latch kept from the previous comparison. However, in case of a small differential voltage, like comparable to the LSB, the latch takes a wrong decision. This problem was solved adding NMOS transistors between the drains of  $M_7$  and  $M_8$  and ground with the gate connected to the reset signal ( $S_3-S_4$  in Figure 3.6).

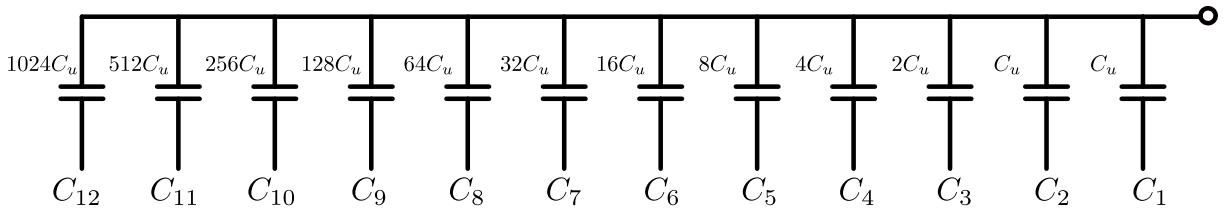
The dimensions of the transistors in the comparator are shown in Table 3.2.

| Transistor                       | $\frac{W}{L} [\mu\text{m}]$ |
|----------------------------------|-----------------------------|
| M <sub>1</sub> -M <sub>2</sub>   | $\frac{30}{0.03}$           |
| M <sub>3</sub> -M <sub>4</sub>   | $\frac{20}{0.03}$           |
| M <sub>7</sub> -M <sub>8</sub>   | $\frac{35}{0.03}$           |
| M <sub>9</sub> -M <sub>10</sub>  | $\frac{15}{0.03}$           |
| M <sub>11</sub> -M <sub>12</sub> | $\frac{10}{0.03}$           |
| S <sub>1</sub> -S <sub>4</sub>   | $\frac{4}{0.03}$            |
| M <sub>5</sub>                   | $\frac{26}{0.03}$           |
| M <sub>6</sub>                   | $\frac{30}{0.03}$           |

**Table 3.2:** Dimensions of the transistors in the dynamic comparator.

### 3.4 DAC

Each DAC in the 12-bit SAR ADC is formed by a binary-weighted array composed by a total of 2048 unit capacitors as shown in Figure 3.7.



**Figure 3.7:** Schematic of the binary-weighted CDAC of the 12-bit SAR ADC.

Each capacitor is implemented with the parallel connection of unit capacitors. The outputs of the DACs are connected to the input terminals of the comparator.

The switching energy of the DAC is directly proportional to the unit capacitance. Thus, the most straightforward way to reduce its energy consumption is reducing as much as possible the value of the unit capacitor. The main limits to the capacitance value are set by noise and mismatch. It can be shown that the power of the thermal noise at the output of an RC circuit is:

$$\sigma_{n,R}^2 = \frac{kT}{C}. \quad (3.21)$$

This noise is present whenever the input signal is sampled, regardless of the resistance of the switches. Since the signal is sampled on the DAC capacitive array, the total capacitance,  $C_{tot}$ , of the array should be chosen such that the noise is below the quantization noise of the 12-bit converter, therefore:

$$C_{tot} \geq \frac{kT}{(\frac{LSB}{\sqrt{12}})^2} \approx 257 \text{ fF}, \quad (3.22)$$

that results in a lower bound for the unit capacitance:

$$C_u \geq 126 \text{ aF}. \quad (3.23)$$

From Chapter 2, the maximum of the standard deviation of the DNL for the monotonic switching algorithm can be expressed as:

$$\sigma_{DNL,monotonic} = \frac{2^{\frac{n}{2}} \sigma_u}{\sqrt{2} C_u}. \quad (3.24)$$

If we set that the standard deviation of the DNL smaller than half LSB, it is possible to obtain the maximum relative mismatch of the unit capacitor from Eq. (3.24):

$$\frac{\sigma_u}{C_u} \leq \frac{1}{\sqrt{22^{\frac{n}{2}}}} = 1.1\%. \quad (3.25)$$

With the same argument as in Section 2.8, the minimum unit capacitance can be expressed as:

$$C_u \geq 2^n k_c^2 c_{spec}. \quad (3.26)$$

In order to compute the Pelgrom coefficient, Monte-Carlo (MC) simulations were performed with MOM

| Layers | C [fF] | $\frac{\sigma_C}{C} [\%]$ |
|--------|--------|---------------------------|
| M2-M4  | 1.3    | 0.57                      |
| M1-M3  | 1.4    | 0.54                      |

**Table 3.3:** Summary of the results of the Monte Carlo simulations with 5000 samples.

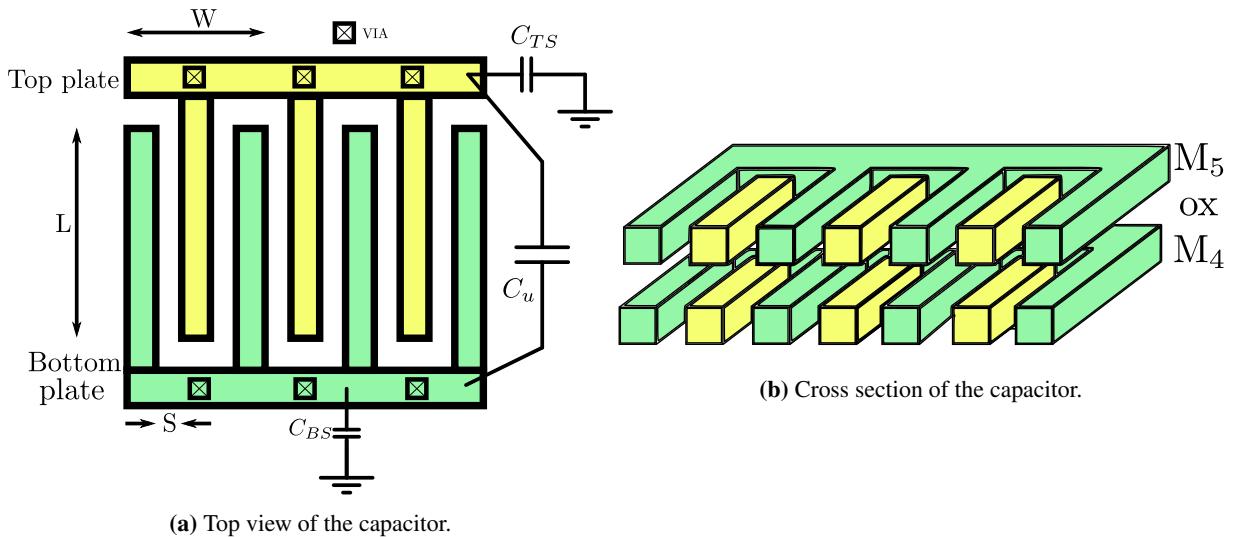
capacitors provided in the technology. A summary of the results is shown in Table 3.3. The  $c_{spec}$  and the Pelgrom coefficient are approximately  $1 \text{ fF}/\mu\text{m}^2$  and  $0.7\% \mu\text{m}$ , respectively. Therefore, the limit imposed by mismatch is:

$$C_u \geq 200 \text{ aF}. \quad (3.27)$$

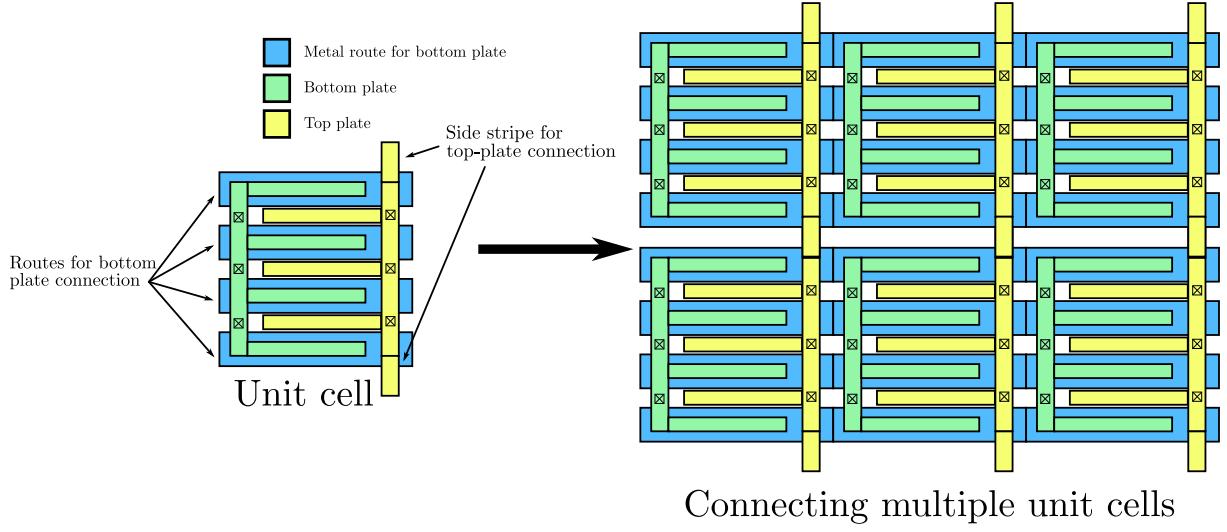
Therefore, the capacitance of the unit capacitor can be chosen as low as 200 aF. However, hundreds-aF capacitors were not available in the technology, thus a custom capacitor was designed.

### 3.4.1 Custom capacitor

There are different kinds of capacitors employed in SAR ADCs, such as poly-insulator-poly (PIP), metal-insulator-metal (MIM) and metal-oxide-metal (MOM) capacitors. MOM capacitors are based on the fringing capacitance between two metal wires belonging to the same metal layer placed close to each other. They are a popular solution in SAR ADCs, since they can be designed with parallel interdigitated metal fingers, without adding specific steps in the fabrication process.

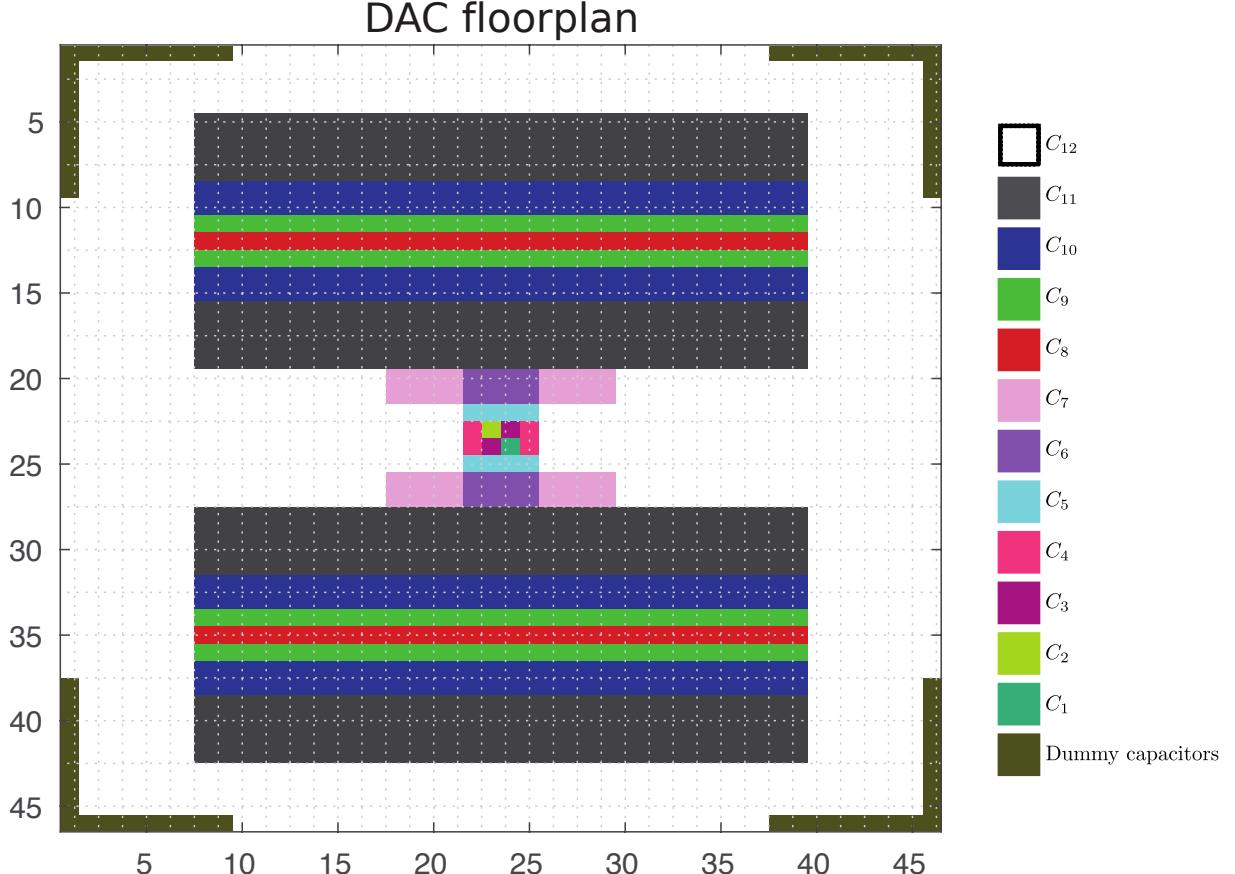


**Figure 3.8:** Structure of the custom capacitor.



**Figure 3.9:** Unitary cell and the placement of the cells in an arrayed structure.

There are various structures proposed in literature[34, 35], but they often involve a time-consuming layout. In order to reduce the time spent on the development of the capacitor, the structure in Figure 3.8 was chosen for its simplicity. It is a MOM capacitor with a comb structure that uses metal layers 4 and



**Figure 3.10:** DAC floorplan. Note that each color refers to a capacitor in the DAC ( $[C_{12}, C_{11}, \dots, C_1]$ ).

5 stacked on top of each other. The metals of the two layers are connected through vias.

In order to simplify the layout of the DAC array, the unit capacitor was designed as a part of a unitary cell of the DAC array as shown in Figure 3.9. Each unitary cell contained the unit capacitor, in metal 4

and metal 5, and below, in metal 1, 4 metal routes in parallel. Moreover, 2 metal strips were added to the two sides of the top plate. In this way, when a group of unitary cells are placed closed to each other, the top plates in each column and the routes in each row result connected (see Figure 3.9).

A possible DAC floorplan is shown in Figure 3.10. The presence of only four metal routes available to connect the bottom plate of each capacitor sets a constraint on the DAC floorplan. In fact, each bottom plate is connected to only one of the routes in each cell through a via. In each row of the floorplan, all the unit capacitors belonging to the same DAC capacitance will be connected on that route. Therefore, it is possible to allocate the unit capacitors in each row to a maximum of four different DAC capacitors. For example, the unit capacitors present in row 24 of the DAC floorplan (see Figure 3.10) belongs to  $C_{12}$ ,  $C_4$ ,  $C_3$  and  $C_1$ . One route is assigned to each one of these four DAC capacitors. Then, it is only a matter of tapping with a via the correct metal route to the bottom plate of the unit capacitor.

In Figure 3.8, three main capacitors have been highlighted: the capacitance between the two nodes of the structure,  $C_u$ , plus two unwanted parasitic capacitors between the nodes and ground,  $C_{TS}$  and  $C_{BS}$ . The former is the parasitic capacitance between the top plate and ground, the latter is between the bottom plate and ground.

|          | C [aF] |
|----------|--------|
| $C_u$    | 807    |
| $C_{TS}$ | 73     |
| $C_{BS}$ | 116    |

|  | W [ $\mu m$ ] | 0.25 |
|--|---------------|------|
|  | L [ $\mu m$ ] | 0.74 |
|  | S [ $\mu m$ ] | 0.05 |

(a) Extracted capacitances of the unit capacitor.

(b) Dimensions of the unit capacitor.

**Table 3.4:** Summary of the capacitances of the unit capacitor and its dimensions.

The effect of  $C_{TS}$  is to reduce the dynamic range of the DAC, resulting in a gain error at the output of the ADC.  $C_{BS}$  does not affect the conversion since it is switched to  $V_{dd}$  or ground by the DAC driver. This means that could result in a long settling time, since the driver has to charge also the parasitic capacitor, but it can be solved designing a strong driver. The capacitances extracted with a 3D electromagnetic simulator and the capacitor dimensions are summarized in Table 3.4.

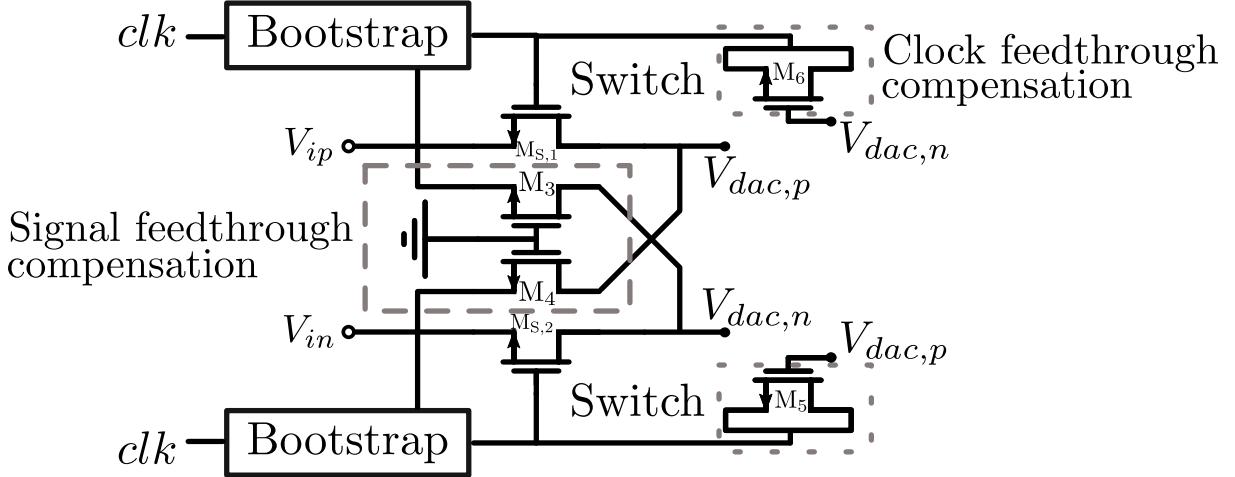
The relative mismatch of the capacitor has been estimated with the data in Table 3.3 as:

$$\frac{\sigma_u}{C_u} = k_c \sqrt{\frac{c_{spec}}{2C_u}} \approx 0.6\%. \quad (3.28)$$

This estimation is based on the assumption that the custom capacitor has the same Pelgrom coefficient of the MOM capacitor provided in the library. This assumption has been made considering that both capacitors are based on inter-digited fingers. Therefore, its value should be considered as a rough estimate of the relative mismatch of the custom capacitor.

### 3.5 Sampling switch

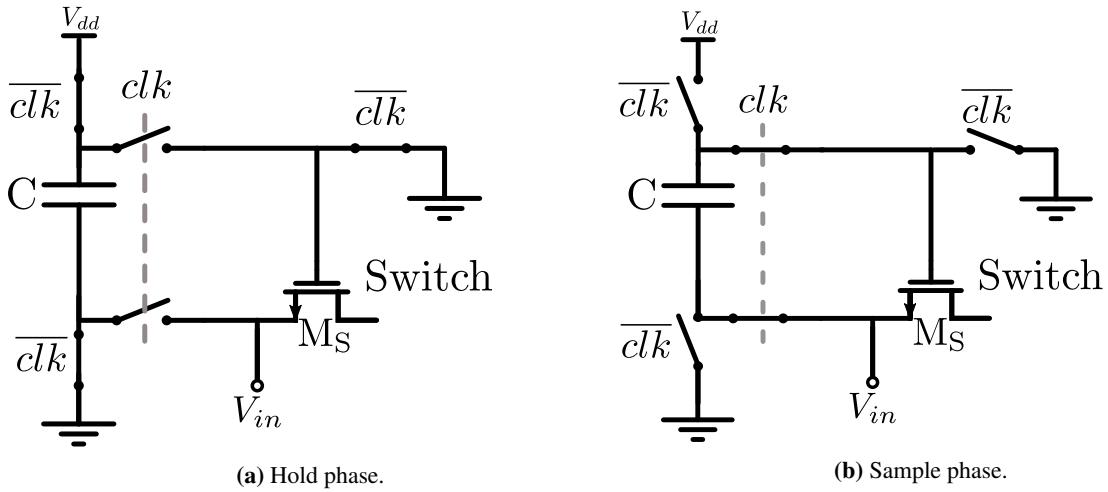
The sampling switch implemented in this SAR ADC is shown in Figure 3.11. The input signals  $V_{ip}$  and  $V_{in}$  are sampled on the top plate of the CDACs through the switches  $M_{S,1}$ - $M_{S,2}$ . Between the gate and the source of the switches there is a bootstrapping circuit controlled by the sampling clock,  $clk$ . This technique is necessary to reduce the distortion caused by variations of the switch on-resistance



**Figure 3.11:** Sampling switches with dummy switch for signal and clock feedthrough reduction, based on [36].

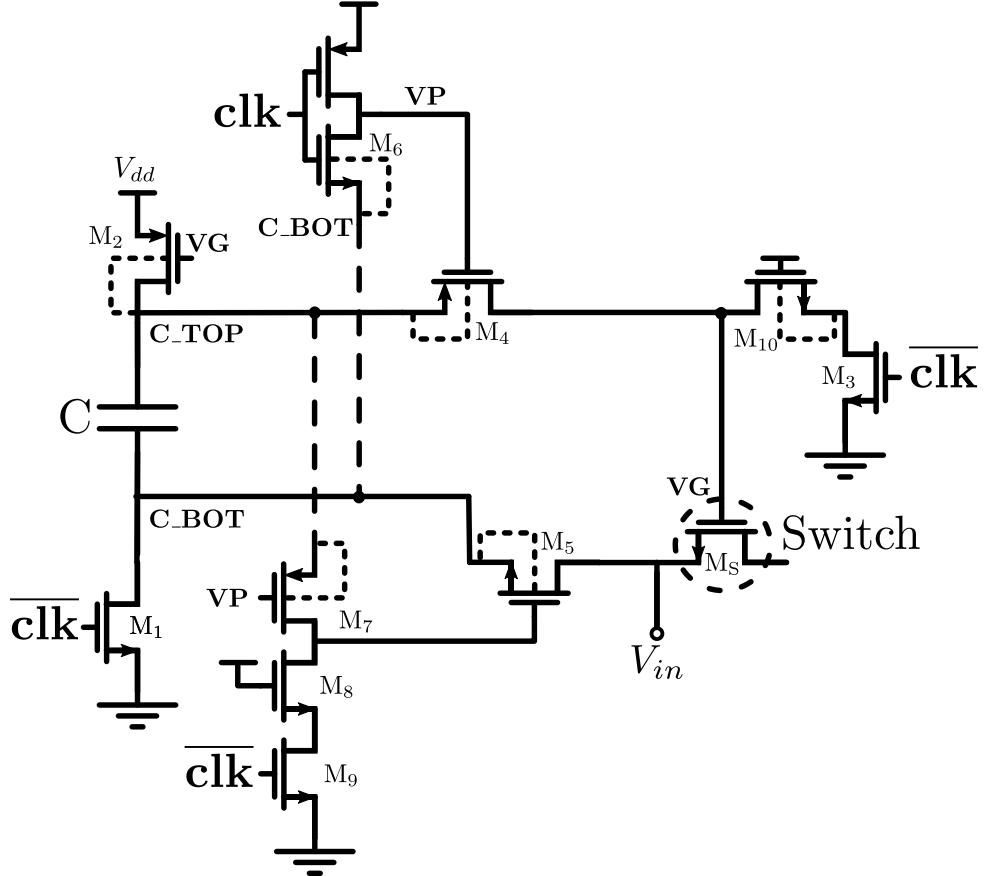
as a function of the input signal for resolutions larger than 8 bits[37]. The bootstrap circuit keeps the gate-source voltage of the switch fixed to  $V_{dd}$ . In this way, the resistance of the switch is kept constant and, consequently, the linearity of the switch is improved with respect to configurations where a simple NMOS or a transmission gate is used to sample the input signal. Finally,  $M_3$ - $M_6$  are added as dummy switches to reduce the signal and clock feedthrough on the differential mode[36].

The sampling switch operates in two phases: sample phase and hold phase. During the sample phase, the voltage  $V_{dac,p}$  ( $V_{dac,n}$ ) tracks the input signal, i.e., the switch is closed. In the hold phase, instead, the switch is open and the sampled signal is held constant on the CDAC capacitors. The equivalent circuits of the two phases with the bootstrapping operation are shown in Figure 3.12. The sampling clock and its complement,  $clk$  and  $\overline{clk}$  (generated with an inverter driven by  $clk$ ) control the activation of the switch. The bootstrapping operations can be summarized as follows:



**Figure 3.12:** Bootstrapping mechanism.

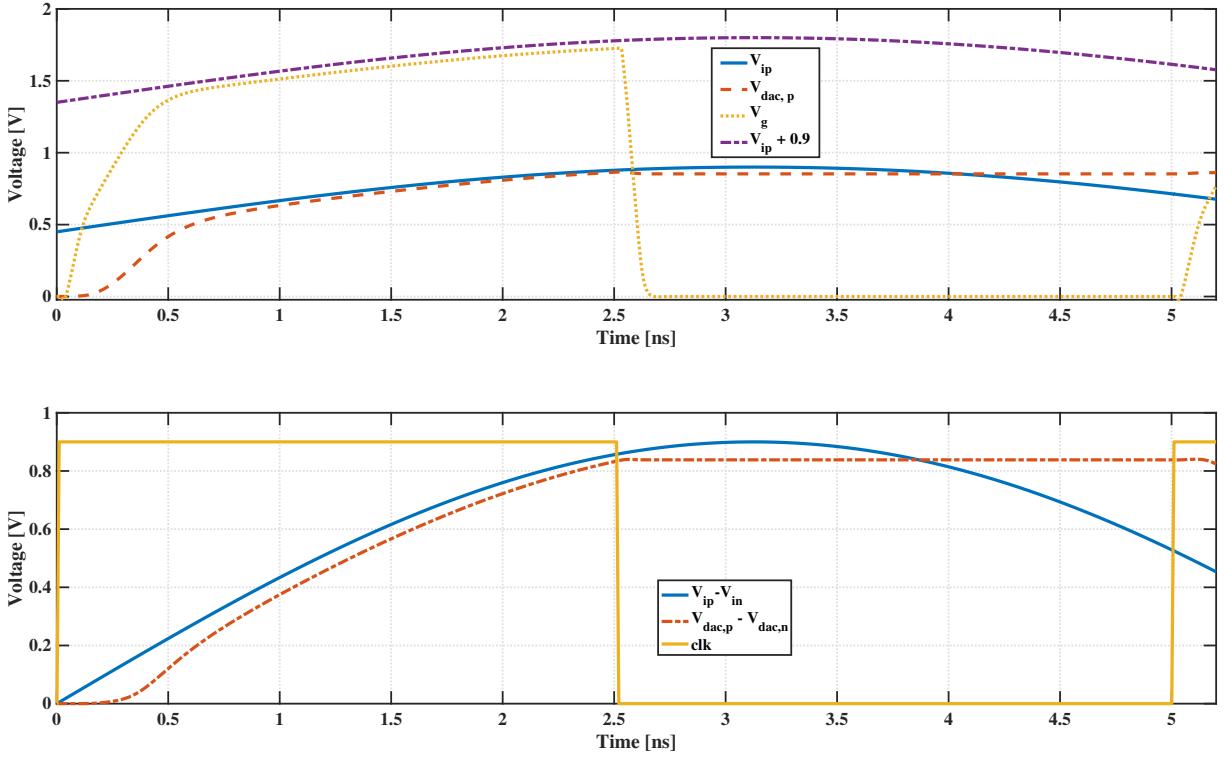
- hold phase ( $clk = 0$ ,  $\bar{clk} = 1$ ), in which the switch  $M_S$  is turned off and the capacitor  $C$  is charged to  $V_{dd}$ ,
  - sample mode ( $clk = 1$ ,  $\bar{clk} = 0$ ),  $C$  is tied between the gate and the source of  $M_S$ , keeping constant the gate-source voltage, hence its on-resistance.



**Figure 3.13:** Bootstrap circuit, based on [38].

The circuit that implements the operations described above is shown in Figure 3.13 and it is based on the topology proposed in [38, 39]. During the hold phase, the capacitor C is connected between ground and  $V_{dd}$  through  $M_1$  and  $M_2$ , charging the capacitor to  $V_{dd}$ .  $M_5$  is switched off with its gate tied to ground by  $M_3$ . The gate of  $M_5$  is connected to ground through  $M_8$ - $M_9$  cutting off the bottom plate node of C, BOT\_C, from the input voltage.  $M_4$  is also turned off since the node VP is charged to  $V_{dd}$ . Therefore, C is disconnected from  $M_5$ . Then, in the tracking phase,  $clk$  is pulled high.  $M_6$  is activated tying the node VP to C\_BOT. As VP is being discharged,  $M_7$  is activated connecting the gate of  $M_5$  to the top plate of C, C\_TOP. In this way,  $M_4$ - $M_5$  are turned on and the capacitor C is connected between the gate and source of the switch acting as a battery for  $M_5$ . From a functional point of view, transistors  $M_{10}$  and  $M_8$  are not important, but they improve the reliability of the circuit reducing the voltage applied to  $M_3$  and  $M_9$ [39], since the nodes VG and C\_TOP reach voltages as high as 2 times the supply voltage. An example of the timing diagram of the most important signals in the sampling circuit is given in Figure 3.14.

The capacitor C is sized (3.33 pF) in order to reduce the charge sharing on the gate of the switch. Transistors M<sub>3</sub> and M<sub>10</sub> set the opening time of the switch. Thus, they are sized large enough to quickly discharge node VG at the end of the tracking phase. Finally, M<sub>4</sub>-M<sub>5</sub> should have a low resistance when they are activated to tie C between the gate and the source of the switch in a small amount of time. The amount of time available to sample the input signals on the top plate of the CDACs is 2.5 ns. When



**Figure 3.14:** Timing diagram of the waveforms in the bootstrap circuit from a simulation in Cadence Virtuoso with an input sinewave with a frequency of 80 MHz and a 2-pF load capacitance.

sampling the input signal, the charging of the DAC capacitance,  $C_{dac}$ , can be modelled as an RC charge, where R is the resistance of the switch. The time constant can be set sizing the dimensions of the switch. In this case, the error between the input signal and the sampled signal should be limited to half LSB, to not limit the resolution of the converter. The error voltage between the input signal and the sampled signal on top of a capacitor being charged to  $V_{dd}$  (worst-case) can be written as:

$$\epsilon(t) = V_{dd}e^{-\frac{t}{\tau}}. \quad (3.29)$$

Setting the error to half LSB, we obtain:

$$t_{sett} = \tau \ln \left( \frac{V_{dd}}{\frac{LSB}{2}} \right) = 8.31\tau. \quad (3.30)$$

Thus, the switch should be sized to have the settling time long approximately 8 time constants.

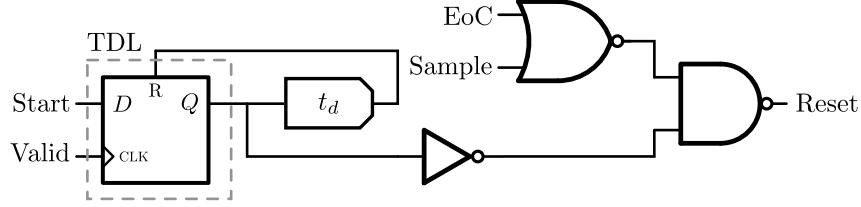
The resistance of the switch assuming 9 time constants to have a safety margin becomes:

$$R \leq \frac{t_{sett}}{9C_{dac}} = 169 \Omega, \quad (3.31)$$

where  $C_{dac} = 2048C_u \approx 1.64 \text{ pF}$ . This condition provided a starting point to set the aspect ratio of the design. However, we need to account that the switch is not immediately closed when  $clk$  is pulled high, because there is some time needed to tie C to the switch and the internal nodes of the bootstrap circuit to settle. The right balance between parasitics and low-resistance paths (connecting the battery to the switch) was found in various iterations, in order to have an acceptable linearity (ENOB > 10) for input signals with a frequency up to 100 MHz (more details in the next chapter).

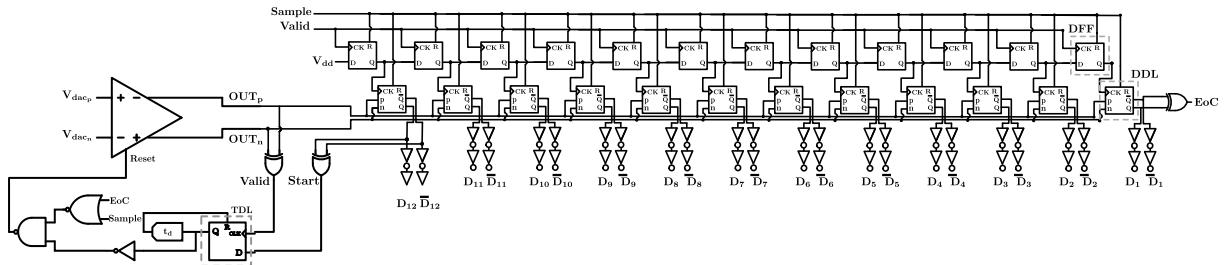
### 3.6 SAR logic

The control logic of the SAR ADC presented in this thesis is based on the work in [40]. The logic is



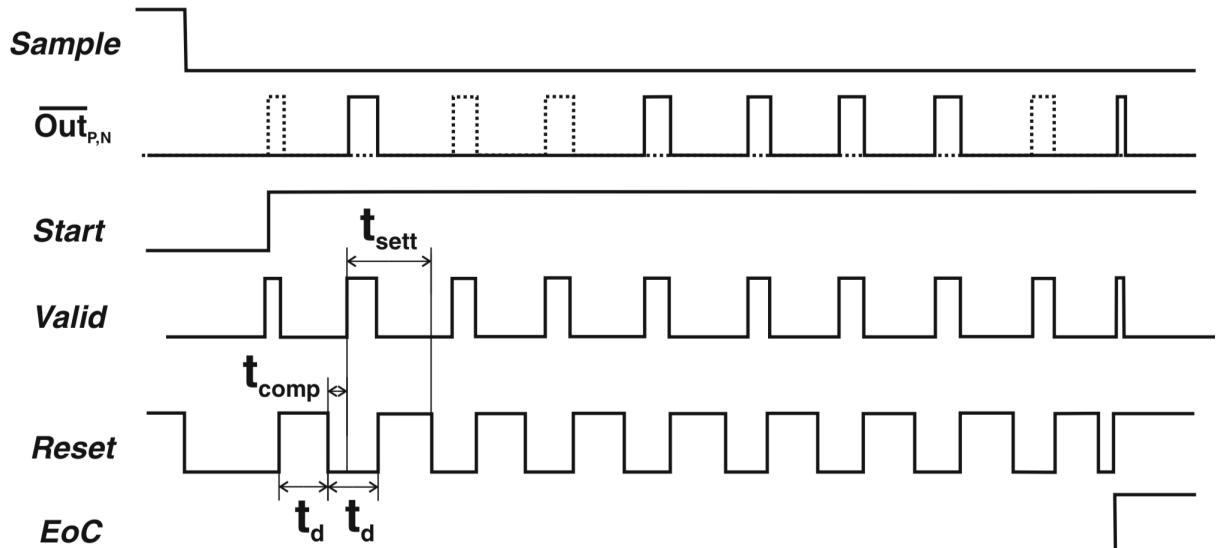
**Figure 3.15:** Schematic of the temporizer[40].

asynchronous and it can be implemented with dynamic logic gates in order to further reduce the power consumption. The self-synchronization of the logic is based on the logic temporizer shown in Figure



**Figure 3.16:** Schematic of the asynchronous logic.

3.15. The function of the temporizer is to reset and enable the comparator in each step of the conversion and it is implemented by a dynamic latch (TDL) periodically reset through a delayed feedback loop.



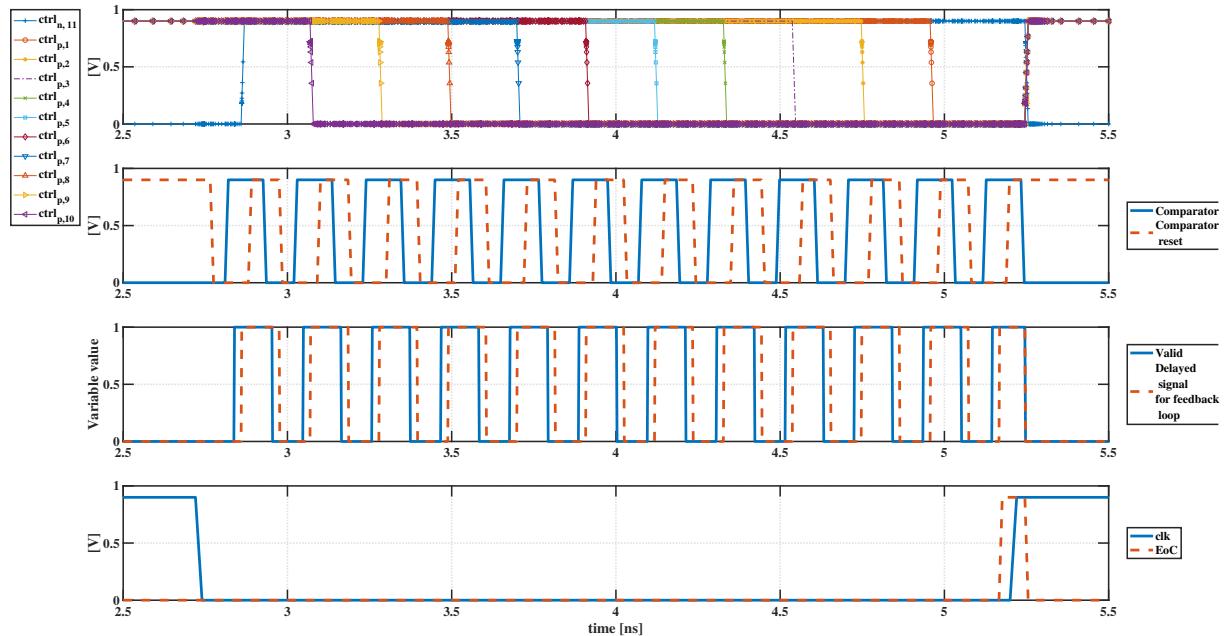
**Figure 3.17:** Timing diagram of the asynchronous logic in [40].

The logic proposed in [40] generalized to the converter presented in this work is shown in Figure 3.16. The first row of logic gates is formed by dynamic flip-flops (DFF) and it implements effectively a shift register clocked by *Valid*. The second row is, instead, composed by dynamic differential latches (DDL) where the bits are stored during conversion. The timing diagram of the signals can be found in Figure 3.17. Here,  $t_d$  and  $t_{comp}$  the period of the reset signal of the comparator and the comparison time, respectively.  $t_{sett}$  is the settling time of the DAC voltage. Let us consider the signals present in the logic:

- *Sample* is the sampling clock,
- $OUT_p$  and  $OUT_n$  are the positive and negative output of the comparator, respectively,
- *Start* triggers the propagation of *Valid* signal through the TDL, activating the first reset of the comparator,
- *Valid* signals the end of each comparison, generated through a XOR gate,
- *Reset* drives the reset of the comparator, and
- *EoC* marks the end of each conversion.

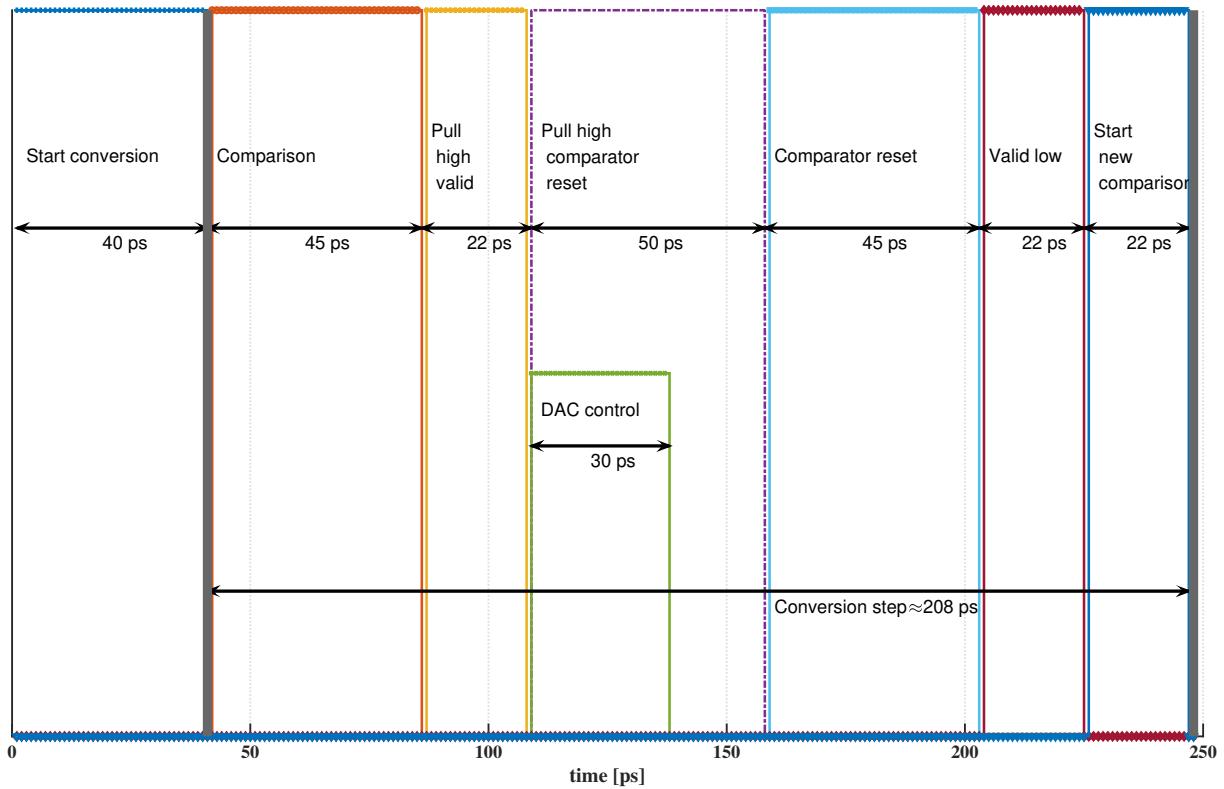
The asynchronous logic operates as follows. When the sampling signal is pulled down the conversion phase starts. Initially, the MSB is evaluated and the *Valid* signal becomes high. *Start* is pulled high when the bottom-plate of the MSB capacitor is set and it becomes low again only at the next sample phase. At this point, the transition of *Start* triggers the propagation of the *Valid* signal through the TDL and, consequently, *Reset* becomes high resetting the comparator. The reset period of the comparator should be approximately 200 ps in this case, as previously mentioned in this chapter. After the output of the TDL has completed the feedback loop, the reset signal becomes low again. The next conversion steps are carried out in the same way until the LSB is evaluated and the *EoC* is pulled high.

In this work, the control logic circuit has been implemented with a model written in Verilog-A.



**Figure 3.18:** Timing diagram of the control signals in the ADC from a simulation in Cadence Virtuoso. Note that, the *Valid* signal is an internal signal of the control logic. The signals  $ctrl_p$  and  $ctrl_n$  are the control signals of the DAC.

The timing diagrams of the control signals of the converter is shown in Figure 3.18. A more detailed timing diagram of each conversion step starting from the MSB is shown in Figure 3.19. After the sample phase, i.e. when *clk* is pulled down, the control logic starts the conversion. The behavioural model of the comparator was set to compare the input differential signal in approximately 50 ps. After the comparison, *valid* is generated by a XOR of the comparator outputs adding a 20-ps delay. When *valid* is pulled high, the next steps are to reset the comparator and activate the control switches of the DAC ( $ctrl_p$  and  $ctrl_n$ ), activated after 30 ps. When the comparator is reset, *valid* is pulled down, thereafter triggering another



**Figure 3.19:** Timing diagram of the behavioural models of the SAR ADC.

comparison. These conversion steps are repeated until the LSB is determined. Thereafter, the EoC is pulled high.

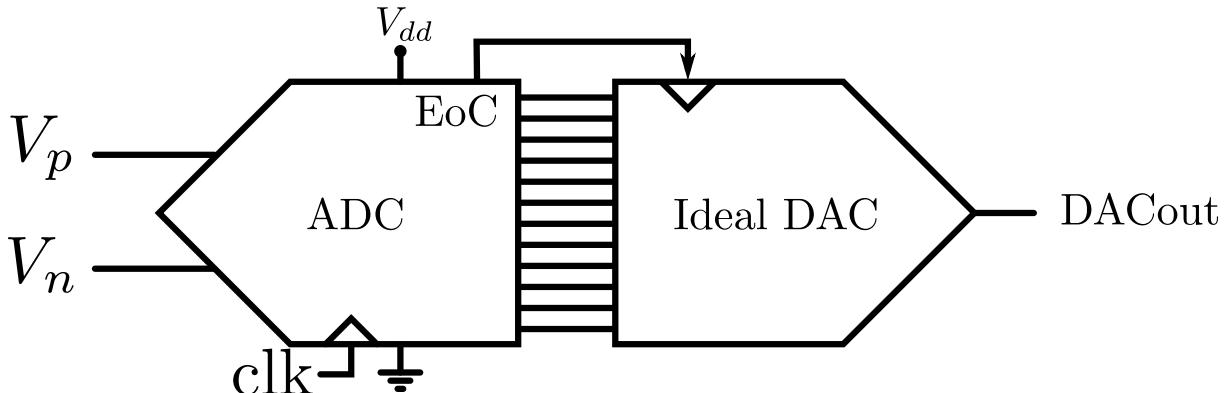
In simple terms, the control logic is like a finite state machine. During the conversion, the various states are executed to reset (or activate) the comparator, control the DACs and provide the digital code at the output. The delay loop in the behavioural model is implemented with two signals. They represent the signals before and after the delay element. They have the same value, but one is the delayed version of the other one. When the delayed signal goes from low to high, it triggers the reset of the comparator. There is also a reset state controlled by an external signal to reset the control logic asynchronously. The delays of the output signals of the SAR logic have been set in order to convert the input signals in less than 2.5 ns. The Verilog-A code can be found in Appendix A.

# Chapter 4

## Simulations, results and discussion

In this chapter, the performance of the designed circuits are examined. The effect of the various blocks of the ADC are evaluated in terms of DNL and INL, i.e., static metrics. The dynamic performance in terms of SNDR of the various blocks is also examined. Finally, there is an estimation of power consumption and FoM of the designed converter. Here, the simulations were performed in Cadence Virtuoso. Then, the output data were exported and processed in Matlab.

The testbench used to test the performance of the SAR ADC is shown in Figure 4.1. The ideal DAC



**Figure 4.1:** Schematic of the testbench

is used to obtain the analog version of the converted input differential signal,  $V_p - V_n$ . The power supply,  $V_{dd}$ , was set to 0.9 V with a 200-MHz sampling clock ( $clk$ ).

Simulating the testbench, both static and dynamic metrics were obtained. The static metrics, i.e., DNL and INL, are computed with the input-output (IO) characteristic of the converter. The simulation for the IO characteristic consisted in applying an input ramp to obtain the output staircase.

In order to obtain dynamic metrics, an input sinewave was applied to the converter. Then, the SNDR, SFDR and SNR were computed analysing the spectrum of the output sinewave. The input frequency was chosen to have coherent sampling in all the simulations. Initially, only one block of the SAR ADC at a time was simulated at transistor level, whereas the other blocks were models in Verilog-A. This was useful to evaluate the effect of the designed blocks on the linearity of the converter. Finally, the SAR ADC was simulated with all the blocks at transistor level. In all the simulations, the temperature was set to 100 °C.

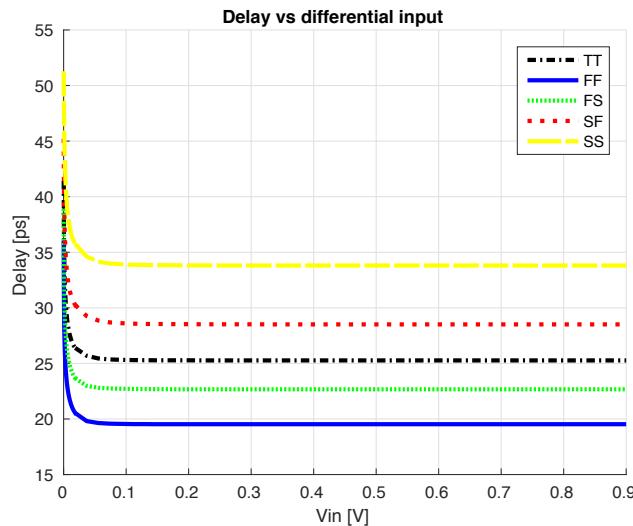
This chapter starts from the performance of the static and dynamic comparator. Then, the effect of the DAC capacitance mismatch is presented, followed by the simulation of the sampling switch in the SAR ADC. Thereafter, the SAR ADC simulations are presented and summarized. Finally, the chapter concludes with a discussion on the results.

## 4.1 Comparator

The design of two comparators is presented in the previous chapter. During the design, their performances were assessed based on the speed and the ability to pass the overdrive recovery test (see below for more details). Then, the converter was simulated with the comparator at transistor level and the other blocks as Verilog-A models to obtain INL and DNL. This allowed to isolate the effect of the comparator on the performance of the ADC.

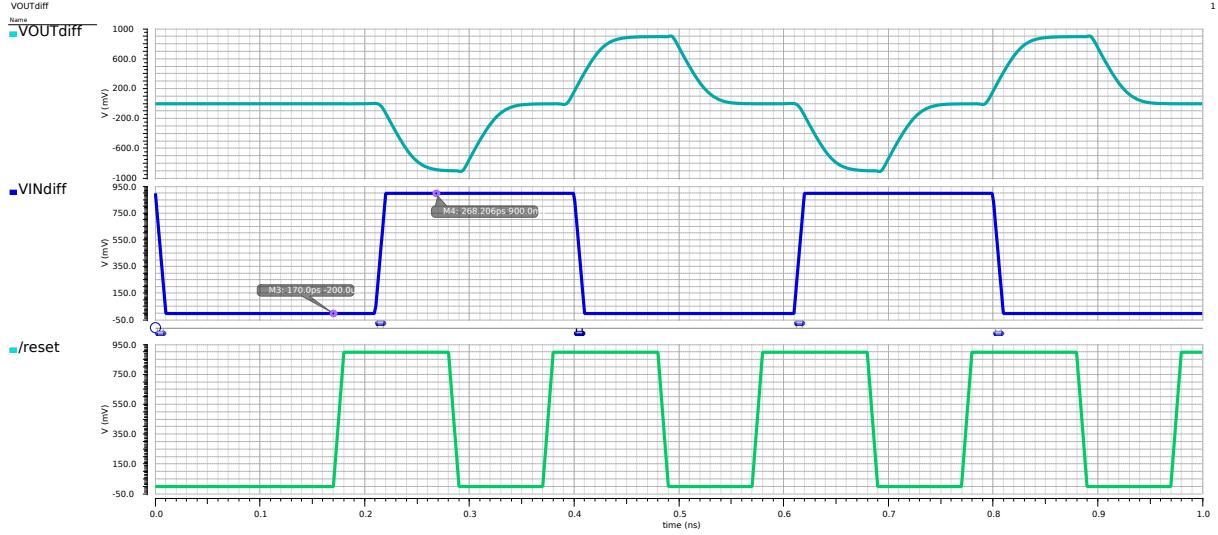
### 4.1.1 Static comparator

**Speed and power consumption** The speed of the comparator is an important requirement for the SAR ADC in question. The comparator delay is a function of the input differential signal amplitude. Therefore, it was tested applying a small differential signal and computing the delay between the reset signal and the output signal. It was simulated for different process corners to verify its reliability and the results are shown in Figure 4.2. It is possible to note that the delay increases when the signal approaches 0 V. This happens because the differential voltage at the input of the latch is small and the regeneration time of the latch increases. Ideally, the delay would be infinite when the input differential signal is zero, i.e., the latch is in the metastable point. This does not happen in a real implementation due to the presence of electronic noise in the circuit. In the typical case (TT), the comparison time ranges approximately between 45 ps and 25 ps, considering an input differential voltage between  $200 \mu\text{V}$  and  $0.9 \text{ V}$ .



**Figure 4.2:** Delay vs. input differential voltage for different process corners of the static comparator.

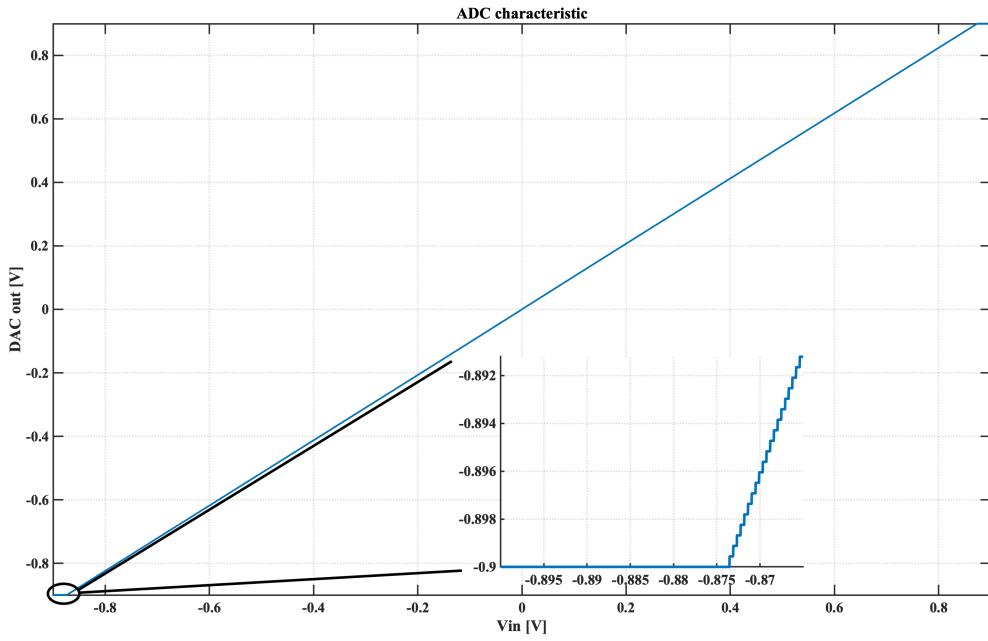
An important test used during the design of the comparator was the overdrive recovery test (ORT)[6], shown in Figure 4.3. In this test, the comparator is tested with an input voltage difference that toggles between a large value, here  $0.9 \text{ V}$ , and a small value of opposite signe, here  $-200 \mu\text{V}$ , in two consecutive cycles. In this way, the outputs of the first stage are completely unbalanced on one side in the first cycle. In the next cycle, the comparator has to be able to recover from that unbalance and amplify correctly the input differential voltage. A similar situation as the ORT can happen in a SAR ADC. Let us consider, for instance, that the input differential voltage of the SAR ADC presented in this work is slightly less than  $450 \text{ mV}$ , e.g.  $449.7 \text{ mV}$ . After the first comparison, the DAC output voltage is decreased by  $450 \text{ mV}$ . Thus, the differential input voltage of the comparator decreases to a negative value of  $300 \mu\text{V}$ . In this case, the comparator should be able to compare in the first cycle a large input differential voltage and in the next cycle a much smaller input with opposite sign, a similar situation as the ORT.



**Figure 4.3:** Overdrive recovery test of the static comparator. In one cycle, the input differential voltage is 0.9 V, whereas it is  $-200 \mu\text{V}$  in the next comparison.

|                         |       |
|-------------------------|-------|
| Delay [ps]              | 45-25 |
| Power [ $\text{mW}$ ]   | 5.3   |
| Noise [ $\mu\text{V}$ ] | 299   |

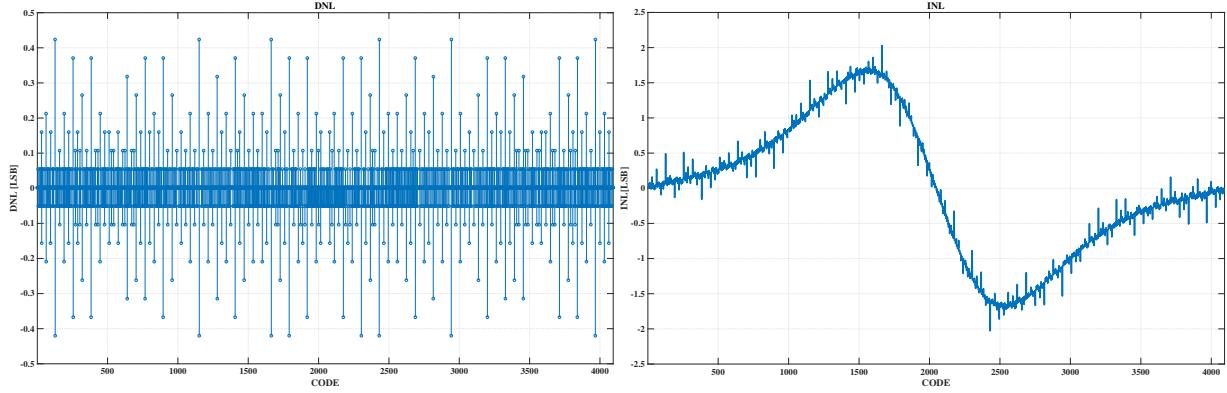
**Table 4.1:** Summary of the performance of the comparator.



**Figure 4.4:** Input-output characteristic of the ADC.

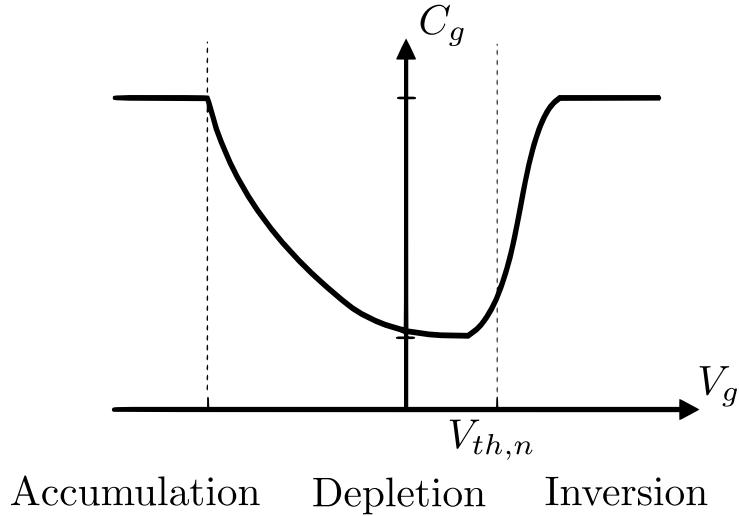
In Table 4.1, it is shown a summary of the performance of the static comparator. The power consumption of the comparator is 5.3 mW with an input referred noise of  $299 \mu\text{W}$ .

**Effect of the static comparator on the linearity of the converter** In order to observe the effects of the comparator on the performance of the ADC, capacitors from the analog library in Cadence Virtuoso were used for the DACs, whereas all the other components were Verilog-A models. Thus, only the comparator



**Figure 4.5:** Effect of the comparator on the linearity of the ADC.

was simulated at transistor level and its effect on the linearity of the converter could be examined. In order to obtain the DNL and INL, a very slow input ramp between -0.9 V and 0.9 V were applied through a parametric simulation to the input of the converter. Then, the digital output of the SAR ADC was fed to an ideal DAC, obtaining the input-output characteristic of the converter. From the characteristic, it was possible to compute the DNL and INL. The resulting input-output characteristic is shown in Figure 4.4. It



**Figure 4.6:** Qualitative trend of the gate capacitance of an NMOS as a function of the gate voltage.

is possible to note the plateau at the beginning and at the end of the of the characteristic. They are caused by the input capacitance of the comparator that reduces the dynamic range of the converter. In other words, the DAC output is attenuated by the presence of the parasitic capacitance. The DNL and INL of the converter are shown in Figure 4.5. The DNL and INL caused by the comparator are within +0.4LSB/-0.4LSB and +1.7LSB/-1.7LSB. The large INL is caused by the input capacitance of the comparator. The qualitative trend of the gate capacitance as a function of the gate voltage is shown in Figure 4.6. From the plot, the input capacitance at the comparator inputs is highly non-linear. The variation of the capacitance as a function of the DAC output voltage causes non-binary thresholds, introducing errors during the conversion of the input signal. In fact, the common mode voltage at the input of the comparator changes during conversion. Thus, the capacitive partition in each conversion step is modulated by the variation of the parasitic capacitance at the input of the comparator. In simple terms, the capacitive partition of the

---

*i*-th conversion step becomes

$$H_i = \frac{C(i)}{C_{dac} + C_p(i)}, \quad (4.1)$$

when the *i*-th capacitor,  $C(i)$ , is switched to ground (or  $V_{dd}$ ). Here,  $C_{dac}$  is the total DAC capacitance and  $C_p(i)$  is the parasitic capacitor at the input terminal of the comparator. Therefore, the DAC output voltage variation in each conversion step is not binary scaled, since  $C_p$  is not constant.

### 4.1.2 Dynamic comparator

**Noise of the dynamic comparator** A dynamic comparator does not operate continuously. Its operation is clocked by the reset signal, therefore its noise cannot be computed with the same noise analysis valid for a continuous-time comparator. The noise of the comparator was obtained with a similar procedure as in [33], based on the following concept. Let us consider a normal distribution:

$$f(x) = \frac{1}{\sigma\sqrt{2\pi}} e^{-\frac{(x-\mu)^2}{2\sigma^2}}, \quad (4.2)$$

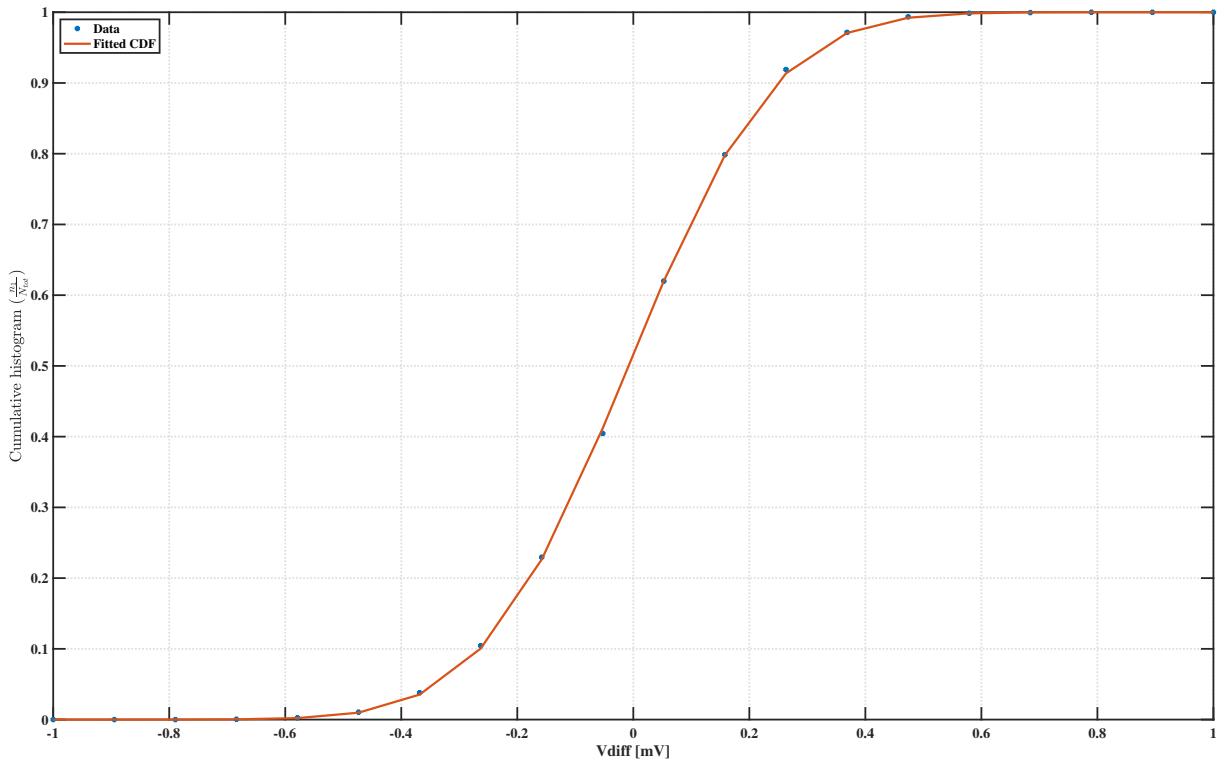
where  $\mu$  is the average value and  $\sigma$  is the standard deviation. The cumulative distribution function (CDF),  $F_A$ , for a random variable A is:

$$F_A(x) = \int_{-\infty}^x f_A(a)da, \quad (4.3)$$

i.e., the probability of obtaining  $A \leq x$ . In case of a normal distribution, the CDF is equal to:

$$F(x) = \frac{1}{2} \left[ 1 + \operatorname{erf} \left( \frac{x-\mu}{\sigma\sqrt{2}} \right) \right]. \quad (4.4)$$

If we consider the comparator with its input shorted and we assume a Gaussian noise in the circuit, the

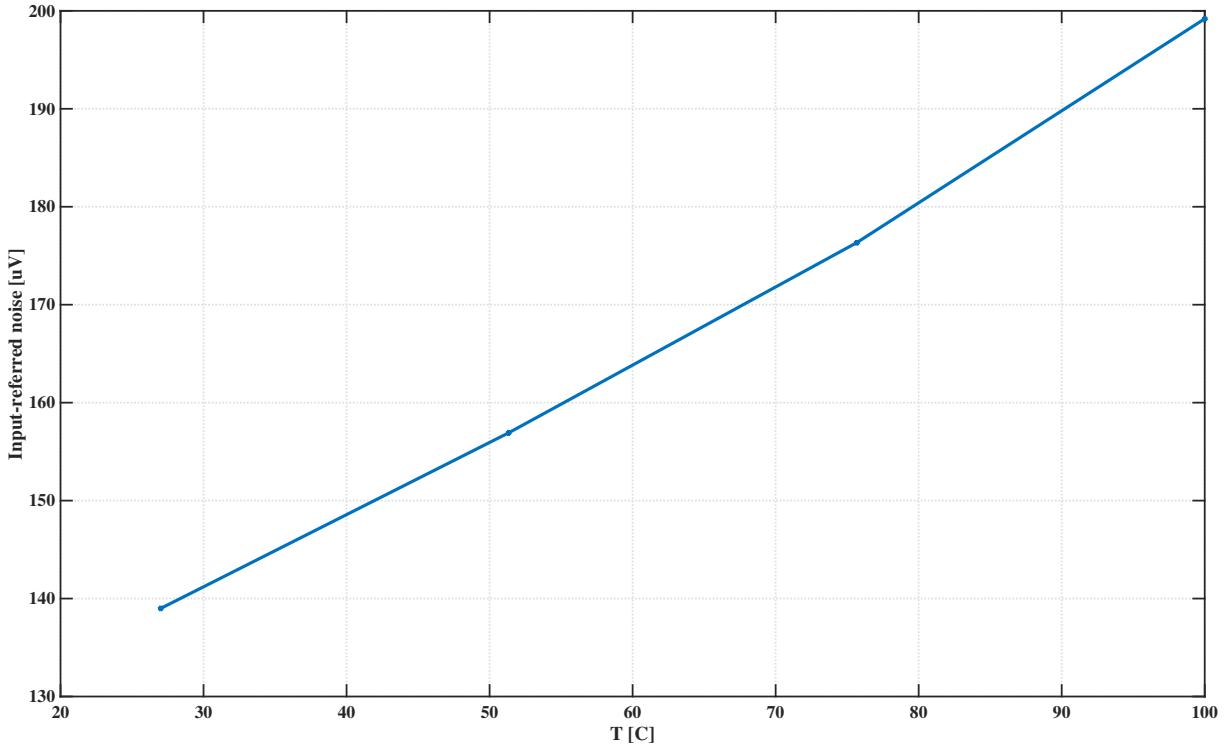


**Figure 4.7:** CDF obtained from the simulations.

output of the comparator is either '1' or '0' with equal probability. When, instead, a small positive input differential voltage is applied, the probability that the output is '1' is larger than '0'. Thus,  $F(x)$  can be obtained applying a ramp of differential voltages and computing the probability of having 1 at the output. This probability as a function of the input differential voltage,  $v_{diff}$ , can be computed averaging the output of the comparator [33]:

$$P(v_{diff}) = \frac{n_1}{N_{tot}} = \frac{1}{2} \left[ 1 + \operatorname{erf} \left( \frac{v_{diff} - \mu}{\sigma\sqrt{2}} \right) \right], \quad (4.5)$$

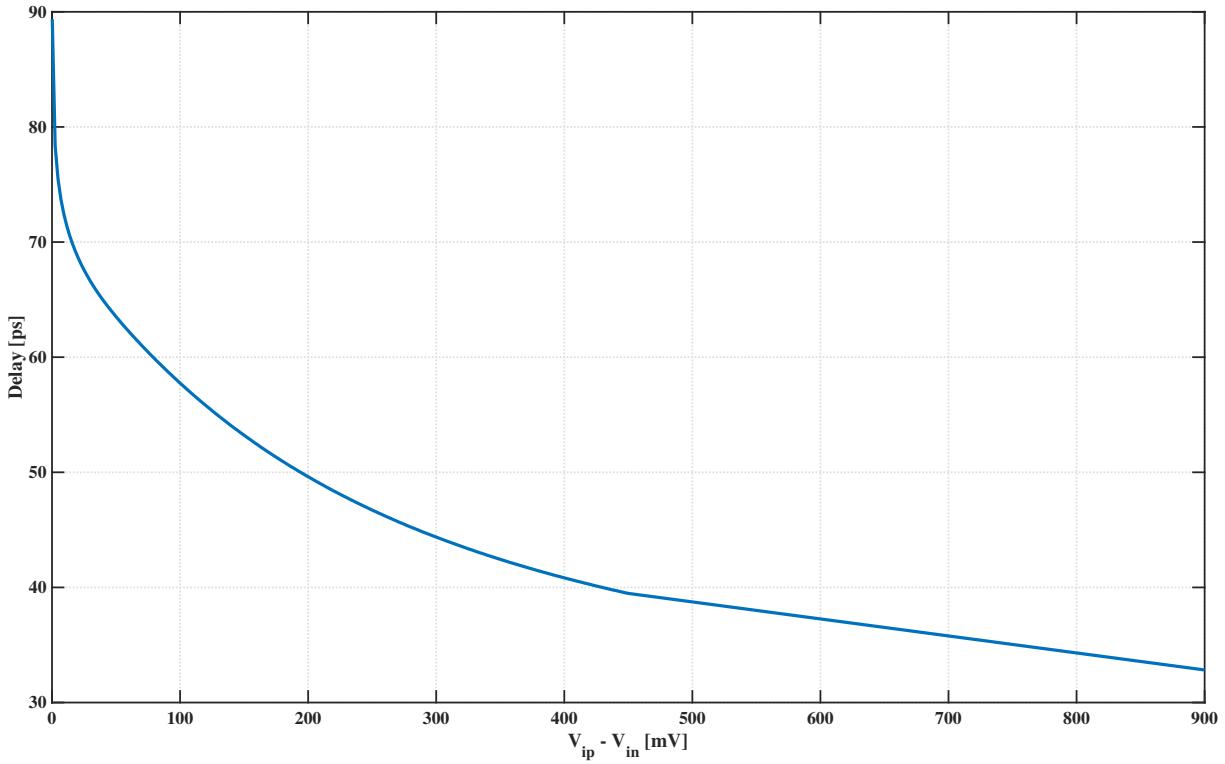
where  $n_1$  is the number of 1s and  $N_{tot}$  is the total number of samples collected in one simulation. For each applied input  $v_{diff}$ , 2000 samples were collected with the noise bandwidth set to 100 GHz. The obtained CDF is shown in Figure 4.7. From the data, it was possible to extrapolate the standard deviation of the distribution, i.e., the input-referred voltage noise of the comparator, approximately equal to  $200 \mu V$ . The noise is larger than expected ( $126 \mu V$ ), i.e., approximately the quantization noise, because the analysis in Section 3.3 included only the contribution of the input differential pair. In particular, the



**Figure 4.8:** Input-referred noise of the dynamic comparator as a function of the temperature.

noise of the second stage was not considered at all, but it is not a correct assumption. Since it is possible to select the block that adds noise in the circuit, when setting the transient noise simulation, the same simulation was repeated considering selectively the noise of the first or the second stage. It turns out that the input-referred noise voltage contributions of the first and second stage of the comparator are  $146 \mu V$  and  $137 \mu V$ , respectively. Thus, the noise of the two stages is comparable and it is not possible to completely neglect the noise of the latch. This is mainly caused by the fact that the amplification of the first stage is low, approximately 3 considering a small differential input voltage. Finally, it is worth mentioning that all the calculations for setting the capacitance at the output nodes of the first stage were carried out considering a temperature of  $27^\circ C$ , whereas the simulation was carried out at  $100^\circ C$ . Therefore, the input-referred noise is larger than expected. Another simulation was performed to compute the comparator noise as a function of the temperature to check whether or not the noise was close to the hand-made estimations. The results are shown in Figure 4.8. It is possible to note how the comparator noise is comprised between  $138 \mu V$  and approximately  $200 \mu V$  for a temperature between  $27^\circ C$  and  $100^\circ C$ . As already pointed out, the noise is larger than expected since the hand-made calculations were based on wrong assumptions.

**Speed and power consumption** The dynamic comparator speed was tested in the same way as for the static comparator. The outputs of the comparator were loaded with 10-fF capacitors, since in a real implementation the control logic circuit will add a capacitive load. A plot of the comparator delay as a function of the input differential voltage is shown in Figure 4.9.



**Figure 4.9:** Delay vs. input differential voltage of the dynamic comparator.

|                   |       |
|-------------------|-------|
| Delay [ps]        | 88-32 |
| Power [ $mW$ ]    | 1.8   |
| Noise [ $\mu V$ ] | 200   |

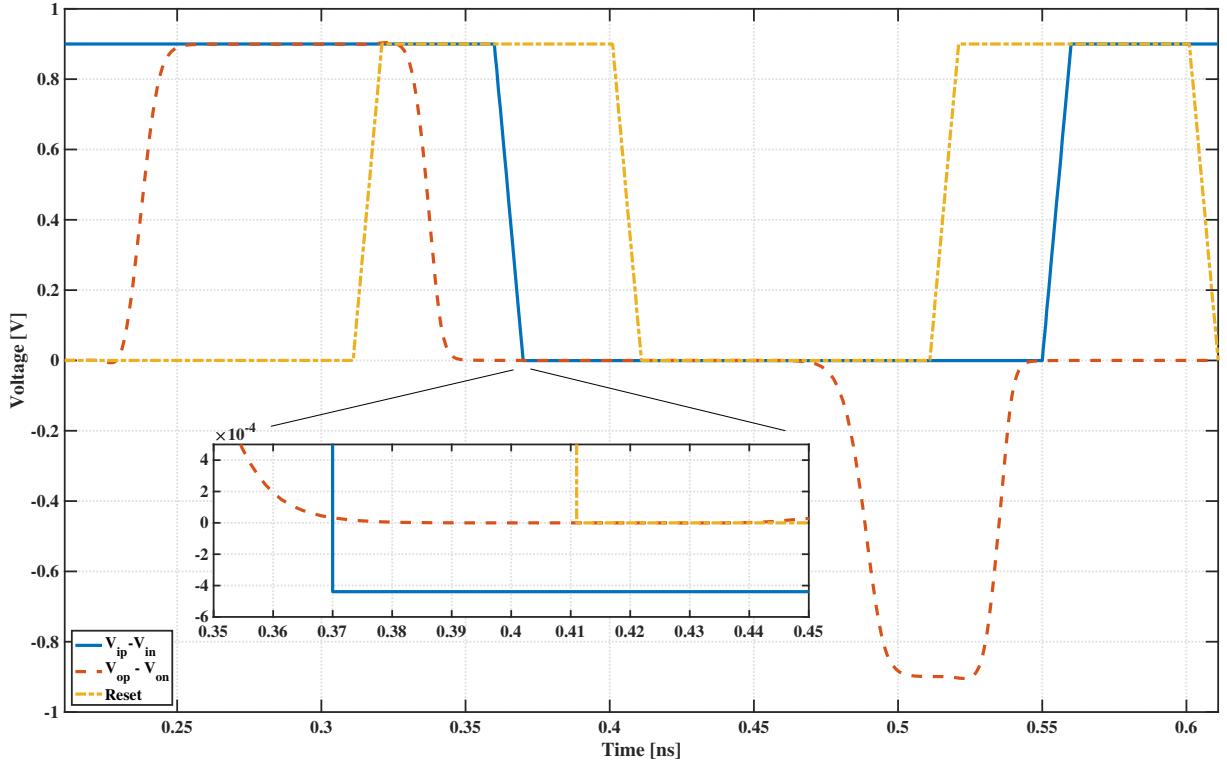
**Table 4.2:** Summary of the performance of the dynamic comparator.

The comparison time ranges between 88 ps and 32 ps considering an input voltage ranging between  $200 \mu V$  and  $0.9 V$ .

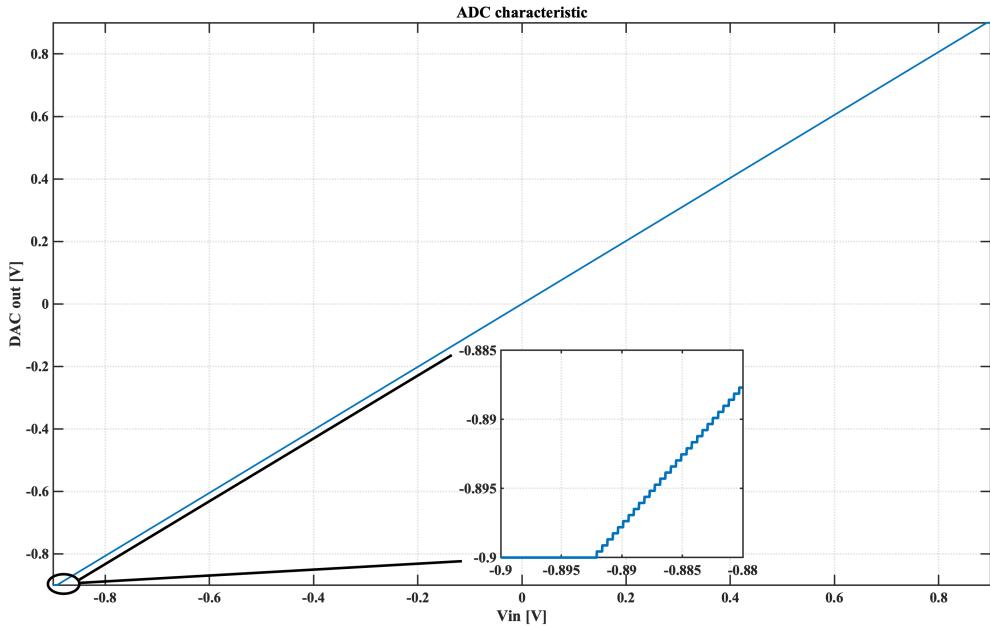
The ORT of the dynamic comparator is shown in Figure 4.10. The test was performed applying a voltage of  $0.9 V$  in the first cycle and  $-1LSB$  in the second cycle. In the case of a dynamic comparator, this test is useful to check whether the nodes in the circuit are correctly reset or not. If not, the comparator takes the wrong decision when it has to compare a small differential voltage of opposite sign in the second cycle of the test.

The comparator power consumption in the SAR ADC is  $1.8 mW$ , computed as the product between the current, averaged on the sampling period, and the supply voltage. If we use Eq. (3.17), replacing the capacitor value with the sum of the capacitors  $C_a$ ,  $C_1$  and  $C_2$  of Figure 3.6, the theoretical value of the power consumption would be  $1.33 mW$ . Therefore, there are approximately  $500 \mu W$  to take into consideration. In this case, the remaining power consumption is mainly caused by the cross-conduction current flowing when the latch of the second stage is toggling. A summary of the performance of the dynamic comparator is shown in Table 4.2.

The power consumption is approximately 5.4 times larger than the energy estimated ( $335 \mu W$ ) in Chapter 2. The error in the estimation is mainly caused by the fact that the capacitance at the output of the first stage of the comparator was computed considering a noise equal to half LSB, instead of the quantization noise. Moreover, the temperature used in the simulation was  $100^\circ C$ , whereas it was assumed  $27^\circ C$  in the computation. Finally, the power dissipated when the latch toggles was completely ignored in the model.

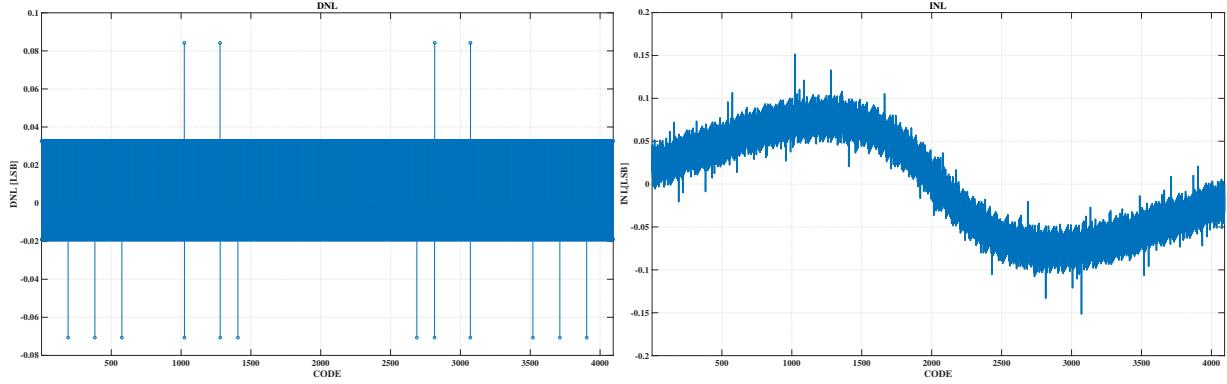


**Figure 4.10:** Overdrive recovery test of the dynamic comparator.



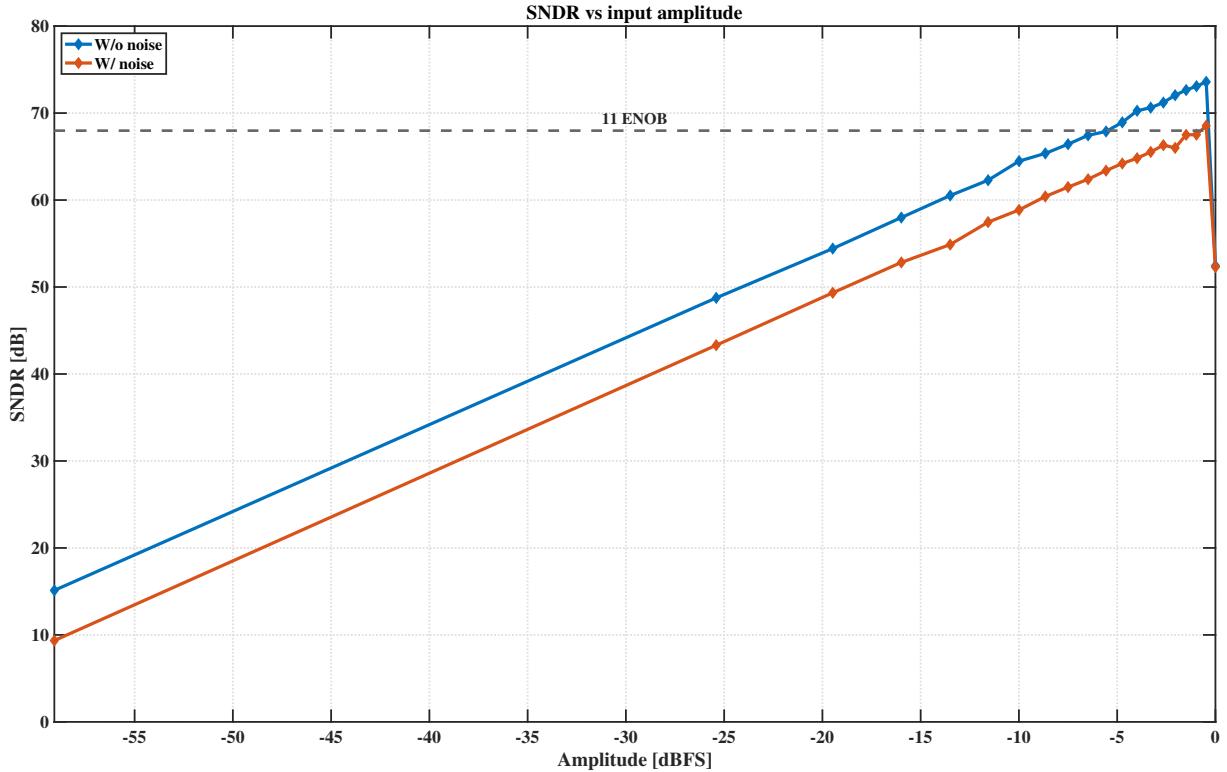
**Figure 4.11:** Input-output characteristic of the SAR ADC with the dynamic comparator.

**Effect of the dynamic comparator on the linearity of the converter** The previous considerations regarding the comparator are related to comparator on its own. However, the comparator is designed to be employed in the SAR ADC. Therefore, both static metrics and dynamic metrics were evaluated to investigate the effect of this block on the linearity of the converter. The input-output characteristic of



**Figure 4.12:** DNL and INL caused by the dynamic comparator.

the converter, simulating only the comparator at transistor level and the remaining block as behavioural models, is shown in Figure 4.11. It can be seen from the zoomed portion that there is a loss of the dynamic range of the converter. In fact, the first step of the characteristic does not start at  $-0.9 \text{ V} + \text{LSB}$ , but approximately at  $-0.8921 \text{ V}$ . This can be explained taking into account the input parasitic capacitance of the comparator. Therefore, the capacitive partition at the DAC output during the conversion is attenuated by this capacitance. The INL and DNL computed from the IO characteristic are shown in Figure 4.12. The DNL is approximately within  $[-0.07, 0.08]$  LSB, whereas the INL is within  $[-0.1, 0.1]$  LSB. Thus,



**Figure 4.13:** SNDR versus the input amplitude of a sinewave at 10.449 MHz with and without noise.

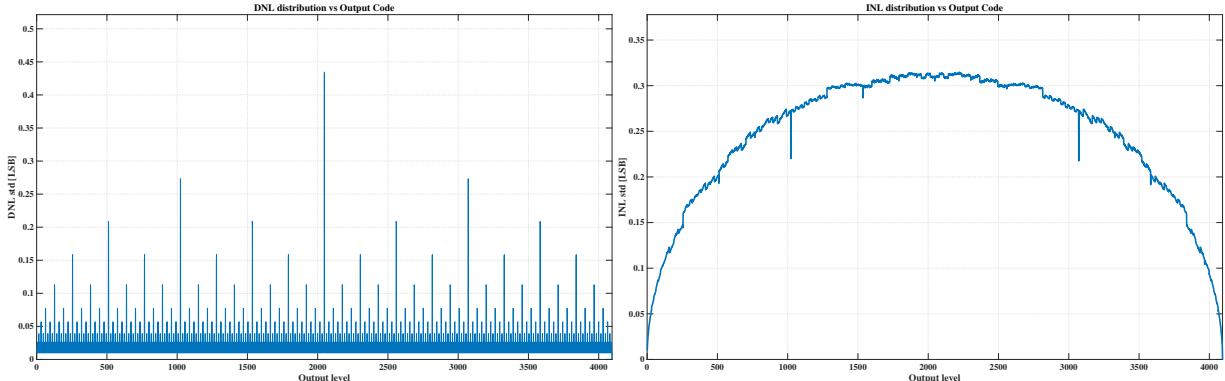
the dynamic comparator does not affect the conversion of the input signal in a significant way as opposed to the static comparator. The effect of the non-linear capacitance at the input terminals of the comparator is present also with the dynamic comparator. However, the area of the input pair is 3.25 times smaller in the case of the dynamic implementation. The dimensions are smaller because the tail transistor behaves like a switch that ties the source of the input pair to ground. In the static comparator, the tail transistor

behaves, instead, as a current source. Therefore, it is necessary to have at least an overdrive voltage between its drain and source in order to have the transistor working in saturation region. The overdrive voltage is, thus, larger in the case of the dynamic comparator, hence smaller transistor dimensions for the same current. An in-depth comparison between the two comparators has not been carried out since it is outside the scope of this work. Moreover, they have different input-referred noise, therefore it would not be a fair comparison. Based on the static metrics, the dynamic comparator was chosen for the implementation of the SAR ADC.

Finally, the dynamic performance were obtained with a simulation of the SNDR as a function of the input amplitude of a sinewave. The result is shown in Figure 4.13 with and without noise. The frequency of the input sinewave was 10.449 MHz for coherent sampling and the number of samples was 2048. The maximum SNDR is 73.58 dB. The effect of the noise reduces the maximum SNDR to 68.54 dB. Therefore, the noise reduces the ENOB of the converter by approximately 0.8 bit. From the spectra of the sinewave, it is possible to compute the noise of the comparator making the difference of the noise power of the spectra with and without noise. The noise introduced by the comparator from this calculation is approximately  $196 \mu V$ , in line with the result shown above regarding the comparator noise.

## 4.2 DAC

The capacitance variability in custom-designed capacitors is unknown, therefore the effect of mismatch between the DAC capacitors could not be simulated in the technology library environment. The effect of the capacitor variability on the linearity of the ADC has been evaluated through the use of Matlab simulations. A Matlab model of the SAR ADC, based on the models presented in [22], was used. The

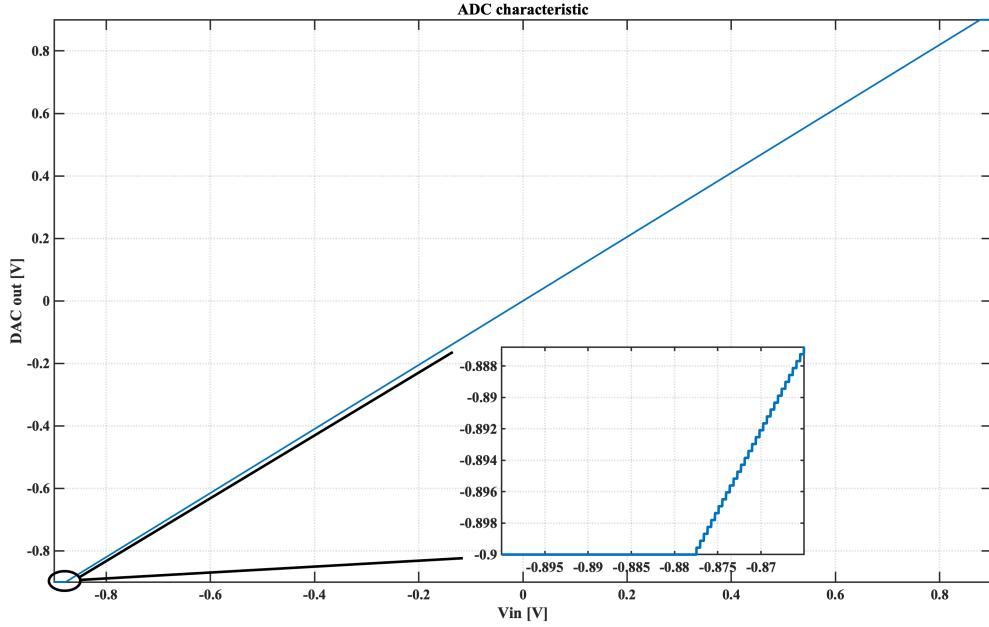


**Figure 4.14:** Standard deviation of the DNL and INL after 1000 MC simulations with a relative mismatch set to 1 %.

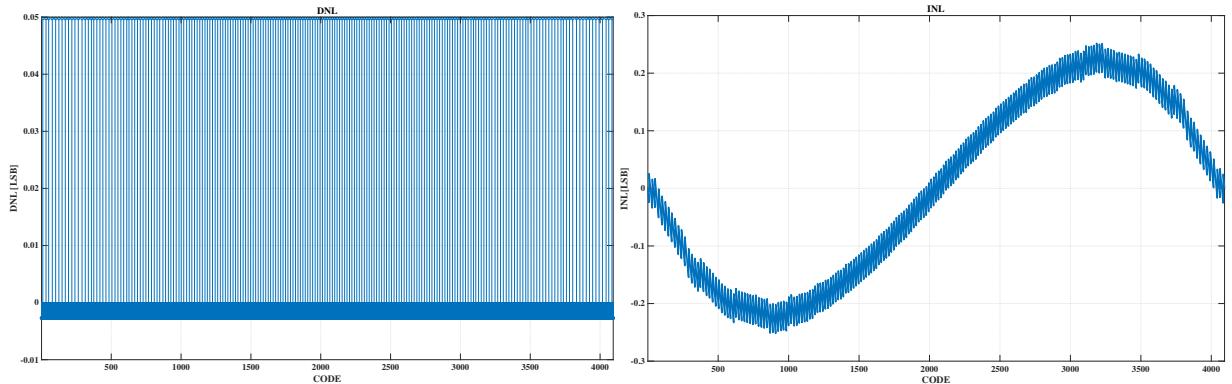
relative mismatch of the capacitors was estimated to be 0.6% in the previous chapter, based on the simulations of the MOM capacitors provided in the library. However, a relative mismatch of 1 % was considered to be conservative. The standard deviation of the DNL and INL obtained with 1000 samples are shown in Figure 4.14. As expected, the peak of the non-linearity happens when all the capacitors are switched, i.e., at the transition between 011111111111 and 100000000000. The standard deviation of the DNL is smaller than 0.5 LSB as predicted by Eq. 2.18.

### 4.3 Sampling switches

The effect of the sampling switches has been tested in the same way as the comparator. Thus, the other blocks in the system were Verilog-A blocks, whereas the sampling switches were simulated at transistor level. The resulting input-output characteristic is shown in Figure 4.15, whereas the DNL and INL are shown in Figure 4.16. The plateaus at the beginning and at the end of the characteristic are caused by the



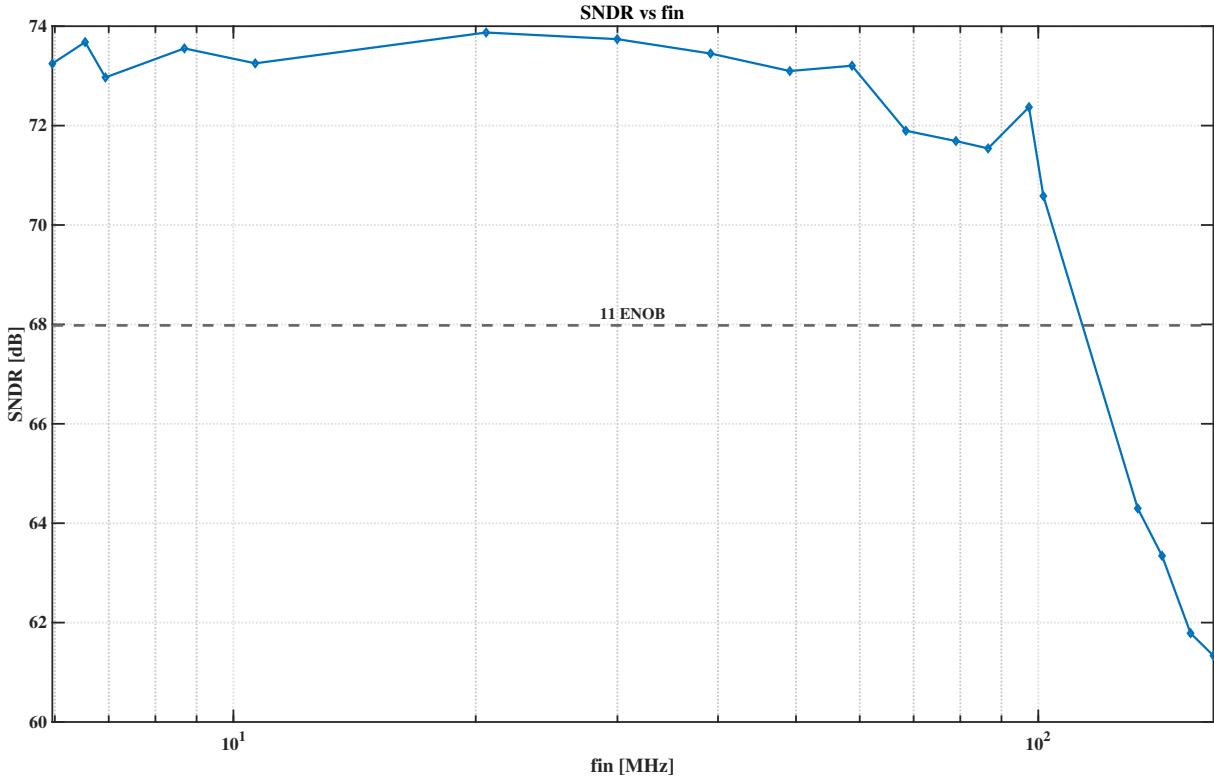
**Figure 4.15:** IO characteristic of ADC simulating the switches at transistor level.



**Figure 4.16:** DNL and INL caused by the sampling switches.

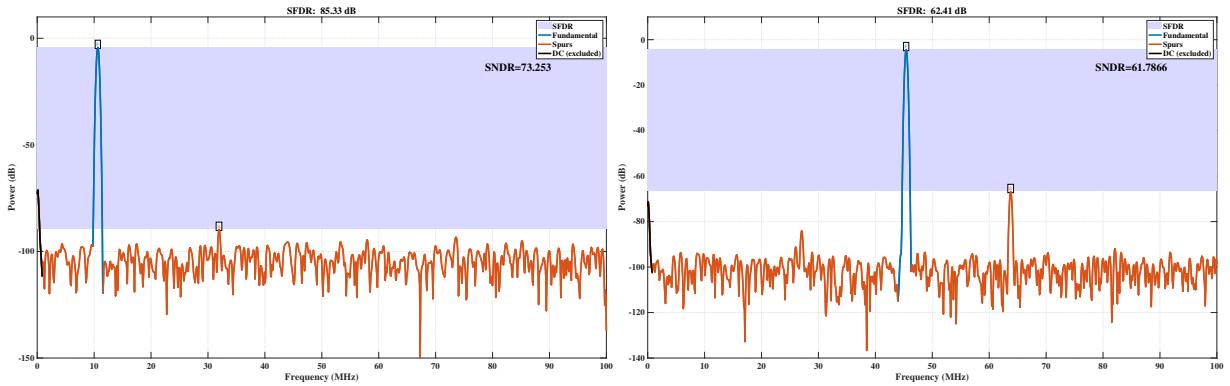
capacitance added by the switches in parallel to the DAC capacitance. The INL caused by the switches ranges approximately between  $-0.2\text{ LSB}$  and  $0.2\text{ LSB}$ , thus they not introduce an excessive non-linearity in the converter and the static performance can be considered acceptable. The power consumption of the sampling switches is  $35 \mu\text{W}$ , computed as the product between the supply voltage and the average current provided to the circuit on the whole sampling period.

As already mentioned, the bootstrap circuit is used to improve the linearity of the sampling switches. Therefore, the SNDR has been obtained as a function of the frequency of a sinewave with a 850-mV amplitude at the input of the SAR ADC with 2048 samples. The results from the simulation are shown



**Figure 4.17:** SNDR as a function of the frequency of an input sinewave.

in Figure 4.17. Since the converter has a 200-MHz sampling frequency, the sampling switches should be able to sample the input signal without adding much distortion at least up to 100 MHz. From the graph, it is possible to note how the SNDR is larger than 68 dB (11 ENOB) for input frequencies up to 100 MHz. However, the performance of the switches worsens as the input frequency gets higher and the SNDR rolls off. If we consider two spectra, one for a low input frequency and the other one for a high



**Figure 4.18:** Spectra of the output sinewave of the ADC for two different frequencies with same amplitude, simulating the sampling switches at transistor level.

input frequency, the third harmonic is much higher in the latter case due to the distortion introduced by the switch. This is shown in Figure 4.18. In the left plot, the frequency of the sinewave is 10.64 MHz, whereas in the right plot there is the spectrum of a 142.48-MHz sinewave. The main difference between the spectra is that there is a much larger third harmonic with the high-frequency sinewave that results in a difference of the spurious-free dynamic range (SFDR) of more than 20 dB. The distortion may be caused by the fact that the bottom plate of the capacitance that behaves like a battery for the switches is not

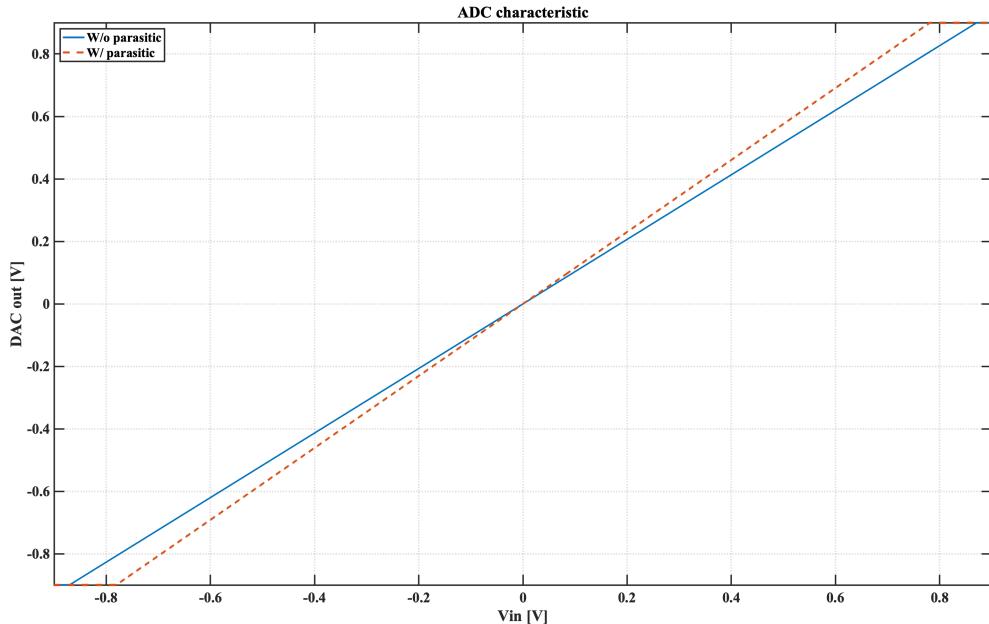
able to follow the variation of the input signal during the tracking time for high-frequency signals. This suggests that the resistance of M<sub>5</sub> in Figure 3.13 should be reduced increasing its aspect ratio. However, this could potentially increase the charge-sharing from the top plate of the capacitor. For the scope of this work, the switch does not limit the performance of the converter since the effective resolution is larger than 11 for frequencies up to the Nyquist limit.

## 4.4 System performance

After evaluating the effects on the linearity caused by the blocks of the converter, the whole SAR ADC was simulated to obtain static and dynamic metrics.

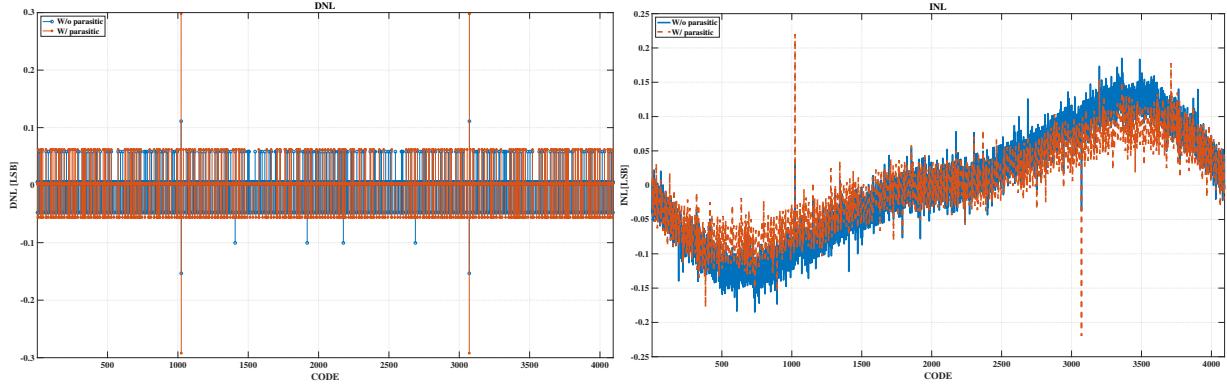
**Static metrics** As it is mentioned in the previous chapter, the DAC is composed of 2048 unit custom-designed capacitors. The value of the unit capacitance has been simulated with a 3-D electromagnetic field-solver. Initially, the IO characteristic of the SAR ADC was obtained simulating the DAC as the parallel connection of capacitors from the analog library in Cadence Virtuoso with a capacitance of 0.8 fF. Then, the capacitors  $C_{TS}$  and  $C_{BS}$  in Table 3.4a were added to model the effect of the parasitic capacitors between the top (bottom) and ground. Finally, the capacitor model from the 3-D simulator was used. These three steps have been carried out to gradually increase the complexity of the system.

The IO characteristics considering ideal capacitors with and without parasitics are shown in Figure 4.19. From the results, it is possible to note how the presence of parasitic capacitors reduces the dynamic

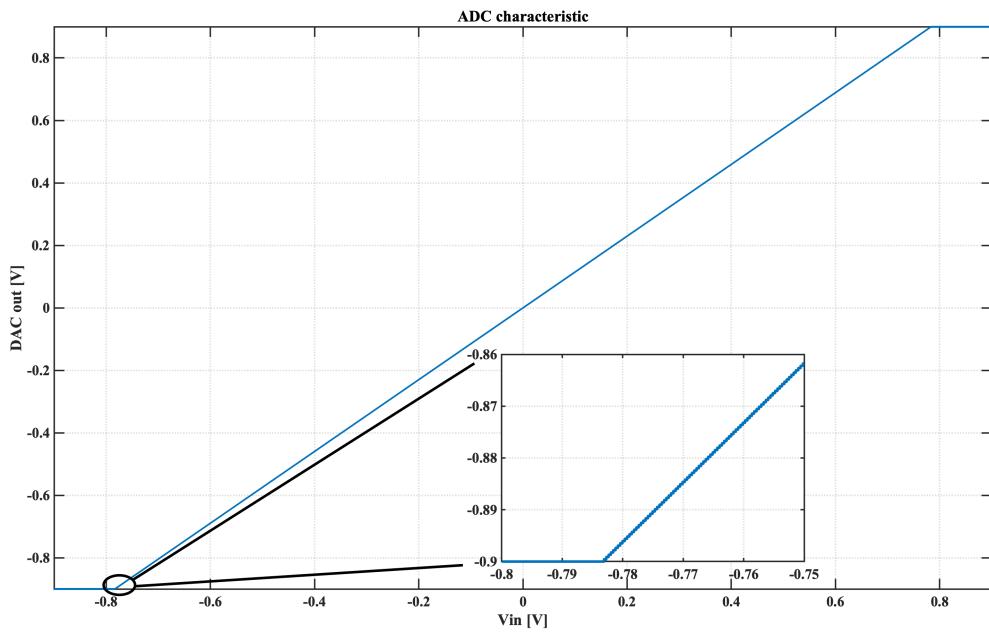


**Figure 4.19:** IO characteristic of the SAR ADC with all the designed circuits simulated at transistor level and ideal DAC capacitors.

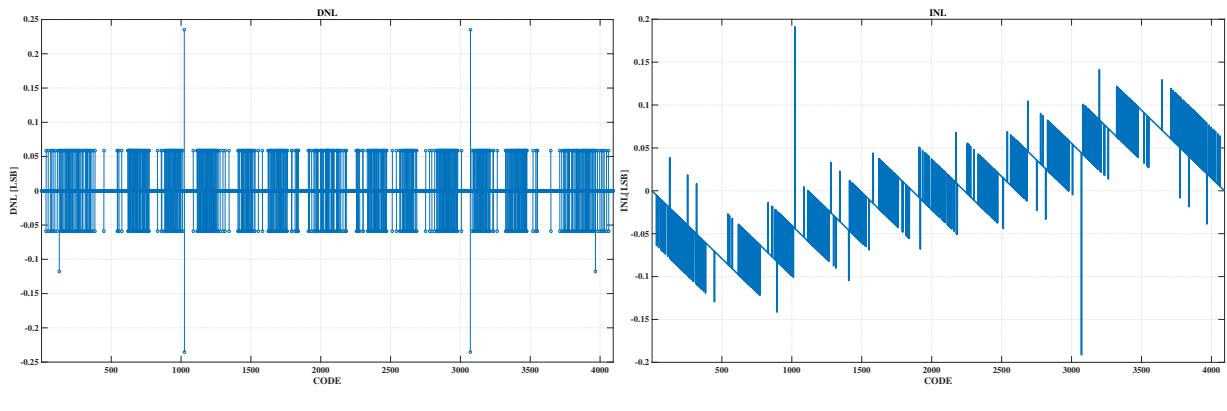
range of the converter. The first step of the stair considering the parasitic is, indeed, at approximately at -0.780 mV. The DNLs and INLs obtained from the two IO characteristics are shown in Figure 4.20. The DNL is within [-0.15, 0.1] LSB and [-0.3, 0.3] LSB without and with the parasitics, respectively, whereas the INL is within [-0.15, 0.15] LSB and [-0.22, 0.22] LSB without and with the parasitic, respectively. If we look closely, the INL increased only in the peaks at codes 1024 and 3072, whereas looking elsewhere it has decreased. A possible explanation is the following. The overall capacitance



**Figure 4.20:** DNL and INL of the ADC simulating an ideal DAC with and without parasitics.



**Figure 4.21:** IO characteristic of the SAR ADC with the custom-designed unit capacitance.



**Figure 4.22:** DNL and INL of the ADC.

of the DAC has increased with respect to its ideal value due to the presence of the top-plate parasitic. Therefore, the weight of the non-linear input parasitic capacitance of the comparator with respect to the

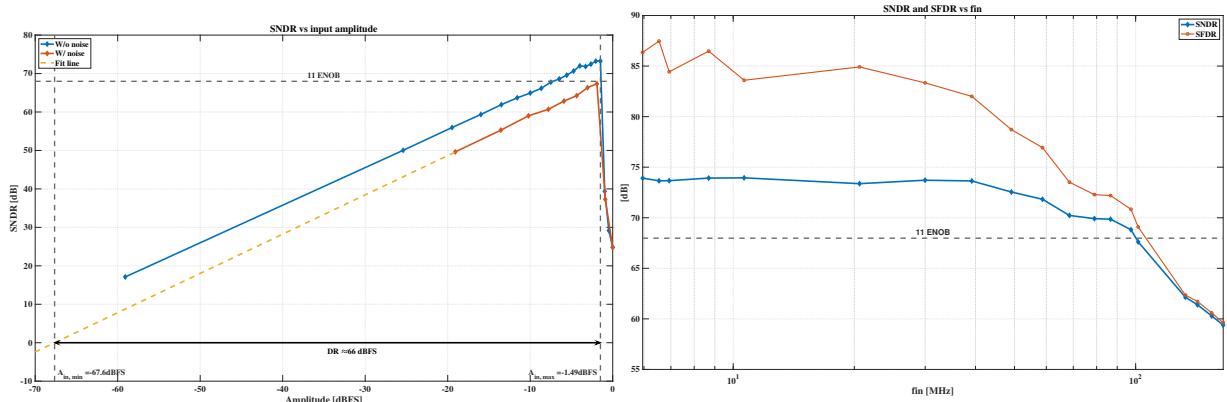
total capacitance of the DAC is reduced, hence a reduced INL and slightly improved linearity.

Finally, the ADC was simulated with the DAC capacitors extracted by the 3-D simulator. The IO characteristic of the designed SAR ADC is showed in Figure 4.21. The resulting DNL and INL are showed in Figure 4.22. The DNL is approximately within [-0.25, 0.25], whereas the INL is within [-0.19, +0.19] LSB. As it is possible to note from the simulations, the result with ideal and extracted capacitor are similar. Therefore, the dynamic metrics has been obtained simulating the DAC with capacitors from the analog library, drastically reducing the simulation time.

**Dynamic metrics** In terms of dynamic metrics, various simulations were run to obtain the following curves:

- SNDR as a function of the input amplitude (see Figure 4.23a), with and without noise, for an input frequency of 20.898 MHz,
- SNDR as a function of the input frequency (see Figure 4.23b) with an input amplitude of 750 mV.

The spectra of the sinewaves were obtained from 1024 samples. From the SNDR versus input amplitude



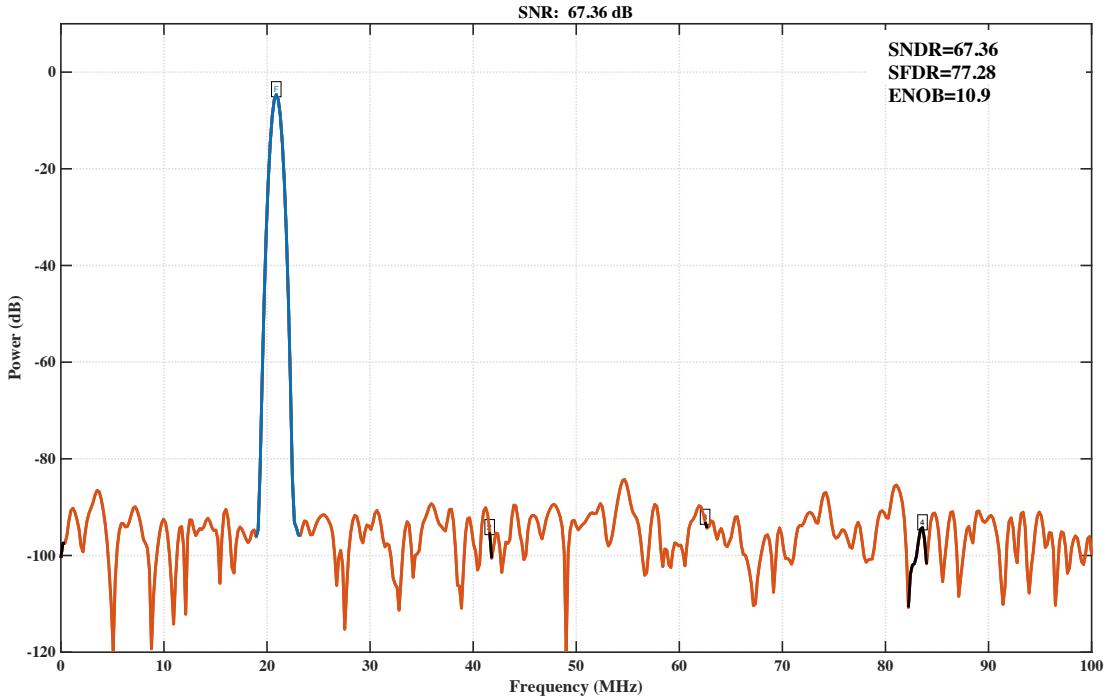
(a) SNDR versus input amplitude, with and without noise. The input frequency is 20.898 MHz.

(b) SNDR and SFDR versus input frequency for an input amplitude of 750 mV. Note that it is not obtained from a transient noise simulation.

**Figure 4.23:** SNDR versus amplitude and input frequency.

with noise the SNDR and SFDR are 67.4 dB and 77.3 dB, respectively. This results in an ENOB of 10.9. Due to the parasitics and noise, the dynamic range (DR) results 66 dB, much smaller than the theoretical value of 74 dB for a 12-bit converter. If we consider, instead, the SNDR versus input frequency, the SNDR remains close to 74 dB up to 40 MHz. Then, it starts to drop approaching 68 dB at 100 MHz. This is due to the distortion caused by the sampling switches. The bandwidth of the converter is 79 MHz. Note that this simulation was not performed with noise since it does not affect the bandwidth of the converter.

The power spectrum for the amplitude corresponding to the peak SNDR (with noise) is showed in Figure 4.24.



**Figure 4.24:** Power spectrum with noise at 200 MSps with a 20.89-MHz input.

To summarize, the converter has:

- an ENOB of 10.9 with an input bandwidth of 79 MHz,
- a dynamic range of 66 dBFS,
- a DNL within [-0.25, 0.25] LSB and an INL within [-0.19, 0.19] LSB.

## 4.5 Power consumption

The power consumption of the converter is divided between the sampling switches, the SAR logic, the comparator and the DAC. It is possible to estimate the DAC power consumption considering the average power consumption of the monotonic switching algorithm. The average switching energy required by the monotonic switching algorithm is approximately  $1023C_uV_{dd}^2$ . The product between energy and sampling frequency gives the power consumption of the DAC:

$$P_{sw} = f_s E_{ave,monotonic} = 132 \mu W. \quad (4.6)$$

If we add also the energy required to sample the input signal, the DAC energy consumption will be:

$$P_{dac} \approx P_{sw} + 2C_{dac}V_{dd}^2f_S = 530 \mu V + 132 \mu V = 662 \mu V. \quad (4.7)$$

Even though the control logic of the converter has not been implemented, it is still possible to have a rough estimate of the order of magnitude of the power consumption. The power consumption of a digital circuit can be expressed as [27]:

$$P_{logic} \approx \alpha CV_{dd}^2f, \quad (4.8)$$

where  $\alpha$  is the switching activity,  $C$  is the capacitance switched in each clock cycle at a frequency  $f$ . An estimate of the logic power consumption can be obtained from the results reporting in [23]. The

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reported SAR ADC is controlled by the same logic as the one used in this work. Therefore, it is possible to have an estimate on the logic power consumption accounting for the technology scaling, different power supply and sampling frequency. In [23], the logic circuit dissipates approximately 200 nW with sampling frequency of 100 kHz and a supply voltage of 0.5 V. In the work presented in this thesis, the power supply has increased by 0.9/0.5 and the sampling frequency by (200MHz/100kHz). However, we need to take into account the technology scaling. The capacitance of the logic scales as  $1/S$ [27], where S is the scaling factor. Thus, a rough estimate of the power consumption taking into consideration the number of bits of the control logic circuit is:

$$P_{logic} \approx 200nW * \left( \frac{28 nm}{130 nm} \right) \left( \frac{0.9}{0.5} \right)^2 * \left( \frac{12}{10} \right) * \left( \frac{200 MHz}{100 kHz} \right) = 335 \mu W. \quad (4.9)$$

|            | P [mW] |
|------------|--------|
| DAC        | 0.662  |
| Comparator | 1.8    |
| Switches   | 0.034  |
| Logic      | 0.335  |
| Total      | 2.83   |

**Table 4.3:** Summary of the power consumption of the blocks in the SAR ADC.

A summary of the power consumption of the blocks in the SAR ADC is shown in Table 4.3. The power consumption is dominated by the contribution of the comparator as it was expected from the estimates given in Chapter 2. The control logic circuit was not implemented at transistor level. However, its contribution is estimated approximately a factor 5 smaller than the contribution of the comparator.

From the power consumption and the results on the SNDR, the FoM of the converter for a sampling frequency of 200 MSps is:

$$FoM = \frac{P_{tot}}{2^{ENOB} f_s} = 7.4 fJ/conv-step. \quad (4.10)$$

## 4.6 Overall discussion and summary

From the results, the converter achieves good performance both in terms of static metrics and dynamic metrics.

Let us consider the static metrics. The circuits that add the highest contribution to the INL of the converter are the sampling circuit and the DAC. It is worth noting that the contribution of the comparator and the sampling circuit have opposite sign, even if the trend is the same S-shape. This results in an overall INL of the converter within [-0.19, 0.19] LSB, as if the effects of the two blocks compensate each other. It is yet to be understood if this is a fortuitous case or it is a systematic effect that can be exploited to improve the performance of the converter. Finally, the parasitic capacitors added by the custom-designed capacitor, the comparator and the sampling switches reduce the dynamic range of the converter. This is due to the attenuation at the DAC output caused by the parasitic capacitors. At this point of the discussion, it is worth pointing out that MC simulations were not performed in Cadence Virtuoso. Thus, the effect of the DAC capacitance mismatch is not accounted for. From the results of the simulations in Matlab, the performances of the converter are limited by the DAC capacitance mismatch, since it adds the largest contribution to the INL of the converter. On top of the mismatch, effect of gradients on the wafer and a non-symmetric layout will further worsen the ADC performance. This is particularly true for

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custom-designed devices, in which no models are available to simulate mismatch effects. To summarize, the INL of the converter is within [-0.19, 0.19] LSB, but this value is expected to increase taking into consideration the DAC capacitance mismatch, which will limit the ADC performance.

Let us consider the dynamic metrics without taking noise into consideration. The ADC is able to achieve almost a 12-ENOB resolution (without the comparator noise) for an input frequency around a tenth of the Nyquist limit. The linearity is mainly limited by the sampling switches for input frequencies larger than approximately 80 MHz. However, the resolution remains approximately larger than 11 ENOB (without the comparator noise) up to the Nyquist limit. Therefore, the bootstrapping circuit correctly samples the signal, but this operation can still be improved to reach a 12-ENOB resolution before going on with the layout of the circuit, for input frequencies up to the Nyquist limit. The main limitation is that the bottom-plate of the capacitance in the bootstrapping circuit is not able to follow the quick variations of the input signal. This suggests, therefore, the possibility to improve the sampling operation focusing on this problem. Something that is worth mentioning is charge-sharing and charge-injection. These two unwanted phenomena add distortion reducing the performances of the sampling circuit and they should also be further reduced to achieve a high-linear sampling operation.

Let us, now, take into consideration noise. There are two main sources of noise, namely comparator and kT/C noise, apart from the quantization noise. The dominant contribution is added by the comparator, whereas kT/C noise is smaller than quantization noise. Therefore, the main limitation in terms of noise is set by the comparator and the resulting ENOB is 10.9. Increasing the capacitance at the output of the first stage could be useful to reduce the input-referred noise. However, it would come at the cost of power consumption and speed. In particular, the comparator would be even slower and it is possible that the converter would fail to successfully convert 12 bits in 2.5 ns. For the scope of this work, the targeted ENOB was larger than 10 as shown in the red box of the left plot in Figure 1.2, thus it can be considered acceptable.

|                    |            |
|--------------------|------------|
| Technology [nm]    | 28         |
| Resolution [bit]   | 12         |
| Supply [V]         | 0.9        |
| Sample rate [MSps] | 200        |
| DNL [LSB]          | -0.25/0.25 |
| INL [LSB]          | -0.19/0.19 |
| DR [dBFS]          | 66         |
| Power [mW]         | 2.83       |
| ENOB               | 10.9       |
| FoM [fJ/conv-step] | 7.4        |

**Table 4.4:** Summary of the SAR ADC performance.

Finally, the power consumption of the converter is 2.83 mW, that results in a FoM of approximately 7.4 fJ/conv-step with a sampling frequency of 200-MSps. The power consumption is mainly dominated by the contribution of the dynamic comparator. The capacitors added to reduce the noise of this block need to be charged and reset between each conversion step requiring a considerable amount of energy from the power supply. This is one of the trade-off between noise and power consumption present in all the analog circuits. Therefore, the power consumption could be reduced at the cost of a larger noise. However, it was found that an important contribution of the comparator power consumption is due to the cross-conduction current that flows between the voltage supply and ground while the latch is toggling. Therefore, a possible way to reduce the power consumption could be to reduce this current. The second

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source of power consumption comes from the DAC. Therefore, reducing the value of the unit capacitance of the DAC could help to reduce the power consumption of the circuit and area. However, this would come at the cost of larger mismatch and worse performance of the ADC.

A summary of the ADC performance is shown in Table 4.4. In order to have a fair comparison with other state-of-the-art SAR ADC, the control logic circuit should have been implemented at transistor level. Therefore, a comparison is not included here.

# Chapter 5

## Conclusions

**Summary** In this work, the development of a fully-differential SAR ADC in a 28-nm technology node is presented. The SAR ADC employs a modified version of the monotonic switching algorithm. This results in a reduction of power consumption and area with respect to the conventional charge-redistribution SAR ADC.

The ADC samples the input signals with bootstrapped switches. The bootstrapping circuit keeps the gate-source voltage of the transistor switch constant. Thus, reducing the distortion caused by the switch on-resistance variation as a function of the input voltage. The signals are sampled on the DAC capacitors. Each DAC is a binary-weighed array of 2048 unit capacitors. In order to reduce the area and the power dissipation, the DAC unit capacitor is a custom-designed device with a capacitance of 0.8 fF. During the development of the SAR ADC, a static and a dynamic comparator were designed. The dynamic comparator has been chosen since it has lower power consumption and it does not limit the linearity of the converter as opposed to the static comparator. In this work, the SAR logic, which controls all the operations in the ADC, has been implemented as a model in Verilog-A. The logic is asynchronous and it can be implemented with dynamic logic gates. The total power consumption of the ADC is 2.83 mW. The comparator is the dominant contribution (1.8 mW). Therefore, it is necessary to focus on the comparator to reduce the ADC power consumption. This comes, of course, at the cost of noise, hence lower resolution. The FoM of the SAR ADC is 7.4 fJ/conv-step at a sampling frequency of 200 MSps.

The effects on the linearity of the converter caused by the designed blocks were evaluated with the co-simulation of Verilog-A models and schematics. Based on the simulations in Cadence Virtuoso and Matlab, the DAC capacitance mismatch is one of the dominant effects for the INL and DNL of the converter. Not taking into account the capacitance mismatch, the DNL and INL of the converter are within [-0.25, 0.25] LSB and [-0.19, 0.19] LSB, respectively. The parasitic capacitors of the DAC, comparator and sampling switches reduce the dynamic range of the converter to 66 dB from the ideal 74 dB for a 12-bit resolution ADC. If we consider the dynamic metrics, the main limitation is caused by the comparator noise that reduces the resolution of the converter. Considering an input signal at 20.89 MHz, the SNDR and SFDR are 67.36 dB and 77.28 dB, respectively. The resulting effective resolution is 10.9 ENOB. When the frequency of the input signal approaches the Nyquist limit, the sampling switches are not able to correctly sample the signal limiting the linearity of the ADC. As a matter of fact, the SNDR is reduced by 3 dB at 79 MHz.

**Future work** The next step of this work should be the implementation of the control logic and the improvements of the designed blocks, before the layout. The bootstrap circuit limits the linearity of

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the ADC when the frequency of the input signals approaches the Nyquist limit. Therefore, it should be improved to increase the bandwidth of the converter. Some of the power consumption of the comparator could be reduced to improve the efficiency of the converter. However, it is necessary an innovation of the circuit or a different topology to have a real boost in performance, since there is not much room for improvement. A possible way to further reduce the power consumption of the DAC is decreasing the value of the unit capacitance. This will cause the ADC to worsen its performance. In fact, the input capacitance of the comparator and the other parasitics will have a greater role. Moreover, the matching between the capacitors will inevitably be reduced. However, the errors caused by mismatch can be potentially compensated with a calibration circuit. Therefore, the unit capacitance value should be reduced to improve the energy efficiency of the converter. Finally, the control logic circuit should be implemented at transistor level and simulated to check whether the performance of the circuit are limited or not by the DAC settling in each conversion step. This issue was not considered in this work, since the switch buffers to control the DAC capacitors have not been designed.

# Bibliography

- [1] K. Dawon and M. Atalla, “Silicon-silicon dioxide field induced surface devices,” in *the Solid State Device Research Conf., Pittsburgh, PA. June 1960*, 1960.
- [2] J. Bardeen and W. H. Brattain, “The transistor, a semi-conductor triode,” *Phys. Rev.*, vol. 74, pp. 230–231, Jul 1948, last accessed: May 26, 2020. [Online]. Available: <https://link.aps.org/doi/10.1103/PhysRev.74.230>
- [3] B. Murmann, “Adc performance survey 1997-2020.” [Online]. Available: <http://web.stanford.edu/~murmann/adcsurvey.html>
- [4] F. Maloberti, *Data Converters*. Springer US, 2007.
- [5] S. A. Zahrai and M. Onabajo, “Review of analog-to-digital conversion characteristics and design considerations for the creation of power-efficient hybrid data converters,” *Journal of Low Power Electronics and Applications*, vol. 8, no. 2, p. 12, 2018.
- [6] B. Razavi, *Principles of data conversion system design*. IEEE Press, 1995.
- [7] W. Kester, “Which adc architecture is right for your application,” in *EDA Tech Forum*, vol. 2, no. 4, 2005, pp. 22–25.
- [8] ———, “Adc architectures iv: Sigma-delta adc advanced concepts and applications,” *Analog Devices, Tutorial MT-023*, 2008.
- [9] W. Kester, “Mt-022: Adc architectures III: Sigma-delta adc basics,” *Analog Devices, Rev. 0*, pp. 02–06, 2006.
- [10] W. M. Goodall, “Telephony by pulse code modulation,” *The Bell System Technical Journal*, vol. 26, no. 3, pp. 395–409, July 1947.
- [11] J. L. McCreary and P. R. Gray, “All-mos charge redistribution analog-to-digital conversion techniques. i,” *IEEE Journal of Solid-State Circuits*, vol. 10, no. 6, pp. 371–379, Dec 1975.
- [12] P. J. Harpe, C. Zhou, Y. Bi, N. P. van der Meij, X. Wang, K. Philips, G. Dolmans, and H. De Groot, “A  $26\mu$  w 8 bit 10 ms/s asynchronous sar adc for low energy radios,” *IEEE Journal of Solid-State Circuits*, vol. 46, no. 7, pp. 1585–1595, 2011.
- [13] D. Stepanovic, “Calibration techniques for time-interleaved sar a/d converters,” Ph.D. dissertation, EECS Department, University of California, Berkeley, Dec 2012. [Online]. Available: <http://www2.eecs.berkeley.edu/Pubs/TechRpts/2012/EECS-2012-225.html>

- 
- [14] P. Harpe, “Successive approximation analog-to-digital converters: Improving power efficiency and conversion speed,” *IEEE Solid-State Circuits Magazine*, vol. 8, no. 4, pp. 64–73, Fall 2016.
  - [15] B. P. Ginsburg and A. P. Chandrakasan, “500-ms/s 5-bit adc in 65-nm cmos with split capacitor array dac,” *IEEE Journal of Solid-State Circuits*, vol. 42, no. 4, pp. 739–747, April 2007.
  - [16] C. Liu, S. Chang, G. Huang, and Y. Lin, “A 10-bit 50-ms/s sar adc with a monotonic capacitor switching procedure,” *IEEE Journal of Solid-State Circuits*, vol. 45, no. 4, pp. 731–740, April 2010.
  - [17] S. Brenna, A. Bonfanti, and A. L. Lacaita, “A 70.7-db snrd 100-ks/s 14-b sar adc with attenuation capacitance calibration in 0.35- $\mu$ m cmos,” *Analog Integrated Circuits and Signal Processing*, vol. 89, no. 2, pp. 357–371, 2016.
  - [18] T. Rabuske, *Charge-Sharing SAR ADCs for Low-Voltage Low-Power Applications*, 1st ed., ser. Analog Circuits and Signal Processing, 2017.
  - [19] B. Ginsburg and A. Chandrakasan, “An energy-efficient charge recycling approach for a sar converter with capacitive dac,” in *2005 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2005, pp. 184–187 Vol. 1.
  - [20] D. Zhang, A. Bhide, and A. Alvandpour, “A 53-nw 9.1-enob 1-ks/s sar adc in 0.13- $\mu$ m cmos for medical implant devices,” *IEEE Journal of Solid-State Circuits*, vol. 47, no. 7, pp. 1585–1593, 2012.
  - [21] G. Huang, S. Chang, C. Liu, and Y. Lin, “A 1- $\mu$ w 10-bit 200-ks/s sar adc with a bypass window for biomedical applications,” *IEEE Journal of Solid-State Circuits*, vol. 47, no. 11, pp. 2783–2795, 2012.
  - [22] S. Brenna, A. Bonetti, A. Bonfanti, and A. L. Lacaita, “A tool for the assisted design of charge redistribution sar adcs,” in *2015 Design, Automation Test in Europe Conference Exhibition (DATE)*, 2015, pp. 1265–1268.
  - [23] S. Brenna, A. Bonfanti, and A. L. Lacaita, “A 6-fj/conversion-step 200-ksps asynchronous sar adc with attenuation capacitor in 130-nm cmos,” *Analog Integrated Circuits and Signal Processing*, vol. 81, no. 1, pp. 181–194, 2014.
  - [24] D. Schinkel, E. Mensink, E. Klumperink, E. van Tuijl, and B. Nauta, “A double-tail latch-type voltage sense amplifier with 18ps setup+hold time,” in *2007 IEEE International Solid-State Circuits Conference. Digest of Technical Papers*, 2007, pp. 314–605.
  - [25] B. Razavi, “The strongarm latch [a circuit for all seasons],” *IEEE Solid-State Circuits Magazine*, vol. 7, no. 2, pp. 12–17, 2015.
  - [26] P. M. Figueiredo and J. C. Vital, “Kickback noise reduction techniques for cmos latched comparators,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 53, no. 7, pp. 541–545, 2006.
  - [27] J. M. Rabaey, A. P. Chandrakasan, and B. Nikolić, *Digital integrated circuits: a design perspective*. Pearson Education Upper Saddle River, NJ, 2003, vol. 7.
  - [28] A. Yu, D. Bankman, K. Zheng, and B. Murmann, “Understanding metastability in sar adcs: Part ii: Asynchronous,” *IEEE Solid-State Circuits Magazine*, vol. 11, no. 3, pp. 16–32, 2019.
  - [29] S. M. Chen and R. W. Brodersen, “A 6-bit 600-ms/s 5.3-mw asynchronous adc in 0.13- $\mu$ m cmos,” *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, pp. 2669–2680, 2006.
-

- 
- [30] B. P. Ginsburg and A. P. Chandrakasan, “Dual time-interleaved successive approximation register adcs for an ultra-wideband receiver,” *IEEE Journal of Solid-State Circuits*, vol. 42, no. 2, pp. 247–257, 2007.
  - [31] V. Tripathi and B. Murmann, “Mismatch characterization of small metal fringe capacitors,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 8, pp. 2236–2242, 2014.
  - [32] H. Omran, H. Alahmadi, and K. N. Salama, “Matching properties of femtofarad and sub-femtofarad mom capacitors,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 63, no. 6, pp. 763–772, 2016.
  - [33] P. Nuzzo, F. De Bernardinis, P. Terreni, and G. Van der Plas, “Noise analysis of regenerative comparators for reconfigurable adc architectures,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 6, pp. 1441–1454, 2008.
  - [34] R. Aparicio and A. Hajimiri, “Capacity limits and matching properties of lateral flux integrated capacitors,” in *Proceedings of the IEEE 2001 Custom Integrated Circuits Conference (Cat. No.01CH37169)*, 2001, pp. 365–368.
  - [35] N. Chen, P. Chou, H. Graeb, and M. P. Lin, “High-density mom capacitor array with novel mortise-tenon structure for low-power sar adc,” in *Design, Automation Test in Europe Conference Exhibition (DATE), 2017*, 2017, pp. 1757–1762.
  - [36] Q. Liu, W. Shu, and J. S. Chang, “A 1-gs/s 11-bit sar-assisted pipeline adc with 59-db snr in 65-nm cmos,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 65, no. 9, pp. 1164–1168, 2018.
  - [37] B. Razavi, “The bootstrapped switch [a circuit for all seasons],” *IEEE Solid-State Circuits Magazine*, vol. 7, no. 3, pp. 12–15, 2015.
  - [38] A. T. Ramkaj, M. Strackx, M. S. J. Steyaert, and F. Tavernier, “A 1.25-gs/s 7-b sar adc with 36.4-db snr at 5 ghz using switch-bootstrapping, uspc dac and triple-tail comparator in 28-nm cmos,” *IEEE Journal of Solid-State Circuits*, vol. 53, no. 7, pp. 1889–1901, 2018.
  - [39] A. Ramkaj, F. Tavernier, and M. Steyaert, “Fast switch bootstrapping for gs/s high-resolution analog-to-digital converter,” in *2015 11th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*, 2015, pp. 73–76.
  - [40] S. Brenna, “Ultra low-power analog and mixed-signal socs for smart sensors applications,” Ph.D. dissertation, Dipartimento di elettronica, informazione e bioingegneria, Politecnico di Milano, Jan 13 2016. [Online]. Available: <http://hdl.handle.net/10589/116622>



## SAR control logic model

The following code implements the SAR control logic:

```
1000
1002 'include "constants.vams"
1003 'include "disciplines.vams"
1004
1005 module logic_async12b(comp_rst_o, comp_rstn_o, ctrln_o, ctrlp_o, data_o, eoc_o,
1006   compn_i, compp_i, conv_i, gnd_logic_aio, rstn_i, vdd_logic_aio);
1007
1008 parameter real td = 10p;      //Time delay from input to output [s]
1009 parameter real tt = 10p;      //Output transition time [s]
1010
1011 output comp_rst_o;          //reset comp
1012 electrical comp_rst_o;
1013
1014 output comp_rstn_o;         //resetn comp
1015 electrical comp_rstn_o;
1016
1017 output [11:0] ctrln_o;      //cap ctrl
1018 electrical [11:0] ctrln_o;
1019
1020 output [11:0] ctrlp_o;      //cap ctrl
1021 electrical [11:0] ctrlp_o;
1022
1023 output [11:0] data_o;       //data out
1024 electrical [11:0] data_o;
1025
1026 output eoc_o;              // End-of-conversion
1027 electrical eoc_o;
1028
1029 input compn_i;              //input comparator
1030 electrical compn_i;
1031
1032 input compp_i;              //input comparator
1033 electrical compp_i;
1034
1035 input conv_i;               //start conversion
1036 electrical conv_i;
1037
1038 input rstn_i;              //logic reset
1039 electrical rstn_i;
```

---

```

1042 input vdd_logic_aio; // supply
electrical vdd_logic_aio;

1044 input gnd_logic_aio; // ground
electrical gnd_logic_aio;

1046

1048 integer logic_p, logic_n, valid_d, logic_rst, start, conv_step, done, done_d,
      comp_rst, eoc, converting, valid;
integer result[11:0], result_tmp[11:0], ctrlp[11:0], ctrln[11:0];
genvar i;

1052 analog begin

1054     @ ( initial_step ) begin
1055         for (i=11; i>=0; i=i-1)begin
1056             result_tmp [i] = 0;
1057             result [i] = 0;
1058             ctrlp [i] = 1;
1059             ctrln [i] = 1;
1060             end
1061             conv_step = 11;
1062             done = 0;
1063             comp_rst = 1;
1064     end

1066     start = V(conv_i) > 0.45;
1067     logic_p = V(compp_i) > 0.45;
1068     logic_n = V(compn_i) > 0.45;
1069     logic_rst = V(rstn_i) > 0.45;
1070
1072     valid_d = (logic_p ^ logic_n) && start;

@ (cross(V(rstn_i) -0.45, -1) or cross(valid - 0.5, +1) or cross(valid - 0.5, -1)
or cross(start - 0.5, +1) or cross(start - 0.5, -1) or cross(done_d -0.5, +1) )
1074     begin
1075         if(V(rstn_i) <= 0.45 ) begin // reset state
1076             for (i=11; i>=0; i=i-1)begin
1077                 result_tmp [i] = 0;
1078                 result [i] = 0;
1079                 ctrlp [i] = 1;
1080                 ctrln [i] = 1;
1081             end
1082             conv_step = 11;
1083             done = 0;
1084             comp_rst = 1;
1085
1086     end
1087     else if ((valid >= 0.5) && (conv_step >=0) && (start >= 0.5) && (done_d <= 0.5) )
1088         begin //comparison and decision
1089             if (logic_p > logic_n) begin
1090                 result_tmp[conv_step] = 1;
1091                 ctrlp [conv_step] = 0;
1092                 ctrln [conv_step] = 1;
1093             end
1094             else begin
1095                 result_tmp[conv_step] = 0;
1096                 ctrlp [conv_step] = 1;
1097                 ctrln [conv_step] = 0;
1098             end
1099             done = 1;
1100     end

```

---

---

```

    else if ((valid <= 0.5) && (start >= 0.5) && (done_d >= 0.5)) begin // signals
      that comparator has been reset
1100      conv_step = conv_step - 1;
1102      done = 0;
1103      if (eoc <= 0.5) begin
1104        comp_rst = 0;
1105      end
1106      else begin
1107        comp_rst = 1;
1108      end
1109
1110    end
1111    else if ((done_d >= 0.5) && (start >= 0.5)) begin // reset comparator
1112      comp_rst = 1;
1113    end
1114    else if (start >= 0.5) begin // start
1115      comp_rst = 0;
1116      conv_step = 11;
1117      for (i=11; i>=0; i=i-1)begin
1118        result_tmp [i] = 0;
1119        ctrlp [i] = 1;
1120        ctrln [i] = 1;
1121      end
1122    end
1123
1124    else if (start <= 0.5) begin // ADC is sampling
1125      comp_rst = 1;
1126      conv_step = 11;
1127      done = 0;
1128      for (i=11; i>=0; i=i-1)begin
1129        result [i] = result_tmp [i];
1130        ctrlp [i] = 1;
1131        ctrln [i] = 1;
1132      end
1133    end
1134
1135  end
1136
1137  eoc = (ctrlp[0] ^ ctrln[0]);
1138
1139
1140  done_d = transition(done, 20p, 2p); // temporary delay
1141  valid = transition(valid_d, 20p, 2p); // XOR
1142  delay to generate the valid signal
1143  V(eoc_o) <+ transition(V(vdd_logic_aio)*eoc, td, tt); // EoC
1144  V(comp_rst_o) <+ transition(V(vdd_logic_aio)*comp_rst, 20p, tt); // Activate or reset comparator
1145  V(comp_rstn_o) <+ transition(V(vdd_logic_aio)*(1-comp_rst), 20p, tt); // Inverse of comparator rst
1146
1147  for (i=0 ; i <=10 ; i=i+1) begin // Set DAC controls
1148    V(ctrlp_o[i]) <+ transition(V(vdd_logic_aio)*ctrlp[i], td, tt);
1149    V(ctrln_o[i]) <+ transition(V(vdd_logic_aio)*ctrln[i], td, tt);
1150  end
1151
1152  // monotonic brenna mode
1153  V(ctrlp_o[11]) <+ transition(V(vdd_logic_aio)*(1-ctrln[11]), td, tt);
1154  V(ctrln_o[11]) <+ transition(V(vdd_logic_aio)*(1-ctrlp[11]), td, tt);

```

---

---

```
1156     for (i=0 ; i <=11 ; i=i+1) begin // Generate output code at the end of the
1157         conversion
1158         V(data_o[i]) <+ transition(V(vdd_logic_aio)*result[i], td, tt);
1159     end
1160 end
1162
endmodule
```

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