Study of Comparator and their Architectures

Article · June 2014

CITATIONS
3

READS
10,069

1 author:

Chandrahash Patel
Central University of Gujarat
16 PUBLICATIONS **16** CITATIONS

SEE PROFILE

International Journal of Multidisciplinary Consortium
Volume – 1 | Issue – 1 | June 2014
ijmc.editor@rtmonline.in| http://ijmc.rtmonline.in | ISSN 2349-073X

Study of Comparator and their Architectures

by

Chandrahash Patel | Research Scholar, Department of Electronics and Communication | Engineering | Technocrats Institute of technology, Bhopal(MP) India | patel.chandrahash@gmail.com

And

Dr. Veena C.S | A.P. | Department of Electronics and Communication Engineering | Technocrats Institute of Technology | Bhopal(MP)India | veena_cs72@yahoo.com

ABSTRACT

Comparator is one of the most important analog circuits required in many analog integrated circuits and also in digital design. It is used for the comparison between two different or same electrical signals. Nowadays, the need for ultra low-power, area efficient and high speed analog-to-digital converters is pushing toward the use of dynamic regenerative comparators to maximize speed and power efficiency. In this paper, study of comparators and their architectures is done and analytical expressions are derived. From the analytical expressions, designers can obtain an intuition about the main contributors to the comparator characteristics and fully explore the tradeoffs in comparator design. Based on study few points are derived based on which new comparator can be designed as the design of Comparator becomes an important issue when technology is scaled down.

KEYWORDS: Double Tail comparator, ADCs, Voltage swing.

INTRODUCTION

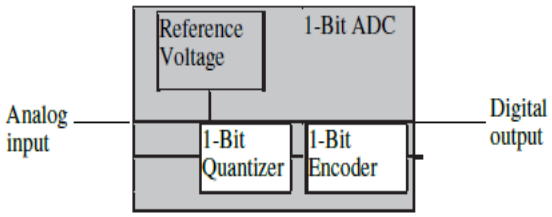
Comparator is a circuit that compares one analog signal with another analog signal or a reference voltage and outputs a binary signal based on the comparison and works on two phases: reset and regeneration phase.

These were developed with the introduction of the first dc-coupled amplifier, at the dawn of the field of electronics. Since then, comparators have remained a very important building block for many types of circuits, including analog-to-digital converters (ADCs), power converters, sensor circuits, and many other types of mixed-signal systems. Over the years, researchers have improved comparator performance in areas such as sensitivity, offset, speed, and power consumption through the use of multistage topologies and other circuit methods[4],[5].Many of the improvements [3] to comparators have focused on improving the comparator as an isolated circuit rather than as part of a larger system. In many applications, e.g., in ADCs and power converters, knowledge of the signals driving the comparator (for

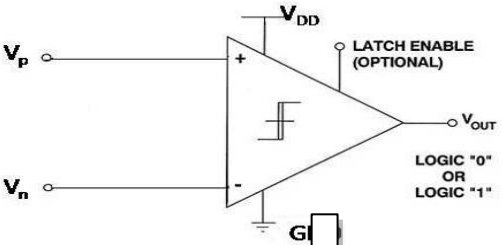
example, pulse-frequency modulation of power converters) may be used to improve the performance of the comparator.

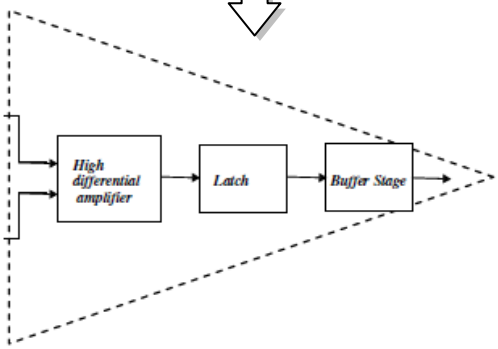
This paper describes basic comparator and their architectures since, designing high-speed comparators is more challenging when the supply voltage is smaller.The schematic symbol and basic operation of a voltage comparator are shown in Figure 1. The comparator can be thought of as a decision-making circuit. If the +, v_+ input of the comparator is at a greater potential than the -, v_- , input, the output of the comparator is a logic 1, whereas if the + input is at a potential less than the - input, the output of the comparator is at a logic 0. Although the basic op- amp can be used as a voltage comparator, in some less demanding low-frequency or speed applications, we will not consider the op-amp as a comparator.

The comparator is basically a 1-bit ADC.



$V_P < V_N$ then $V_O = V_{SS}$ =logic 0
$V_P > V_N$ then $V_O = V_{DD}$ = logic 1





International Journal of Multidisciplinary Consortium
Volume – 1 | Issue – 1 | June 2014
ijmc.editor@rtmonline.in| http://ijmc.rtmonline.in | ISSN 2349-073X

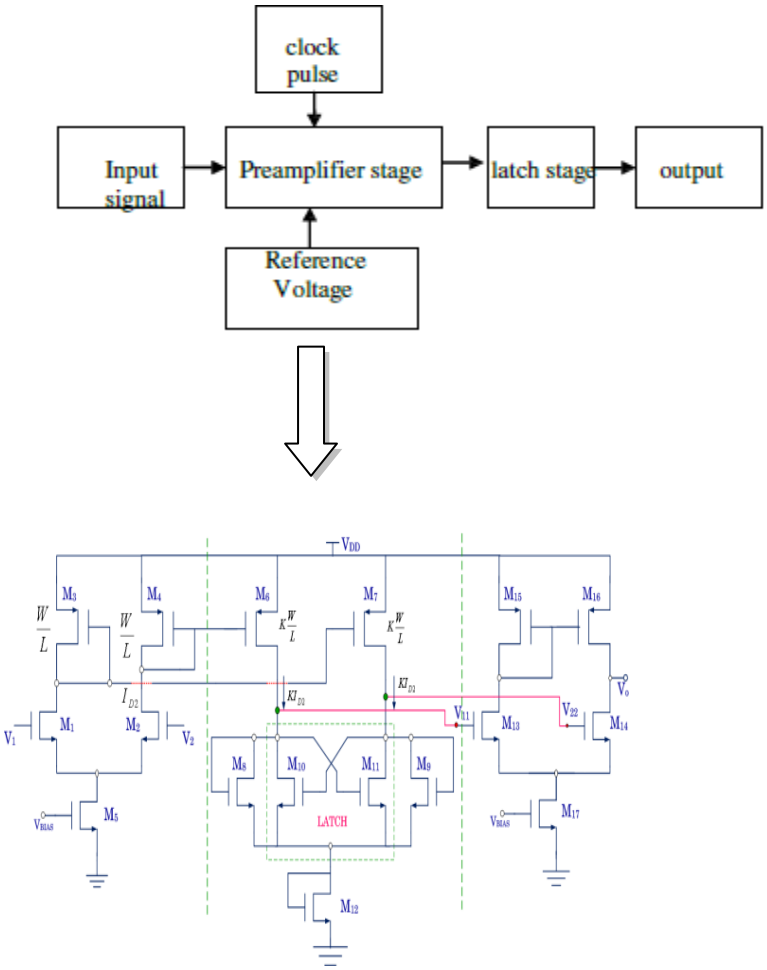


Figure1: Basic comparator diagram and its basic blocks

Voltage transfer characteristics of basic comparator in ideal mode

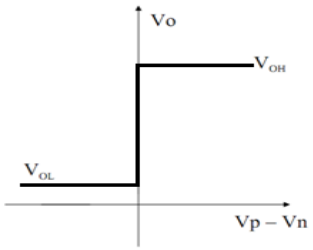


Figure 2: Voltage Transfer Characteristic

Important characteristics of comparator which is to be cheeked while designing comprises of two parts:

1. Static characteristics
   - Gain

$$\text{Gain} = A_v = \lim_{\Delta V \to 0} \frac{V_{OH}-V_{OL}}{\Delta V} \quad \text{where } \Delta V \text{ is the input voltage change}$$

   - Output high and low states

     V_{OH} V_{OL} V_{IL} V_{IH}

$$\text{The voltage gain is } A_v = \frac{V_{OH} - V_{OL}}{V_{IH} - V_{IL}}$$

   - Input resolution

It is the input voltage change which is necessary to make output swing to valid binary states

- Offset
  Offset in the comparators generates due to input transistor mismatches.

- Noise

- ICMR

2. Dynamic characteristics

- Propagation delay(t_p)
  propagation delay is the delay between output and input

- Slew Rate(SR)

Relation between t_p and SR

$$t_p=\Delta T=\Delta V/SR=(V_{OH}-V_{OL})/2.SR$$

COMPARATOR ARCHITECTURES

High gain amplifiers are often used as comparators since the outputs of most amplifiers naturally clip at high and low levels when overdriven. Some comparators are clocked and only provide an output after the transition of the clock. The value of the input to a clocked comparator is only of concern in a short time interval around the clock transition. The speed of clocked comparators can be very high and the power dissipation of clocked comparators can be very low. Clocked comparators are often called Dynamic Comparators and are widely used in the design of high-speed ADCs. Regenerative feedback is often used in dynamic comparators and occasionally in non-clocked comparators.

Basically there are various architectures available in modern days which are then summarized into three categories:

A. Open Loop Comparator
B. Regenerative
C. High Speed Comparator

- Open Loop Comparators

These comparators are basically operational amplifier without compensation shown in figure 3 to obtain the largest bandwidth, hence improving its time response. Since the precise gain and linearity are of no interest in comparator design no compensation does not pose a problem. However, due to its limited gain-bandwidth product, open loop comparators are too slow for much application

International Journal of Multidisciplinary Consortium
Volume – 1 | Issue – 1 | June 2014
ijmc.editor@rtmonline.in| http://ijmc.rtmonline.in | ISSN 2349-073X

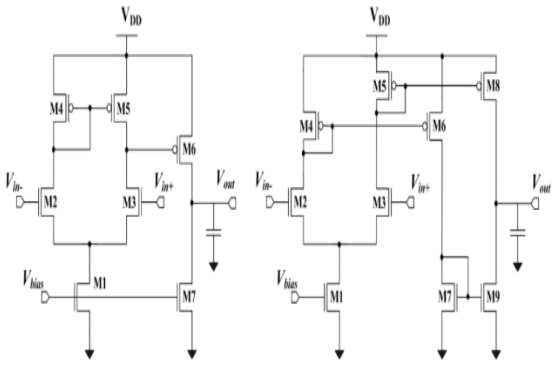


Figure 3: (a) Two-stage open-loop comparator (b) Push-pull output open-loop comparator

- Regenerative Comparator

These comparators use positive feedback like latch to compare signals shown in figure 4, 5, 6.

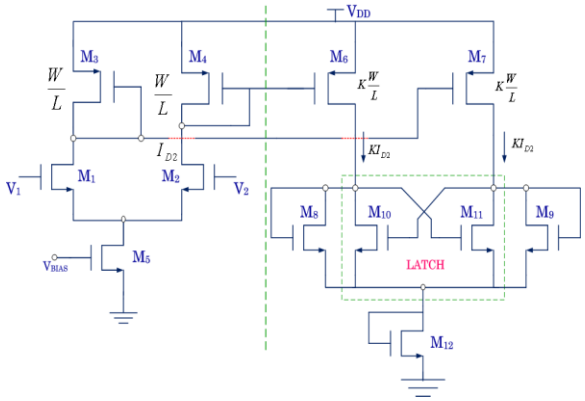


Figure 4: Fully differential amplifier and Latch

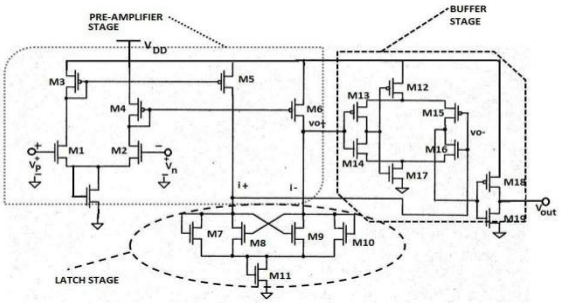


Figure 5: Preamplifier based comparator

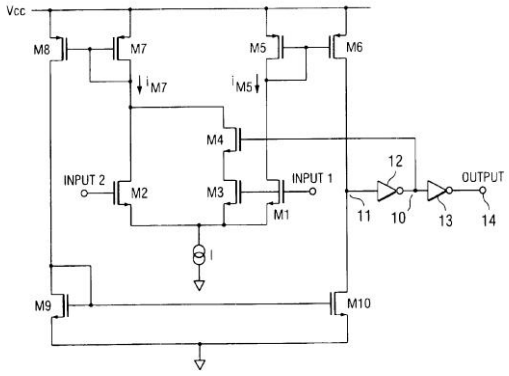


Figure 6 : Comparator with hysteresis

A. High Speed Comparator

These comparators are combination of above two types of comparator which leads to faster response

.

DYNAMIC COMPARATOR

Among different types of comparators, clocked regenerative comparators (called dynamic comparators) have found wide applications in many high-speed ADCs since they can make fast decisions due to the strong positive feedback in the regenerative latch. Recently, many comprehensive analyses have been presented which investigate the performance of these comparators from different aspects such as noise [6], offset [8], [9], random decision errors [12], delay [1] and kick-back noise [11].Even the power of the dynamic comparators can also be investigated by the well-known formula, (1), for dynamic power consumption considering leakage current is used to estimate the power.

$$Power = fClkCLVDD + VDD.Ileakage \quad (1)$$

This formula would provide the designers with acceptable estimation, but it does not reveal the design parameters which contribute to the power consumption. While a comparator is by definition a nonlinear circuit element that makes a hard decision on the input signal polarity, almost every clocked comparator does so by sampling the input signal and then regeneratively amplifying it, each of which operation can be treated as that of a linear system. Thus, comparator can be treated as a linear periodically time-variant (LPTV) system.

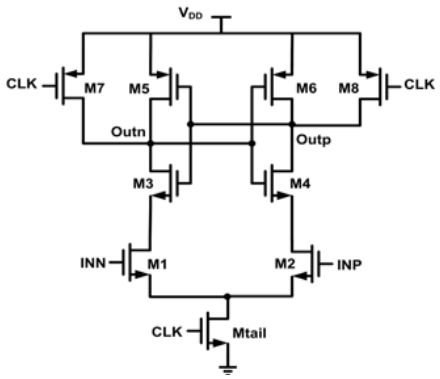


Figure 7: Conventional Dynamic Comparator

International Journal of Multidisciplinary Consortium
Volume – 1 | Issue – 1 | June 2014
ijmc.editor@rtmonline.in| http://ijmc.rtmonline.in | ISSN 2349-073X

A. Conventional Dynamic Comparator

The schematic diagram of the conventional dynamic comparator [1],[2],[13]shown if fig 7 which is widely used in A/D converters, with high input impedance, rail-to-rail output swing, and no static power consumption is shown in fig. The operation of the comparator is as follows.

During the reset phase when CLK = 0 and *M*tail is off, reset transistors (*M*7–*M*8) pull both output nodes Out*n* and Out*p* to *V*DD to define a start condition and to have a valid logical level during reset.

In the comparison phase, when CLK = *V*DD, transistors *M*7 and *M*8 are off, and *M*tail is on. Output voltages (Out*p*, Out*n*), which had been pre-charged to *V*DD, start to discharge with different discharging rates depending on the corresponding input voltage (INN/INP). Assuming the case where $V_{INP} > V_{INN}$, Out*p* discharges faster than Out*n*, the corresponding pMOS transistor (*M*5) will turn on initiating the latch regeneration caused by back-to-back inverters (*M*3, *M*5 and *M*4, *M*6). Thus, Out*n* pulls to *V*DD and Out*p* discharges to ground. If *V*INP < *V*INN, the circuits works vice versa.

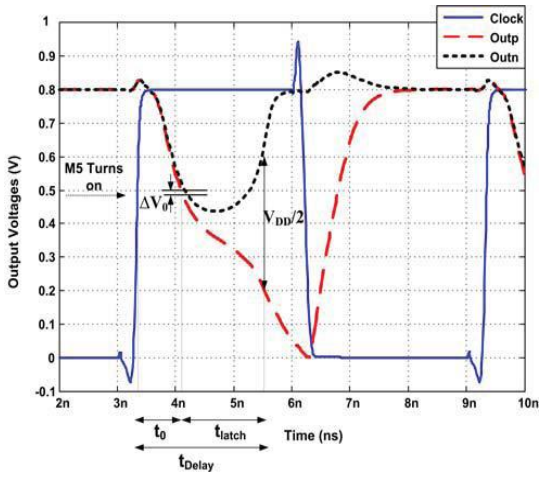


Fig 8. Transient response of the conventional dynamic comparator

As shown in Fig. 8 the delay of this comparator is comprised of two time delays, t_0 and t_{latch}. The delay t_0 represents the capacitive discharge of the load capacitance *C*L until the first p-channel transistor (*M*5/*M*6) turns on. Here the discharge delay(*t*0) is given by

$$t_0 = \frac{C_L |V_{thp}|}{I_2} \cong 2\frac{C_L |V_{thp}|}{I_{tail}}. \qquad (2)$$

In equation (2), since *I*2 = *I*tail/2 + _*I*in = *I*tail/2 + *g*m1,2Δ*V*in, for small differential input (Δ*V*in), *I*2 can be approximated to be constant and equal to the half of the tail current.

The second term, t_{latch}, is the latching delay of two cross coupled inverters. Here it is assumed that a voltage swing of Δ*V*out = *V*DD/2 has to be obtained from an initial output voltage difference Δ*V*0 at the falling output (e.g., Out*p*). Half of the supply voltage is considered to be the threshold voltage of the comparator following inverter or SR latch. Hence, the latch delay time is given by,

$$t_{latch} = \frac{C_L}{g_{m,eff}} \cdot \ln\left(\frac{\Delta V_{out}}{\Delta V_0}\right) = \frac{C_L}{g_{m,eff}} \cdot \ln\left(\frac{V_{DD}/2}{\Delta V_0}\right) \qquad (3)$$

where *gm*,eff is the effective transconductance of the back-to back inverters. In fact, this delay depends, in a logarithmic manner, on the initial output voltage difference at the beginning of the regeneration (i.e., at $t = t0$). Based on (2), ΔV0 can be calculated from (4)

$$\begin{aligned}\Delta V_0 &= \left|V_{outp}(t=t_0) - V_{outn}(t=t_0)\right| \\ &= \left|V_{thp}\right| - \frac{I_2 t_0}{C_L} = \left|V_{thp}\right|\left(1 - \frac{I_2}{I_1}\right).\end{aligned} \tag{4}$$

The current difference, Δ*I*in = |*I*1 − *I*2|, between the branches is much smaller than *I*1 and *I*2. Thus, *I*1 can be approximated by *I*tail/2 and (4) can be rewritten as

$$\begin{aligned}\Delta V_0 &= \left|V_{thp}\right| \frac{\Delta I_{in}}{I_1} \\ &\approx 2\left|V_{thp}\right| \frac{\Delta I_{in}}{I_{tail}} \\ &= 2\left|V_{thp}\right| \frac{\sqrt{\beta_{1,2} I_{tail}}}{I_{tail}} \Delta V_{in} \\ &= 2\left|V_{thp}\right| \sqrt{\frac{\beta_{1,2}}{I_{tail}}} \Delta V_{in}.\end{aligned} \tag{5}$$

In equation (5), $\beta 1,2$ is the input transistors' current factor and *I*tail is a function of input common-mode voltage (*V*cm) and *V*DD. Now, substituting Δ*V*0 in latch delay expression and considering *t*0, the expression for the delay of the conventional dynamic comparator is obtained as

$$\begin{aligned}t_{delay} &= t_0 + t_{latch} \\ &= 2\frac{C_L\left|V_{thp}\right|}{I_{tail}} + \frac{C_L}{g_{m,eff}} \cdot \ln\left(\frac{V_{DD}}{4\left|V_{thp}\right|\Delta V_{in}}\sqrt{\frac{I_{tail}}{\beta_{1,2}}}\right).\end{aligned} \tag{6}$$

Equation (6) explains the impact of various parameters.

The total delay is inversely proportional to the input difference voltage (Δ*V*in) and directly proportional to the comparator load capacitance C_L. Besides this the delay also depends indirectly to the input common-mode voltage (*V*cm).

In principle, this structure has the advantages of high input impedance, rail-to-rail output swing, no static power consumption, and good robustness against noise and mismatch.

But the disadvantage on the other hand, is that due to several stacked transistors, the delay time of the latch becomes large due to lower transconductances.

Another important drawback of this structure is that there is only one current path, via tail transistor M_{tail}, which is not favourable for regeneration.

International Journal of Multidisciplinary Consortium
Volume – 1 | Issue – 1 | June 2014
ijmc.editor@rtmonline.in| http://ijmc.rtmonline.in | ISSN 2349-073X

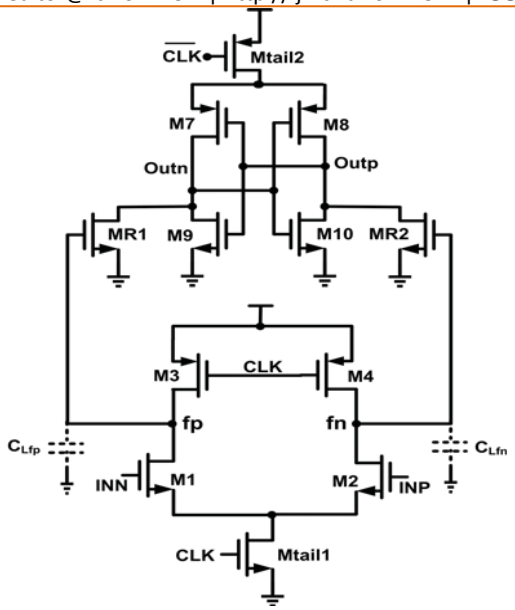


Figure 9: Schematic diagram of the conventional double-tail dynamic comparator.

B. Conventional Double-Tail Dynamic Comparator

As there are some disadvantages in conventional dynamic comparator so here we are going to study a conventional double-tail comparator is shown in Fig.9. [1], [10]. This topology has less stacking and therefore can operate at lower supply voltages. Here the double tail enables both a large current in the latching stage and wider *M*tail2, for fast latching independent of the input common-mode voltage (*V*cm), and a small current in the input stage (small *M*tail1), for low offset.

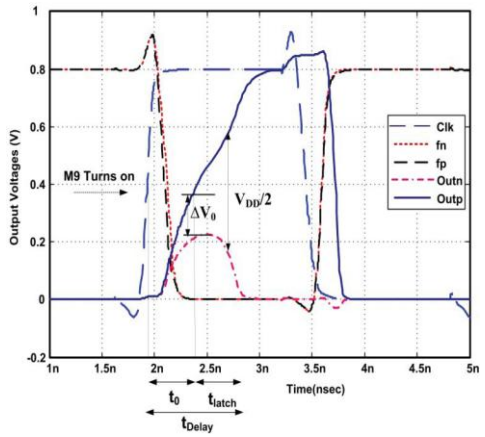


Figure 10: Transient simulations of the conventional double-tail dynamic comparator

Operation of this comparator as follows

During reset phase (CLK = 0, *M*tail1, and *M*tail2 are off), transistors *M*3-*M*4 pre-charge fn and fp nodes to *V*DD, which in turn causes transistors *M*R1 and *M*R2 to discharge the output nodes to ground.

During decision-making phase (CLK = VDD, *M*tail1 and *M*tail2 turn on), *M*3-*M*4 turn off and voltages at nodes fn and fp start to drop with the rate defined by IMtail1/Cfn(p) and on top of this, an input-dependent Differential voltage ΔVfn(p) will build up. The

intermediate stage formed by *M*R1 and *M*R2 passes *V*fn(p) to the cross coupled inverters and also provides a good shielding between input and output, resulting in reduced value of kickback noise.

Similar to the conventional dynamic comparator, the delay of this comparator comprises two main parts, t_0 and $t_{latch.}$ shown in fig 10.
Here

$$t_0 = \frac{V_{Thn} C_{Lout}}{I_{B1}} \approx 2\frac{V_{Thn} C_{Lout}}{I_{tail2}} \quad (7)$$

$$\Delta V_0 = \left|V_{outp}(t = t_0) - V_{outn}(t = t_0)\right| = V_{Thn} - \frac{I_{B2} t_0}{C_{Lout}}$$
$$= V_{Thn}\left(1 - \frac{I_{B2}}{I_{B1}}\right) \quad (8)$$

where IB1 and IB2 are the currents of the latch left- and right side branches of the second stage, respectively.
Considering $\Delta I_{latch} = |IB1 - IB2| = gmR1, \Delta Vfn/fp$, (8) can be rewritten as

$$\Delta V_0 = V_{Thn}\frac{\Delta I_{latch}}{I_{B1}} \approx 2V_{Thn}\frac{\Delta I_{latch}}{I_{tail2}} = 2V_{Thn}\frac{g_{mR1,2}}{I_{tail2}}\Delta V_{fn/fp} \quad (9)$$

where *g*mR1,2 is the transconductance of the intermediate stage transistors (*M*R1 and *M*R2) and Δ*V*fn/fp is the voltage difference at the first stage outputs (fn and fp) at time *t*0. In fact, here intermediate stage transistors amplify the voltage difference of Δ*V*fn/fp causing the latch to be imbalanced. So

$$\Delta V_{fn/fp} = \left|V_{fn}(t = t_0) - V_{fp}(t = t_0)\right|$$
$$= t_0 \cdot \frac{I_{N1} - I_{N2}}{C_{L,fn(p)}}$$
$$= t_0 \cdot \frac{g_{m1,2}\Delta V_{in}}{C_{L,fn(p)}}. \quad (10)$$

Where I_{N1}-I_{N2} refer to discharging currents of input transistors (M1 and M2) which are dependent on the input differential voltage ΔI_N So from (10) & (9) we have ΔV_0 as

$$\Delta V_0 = 2V_{Thn}\frac{g_{mR1,2}}{I_{tail2}}\Delta V_{fn/fp}$$
$$= \left(\frac{2V_{Thn}}{I_{tail2}}\right)^2 \cdot \frac{C_{Lout}}{C_{L,fn(p)}} \cdot g_{mR1,2} g_{m1,2}\Delta V_{in}. \quad (11)$$

This equation((11) shows that Δ*V*0 depends strongly on the transconductance of input and intermediate stage transistors, input voltage difference (Δ*V*in), latch tail current, and the capacitive ratio of *CL*out to *CL*,fn(p).Here the total delay of this comparator is achieved as follows:

$$t_{delay} = t_0 + t_{latch} = 2\frac{V_{Thn}C_{Lout}}{I_{tail2}} + \frac{C_{Lout}}{g_{m,eff}} \cdot \ln\left(\frac{V_{DD}/2}{\Delta V_0}\right)$$
$$= 2\frac{V_{Thn}C_{Lout}}{I_{tail2}} + \frac{C_{Lout}}{g_{m,eff}} \cdot \ln\left(\frac{V_{DD} \cdot I_{tail2}^2 \cdot C_{L,fn(p)}}{8V_{Thn}^2 \cdot C_{Lout}g_{mR1,2}g_{m1,2}\Delta V_{in}}\right). \quad (12)$$

So comparing both architecture we found that delay get reduced and even power is consumed low which is to seen while designing.

CONCLUSION

Hence in this paper only explanation about the Comparator their characteristics, architecture and various parameters such as delay, offset voltage, output impedance and voltage gain is done which are further needed to be considered in any design. But, the selection of any topology is based on the application and the requirements.

REFERENCES

[1] Samaneh Babayan-Mashhadi and Reza Lofti, "Analysis and Design of a Low- Voltage Low-Power Double-Tail Comparator", in IEEE Transaction on VLSI System Jan. 2013/14.

[2] B. Goll and H. Zimmermann, "A comparator with reduced delay time in 65-nm CMOS for supply voltages down to 0.65," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 56, no. 11, pp. 810–814, Nov. 2009.

[3] A. Mesgarani, M. N. Alam, F. Z. Nelson, and S. U. Ay, "Supply boosting technique for designing very low- voltage mixed-signal circuits in standard CMOS," in Proc. IEEE Int. Midwest Symp. Circuits Syst Dig. Tech. Papers, Aug. 2010, pp. 893–896.

[4] B. Goll and H. Zimmermann, "A 0.12 μm CMOS comparator requiring 0.5V at 600MHz and 1.5V at 6 GHz," in Proc. IEEE Int. Solid-State Circuits Conf., Dig. Tech. Papers, Feb. 2007, pp. 316–317.

[5] B. Goll and H. Zimmermann, "Low-power 600MHz comparator for 0.5 V supply voltage in 0.12 μm CMOS," IEEE Electron. Lett., vol. 43, no. 7, pp. 388–390, Mar. 2007.

[6] P. Nuzzo, F. D. Bernardinis, P. Terreni, and G. Van der Plas, "Noise analysis of regenerative comparators for reconfigurable ADC architectures," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 55, no. 6, pp. 1441–1454, Jul. 2008.

[7] A. Nikoozadeh and B. Murmann, "An analysis of latched comparator offset due to load capacitor mismatch," IEEE Trans. Circuits Syst.II, Exp. Briefs, vol. 53, no. 12, pp. 1398–1402, Dec. 2006.

[8] S. Babayan-Mashhadi and R. Lotfi, "An offset cancellation technique for comparators using body-voltage trimming," Int. J. Analog Integr.Circuits Signal Process., vol. 73, no. 3, pp. 673–682, Dec. 2012.

[9] J. He, S. Zhan, D. Chen, and R. J. Geiger, "Analyses of static and dynamic random offset voltages in dynamic comparators," IEEE Trans .Circuits Syst. I, Reg. Papers, vol. 56, no. 5, pp. 911–919, May 2009.

[10]D. Shinkel, E. Mensink, E. Klumperink, E. van Tuijl, and B. Nauta, "A double-tail latch-type voltage sense amplifier with 18ps Setup+Hold time," in Proc. IEEE Int. Solid-State Circuits Conf., Dig. Tech. Papers, Feb. 2007, pp. 314–315.

[11]P. M. Figueiredo and J. C. Vital, "Kickback noise reduction technique for CMOS latched comapartors," IEEE Trans. Circuits Syst. II, Exp.Briefs, vol. 53, no. 7, pp. 541–545, Jul. 2006.

[12] J. Kim, B. S. Leibowits, J. Ren, and C. J. Madden, "Simulation and analysis of random decision errors in clocked comparators," IEEE Trans.Circuits Syst. I, Reg. Papers, vol. 56, no. 8, pp. 1844–1857, Aug. 2009.

[13] B. Wicht, T. Nirschl, and D. Schmitt-Landsiedel, "Yield and speed optimization of a latch-type voltage sense amplifier," IEEE J. Solid-State Circuits, vol. 39, no. 7, pp. 1148–1158, Jul. 2004.

[14] D. Johns and K. Martin, Analog Integrated Circuit Design, New York USA: Wiley, 1997.