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Reduction of Kickback Noise in Latched Comparators for Cardiac IMDs

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Abstract

Background/Objectives: The latched regenerative comparator is an essential block in all ADC architectures. It majorly suffers from the non-idealities such as kickback noise, thermal noise and offset voltage. Especially in an ADC implemented in Cardiac IMDs, the generated kickback noise in latched comparator can make a difference to the accuracy, resolution and settling time to an extent. The main objective of this work is to implement a technique for kickback noise reduction in latched comparators. **Methods/Statistical Analysis:** This work reviews the various architectures of latched comparators implemented in Cardiac IMDs and also make assessment of the available solutions to reduce the generated kickback noise in a latched comparator. The available kickback noise reduction techniques are implemented in SR latched dynamic comparators and resultant findings are compared. **Findings:** This brief proposes a new solution to cancel out the unwanted charge injections in the comparator and thus reduces the kickback noise effectively. The proposed solution is implemented in the latched comparator with SR latch and also compared with the already available solutions with regard to kickback noise and power dissipation. **Application/Improvements:** The proposed Kickback noise reduction technique reduces the noise to 40% more when compared with the other techniques and this technique is applicable to the dynamic Comparators used in Cardiac IMDs.

Keywords: Carddiac IMDs, Cmos Technology, Kickback Noise, Latched Comparator, Offset Voltage, Random Noise

1. Introduction

All the physically available biomedical signals are analog in nature; as a result an ADC is involved to process them into digital signals before they are processed in sophisticated digital signal processors. For the cardiac Implantable Medical devices, it is required to implement SAR ADC because they provide high accuracy and good conversion rate[1].

The dynamic latched comparator has an important role in SAR analog-to-digital converters. The commonly used architecture of a dynamic latched comparator is demonstrated in Figure 1. The operation of the dynamic latched regenerative comparator is performed synchronously with respect to the applied clock signal and it is indicated through its respective digital output, irrespective of the differential input signals applied. Due to the existence of the positive feedback mechanism in the latched dynamic comparator, the analog input signals are regenerated to digital output level. The non-idealities of dynamic comparators are thermal noise, offset voltage and kickback noise. The presence of non-idealities can restrict the resolution, accuracy, conversion speed and ENOB of ADCs. The offset voltage in a dynamic comparator occurs due to the mismatches and process variations[2–4]. Thermal noise in a dynamic comparator can be reduced by upsizing the input MOS transistor pair, which in turn generates the kickback noise. The generated kickback noise is proportional to the parasitic capacitance of the input transistors and can operate in all the regions (triode, cut-off and saturation) during the comparison process, seriously affecting the accuracy of the decision taken by the comparator[5,6].

In latched regenerative comparators, on wide voltage variations the cross coupled inverters forms a regenerative

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latch coupled to the input MOS transistors through the unwanted parasitic capacitance present at the input transistor pair. As the circuit before it do not have any output impedance, the relevant input voltage level of the latched regenerative comparator is distributed; this degrades the resolution, accuracy and efficiency of the ADC. This voltage disturbance caused at the inputs of the comparator is called as kickback noise[7].

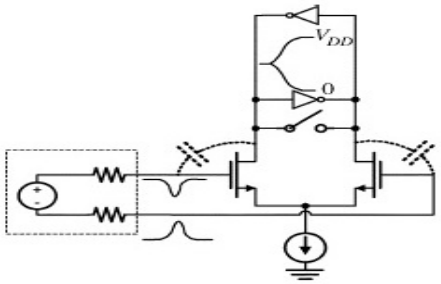

Figure 1. Latched comparator showing the generation of kickback noise.

This work is divided into five sections, Section 1 is the introduction. In Section 2 comparison of various existing architectures of dynamic comparators present in Cardiac IMDs with regard to generated kickback noise and Power dissipation is carried out. In section III a recall of the available solutions for kickback noise reduction and a new solution for reducing kickback noise is proposed. In Section 4 comparative results of existing kickback noise techniques with the proposed technique are discussed. Section 5 draws the conclusion.

2. Latched Comparators used in Cardiac Implantable Medical Devices

There is a wide variety of CMOS regenerative latched comparator architectures used in cardiac IMDs, and it is impossible to demonstrate a detailed survey of the architectures. In this paper, all the fundamental architectures are compared with regard to kickback noise generation and power dissipation.

2.1 Balanced Type Latched Regenerative Comparator

The circuit of balanced type latched Regenerative comparartor is depicted in Figure 2. Based on the clock input applied, the comparator works in Comparison mode and reset mode. In reset mode of operation clock input is given as 0V, the corresponding Mtail transistor in the comparator architecture turns OFF resulting the voltage output nodes to VDD. In comparision mode the Mtail transistor is ON as the clock input is equal to VDD. Therefore both the output nodes starts to discharge through the Mtail transistor. Depending on the input voltages, regeneration of latch is acheived by one of the cross coupled inverters leading the ouputs to be 0 and VDD volts. In this circuit the capacitors are arranged in parallel form in order to reduce thermal noise. But reducing thermal noise contridictorily generates kickback noise.In this latched comparator architecture almost all the transistors function in the weak inversion region[8].

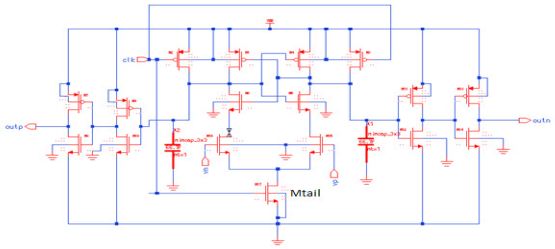

Figure 2. Schematic diagram of balance type latched regenerative comparator.

2.2 Dynamic Regenerative Comparator with SR Latch

The regenerative comparator is shown in Figure 3. Depending on the clock input latched comparator operates in two modes i.e., reset mode and regeneration mode. In the reset phase the voltage at the outputs nodes is pulled to 0V. In the regeneration phase, final output of the comparator is acheived by one of the cross copled invertes where one of the outputs is pulled to a voltage of 0v and the other output node to a voltage of VDD volts. The SR latch present in the circuit stores the resultant value of comparison during the regenerative mode for the entire clock cycle. In this architecture, the output loading is kept unique with the use of inverters. For the reduction of kickback noise the common mode voltage is kept in mid rail voltages[9].

2.3 Single Clocked Dual Rail Clocked Regenerative Comparator

The architecture of the Single Clocked dual rail dynamic comparator is demonstrated in Figure 4. The circuit

operates in two phases i.e., in precharge phase clock is set to '0V' and in evaluation phase clock is kept at VDD. During the precharge phase, the nodes DP and DN are precharged to VDD, while the nodes VN and VP are discharged to zero volts. When the clock input raises, the Mtail transistor will be switched on resulting an input dependent differential voltage at the nodes DN and DP. In the evaluation phase, final output of the comparator is acheived by one of the cross copled invertes where one of the outputs is pulled to voltage of 0v and the other output node is pulled to VDD volts.Eventhough dual rail dynamic comparator consumes more power when compared with single rail dynamic comparator, dual rail latched compared is choosen because it generates less kickback noise[10].

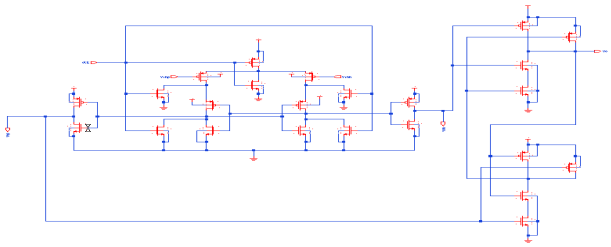

Figure 3. Schematic diagram of SR latched dynamic comparator.

Table 1. Comparison of existing latched comparators in cardiac IMDs

Comparator architecture	Power dissipation (nW)	Kickback noise(mV)
Balanced latched Comparator	2.6319	1767.6964
Single Clock phase dual rail latched Comparator	1.1370	1145.2952
Dynamic regenerative latched comparator with SR latch	6.0143	

From the Table 1 it can be concluded that dynamic regenerative latched comparator generates less kickback noise when compared with the conventional latched comparators used in cardiac IMDs but on the other side it dissipates more power. In this brief the major focus is on reducing the kickback noise, therefore in the next section new technique for reducing kickback noise is proposed and implemented in dynamic regenerative latched comparator with SR latch.

3. Reduction Techniques for Kickback Noise

This section kicksoff with the revision of existing solutions and a new technique is being proposed for reducing kickback noise.

3.1 Existing Techniques for Reduction of generated kickback Noise

The most popular technique for reducing the kickback noise in a latched regenerative comparator is to add a pre-amplifier circuit preceding the latch stage in a comparator. Although this is an effective technique, reduces the power efficiency of the latched comparator by introducing static consumption of power[11].

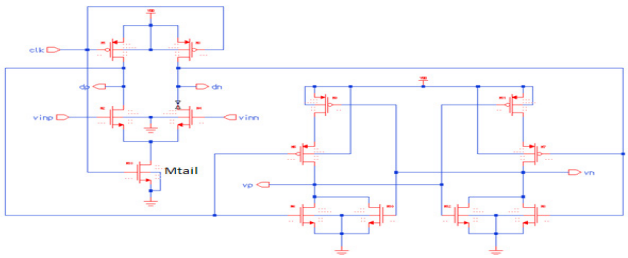

Figure 4. Circuit diagram exhibiting single clocked dual rail dynamic latched comparator.

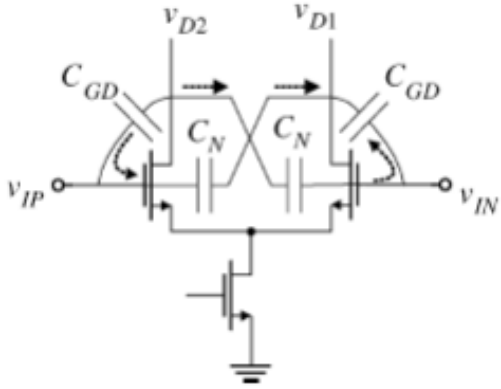

Figure 5. Neutralization technique.

MOS sampling switches can be fitted at the inputs of the latched comparators such that these switches open up during regeneration or comparison phase. This existing technique provides a sampling function that detaches the input nodes during the regenerative phase, thereby reduces the kickback noise. However, the input voltage

disturbances prevail because the applied voltage at the input differs from the previous voltage samples applied[12].

A neutralization technique shown in Figure 5 is also used for kickback noise reduction, but only provides moderate improvements[13].

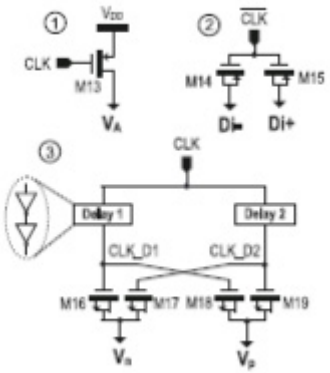

Figure 6. Clocked PMOS-NMOS technique.

Clocked PMOS-NMOS capacitor technique shown in Figure 6 is used to compensate the kickback noise by eliminating undesired charges present at the input MOS transistor pair at regular time intervals[14].

From the simulation results it can be exhibited that existing solutions for kickback noise reduction either increases the power dissipated considerably during the comparison stage or cannot able to effectively reduce the generated kickback noise.

3.2 Proposed Solution for Kickback Noise Reduction

The main aim of this technique is to reduce the kickback noise in latched comparators used in cardiac IMDs.

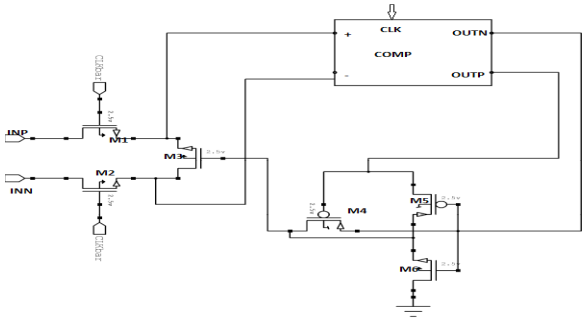

Figure 7. Proposed circuit for reducing kickback noise.

The proposed circuit for reducing the kickback noise is shown in the Figure 7. The transistors M1 and M2 are used to prevent the input nodes named INP and INN from the distortion caused by the latched comparator. In the reset phase clk input is equal to zero, the transistors M1 and M2 are in ON state and the outputs outn and outp reaches to equal logic values, resulting the transistor M3 to be in OFF state and therefore the inputs of the latched regenerative comparator are charged to voltages applied at INP and INN respectively. In the comparison phase or regeneration phase clk becomes high and therefore the transistors M1 and M2 are in OFF state, also M3 is initially in OFF state and the latch regenerates and produces a decision at the nodes OUTP and OUTN. As the transistors M1 and M2 are in OFF state, the kickback noise generated due to the fast regeneration of latch, the input nodes INP and INN are ruled out from kickback noise. The outputs of comparator are forced to complementary values OUTN and OUTP, then the transistors M4-M5-M6 forces the transistor M3 to ON state and therefore unwanted charge injections are shorted and eliminated.

4. Simulation Results and Discussions

This section starts with the implementation of proposed kickback noise reduction solution in dynamic regenerative latched comparator with SR latch followed by the comparison of different kickback noise reduction techniques implemented in dynamic regenerative latched comparator with SR latch. The circuit for reducing the kickback is implemented in latched dynamic comparator and it is exhibited in Figure 8.

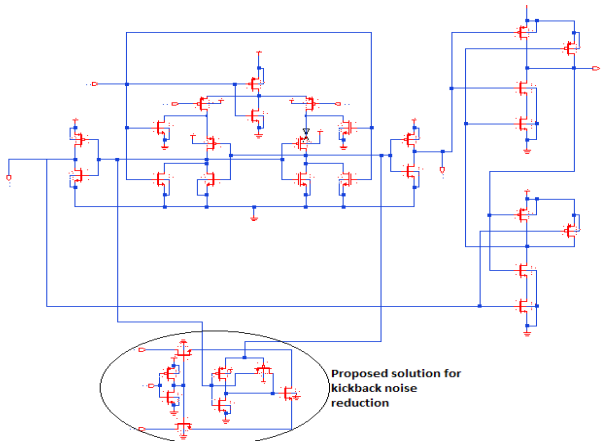

Figure 8. Schematic of the proposed solution implemented in dynamic latched regenerative comparator with SR latch.

The proposed kickback noise efficient latched regenerative comparator works in reset phase and regeneration phase. Initially in the reset phase of the comparator, the inputs are pre-charged to the same values applied at the inputs of the proposed technique. In the regeneration phase, latch is regenerated to deliver the decision at the outputs. The proposed solution cancels out the charge injections from the latched comparator.

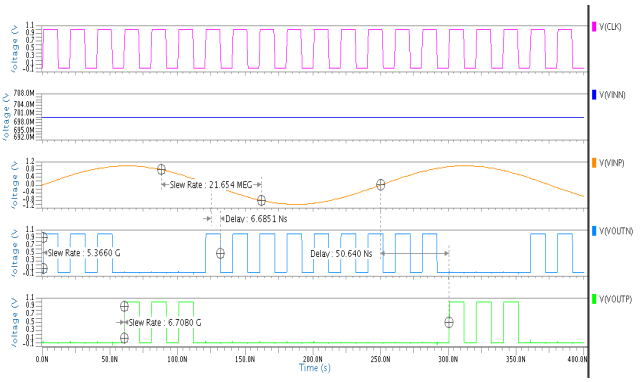

Figure 9. Transient response of proposed solution implemented in latched comparator.

The transient response of proposed kickback noise reduction solution is shown in the figure 9 with the input specification of Vinp = 1V amplitude sinusoidal wave with frequency of 4 MHz, Vinn = 0.5V constant reference voltage. Clk = 1V with pulse waveform with time period of 20 nsec. With help of EZ Wave analyzer, comparator outputs are analysed and the parameters like Slew rate and delay are measured from that waveforms. A Monte-carlo simulation analysis with 250 runs is carried out to examine the influence of mismatches in transistors. The transistor mismatches have insignificant effect on the reduction of kickback noise achieved by the proposed solution.

Table 2. Comparison of existing Kickback noise reduction Techniques with Proposed Solution

Kickback Noise Reduction Techniques in SR latched Dynamic Comparator	Power Dissipation (nW)	Kickback Noise (uV)
Neutralization Technique	7.24	820.23
Sampling Switches	6.22	608.00
Clocked PMOS-NMOS Capacitor Technique	6.7809	523.49
Proposed Technique	6.42	312.32

From the above comparison Table 2 it can be unveiled that existing kickback noise reduction solutions either increases the dissipated power dissipation considerably or do not able to reduce the generated kickback noise effectively. When proposed solution is used the power dissipation raises from 6.0143 nW to 6.42nW. The extra power dissipated during the operation of the latched regenerative comparator is the dynamic power which is mostly desirable in all frequency varying systems.

5. Conclusion

This work reviewed the architectures of latched comparators implemented in cardiac IMDs, and it was inferred that the latched comparators that dissipate less power generate more kickback noise and vice-versa. The existing noise reduction solutions are not able to reduce the generated kickback noise effectively in spite they increase the power dissipation considerably. The new proposed solution achieves considerable results and it is clearly shown with simulations carried out using Mentor Graphics EDA tools in 0.13 um technology.

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