Flying-Capacitor Bottom-Plate Sampling Scheme for Low-Power High-Resolution SAR ADCs

Dmitry Osipov and Steffen Paul
The Institute of Electrodynamics and Microelectronics (ITEM)
University of Bremen
Bremen, Germany
osipov@item.uni-bremen.de

***Abstract*—A new sampling scheme for successive approximation register (SAR) analog-to-digital converters (ADCs) is proposed in this paper. The switching scheme eliminates two major problems of traditional SAR ADC architectures: first, the high energy demand of the input driver, because of high input capacitance; and second, the trade-off between linearity and, consequently, bottom-plate sampling, and area savings and, consequently, upper-plate sampling. The proposed sampling scheme allows reduction of the sampling capacitance to a single unit capacitor and the use of high linear bottom-plate sampling without sacrificing the double area on digital-to-analog converter (DAC). This method works with most previously published switching schemes.**

***Index Terms*—SAR ADC, switching scheme, sampling, bottom-plate sampling**

I. Introduction

Recently, many different switching schemes have been published for successive approximation register (SAR) analog-to-digital converters (ADCs) [1]–[6]. The main topic addressed in these publications concerned the decrease of switching energy of capacitive digital-to-analog converters (DACs). The decrease of switching energy and, consequently, the supply or reference power is the natural choice of overall ADCs power optimization as the Waldens FoM [7] does not contain any other power. However, if we consider the ADC as a block of more complex system-on-chip the input signal source energy should also be considered as part of the ADCs power consumption. Particulary, in bio signal acquisition the direct input of the system is amplified and filtered first. So, the amplifier realized on the same chip and connected to the same supply will load the sampling capacitance of the SAR ADC. Thus, the reduction of sampling energy will decrease the energy consumption of the system to the same extent as the reduction of switching energy.

The architecture generally denoted as "classical" SAR ADC architecture (Fig. 1) is unpopular today. In the most up-to-date architectures (Fig. 2), the capacitive DAC and SHA typically are joined into a single block. This allows elimination of the special SHA block and simplification of the comparator design in differential mode. Furthermore, the top-sampling is usually implemented in 8-10 bit SAR ADCs – as this method allows the area and switching power of the DAC to be reduced twice.

This research was supported by DFG (German Research Foundation) grant (project number 89481053).

978-1-5386-7656-1/18/$31.00

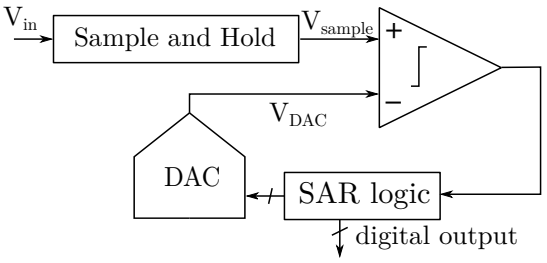

Fig. 1. Classical SAR ADC Architecture

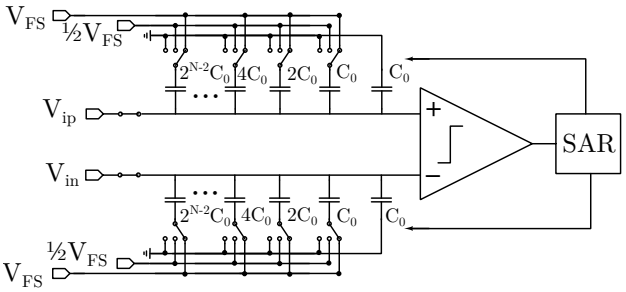

Fig. 2. Popular tri-level SAR ADC Architecture with the upper plate sampling

In the case of upper-plate sampling technique, the first comparison can be done without any switching of DACs capacitors. However, upper-plate sampling has very poor linearity in comparison with bottom-plate sampling: the use of a bootstrapped sampling switch is obligatory.

In this paper we propose the flying-capacitor sampling scheme, which provides the solution to both of the problems just discussed. It reduces the sampling capacitance to a single unit capacitor, and makes it possible to use almost any switching scheme with a high linear bottom-plate sampling technique.

II. Sampling Energy Calculation

The issue of sampling energy was, as the authors know, first raised in [8], where the sampling energy is estimated for the near Nyquist input signal. The minimum input buffer current is calculated for the Nyquist signal as: $I_{min} = N \times C_s \times (\Delta V_{max}/T_{Track})$, where ΔV_{max} is the maximum input

change, C_s is the capacitance of the sampling capacitor, and N is the number of time constants required for the $1/2$ LSB settling at the end of tracking period T_{track}.

In this paper, we use an other approach, because our main goal is to evaluate the sampling energy in comparison to the switching energy. The average switching energy is typically defined as an average through all possible DAC codes. In a similar way, for our sampling energy estimation we estimate the average sampling energy for a linear input signal, which causes a sequental switching of all ADCs codes from zero to $(2^N - 1)$:

$$E_{average}^{in} = \frac{\frac{C_S}{2} \sum_{i=0}^{2^N-1} \left(\frac{V_{ref}}{2^N-1} \times i \right)^2}{2^N - 1}, \quad (1)$$

where C_S is the sampling capacitance, V_{ref} is the reference voltage and N is the resolution of the SAR ADC. So, for example, for the 10-bit SAR ADC, which is usually used to compare different switching schemes, the average sampling energy will equal $E_{average}^{in} \approx 0.17 C_S V_{ref}^2$.

III. State-of-the-art low sampling capacitance SAR architectures

The most energy efficient switching scheme among previously reported was proposed in [9] (Fig. 3). During the sampling phase the sampling capacitors are charged to differential input voltage, while the DAC capacitors are connected with both plates to ground voltage (so, reset energy [10] is equal to zero). The average sampling energy will equal $0.17 C_S V_{ref}^2 = 0.17 C_0 V_{ref}^2$ only. When the conversion phase begins the sampling capacitors upper plates are disconnected from the input signal source. The upper plates of the DAC capacitors and bottom plates of the sampling capacitors are disconnected from ground. The upper plates of the sampling capacitors are flying, so the comparator differential input voltage will be equal to:

$$V_{cmp} = V_{in}^{sampled} + V_{DAC}, \quad (2)$$

where $V_{in}^{sampled}$ is the sampled differential input voltage and V_{DAC} is the differential voltage of the capacitive DAC. Then, the usual SAR alghorithm can start. Actually, almost all recently published switching schemes can be used to provide the needed V_{DAC} voltage.

However, the authors in [9] use the upper plate sampling, which degrades the linearity of the resulting circuit.

The bottom-plate sampling, which provides much better linearity was used in low sampling capacitance switching schemes in [11], [12] (Fig. 4). Although the main focus of these works was on introducing the power-efficient bottom plate sampling, these schemes can also be used to lower the sampling capacitance of SAR ADC.

The switching scheme proposed in [11] is shown in Fig. 4(a). In the figure, the sampling capacitance is equal to the 2^{N-2}, which is $256C_0$ in the case of 10 bit ADC. The main

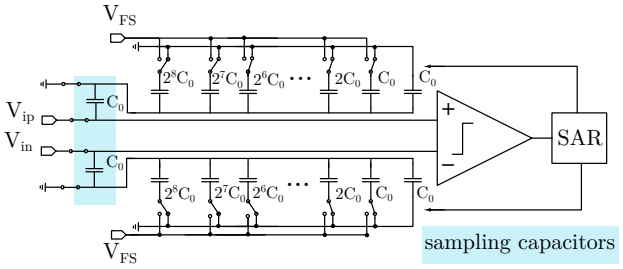

Fig. 3. Low sampling capacitance SAR ADC architecture proposed in [9]

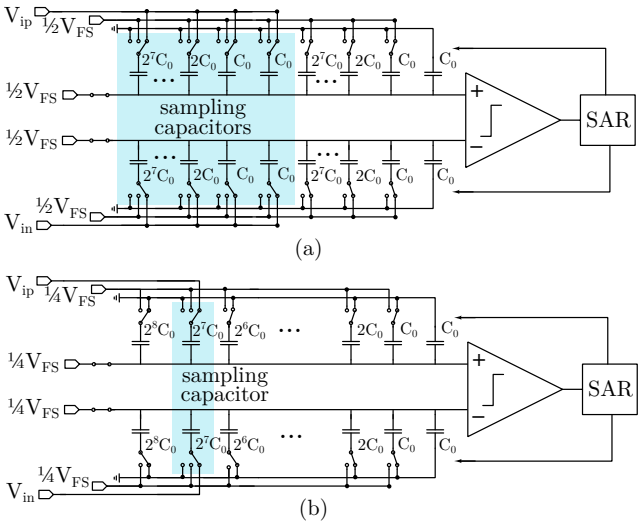

Fig. 4. Split capacitor array switching schemes (both switching schemes are shown in sampling phase): (a) half of the capacitor array is split [11]; (b) single-capacitor sampling scheme [12]

advantages of this switching scheme are: the use of bottom plate sampling, which means potentially higher linearity, and the need of only one reference voltage equal to half of full-scale voltage. In this switching scheme the ADC converts half of the real input voltage. The sampling capacitance can be decreased only by incurring further decrease of reference voltage and increase of input voltage divider. This is demonstrated in Fig. 4(b), where the next switching scheme proposed by the same authors is shown. The reference voltage is decreased to one quarter of full-scale voltage.

In the 10 bit SAR ADC case, the average sampling energy will equal to 43.52 $C_0 V_{ref}^2$ and 21.76 $C_0 V_{ref}^2$, for the switching schemes proposed in [11] and [12], respectively.

In the SAR ADC switching-related articles, the efficiency of the switching scheme is usually established for the 10 bit case. In Table 1, we compare the switching energy of some recently published switching schemes with their average sampling energy defined by equation (1). The first two switching schemes [3], [4] implement the typical tri-level switching with the upper-plate sampling, so the sampling capacitance equals the entire capacitance of the DAC. It can be seen that the sampling energy is comparable with the whole switching energy of the DAC. Similary, the very recent scheme in

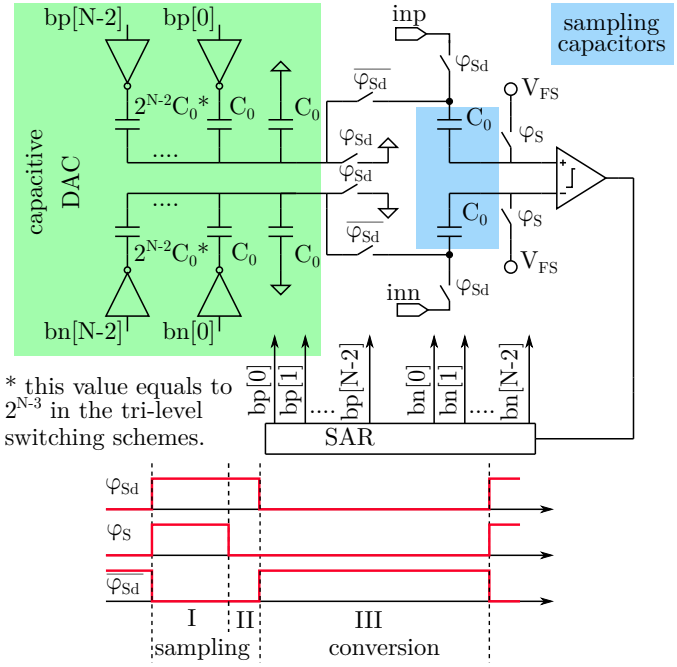

Fig. 5. Proposed SAR ADC architecture (any DAC architecture can be used instead of the binary weighted architecture shown in the figure)

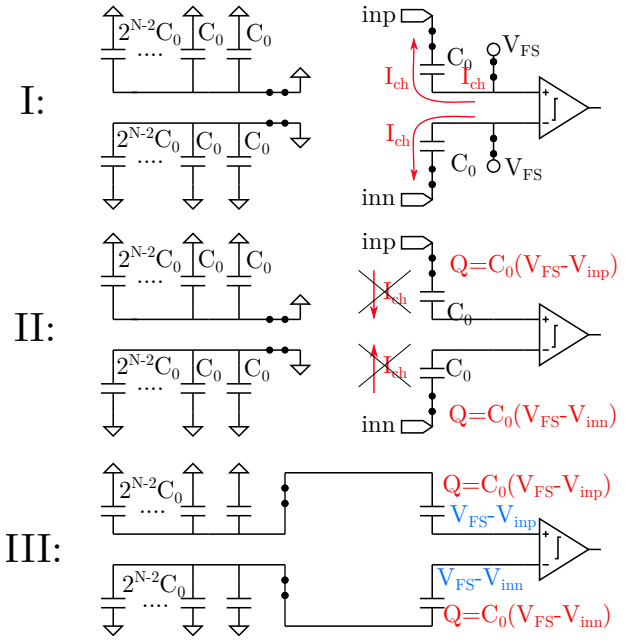

Fig. 6. SAR ADC configuration during different phases: I,II – bottom-plate sampling, III – conversion begin (first comparison can be made without switching of any DAC capacitors)

[2] uses a new third reference voltage level (one quarter of V_{ref}) and reduces the DAC capacitance further to $256C_0$, but the sampling capacitance is still equal to the whole DAC capacitance. The switching schemes in [11], [12] provide an interesting capability to combine advanced switching with bottom-plate sampling, but the sampling capacitance is also high and the bottom plate sampling is done by the cost of dividing the input signal by two.

TABLE I
COMPARISON OF SWITCHING ENERGY WITH SAMPLING ENERGY OF SOME RECENTLY PUBLISHED SAR ADC SCHEMES

Scheme	Sampling capacitance, C_0	Sampling Energy, $C_0V_{ref}^2$	Switching Energy, $C_0V_{ref}^2$
Zhu, Xiao and Song [4], 2013	512	85.7	31.88
Tong and Ghovanloo [3]*, 2015	512	85.7	143.7
V_{aq} switching scheme [2], 2018	256	43.5	48.03
Split DAC scheme [11], 2016	512	85.7	21.2
Single capacitor sampling [12], 2016	256	43.5	7.97

*The reset energy was not considered by the authors, estimation was done in [10]

IV. Proposed Sampling Scheme

The proposed SAR ADC architecture is shown in Fig. 5 along with the sample signal phases needed to perform bottom plate sampling. The sampling scheme combines the flying-capacitor technique [13] with the bottom-plate sampling method. The sampling signal consist of three phases: actual sampling phase – φ_S, delayed falling edge phase – φ_{Sd} and inverted delayed falling edge phase $\overline{\varphi_{Sd}}$. The sampling process can be split into two stages denoted in Fig. 5 as I and II. The conversion is also denoted as stage III in the figure 5.

The SAR ADC configuration in these three stages is shown in Fig. 6. During stage I, the bottom plates of the sampling capacitors are connected to the input signal, whereas the top plates are connected to the reference voltage (denoted as V_{FS} in the figures 5 and 6). The sampling capacitors of the upper and bottom halves of the differential ADC are charging to $Q_p = C_0(V_{FS} - V_{inp})$ and $Q_n = C_0(V_{FS} - V_{inn})$, respectively. Then, in stage II, the reference voltage is disconnected from the upper plates of the sampling capacitors, which effectively fly in this stage and next stage III. This prevents any current flow from the input source, so the charge injection from the sampling switch is eliminated (bottom-plate sampling principle). This allows very simple implementation of sampling switches as they have no influence on the linearity of the sampling process. The sampling phase ends.

The conversion stage (also denoted as III in figures 5 and 6 begins. The first comparison can be made without any DAC switching, as the differential comparator input voltage is equal to $V_{inn} - Vinp$ as in most up-to-date upper-plate sampling switching schemes. So, the size of the DAC capacitive matrix can be also reduced twice in comparison to the "traditional" bottom plate sampling SAR ADC. The use of bottom-plate sampling also means, that simple single transistor switches can be used for all switches.

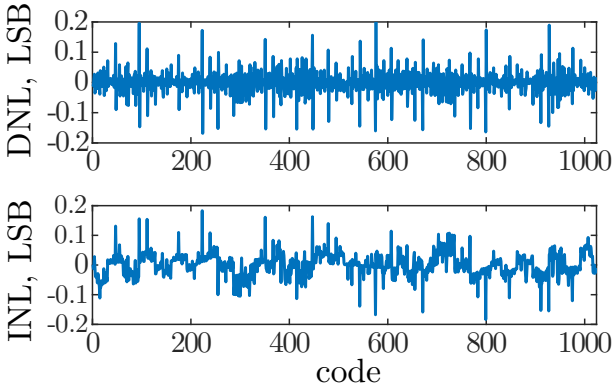

Fig. 7. DNL and INL simulation results for 10-bit SAR ADC implementation in 65 nm CMOS

V. Simulation Results

To verify our theoretical considerations we also performed the semibehavioral simulations of our architecture in the standard 65 nm CMOS technology of UMC. The comparator and SAR algorithm were simulated at the behavioral level with the help of Verilog-AMS, whereas all the switches, inverters and capacitors were simulated on the transistor level.

We used the minimum available metal-insulator-metal (MIM) capacitor available in the considered technology – 51.16 fF. We also used the minimum size low threshold voltage transistors as sampling switches (80nm/60nm). The same transistors were used for the inverters to provide low supply operation of the circuit (the reference voltage was set to 0.5 V). The sampling switch was clocked with the doubled amplitude to provide the fullscale input, all other switches were clocked with the clock signal with the amplitude equal to the reference voltage. The "normal" monotonic switching scheme was used for the DAC [14], but any other switching scheme generally can be used.

The simulation results of differential nonlinearity (DNL) and integral nonlinearity (INL) are shown in Fig. 7.

As can be seen, even simple one-transistor switches provide relatively high linearity of ADC because of bottom plate sampling. The maximum INL error does not exceed 0.18 LSB (least significant bit). Fig. 8 shows the dynamic performance at 490.02 kHz fullscale input sampled at 983.04 kHz.

VI. Conclusion

The proposed sampling scheme has several important advantages: first, it allows the use of bottom-plate sampling with almost any previously reported switching scheme. This means that the ADC incorporating our sampling scheme will benefit from low power features of the advanced switching scheme without loss of accuracy because of upper-plate sampling. Second, the sampling capacitance is dramatically reduced in comparison with any previously reported SAR architectures, thus allowing the proportional reduction of sampling power and, consequently, reduction of the overall system power.

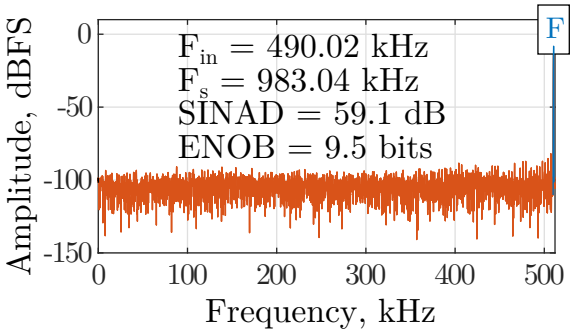

Fig. 8. Dynamic characteristics of 10-bit SAR ADC implementation in 65 nm CMOS

References

[1] L. Xie, W. Nie, L. Xiong, and J. Su, "Energy-efficient capacitor-swapping reset scheme with msb-split dac for sar adcs," *Electronics Letters*, vol. 53, no. 7, pp. 458–459, 2017.

[2] J. Zhao, N. Mei, Z. Zhang, and L. Meng, "Vaq-based tri-level switching scheme for sar adc," *Electronics Letters*, vol. 54, no. 2, pp. 66–68, 2018.

[3] X. Tong and M. Ghovanloo, "Energy-efficient switching scheme in sar adc for biomedical electronics," *Electronics Letters*, vol. 51, no. 9, pp. 676–678, 2015.

[4] Z. Zhu, Y. Xiao, and X. Song, "Vcm-based monotonic capacitor switching scheme for sar adc," *Electronics Letters*, vol. 49, no. 5, pp. 327–329, February 2013.

[5] D. Osipov and S. Paul, "Two advanced energy-back sar adc architectures with 99.21 and 99.37 % reduction in switching energy," *Analog Integrated Circuits and Signal Processing*, vol. 87, no. 1, pp. 81–91, Apr 2016.

[6] R. Ding, H. Liang, and S. Liu, "A novel switching scheme and area-saving architecture for sar adc," *Analog Integrated Circuits and Signal Processing*, vol. 91, no. 1, pp. 149–154, Apr 2017. [Online]. Available: https://doi.org/10.1007/s10470-017-0924-4

[7] R. H. Walden, "Analog-to-digital converter survey and analysis," *IEEE Journal on Selected Areas in Communications*, vol. 17, no. 4, pp. 539–550, Apr 1999.

[8] H. S. Bindra, A. J. Annema, S. M. Louwsma, E. J. M. van Tuijl, and B. Nauta, "An energy reduced sampling technique applied to a 10b 1ms/s sar adc," in *ESSCIRC 2017 - 43rd IEEE European Solid State Circuits Conference*, Sept 2017, pp. 235–238.

[9] G. Y. Huang, C. C. Liu, Y. Z. Lin, and S. J. Chang, "A 10-bit 12-ms/s successive approximation adc with 1.2-pf input capacitance," in *2009 IEEE Asian Solid-State Circuits Conference*, Nov 2009, pp. 157–160.

[10] D. Osipov and S. Paul, "Two-step reset method for energy-efficient sar adc switching schemes," *Electronics Letters*, vol. 52, no. 10, pp. 816–817, 2016.

[11] B. Yazdani, A. Khorami, and M. Sharifkhani, "Low-power bottom-plate sampling capacitor-splitting dac for sar adcs," *Electronics Letters*, vol. 52, no. 11, pp. 913–915, 2016.

[12] ——, "Low power dac with single capacitor sampling method for sar adcs," *Electronics Letters*, vol. 52, no. 14, pp. 1209–1210, 2016.

[13] L. Der, S. H. Lewis, and P. J. Hurst, "A switched-capacitor differencing circuit with common-mode rejection for fully differential comparators," in *Proceedings of 36th Midwest Symposium on Circuits and Systems*, Aug 1993, pp. 911–914 vol.2.

[14] C. C. Liu, S. J. Chang, G. Y. Huang, and Y. Z. Lin, "A 10-bit 50-ms/s sar adc with a monotonic capacitor switching procedure," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 4, pp. 731–740, April 2010.