











### **Outline**

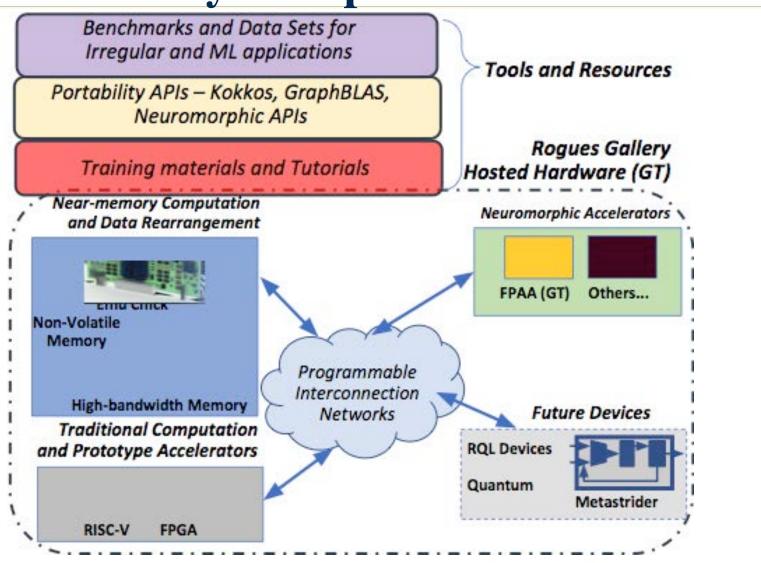
- Neuromorphic Computing
  - Field Programmable Analog Arrays
  - DANNA
  - Other future platforms
- Reconfiguable Computing
- Benchmarking and Tools







# Rogues Gallery Recap



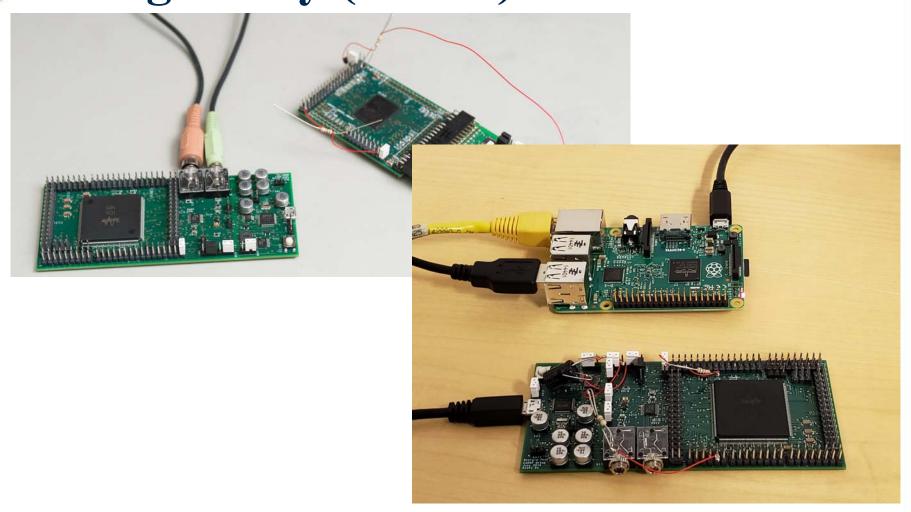
Field Programmable











# Why Physical / Analog

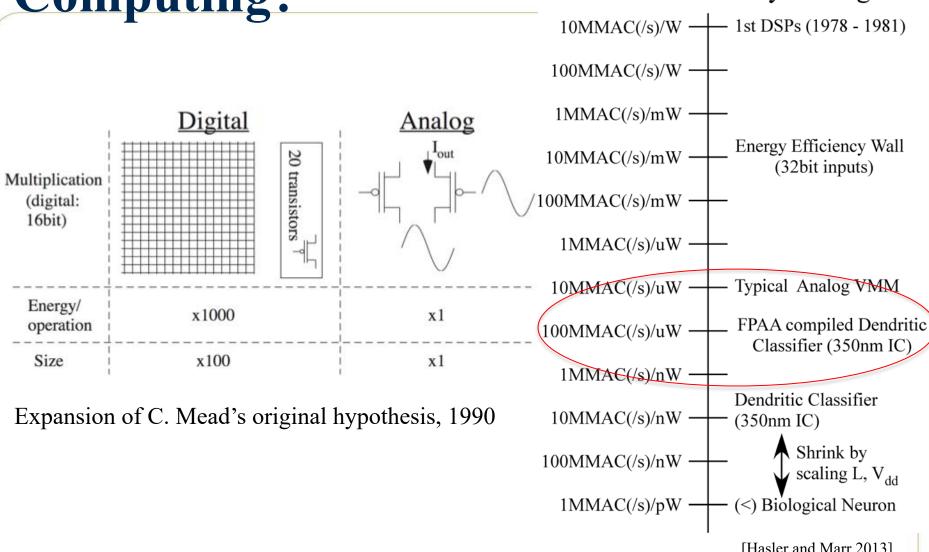






Computing?

#### Power Efficiency Scaling



[Hasler and Marr 2013]

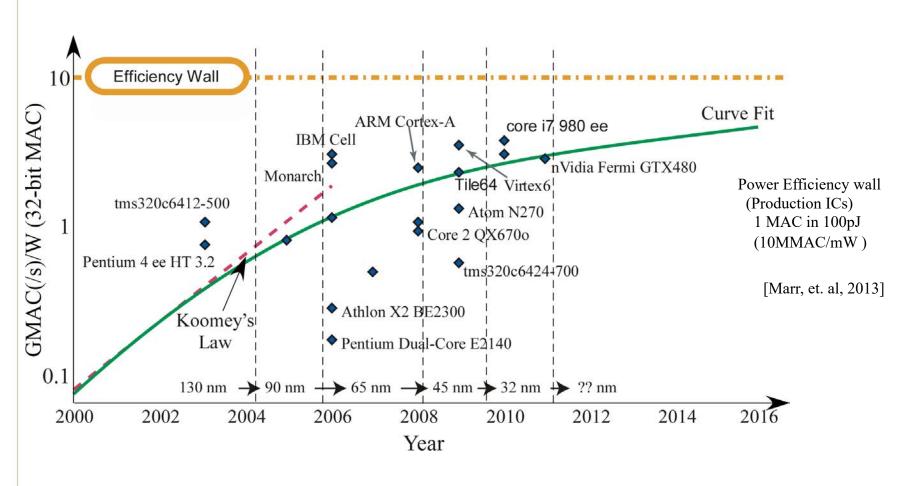
# Why Physical / Analog Computing?







#### <u>Digital Hitting Limits of Power Efficiency – Koomey's Law</u>



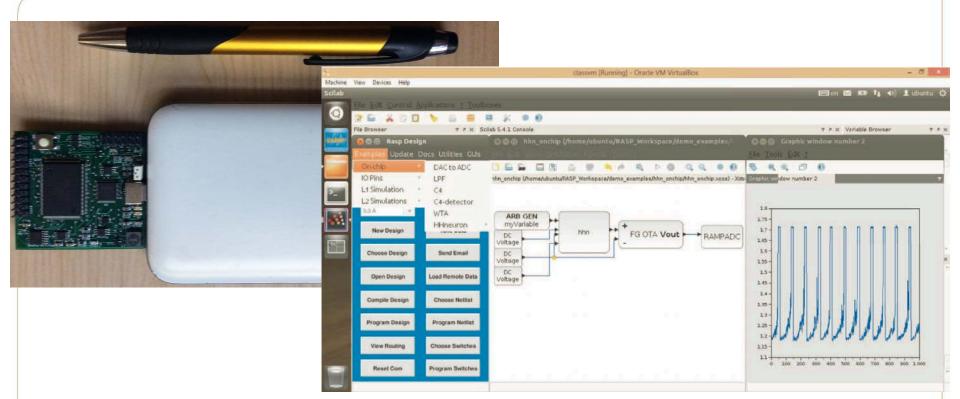
## FPAAs enable Ultra-low







Power Computing



The FPAA provides a mixed analog/digital platform with a general and configurable design that can be used create secure and legacy resistant mixed-signal devices

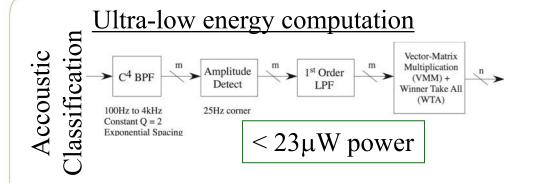


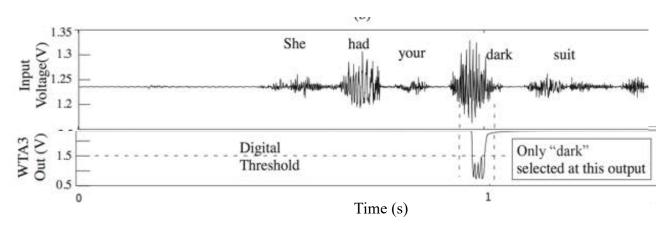






### FPAA Classification Task





Embedded learning & classification: 20-30μW on full, 1s Nzero database (GOMAC 2016)

### **FPAA Classification to Date**







Built on Analog Vector-Matrix Multiplication (VMM), including in routing, Winner Take All (WTA), etc.

Initial Command-Word Classification (Hand-tuned Weights) (2015)

Biomedical classifier (Hand-tuned weights) and computational measures (Knee sounds, Heart monitoring)

Speech – No-Speech Detector (Hand tuned weights)

Acoustic Classification and Learning:

- Developed Theory and Training Algorithm for VMM+WTA Classification
- Trained using modified Lincoln Lab's acoustic data set for Nzero program.
- Yielded correct detection on all sets

Current work on Image classification (2-D sensor inputs) 2-layer NN or DNN are possible...

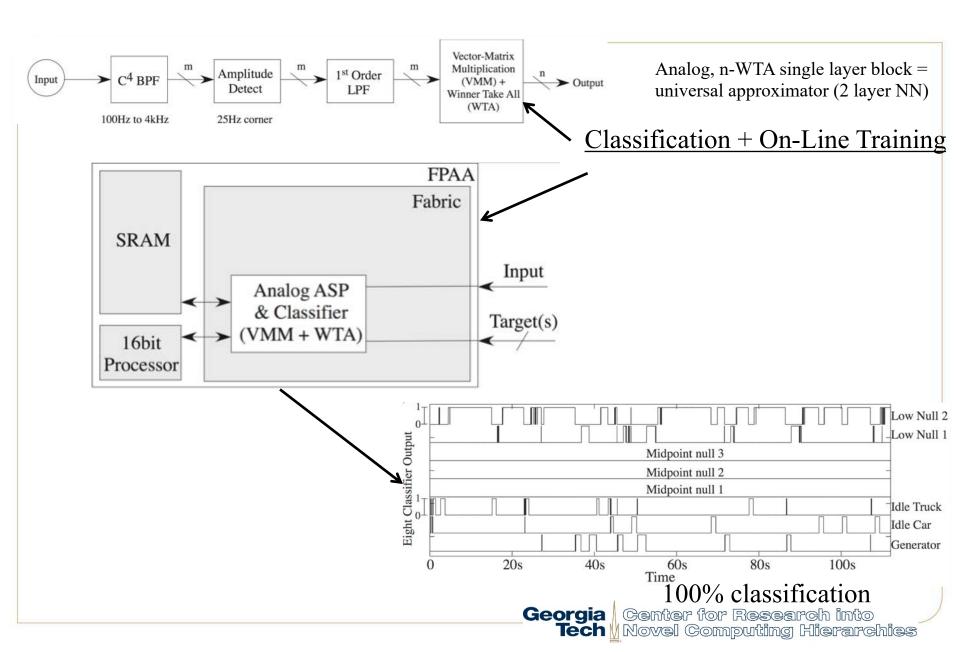
- VMM+WTA has worked well so far
- Can develop modular spiking (HH neuron) networks



### **More Analog Classifier (VMM+WTA)**





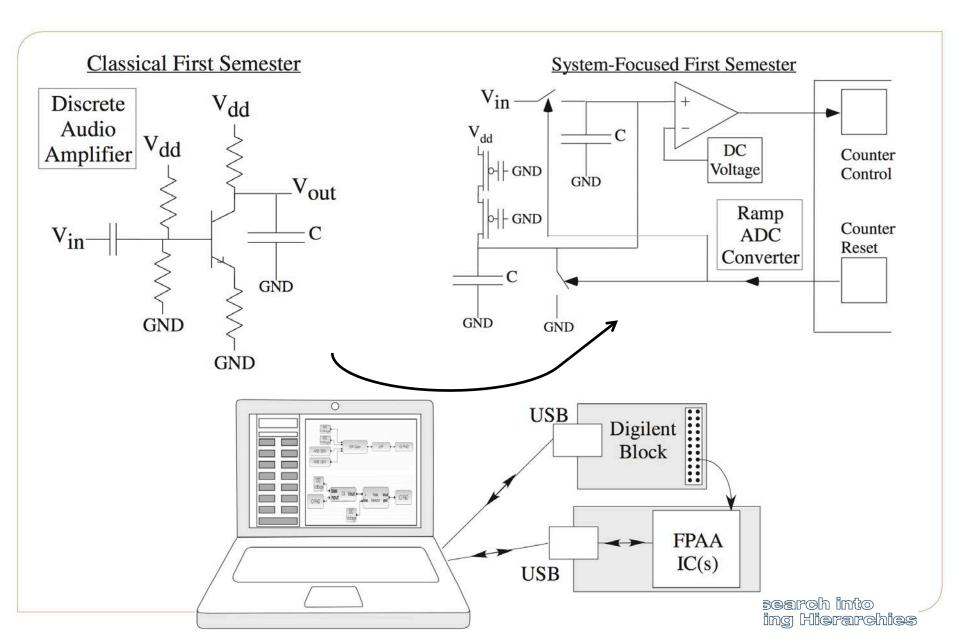








### **SoC FPAAs in the Classroom**

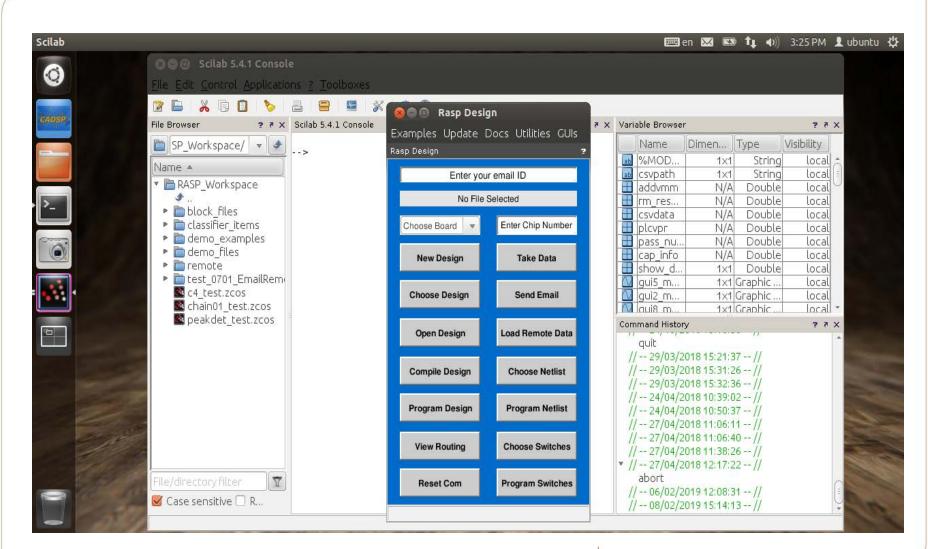








# FPAA Toolflow and Examples (1)

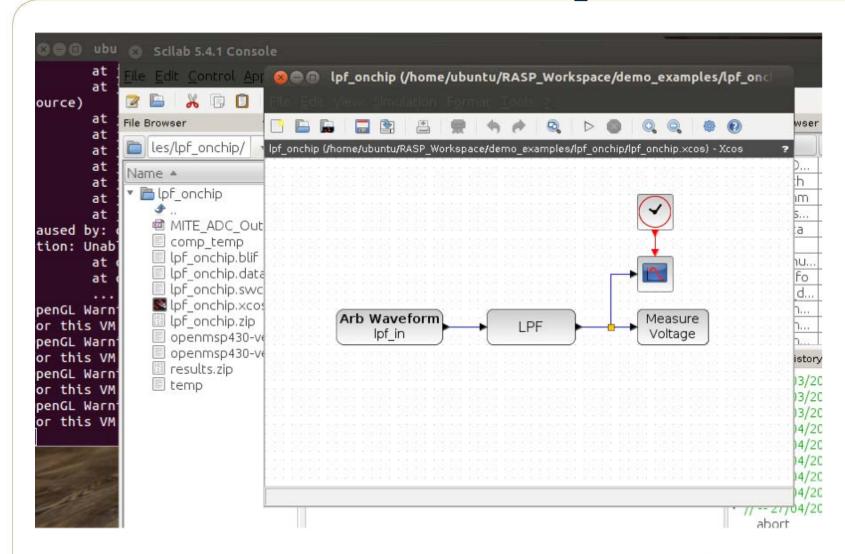








# FPAA Toolflow and Examples (2)

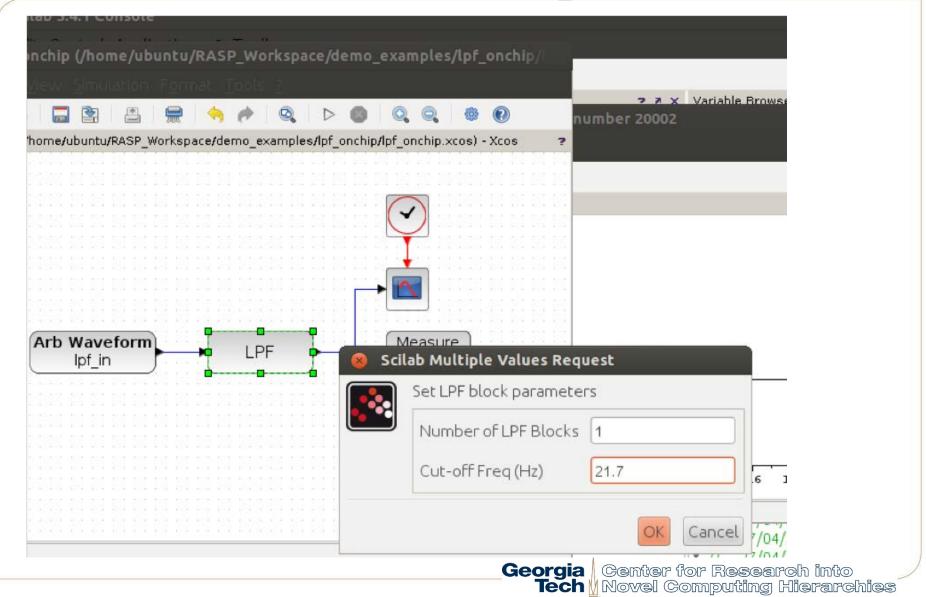








# FPAA Toolflow and Examples (3)

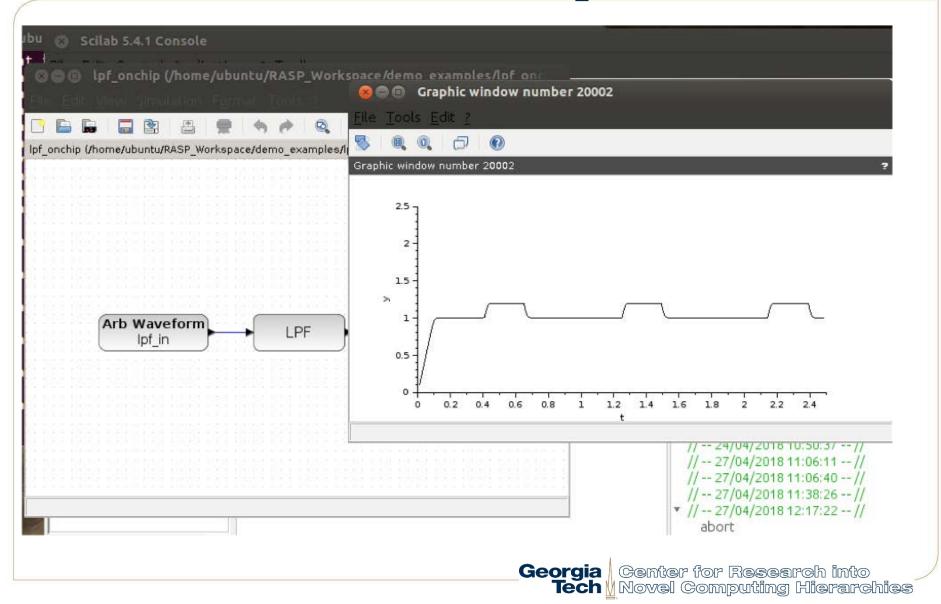








# FPAA Toolflow and Examples (4)

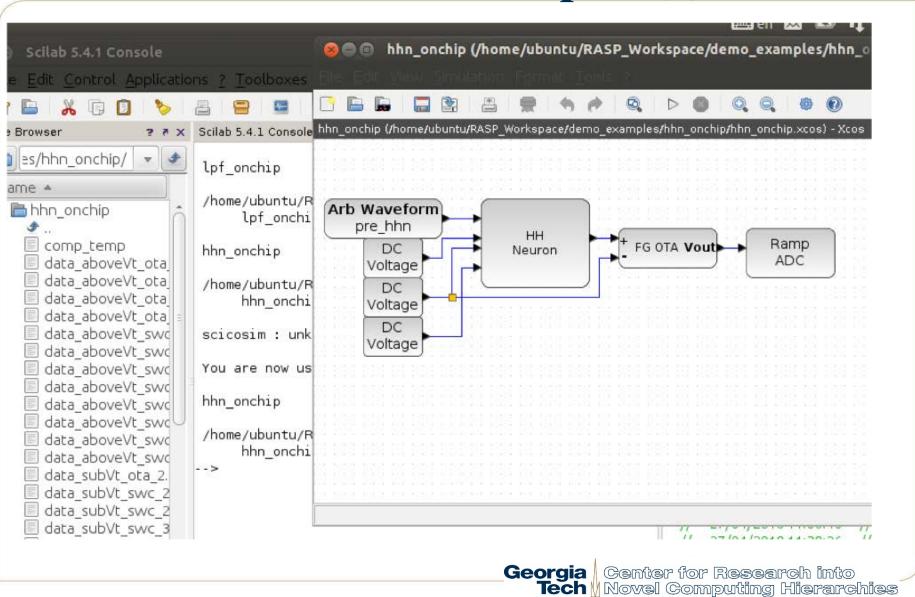








# FPAA Toolflow and Examples (5)

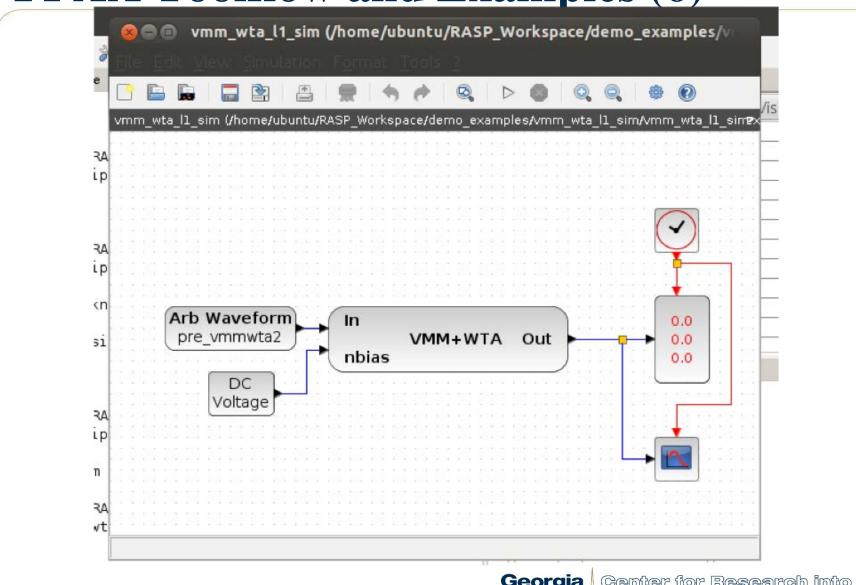








FPAA Toolflow and Examples (6)



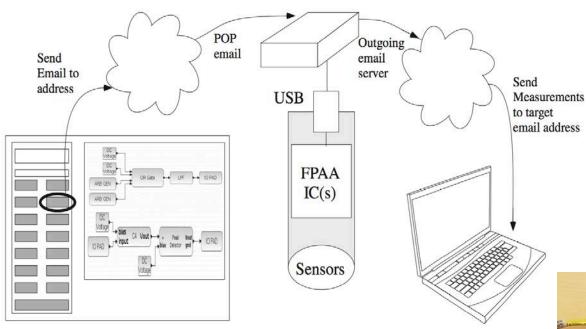
### **FPAA Infrastructure Details**











#### Pi-hosted FPAAs









# **FPAA** for Neuromorphic Computing

Near-term work is looking at interfacing with other neuromorphic APIs like EONS (Evolutionary Optimized Neuromorphic Systems)

We are also looking to host a prototype of UTK's DANNA architecture, which allows for testing neuromorphic architectures.

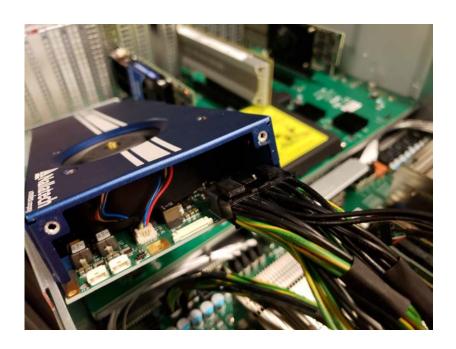






## FPGAs as Rogue Enablers





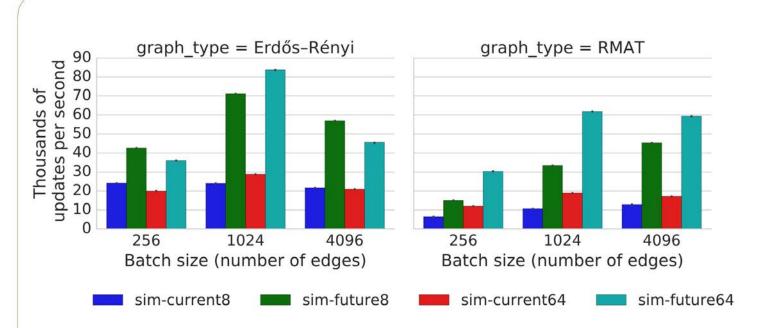
Boards with HBM enable high bandwidth for mapping algorithms, machine learning, and neuromorphic computing (Intel Loihi, DANNA)







### RG Benchmarking - Emu Microbench (STINGER)



Focused on Streaming BFS

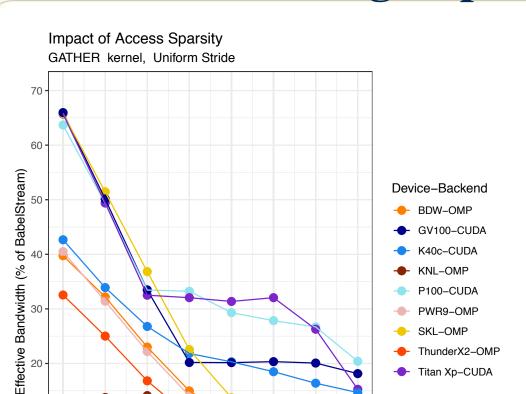
Code available at <a href="https://github.com/ehein6/emu-microbench">https://github.com/ehein6/emu-microbench</a> and increasingly as part of Emu toolchain releases







# **RG** Benchmarking - Spatter



32

Sparsity

128

10

Titan Xp-CUDA

#### **Code available at Spatter.io**

Spatter provides a new benchmark to evaluate gather/scatter accesses across different CPU and GPU platforms.

Emu and FPGA backends are in progress!







# RG Libraries – ParTI (Parallel Tensor Infrastructure)

Hardware

Multicore CPUs

**GPUs** 

Distributed Memory



#### **ParTI! Library**

https://github.com/hpcgarage/ParTI



Baseline Tensor Routines Tensor Decomposition

**Algorithms** 

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### **RG** Libraries - ParTI

Data Structures/ Platforms	Algorithms	Multicore CPUs	GPUs	Distributed Systems	Emu
coo	СР	<b>√</b>	<b>√</b>	<b>√</b>	<b>√</b>
	Tucker	<b>√</b>	$\checkmark$		
HiCOO	CP	<b>√</b>	<b>√</b>		
	Tucker				

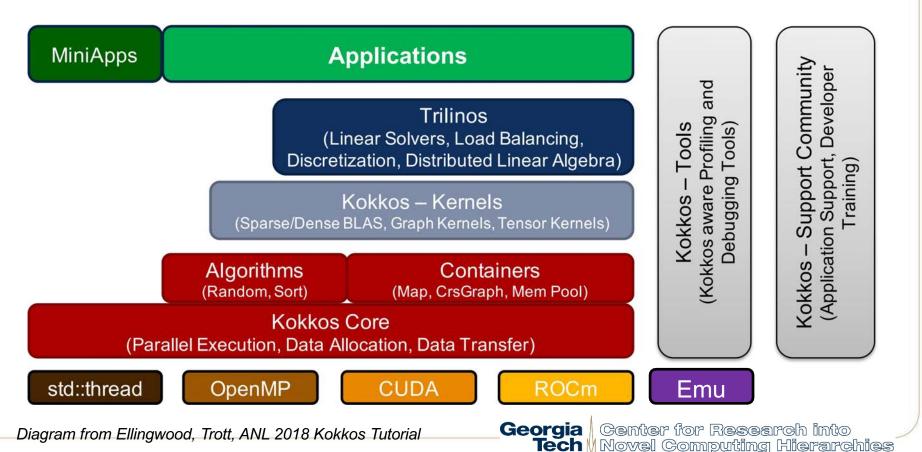
### **RG** Tools - Kokkos







 Kokkos is a C++ library that is focused on performance portability through the mapping of parallel patterns



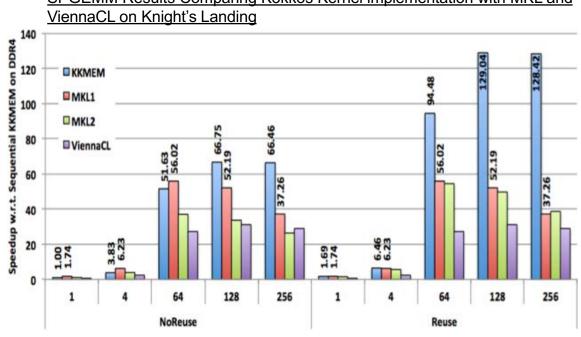
### **RG** Tools - Kokkos







- Kokkos Kernels provide implementations of common sparse, dense linear algebra, and graph-related operations
  - BLAS, SPARSE, AXPY, graph coloring, tensor contraction
  - Common front-end implementations benefit from mapping to Kokkos
    SPGEMM Results Comparing Kokkos Kernel implementation with MKL and



From Rajamanickam, et al. KokkosKernels: Compact Layouts for Batched Blas and Sparse Matrix-Matrix multiply, Batched BLAS Workshop, 2017

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# How to Work with the Rogues Gallery

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- Dr. Ümit Çatalürek (GT CSE)
- Dr. Tom Conte (GT CS/ECE)
- Dr. Vivek Sarkar (GT CS/ECE)
- Dr. Bora Uçar (ENS Lyon CNRS)
- Dr. Rich Vuduc (GT CSE)

#### Code:

- crnch-rg.gitlab.io front-end for public resources
- <a href="https://github.com/ehein6/emu-microbench">https://github.com/ehein6/emu-microbench</a>
- Spatter.io Spatter benchmark
- ParTI <a href="https://github.com/hpcgarage/ParTI">https://github.com/hpcgarage/ParTI</a>









### **Tutorial Feedback**

- Feel free to email us:
  - Jason jason.riedy@cc.gatech.edu
  - Jeff jyoung9@gatech.edu
- We also have a survey for you to fill out on the event webpage at

crnch-rg.gitlab.io/asplos-2019

