Novel Architectures for Applications in Data Science and Beyond

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Apps: Massive+-scale data analysis

Cyber-security	Identify anomalies, malicious actors
Health care	Find outbreaks, population epidemiology, similar patient association
Social networks	Advertising, searching, grouping
Intelligence	Decisions at scale, regulating markets, smart & sustainable cities
Systems biology	Understanding interactions, drug design
Power grid / Smart cities	Disruptions, conservation, prediction

Irregular data access. Changing data.

High-Performance Data Analysis (HPDA)

Novel applications:

- Data at scale and speed needs new ideas for computing analysis.
- “Big data” platforms fare poorly v. a single thread plus large SSD even for static data sets. (McSherry, Isard, Murray. “Scalability! But at what COST?” HotOS XV, 2015.)
- Many high-level codes are written and re-written to answer one question: need flexibility.
- *Some* primitives may be tuned and re-used.

HPDA and Architectures

- Current architectures are hitting limits on manufacturing, heat dissipation, memory latency...
- New architecture proposals are difficult to evaluate via simulation and modeling alone.
- What happens when novel prototypes hit reality?
- Architects/designers need rapid feedback on new ideas.
- New ideas only become successful with a community: software ecosystem, **trained students**.

Need bridges between apps and architects.

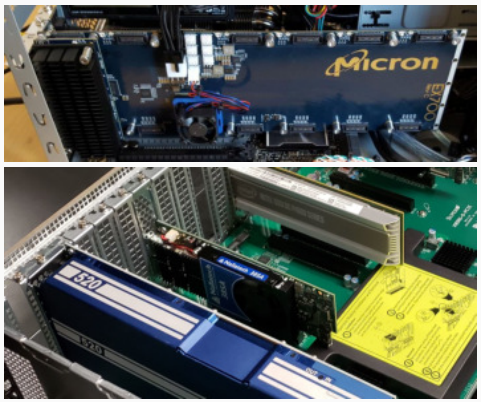
Introducing the CRNCH Rogues Gallery

Georgia Tech | Center for Research into Novel Computing Hierarchies

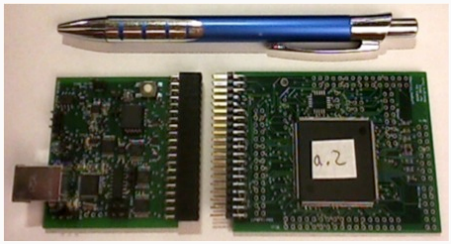
A physical & virtual space for hosting novel computing architectures, systems, and accelerators.

Emu Chick

FPGAs & HMC/HBM



FPAA

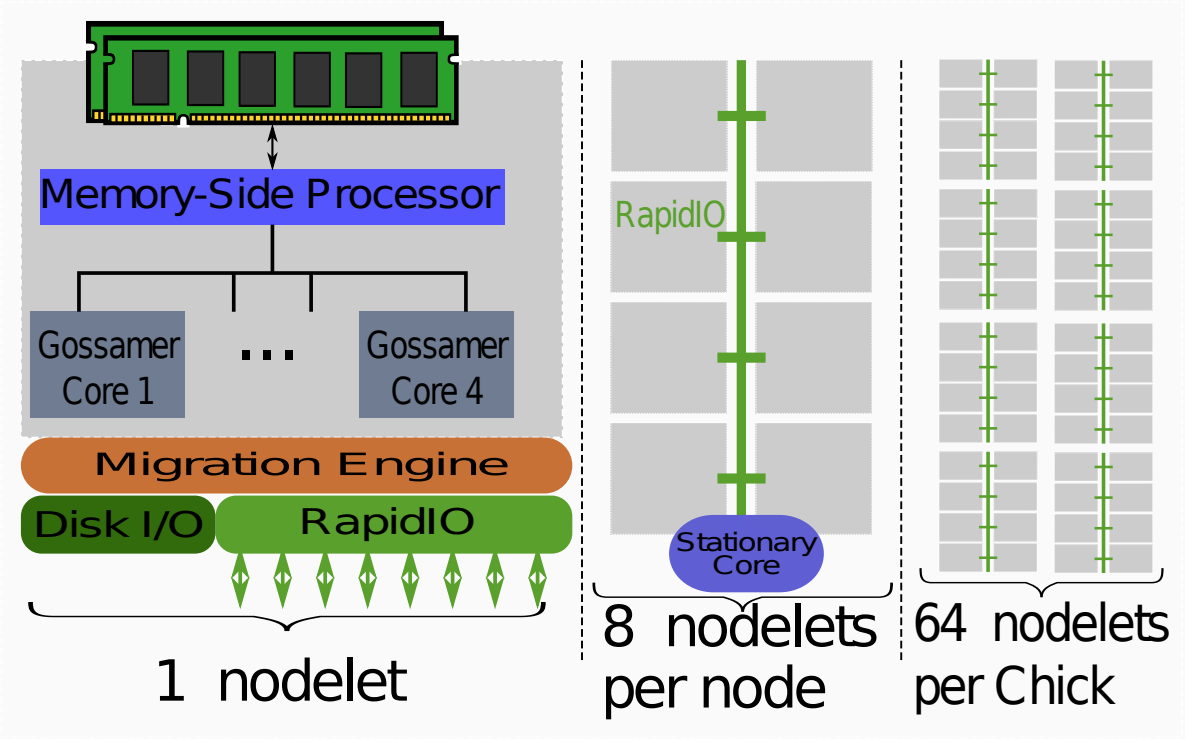


Amortize effort and cost of trying novel architectures.

Break the “but it’s too much work” barrier.

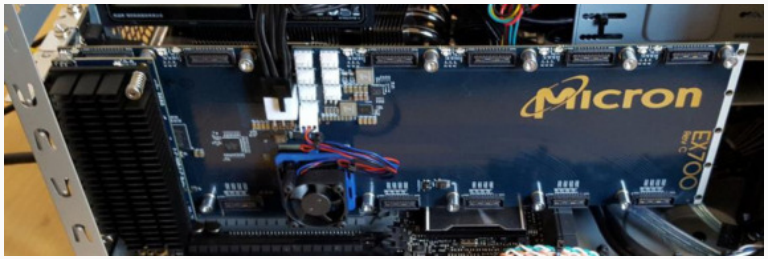
`http://crnch.gatech.edu/rogues-gallery`

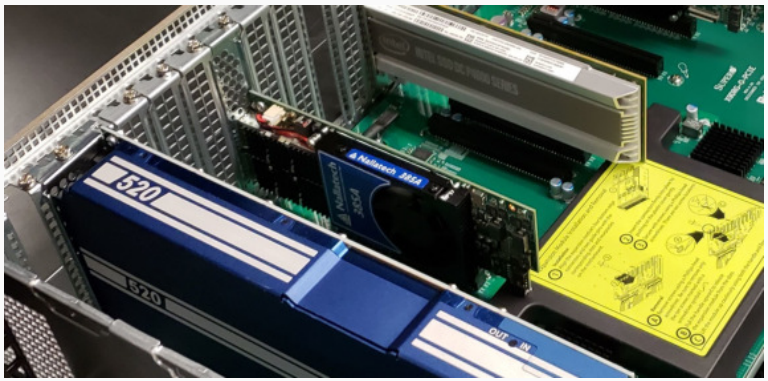
Emu Technology's PGAS Architecture



- Multithreaded multicore
- Memory-side "processor" for operations in narrow-channel DRAM
- Stationary core for OS
- **Threads migrate *in hardware* on reads!**
- Optimize for weak locality

3D Stacked Memory and FPGAs



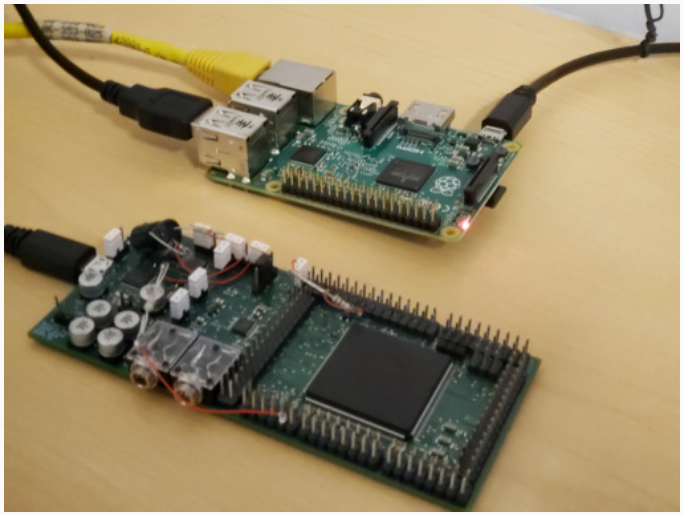


FPGAs enable flexible "near-memory" research for both hardware **and programming models**:

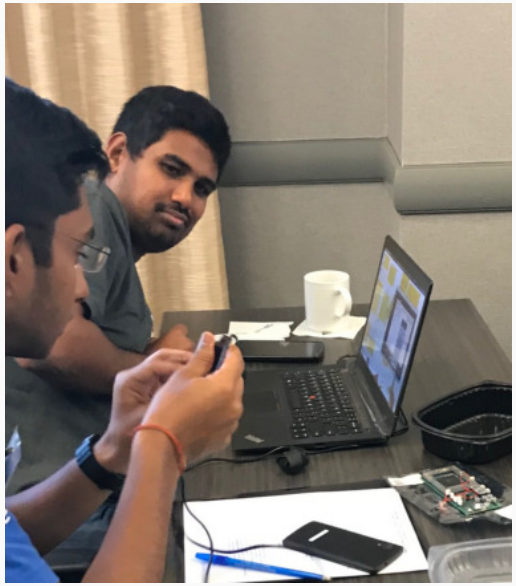
- Micron/Pico EX700 & HMC
- Nallatech 385s (Arria 10)
- Intel Arria10 DevKit
- Nallatech 520N (Stratix 10)
- Xilinx MpSOC

Neuromorphic Systems

- Field-Programmable Analog Array (FPAA) System-On Chip, designed in the lab of Dr. Jennifer Hasler.
- Analog arrays can achieve unprecedented power and size reductions.

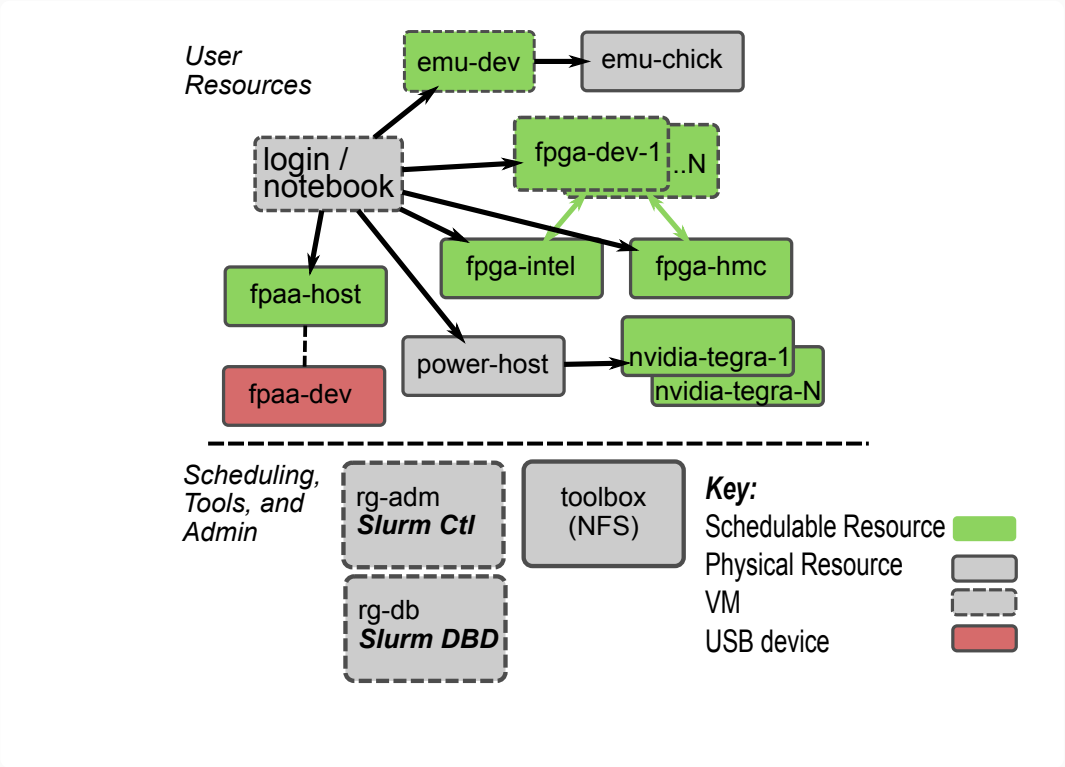


FPAA “driven” by a RPi



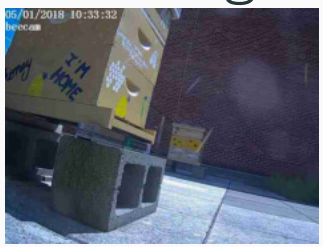
Neuromorphic Workshop, 27 Apr 2018

Flexible Infrastructure



Powell, Riedy, Young, and Conte. "Wrangling Rogues: Managing Experimental Post-Moore Architectures."
`https://arxiv.org/abs/1808.06334`

- Available. Plans to integrate with NSF XSEDE.
- Scheduler being deployed.
- Incorporates Singularity and virtual machines for OS/library versioning.
- Fun tools: `usbip` for FPAA... Analog inputs?



Rogues Gallery Press

On *The Next Platform*, a partner of *The Register*:

`https://www.nextplatform.com/2018/08/27/a-rogues-gallery-of-post-moores-law-options/`

Neuromorphic Workshop - April 2018

FPAA-focused workshop led by Dr. Hasler introduced the wider community to FPAA programming for neuromorphic systems.

- Tutorial-style class
- Lightning talks from GT and DoE researchers
- `http://crnch.gatech.edu/neuro-workshop18`

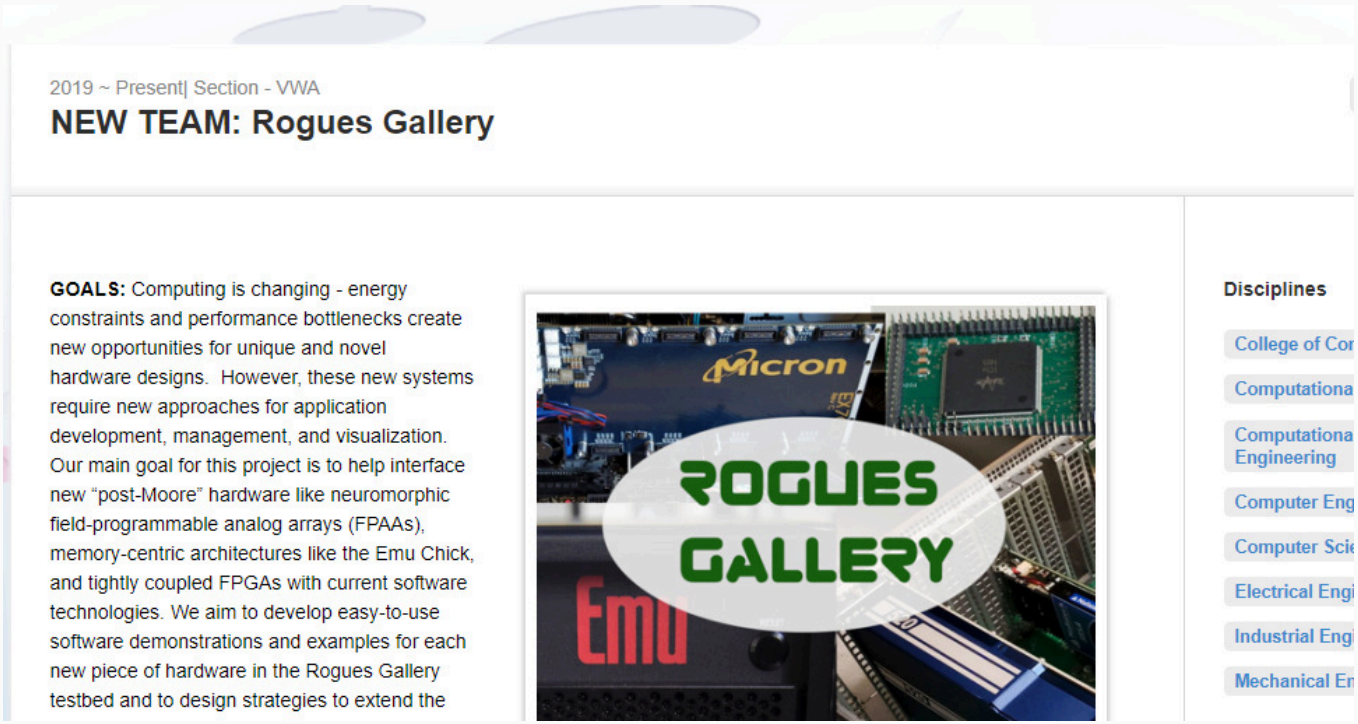
Rogues Gallery ASPLOS Tutorial

Programming Novel Architectures in the Post-Moore Era
with The Rogues Gallery

`https://crnch-rg.gitlab.io/rg/asplos-2019/`

- To be held at ASPLOS 2019 in Providence, RI.
- 14 April 2019, 8.30am – 12.00pm
- Architecture detailed descriptions
- Hands-on with the Emu Chick and (hopefully) the FPAA

Rogues Gallery VIP Team



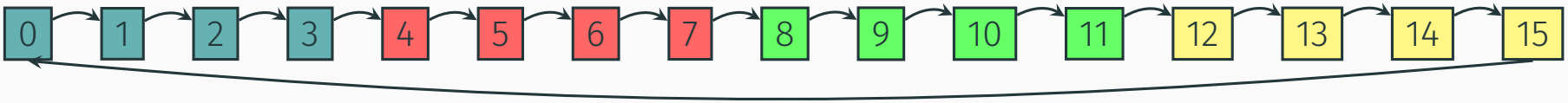
Rogues Gallery VIP team has started in Spring 2019. This course allows undergraduates to get research experience working with software for novel architectures.

`http://www.vip.gatech.edu/teams/new-team-rogues-gallery`

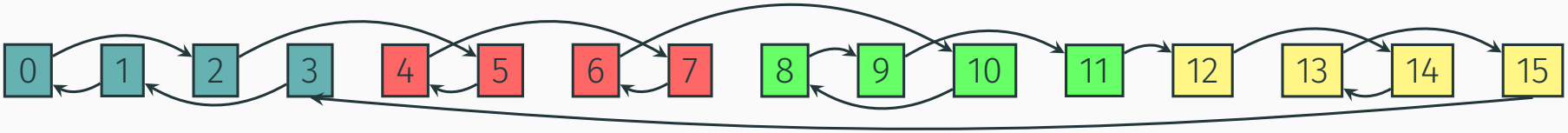
Selected Results: Emu Pointer-Chasing Benchmark

Data-dependent loads, fine-grained access[1]

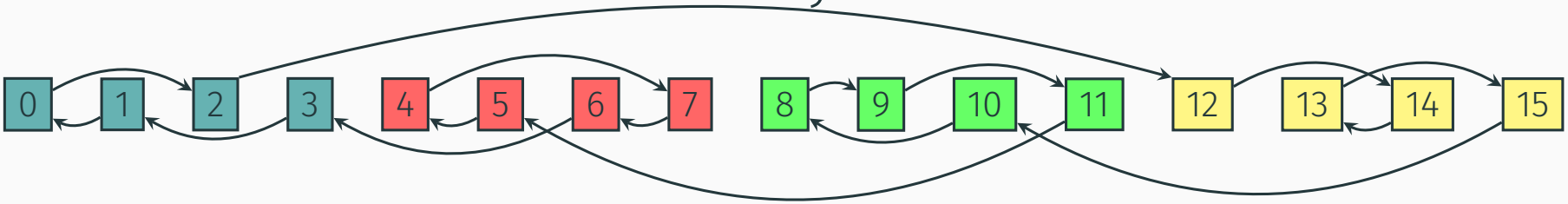
Ordered



Intra-block shuffle: weak locality

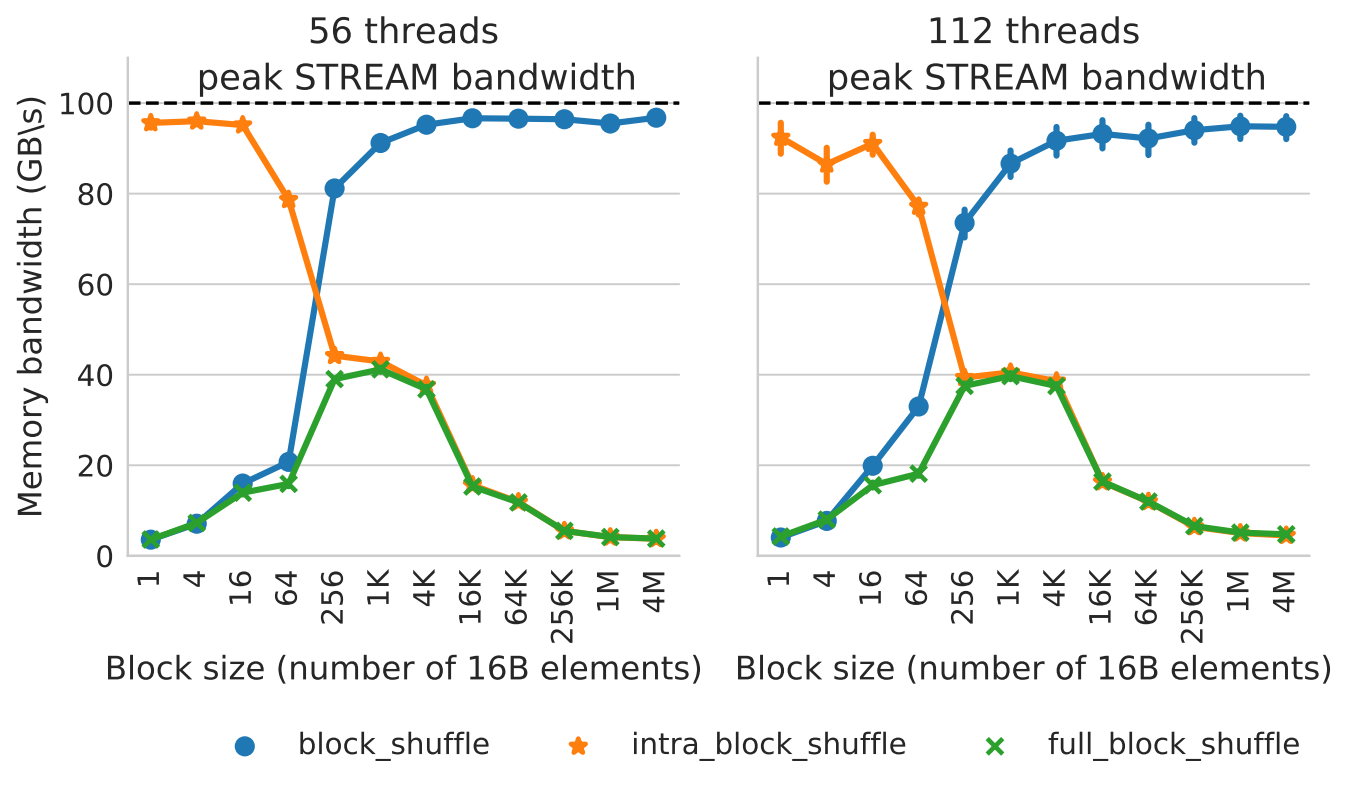


Full block shuffle: weak locality



[1] Eric Hein, Young, Srinivas Eswar, Jiajia Li, Patrick Lavin, Vuduc, Riedy. "An Initial Characterization of the Emu Chick," Workshop on Accelerators and Hybrid Exascale Systems (AsHES) 2018.

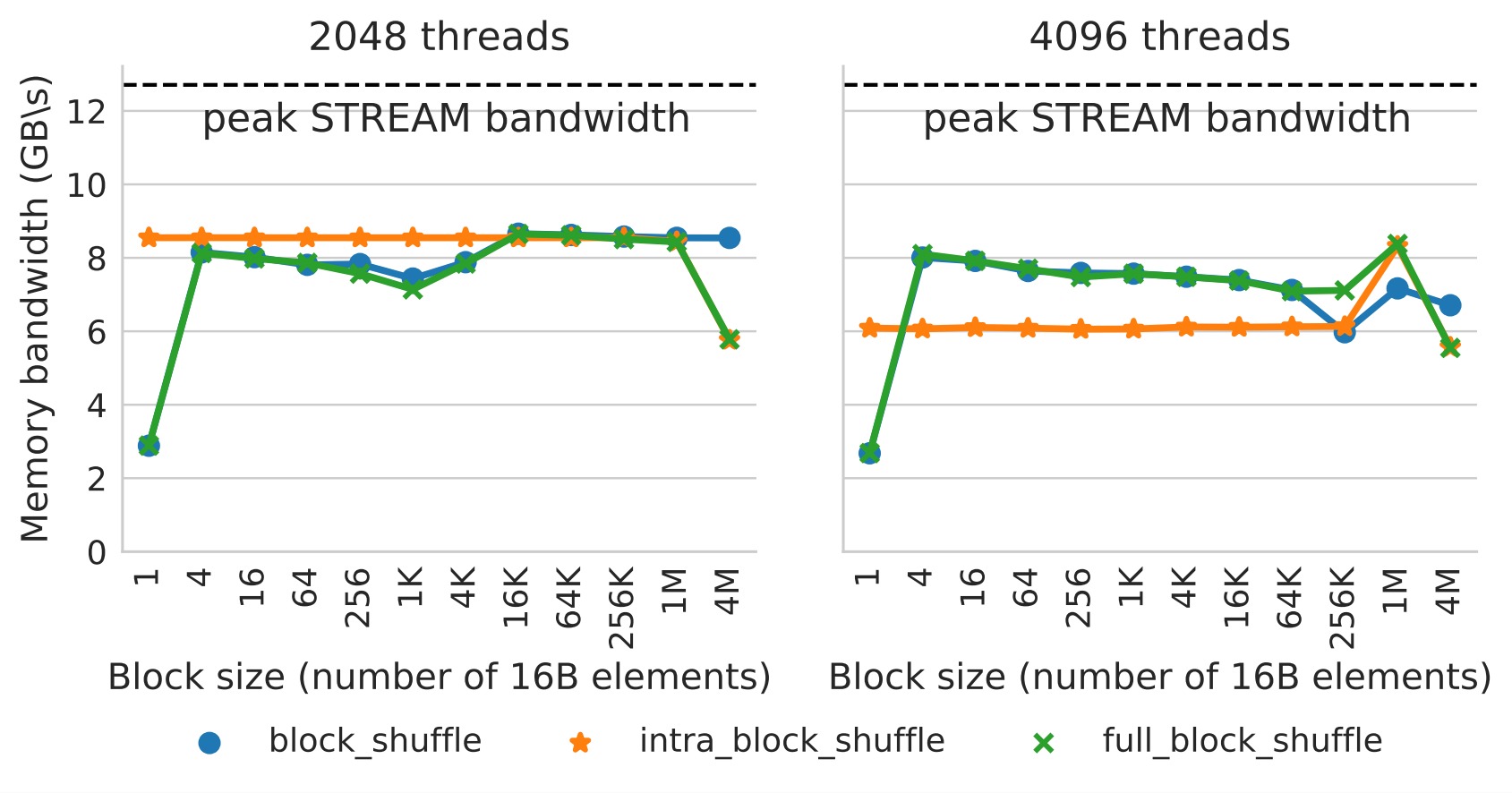
Selected Results: x86 Pointer-Chasing Benchmark



Haswell results, every pattern is different.[2]

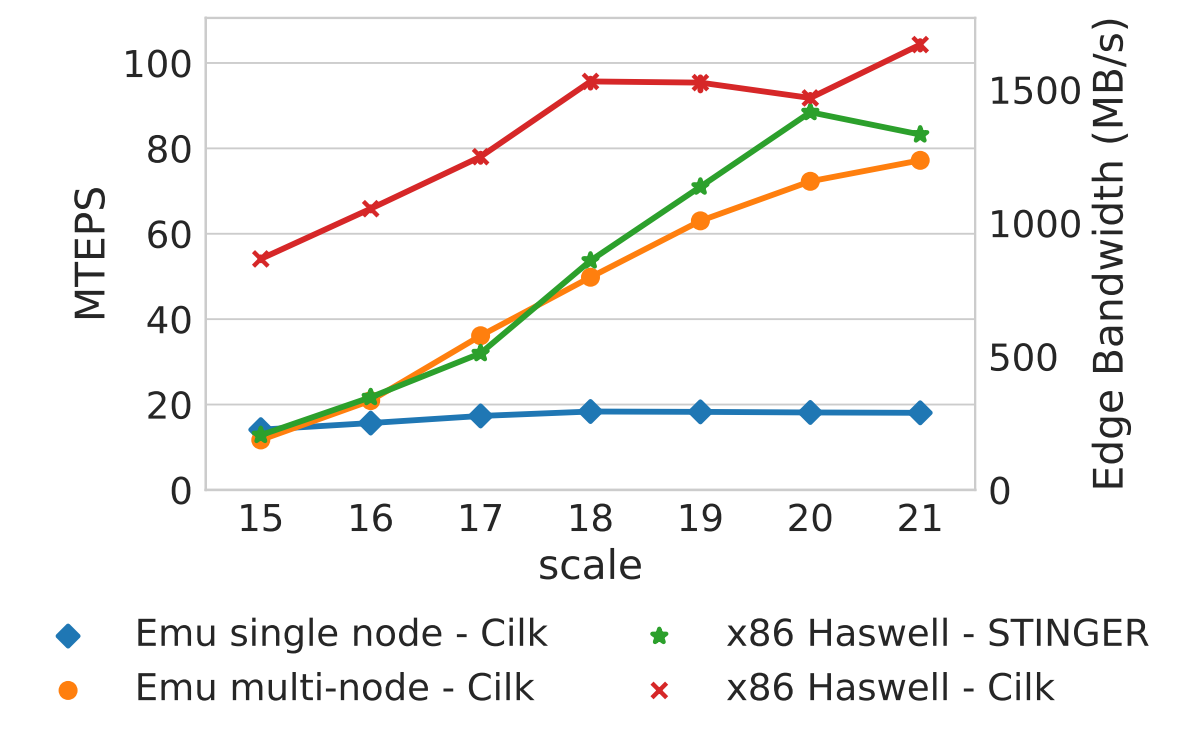
[2] Eric Hein, Young, Srinivas Eswar, Jiajia Li, Patrick Lavin, Riedy, Vuduc, Conte. "A Microbenchmark Characterization of the Emu Chick." `https://arxiv.org/abs/1809.07696`

Selected Results: Emu Pointer-Chasing Benchmark



Mostly flat performance, high utilization.[2]

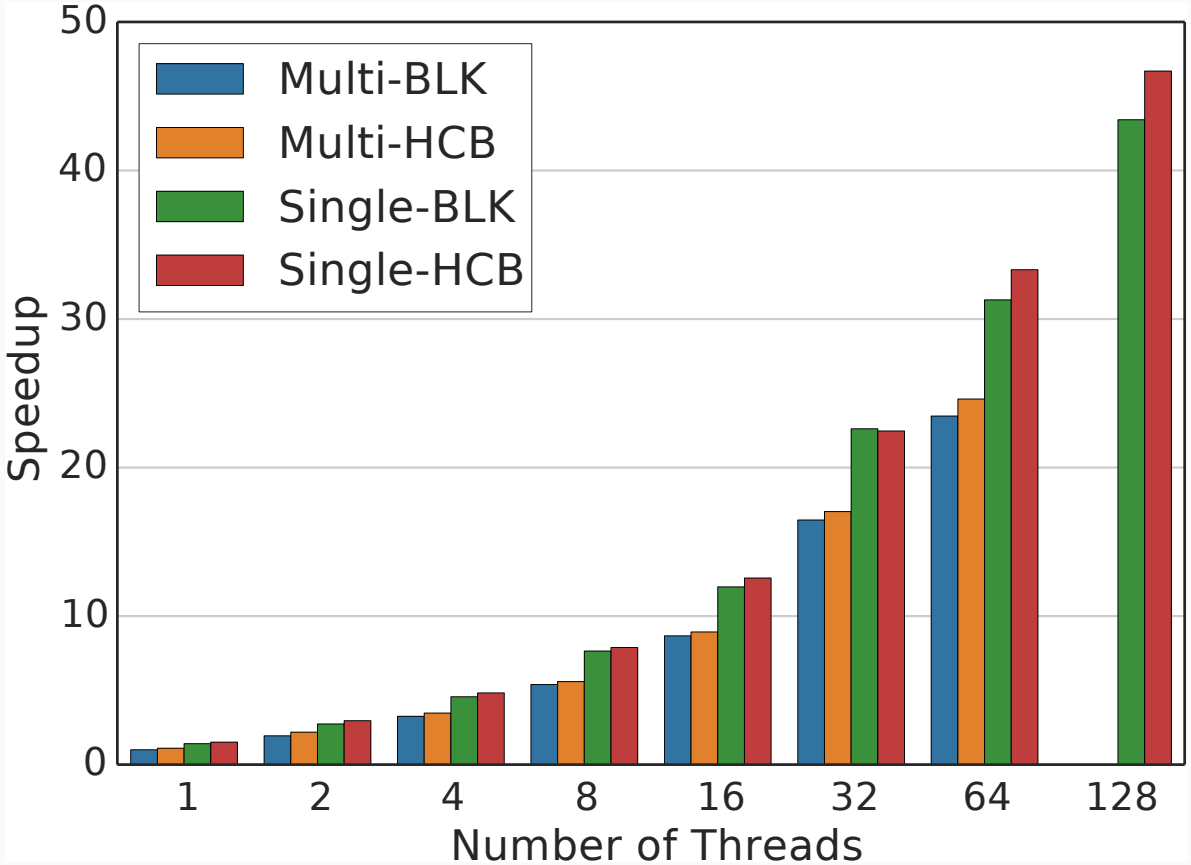
Selected Results: BFS on a Dynamic Data Structure



Note: Streaming data structure, not statically optimized. [3]

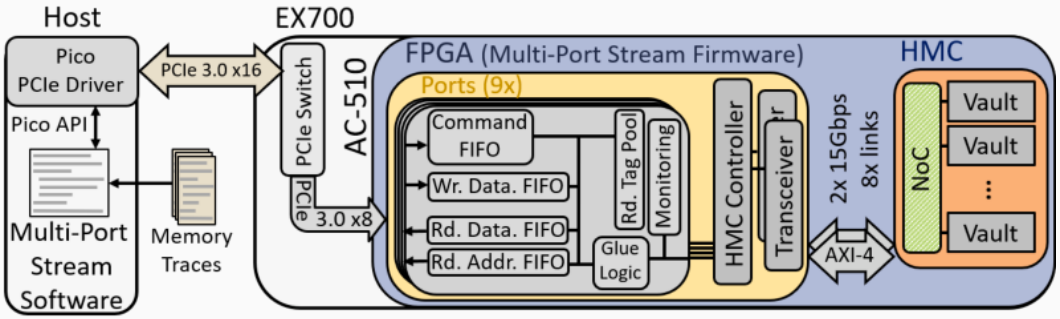
[3] Hein, Eswar, Abdurrahman Yasar, Prasanth Chatarasi, Li, Young, Conte, Ümit Çatalyürek, Vuduc, Riedy, Bora Uçar. "Programming Strategies for Irregular Algorithms on the Emu Chick." `https://arxiv.org/abs/1901.02775`

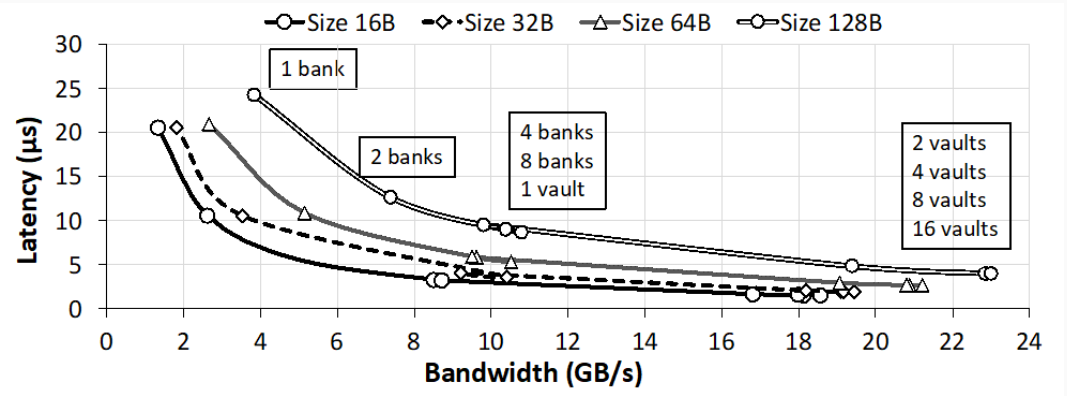
Selected Results: Labeled Subgraph Alignment



GSANA, the first parallel algorithm, strong scaling on DBLP graph (2048 vertices)[3]

Selected Results: FPGAs





Hadidi, Asgari, Young, Mudassar, Garg, Krishna, Kim. "Performance Implications of NoCs on 3D-Stacked Memories: Insights from the Hybrid Memory Cube (HMC)," ISPASS 2018

- Characterizations with FPGA and Hybrid Memory Cube show latency/bandwidth tradeoff.
- Other FPGA work is focused on compilers, HPC prototyping, and sparse algorithms for Intel and Xilinx FPGAS.

Lessons Learned, Emu Chick i

- Finding appropriate metrics is difficult, *e.g.* for the Emu:
  - Comparing ASICs (*e.g.* x86) to FPGA-based prototypes can be unfair either way.
  - Fraction of peak bandwidth for the *idealized* problem?
  - SpMV: FLOP/s $\propto$ BW, level 2 sparse BLAS op.
  - Graph500 BFS: TEPS $\propto$ BW

Lessons Learned, Emu Chick ii

- Distilling observations on architecture $\leftrightarrow$ programming model:
  - Program data location for load (BW) balance.
  - Remote memory operations v. migration exposes the architecture.
  - Migrations cost more than it appears. Computation?
  - Stack spills/access can cause ping-ponging.
  - How does HW support for top-down (Cilk-ish) affect bottom-up (UPC/SHMEM) PGAS programming?
    - Memory allocation similar to UPC, SHMEM
    - UPC++ `rpc_ff` v. Emu thread migration?

Acknowledgments

Fantastic students and colleagues:

- Srinivas Eswar (GT CSE)
- Dr. Eric Hein (GT ECE ⇒ Emu)
- Patrick Lavin (GT CSE)
- Dr. Jiajia Li (GT CSE ⇒ PNNL)
- Abdurrahman Yaşar (GT CSE)
- Dr. Ümit Çatalürek (GT CSE)
- Dr. Tom Conte (GT CS/ECE)
- Dr. Bora Uçar (ENS Lyon CNRS)
- Dr. Rich Vuduc (GT CSE)
- Dr. Jeffrey S. Young (GT CS)

Code (ideally will have links from `crnch.gatech.edu`):

- `https://gitlab.com/crnch-rg` (soon)
- `https://github.com/ehein6/emu-microbench`

Other testbeds:

- ORNL: ExCL
- PNNL: CENATE
- Argonne
- Sandia
- Berkeley: AQCT
- (others?)

Rogues Gallery: Active and Growing

- Added FPGA resources, integrating FPAAs
- Tight development loop with Emu
- Active research projects and publications
- Community outreach and education underway
- One GT student has made the leap to industry already...

CRNCH Rogues Gallery connects researchers *and students* with novel architectures and architects with upcoming applications.

Let us host / manage your neat stuff!

`http://crnch.gatech.edu/rogues-gallery`