The Rogues Gallery: A Novel Architecture Testbed

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Georgia Tech

The Rogues Gallery

The Rogues Gallery is a ***disaggregated testbed*** *consisting of hardware, VMs, and services hosted across 3 GT buildings*.

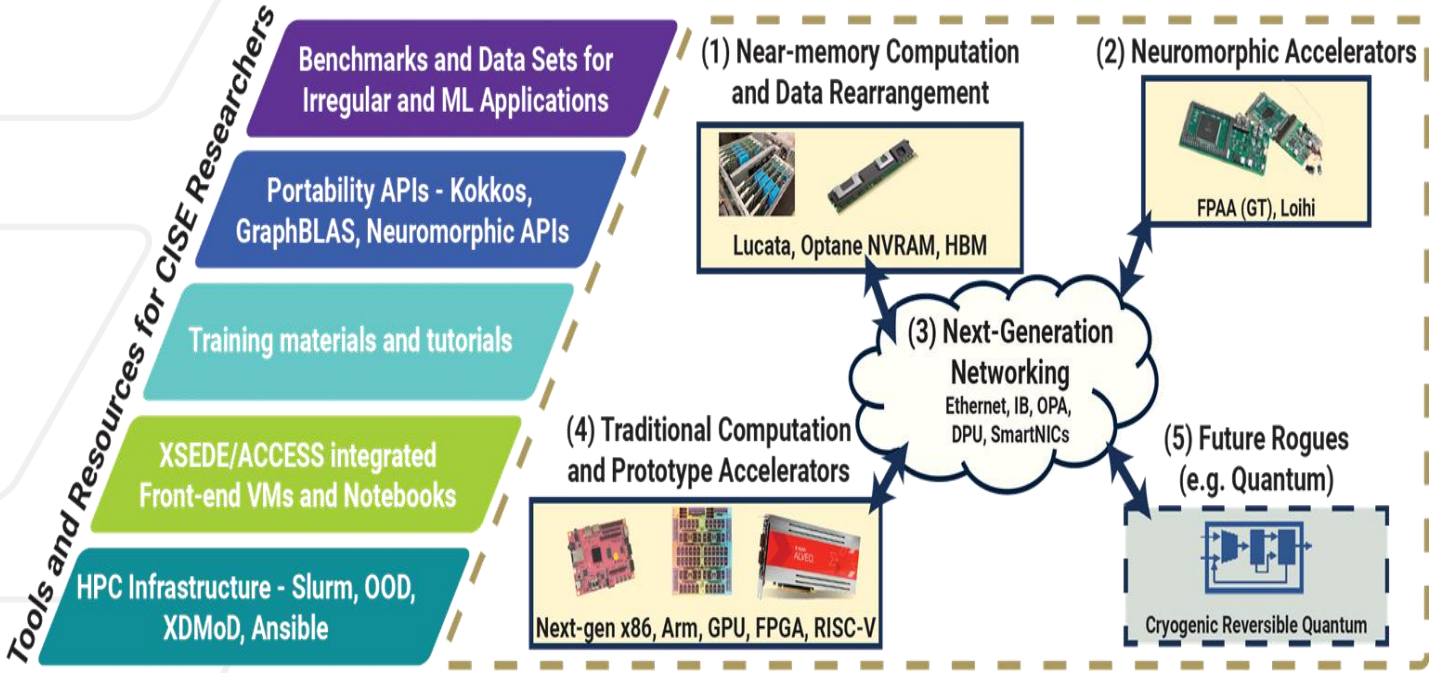
The Rogues Gallery an NSF funded post-Moore testbed for CISE researchers and the community.

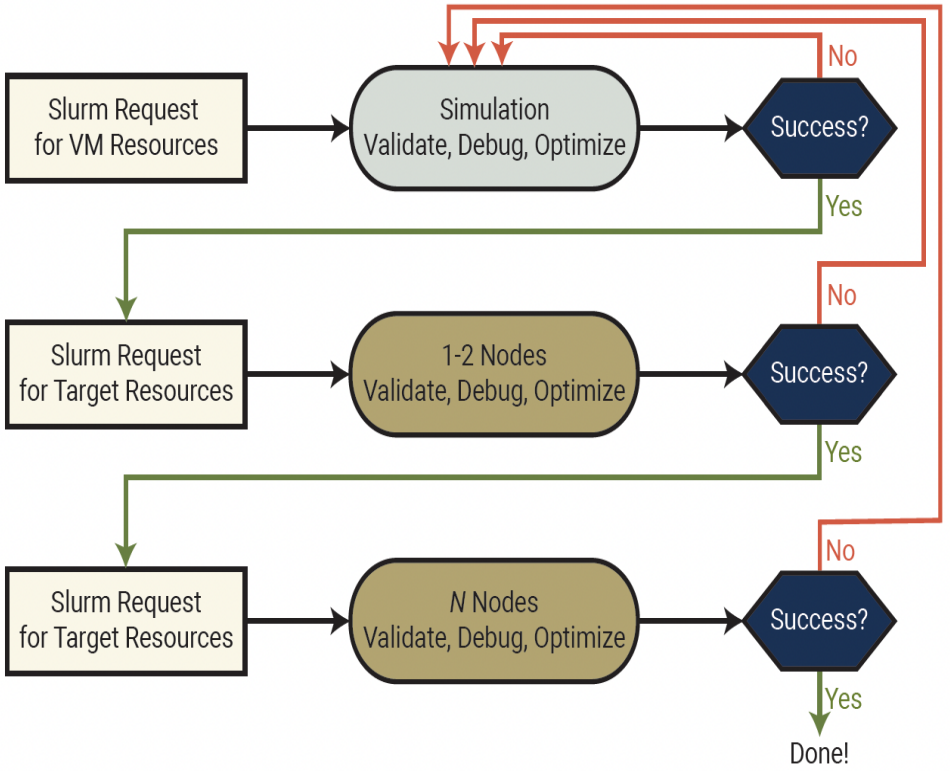
CNS-2016701, $1.3M over 3 years

- Supports deploying:
  - Rack-scale Lucata Pathfinder 32 node system
  - Neuromorphic accelerators
  - Smart networking and 5G equipment
  - Backend infrastructure

This grant focuses on ***community engagement and post-Moore training***

The Rogues Gallery

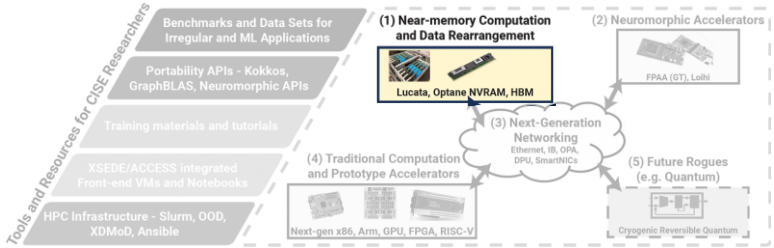




Typical Rogues Gallery workflow for users

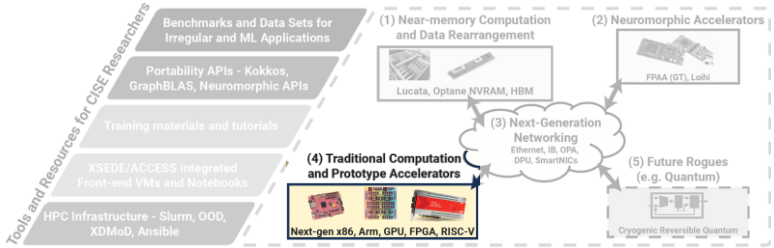
Near-Memory

- 4-chassis Lucata Pathfinder system
  - 8 nodes per chassis, 24 cores per node = 768 total cores
  - Cilk-based workflow and Lucata-specific APIs and tools
  - High-efficiency for sparse data operations via HW-thread migration (on the Graph500 and Green Graph500)
- 4 Intel ICX systems with Optane DCPMM
  - Configurable for DRAM/Optane mixed workloads
- A64FX, x86 systems with HBM
  - Novel HPC architectures providing high-bandwidth memory to the main processor



Reconfigurable

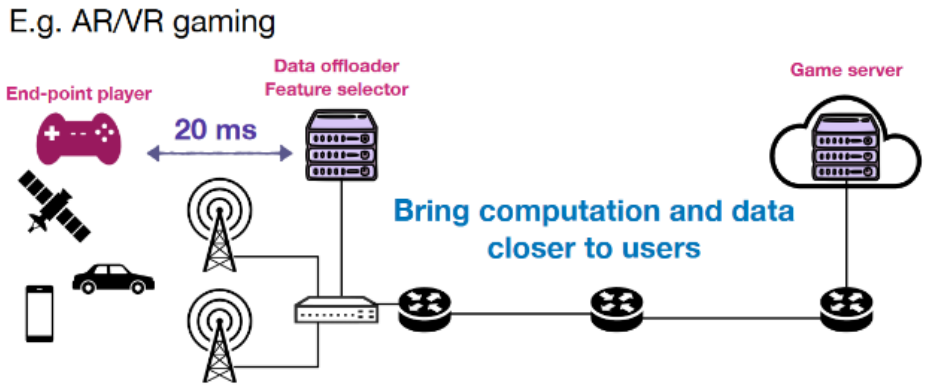
- Collection of datacenter FPGAs
  - Xilinx Alveo U50/U250/U280
  - Intel Arria10 PAC, Stratix 10 PAC, Bittware 385/520N/840F
- Xilinx SmartSSD
  - Used to accelerate storage-oriented workloads
- Pynq Cluster
  - 76x Pynq-Z2 SoC for education (CS3220, ECE8893, RG VIP)
  - Conservatively saves students ~$10k/semester

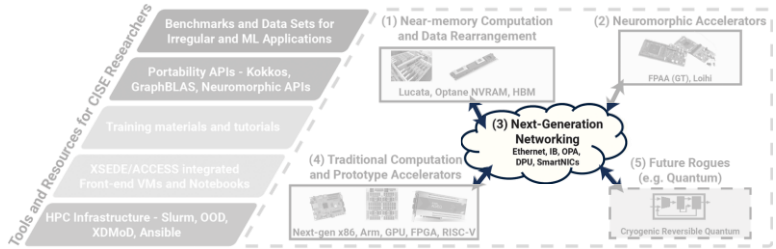


Young J, Jezghani A, Valdez J, Jijina S, Liu X, Weiner MD, Powell W, Sarajlic S. Enhancing HPC Education and Workflows with Novel Computing Architectures. Journal of Computational Science. 2022;13(2). https://doi.org/10.22369/issn.2153-4136/13/2/6

Next-Gen Networking

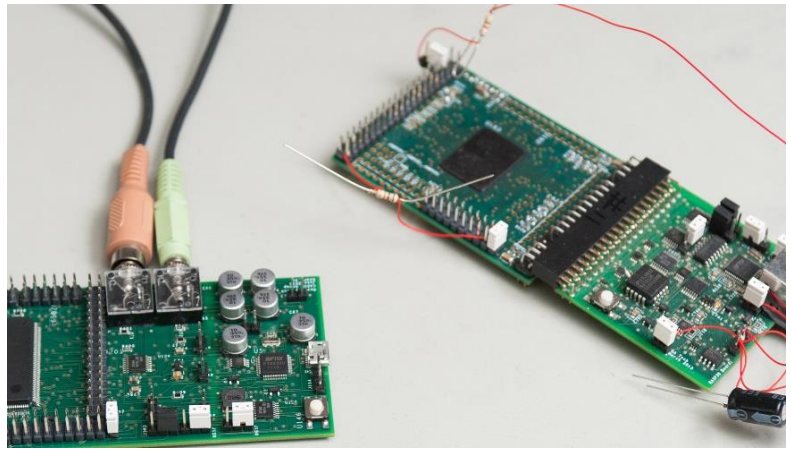
- Focus on “smart” networking with SmartNICs like NVIDIA Bluefield, InnovaFlex, and FPGA-based NICs
- Other NSF-funded testbeds are more focused on 5G efforts
  - However, CRNCH RG may host some hardware for 5G software stack development

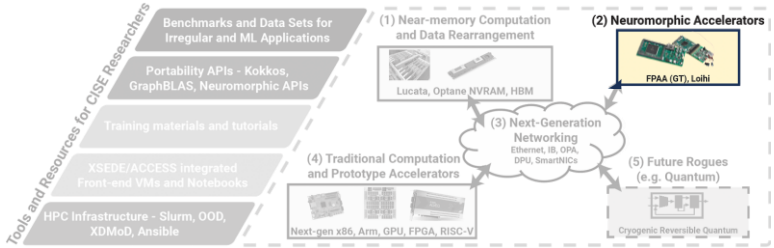




Neuromorphic Accelerators

- The FPAA provides a mixed analog/digital design platform with open-source tooling for low-power neuromorphic exploration
  - Next generation of FPAA anticipated to be deployed in Summer 2023
  - Development is proceeding for a “large-scale” Field Programmable Analog Array (FPAA) based on designs by Dr. Jennifer Hasler’s group
- Neuromorphic software exploration of SNN-based designs is supported via Nengo and Lava, Intel’s Loihi-targeted framework.

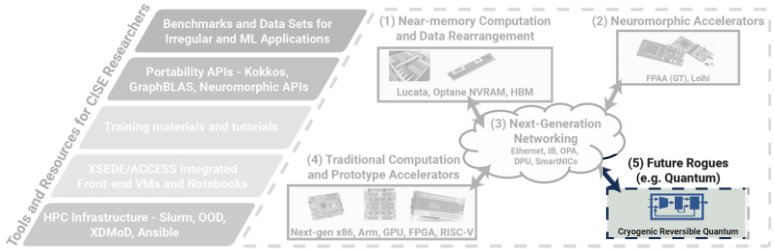




Learn more about FPAAs: Jennifer Hasler, “Large-Scale Field-Programmable Analog Arrays”, Proceedings of IEEE 2020

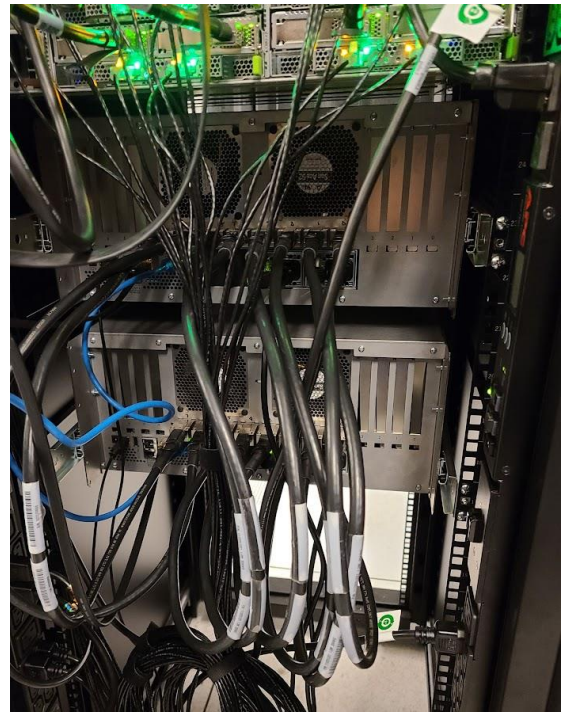
Quantum Computing

- Currently, no hardware as part of RG
  - Ongoing collaborations with Georgia Tech Research Insitute (GTRI) using their local ion-trap system
- Efforts largely focused on supporting simulation and cloud
  - cuQuantum in Apptainer workflow on A100 GPUs designed to scale on Phoenix
  - Libraries and documentation provided for supporting use of IBM Qiskit



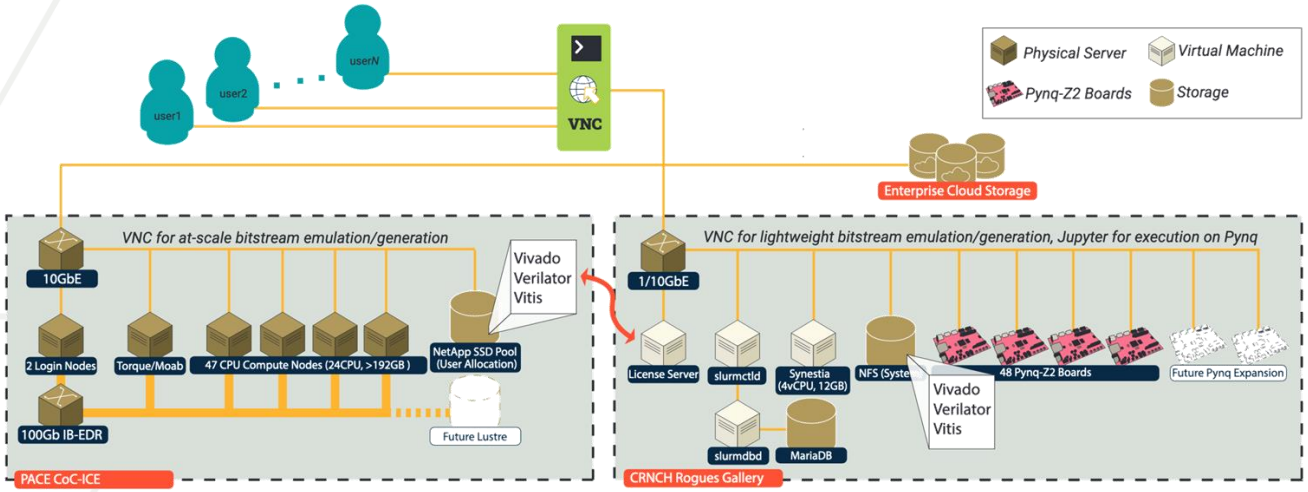
Network and Storage

- 2 fileservers for backed up home directories and fast NVMe scratch storage
  - Supported via traditional tools like NFS, autofs, with SSSD/LDAP authentication
- All servers connected via 10 GbE
  - Many connected via 40 GbE switch
  - InfiniBand EDR for A64FX
  - OmniPath 100 Gb for Ice Lake mini-cluster



Slurm and Open OnDemand

- Slurm scheduling across most resources
  - Interesting challenges with “edge device” integration
  - Currently working on migration to 23.02.x for new features
- Open OnDemand support to ease entry

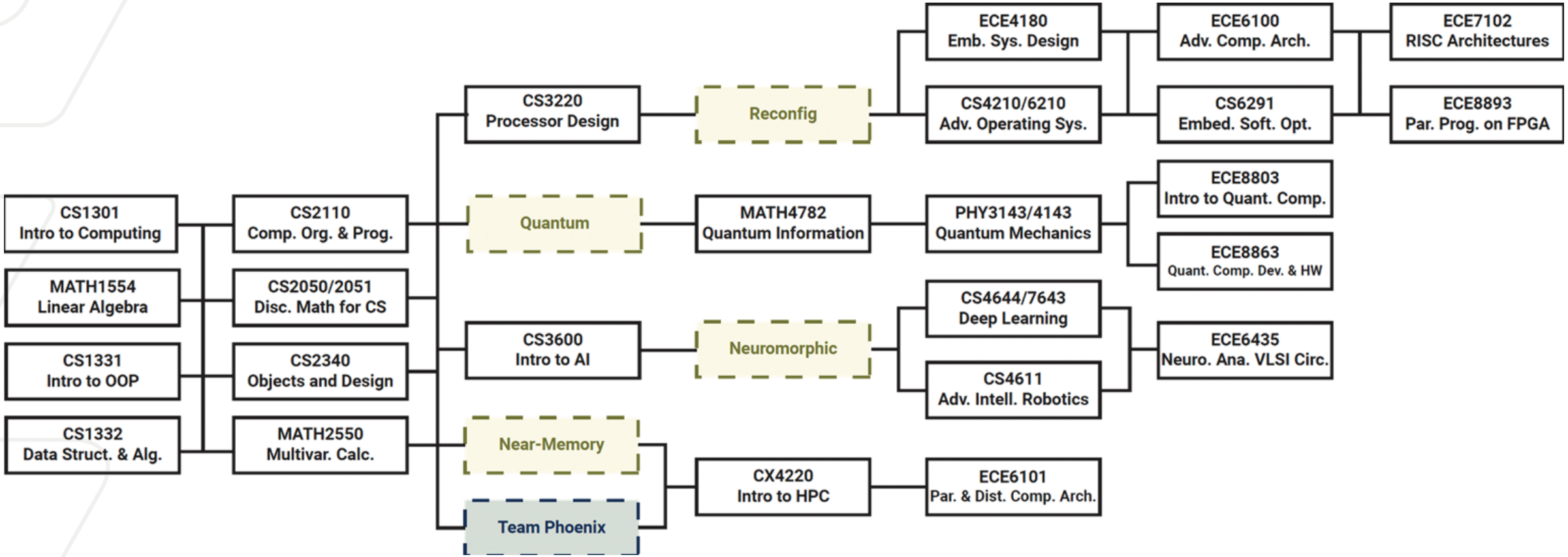


Jezghani A, Manalo K, Powell W, Valdez J, Young, J. Onboarding Users to A64FX via Open OnDemand. International Conference on High Performance Computing in Asia-Pacific Region Workshops. 2022; 78-83. https://doi.org/10.1145/3503470.3503479

Future Computing with the Rogues Gallery

- The Vertically Integrated Projects (VIP) Program has been active since the 1990s, with a focus on:
  - Multidisciplinary team composition, bringing students from across campus
  - Vertically integrated, including a range of undergrad & graduate ranks
  - Large-scale, with teams of at least 10 students
  - Long-term, encouraging students to participate for at least 3 semesters
- Georgia Tech hosts 80 VIP teams
  - 40 institutions world-wide are part of the larger VIP consortium
- The Rogues Gallery VIP was started in Fall 2019 semester as a venue for students to explore FPGAs, near-memory compute, and HPC architectures
  - 4 subteams: Near-memory, Reconfigurable, Neuromorphic, Quantum

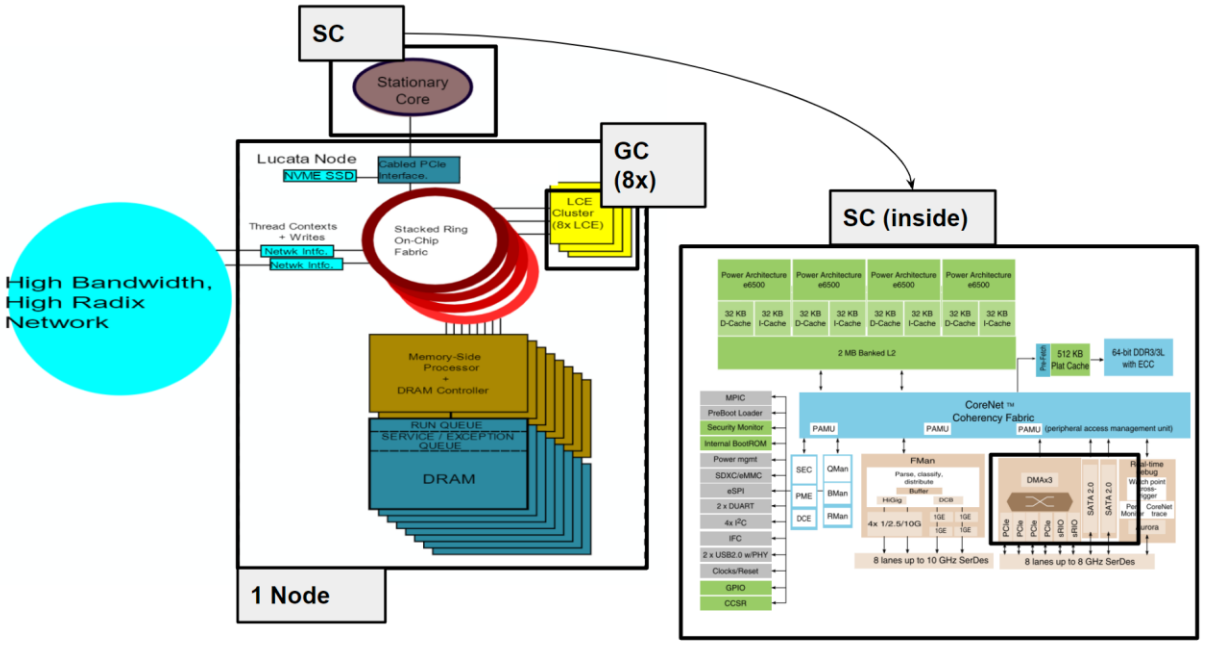
Filling the “Missing Middle”



Check out our paper on the CRNCH RG VIP class in EduPar 2023: https://bit.ly/3Z3ZbYy

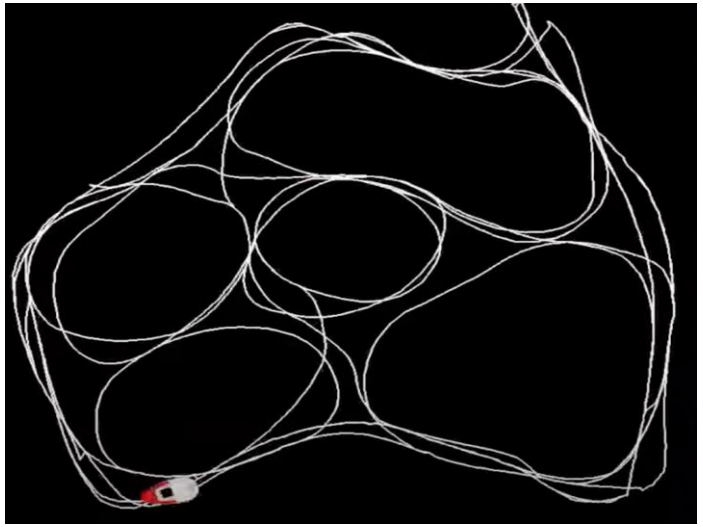
Near-Memory and the Lucata Pathfinder

- Use Cilk to program algorithms related to graph and sparse data analytics
- Explore traditional benchmarks like pointer chase, hpcg, BFS, etc.
- Implement DMA FIFO in compute nodes for improved memory throughput



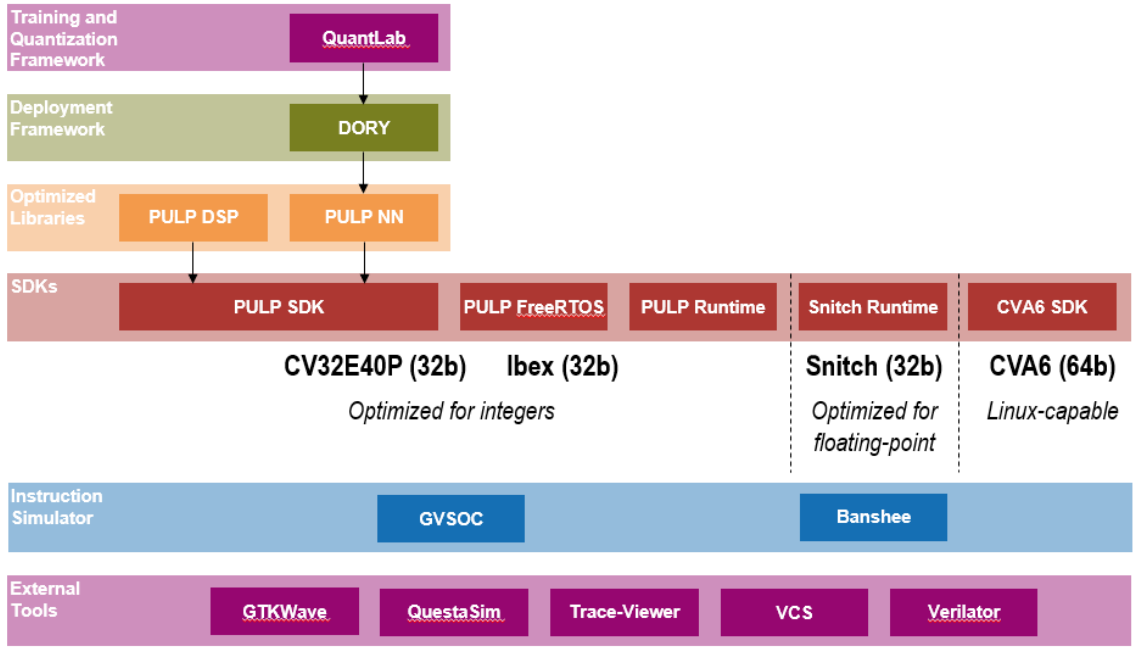
Neuromorphic and SNNs

- Focused on multiple projects related to Simultaneous Location and Mapping (SLAM)
  - Focus on rodent-inspired RatSLAM
- “NeuroCar” is working on a spiking neural network (SNN) for an autonomous racecar
- Introduce students via Nengo framework for simple SNN maze navigation, as well as OpenAI Gym problems
- Also exploring Lava for implementing SNNs on Intel Loihi



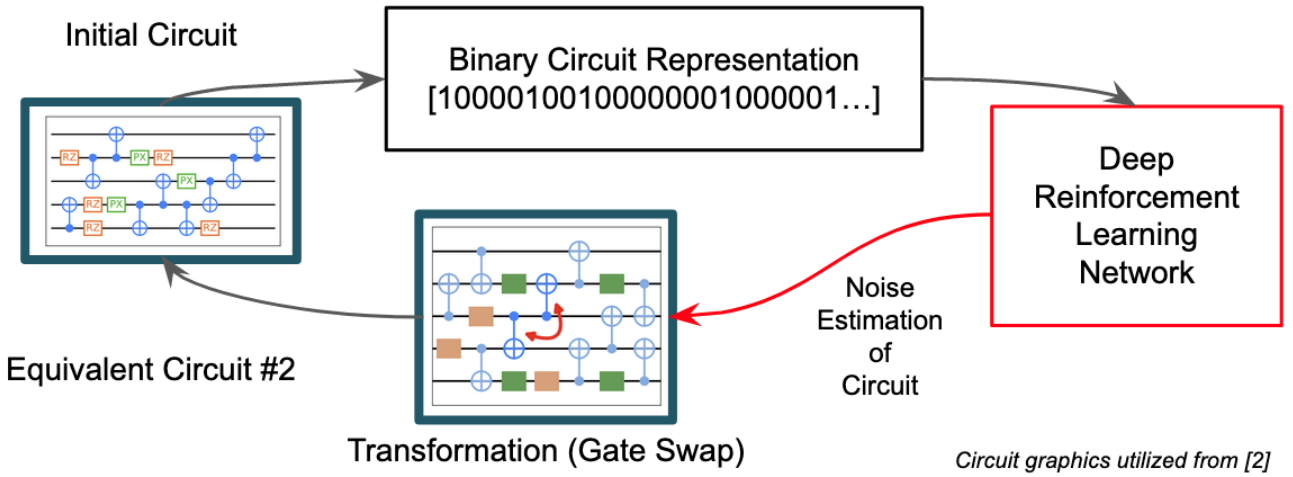
Reconfigurable and RISC-V

- Work in high-level language like Chisel or frameworks like Vitis HLS
- Leverage publicly available RISC-V design such as Chipyard and PULP projects
- Develop NN on Xilinx FPGAs for efficient drone navigation controller



Quantum and Simulation

- Onboard by learning concepts through Nielsen and Chuang, Qiskit docs
- Investigate ML to reduce noise in quantum circuits
- Run accelerated simulation using Nvidia's cuQuantum



Impact Summary

- Template for novel testbed replication
  - Frequent(-ish) publications, talks detailing lessons learned, workflows, etc.
  - Documentation and tutorial content in public repos
- Growing user base
  - 250-300 users (typ. 20-50 active daily), with 15-20% external
  - ~150 students/semester
- Numerous Tutorials/Workshops
  - HPEC, PEARC, ASPLOS, MICRO, Telluride, Hot Interconnects, DAC

Any US-based researcher can apply for access to CRNCH RG via our website at crnch-rg.cc.gatech.edu

Future Work

- Finalize some of the "edge device" infrastructure pieces
  - Better scheduling support for FPGAs and SmartNICs/BFs
- Improved documentation and software support
  - Looking to crowd-source documentation and containerized software
    - Existing documentation at https://gt-crnch-rg.readthedocs.io
  - Integration of custom hardware scripts as APIs for Slurm plugins
- Further democratization of resources
  - Overcome personnel limitations, develop additional training, and establish workflows (e.g. gateways)

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