Facilitating Instruction on Exotic Architectures

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NSF ACCESS All Champions Meeting
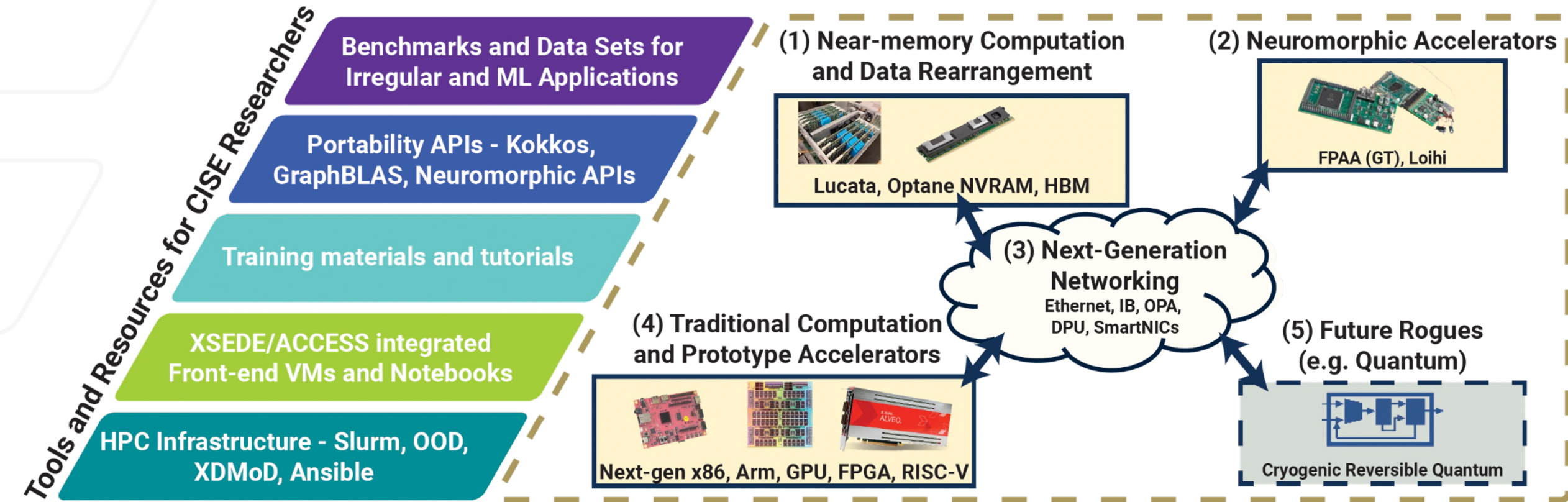
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The Rogues Gallery

The Rogues Gallery an NSF funded post-Moore testbed for CISE researchers and the community.
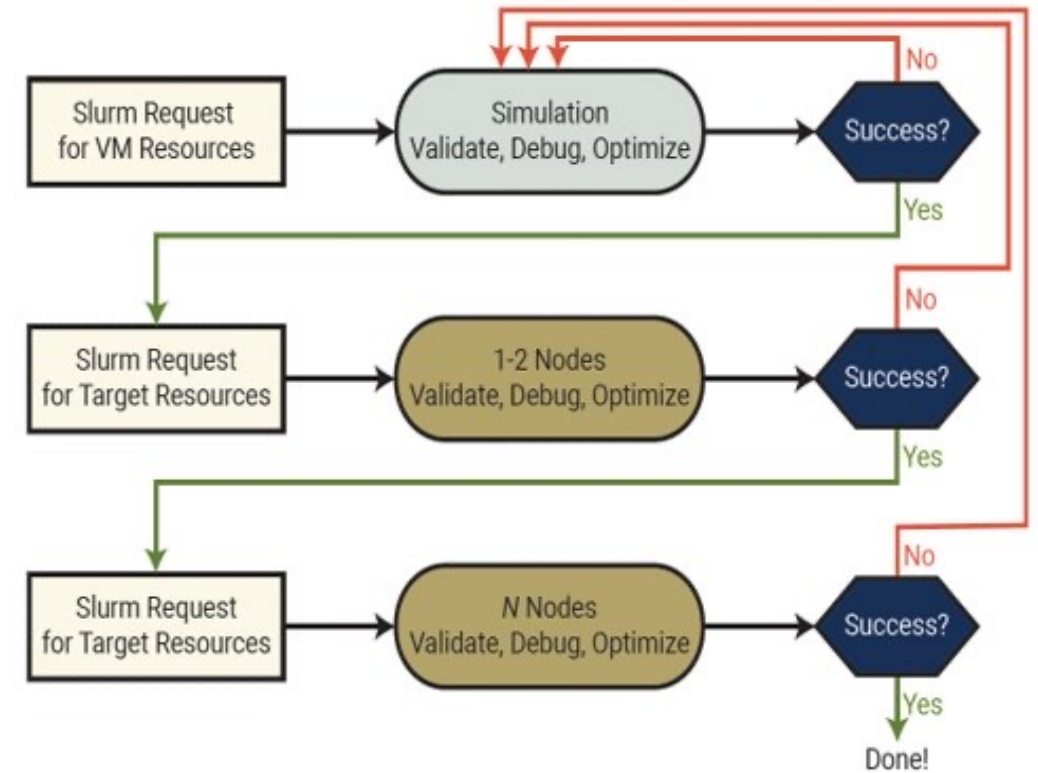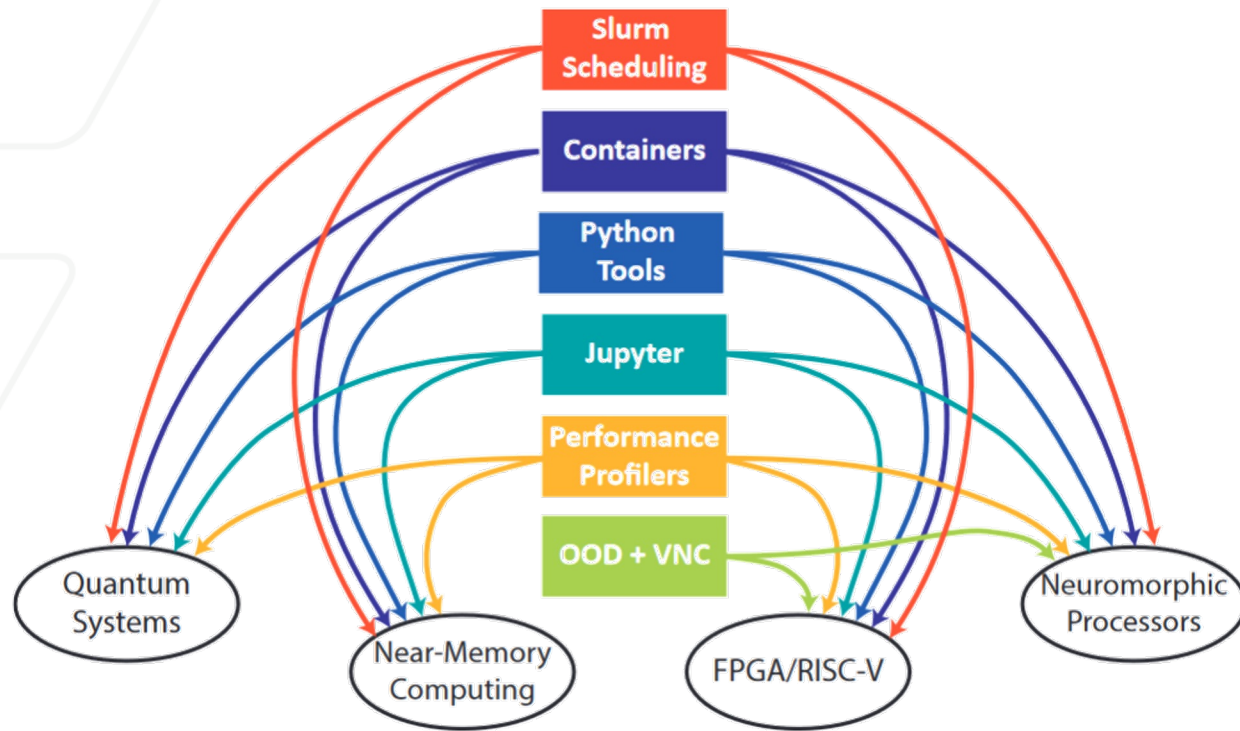
CNS-2016701, $1.3M over 3 years

- Supports deploying:
  - Rack-scale Lucata Pathfinder 32 node system
  - Neuromorphic accelerators
  - Smart networking and 5G equipment
  - Backend infrastructure

The Rogues Gallery is a **disaggregated testbed** *consisting of hardware, VMs, and services hosted across 3 GT buildings.*

This grant focuses on **community engagement and post-Moore training**

The Rogues Gallery

Tools and Resources for CISE Researchers

- Benchmarks and Data Sets for Irregular and ML Applications
- Portability APIs - Kokkos, GraphBLAS, Neuromorphic APIs
- Training materials and tutorials
- XSEDE/ACCESS integrated Front-end VMs and Notebooks
- HPC Infrastructure - Slurm, OOD, XDMoD, Ansible

(1) Near-memory Computation and Data Rearrangement
Lucata, Optane NVRAM, HBM

(2) Neuromorphic Accelerators
FPAA (GT), Loihi

(3) Next-Generation Networking
Ethernet, IB, OPA, DPU, SmartNICs

(4) Traditional Computation and Prototype Accelerators
Next-gen x86, Arm, GPU, FPGA, RISC-V

(5) Future Rogues (e.g. Quantum)
Cryogenic Reversible Quantum

Managing Workflows for Novel Architectures

The VIP Program at Georgia Tech

- Vertically Integrated Projects (VIP) Program: late 1990s
  - Engage more students in research
- Teams are
  - Multidisciplinary (e.g. CS, ECE, physics)
  - Span student classifications (sophomore -> graduate)
  - Large-scale (>10 students)
- Projects are meant to be long-term
  - 3 semesters, 6 credits total (1, 2, 3 credits/semester)
  - Increasing leadership and technical ownership
- GT hosts more than 80 teams
  - 40 institutions world-wide form the VIP consortium

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Future Computing with the Rogues Gallery VIP

- Started in Fall 2019
  - Drs. Jeffrey Young and Jason Riedy

- Vision focused on hardware on hand
  - Flagship "Emu Chick" for near-memory compute
  - Prototype FPGAs
  - Emerging HPC hardware (A64FX, Skylake, Epyc)

- Initial team comprised of 9 students
  - Big surprise was ask to explore quantum hw/sw -> new subteam created accordingly!

- Today we have 35 students/semester + a waitlist

Today's Future Computing VIP

- Near-memory subteam
  - Focus on high-level frameworks (Cilk, GraphBLAS, etc.) and API calls
  - Micro benchmarks (pointer chase), macro benchmarks (BFS, hpcg)

- Quantum subteam
  - AI-driven circuit design
  - Train model based on Qiskit results -> simulate w/cuQuantum -> dispatch generated circuit

- Reconfigurable subteam
  - RISC-V architectures for specialized, efficient accelerators
  - Chisel/Chipyard + Vivado toolchain

- Neuromorphic subteam
  - Previously focused on SNNs for autonomous RC car navigating track
 - Extending to OpenAI Gym problems, targeting Lava + Loihi dispatch

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Critical Infrastructure for Success

- Presenting "funky" in a way that looks like "enterprise"
  - Slurm managed compute resources
  - Open OnDemand for interactive sessions
  - Lmod software stack
  - Apptainer containers for portability and simplicity
  - NFS mounts
- Abstracting complexity
  - 11 Slurm builds across 5 OSes!
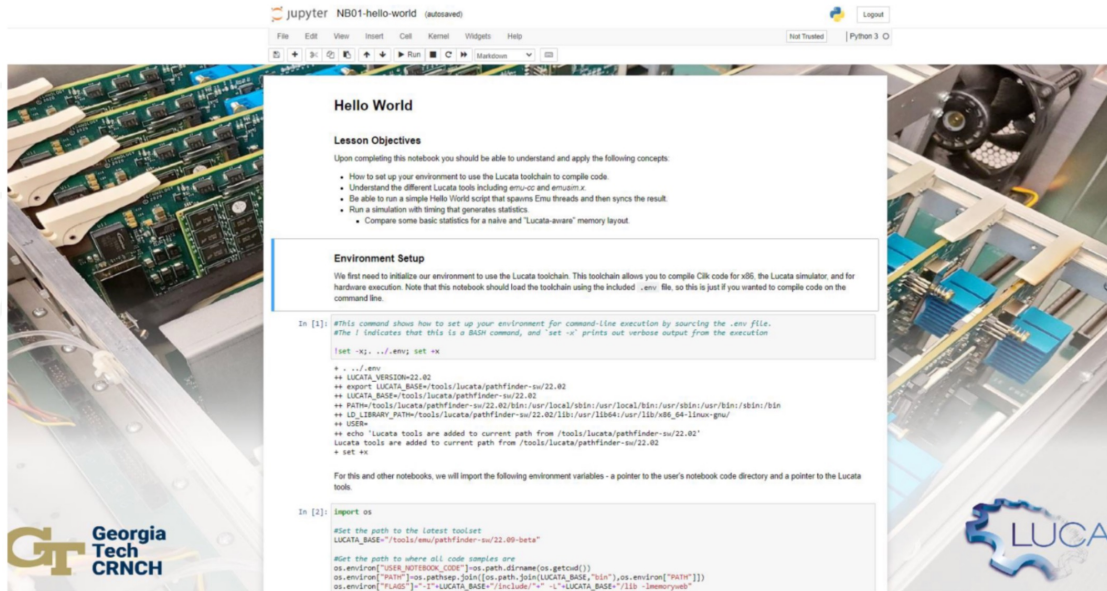
Designing Curriculum to Foster Growth

- Student onboarding a big focus given vertical component of classes
  - Weekly how-to sessions focused on fundamentals, with increasing complexity
  - SSH -> git -> Slurm jobs -> Python environments -> Distributed workflows -> Containers
- Subteams develop documentation and examples to facilitate knowledge share
  - Hosted in central repo
- Weekly notebook entries to encapsulate work
  - Contributions, developments
  - Blockers
  - Links to documentation

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Leveraging Knowledge to Provide PYNQ Capacity

- Curriculum change and supply change issues introduced new demand
  - CS3220: Processor Design required for all threads (100+ students/semester)
  - Additionally, ECE8893 FPGA Special Topics
  - Campus bookstore unable to stock sufficient FPGA development boards to meet need

- Used TechFee funds to procure 60 boards, set up Slurm-managed cluster
  - OOD VNC session on development VMs for Xilinx tools and overlay development, Jupyter for PYNQ

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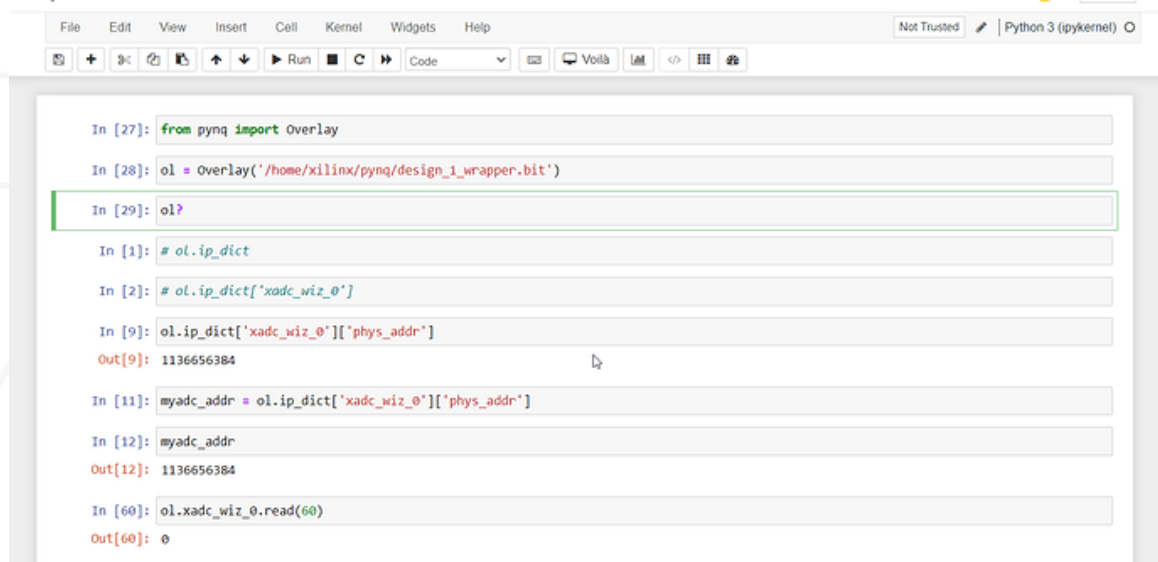
Hacking to a Functional Solution

- PYNQ boards are inherently designed for running python via Jupyter
  - Direct login as root
  - Notebooks, overlays expected to be in root-owned path
- Open OnDemand follows typical Jupyter job, with minor tweaks
  - /etc/sudoers includes a line allowing launch of jupyter lab with privilege
  - Prolog symlinks user's home directory into expected location

Scaling out to Central Infrastructure

- PACE resources (Phoenix and ICE) provide more capacity and capability, so as problems outgrow RG, extend workflows accordingly
  - Xilinx libraries on ICE for FPGA development
  - Chisel/Chipyard workflows on Phoenix
  - CuQuantum containers and support

Students Like Familiarity

- Like to work on laptops
  - Need encouragement to adopt cluster hardware
- Expectations like root access
  - Learning Python virtual environments, etc.
- Many of same challenges in regular clusters

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Emerging Companies bring Growing Pains

- Emu chick -> Lucata Pathfinder transition
  - New architecture, scale, APIs

- Constantly evolving libraries
  - Often, semester to semester the standard would change and require time to rework existing code

- Sharing time with vendor engineers
  - Sharing prototype/development and "production" environments caused headaches
  - Lack of privilege for students meant pokes for support

...Including Disappearing

- Lucata recently announced that the company was being dissolved
  - No more engineering support for an *extremely* exotic system
- Taking the opportunity to encourage final publication of work/experience (PEARC?)
- Looking to the next project
  - A64FX, SPR-Max, GH100 all share near-memory concept
  - Can look to existing workflows on new architectures (with better support)

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In Summary

- For 5 years, we have supported Future Computing VIP
  - Seen significant growth
- We've extended efforts for other core curriculum
  - 120+ students/semester on PYNQ cluster - $10k/semester in savings
- Continuing to add support for more exotic HW at GT!