

Optimizing the “Last Mile” with Network-Compute Co-Design

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CNRCH Summit, January 29th 2021

Large-Scale Online Services

Online services live in massive datacenters

- 10,000s of servers

Tight quality guarantees (SLOs)

- Care about “worst-case” (tail) latency



Data distributed across thousands of servers

Servers communicate over datacenter network

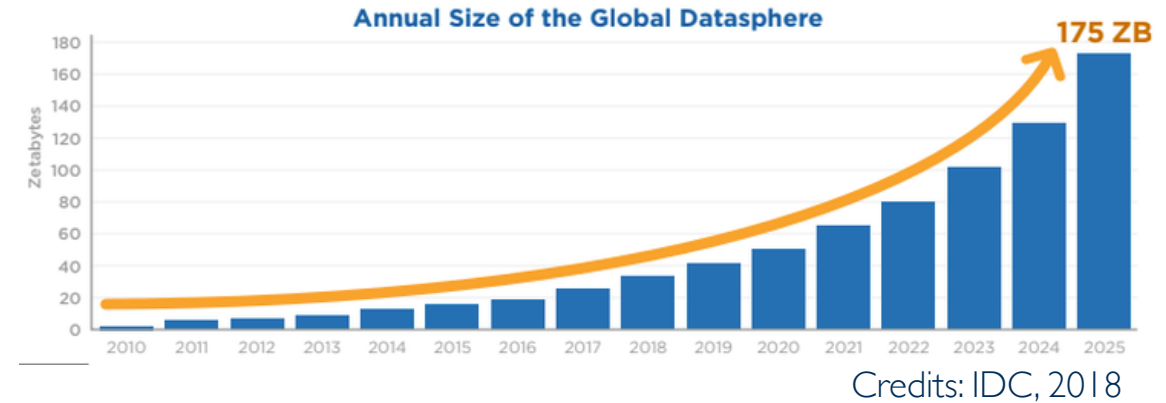


Distribution enables scalable performance & low response latency

Growing Pressure on the Network

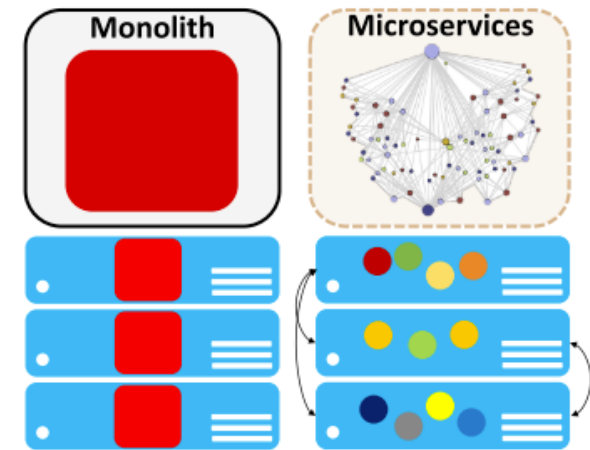
Trend I: More data → more scale-out

- 66% growth per year



Trend II: Software decomposition (microservices, serverless)

- Service times in μ s domain
→ network message every few k CPU cycles!



Credits: Gan, ASPLOS'19

Network emerging as key performance determinant

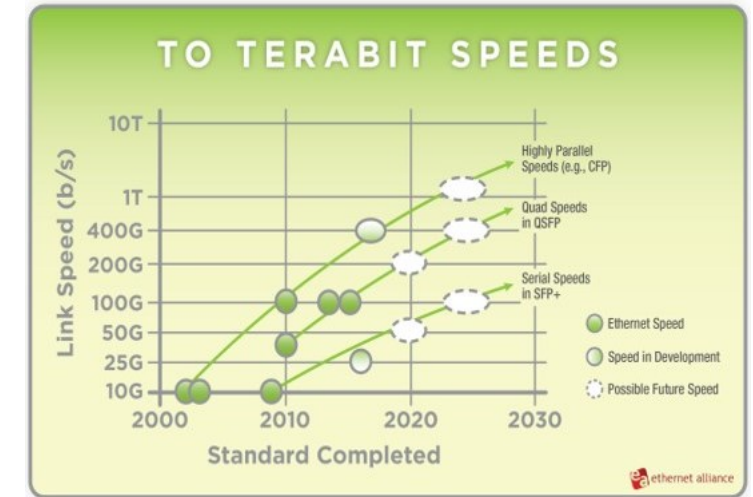
Datacenters Keeping up with Growing Demand

Growing bandwidth & high path diversity

- Datacenter-wide roundtrips $< 20\mu\text{s}$

Optimized protocols cut messaging costs

- From $10+\mu\text{s}$ to sub- μs



Credits: Ethernet Alliance, 2015

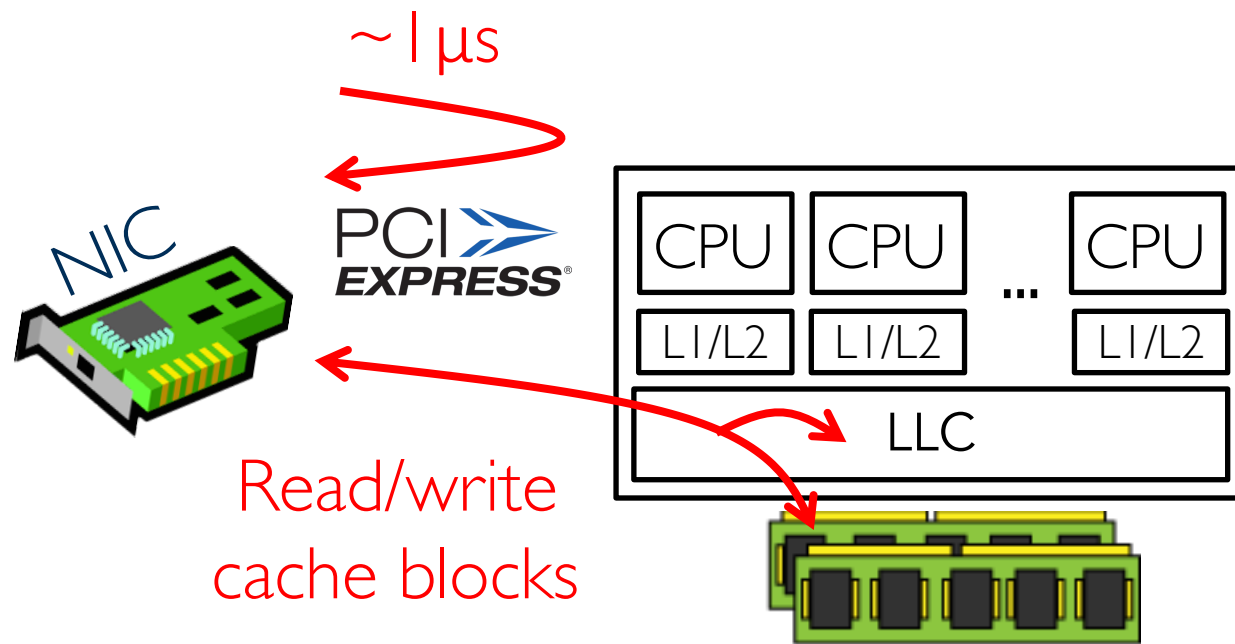
...despite networking evolution, NIC-CPU interface still architected as IO

- Bandwidth-optimized, high latency
- Performance and semantic obstacles

PCI
EXPRESS

Need architectural revisiting of “last mile”

What's Wrong in this “Last Mile”?



Need

- New interfaces
- Richer operations
- Advanced interactions with compute & memory

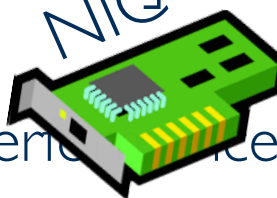
Making the NIC a First-Class Citizen

Optimize Network-Compute interface via NIC integration

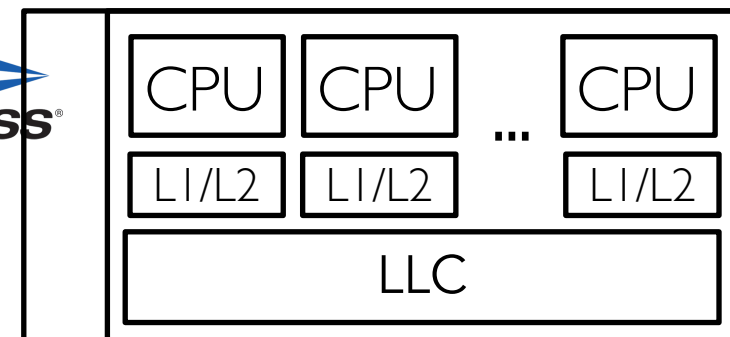
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| New Interfaces |
| Richer Operations |
| Advanced Interactions |

Scale-Out NUMA architecture [ASPLOS'14]

- NIC in coherence domain
- Rack-scale scale-out systems w/ NUMA per node: remote memory within $\sim 3x$ of local



PCI
EXPRESS



More than immediate latency gains

- Paves way for higher-level operations with richer semantics

Integration facilitates network-compute co-design

From Cache Blocks to Memory Objects

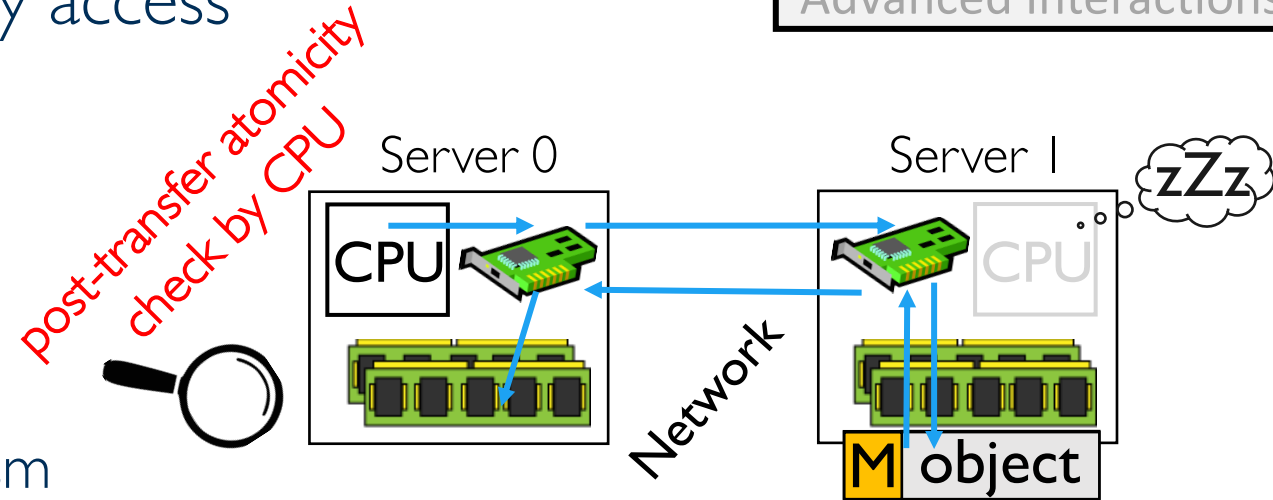
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RDMA enables direct remote memory access

- Great for distributed object stores

No object-level atomicity guarantees with basic "read" primitive!

- Need out-of-band verification mechanism



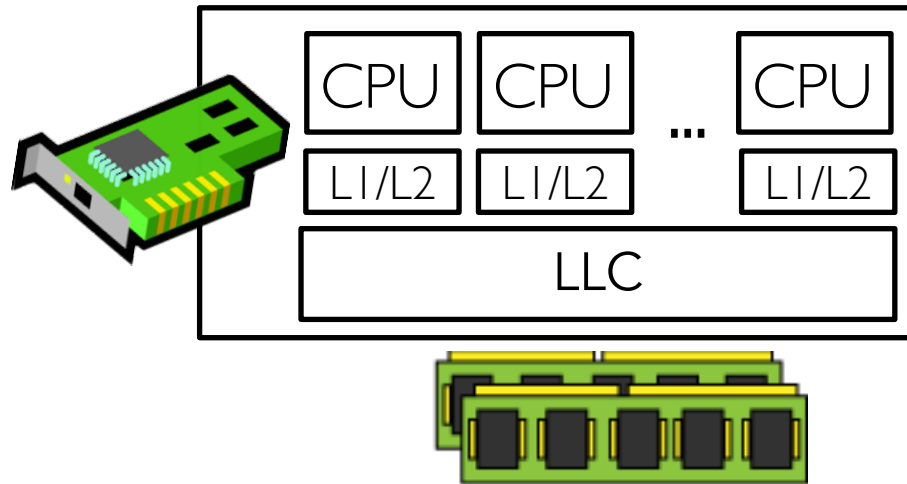
NIC in coherence domain → snoop coherence traffic to target object [MICRO'16]

- On-the-fly atomicity check, no software involvement
- 35-50% faster atomic object reads from remote memory

Tight NIC-compute coupling enables Atomic Object Read hardware primitive

NIC-driven Load Balancing Opportunities

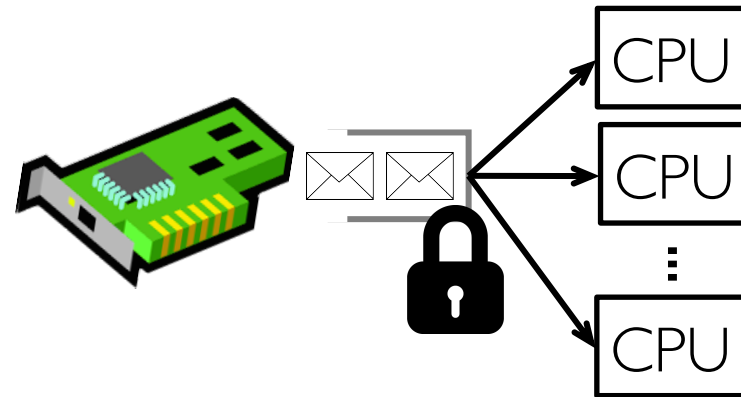
Packet distribution to cores critical for scalability



NIC-driven Load Balancing Opportunities

Packet distribution to cores critical for scalability

- Software-based mechanisms expensive for μ s-scale services



NIC-driven Load Balancing Opportunities

New Interfaces

Richer Operations

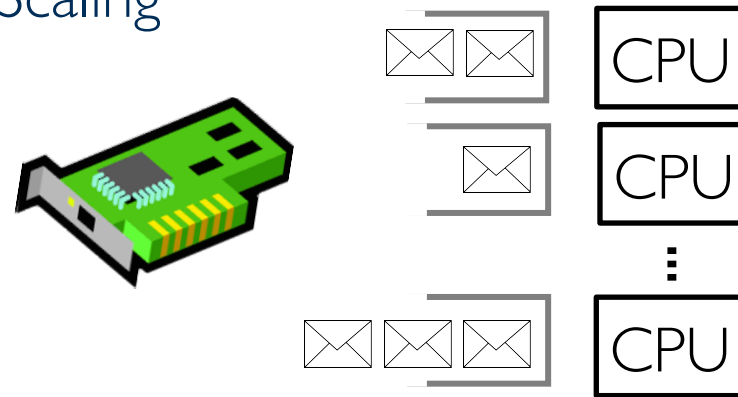
Advanced Interactions

Packet distribution to cores critical for scalability

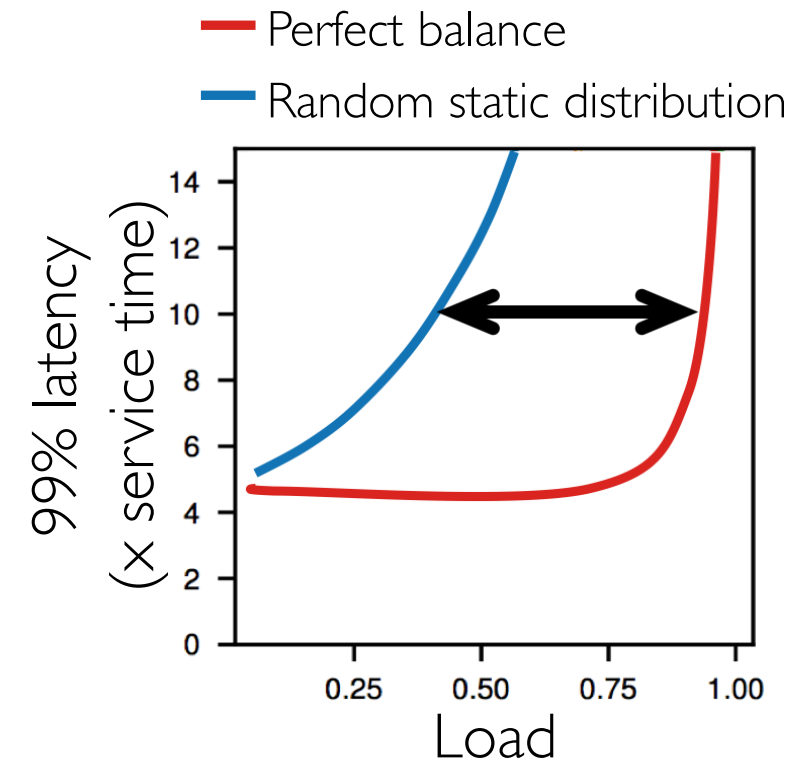
- Software-based mechanisms expensive for μ s-scale services

NIC can spread incoming load to cores

- e.g., Receive-Side Scaling



But static decisions \rightarrow load imbalance \rightarrow hurts tail latency



Integration Facilitates Load Balancing

New Interfaces

Richer Operations

Advanced Interactions

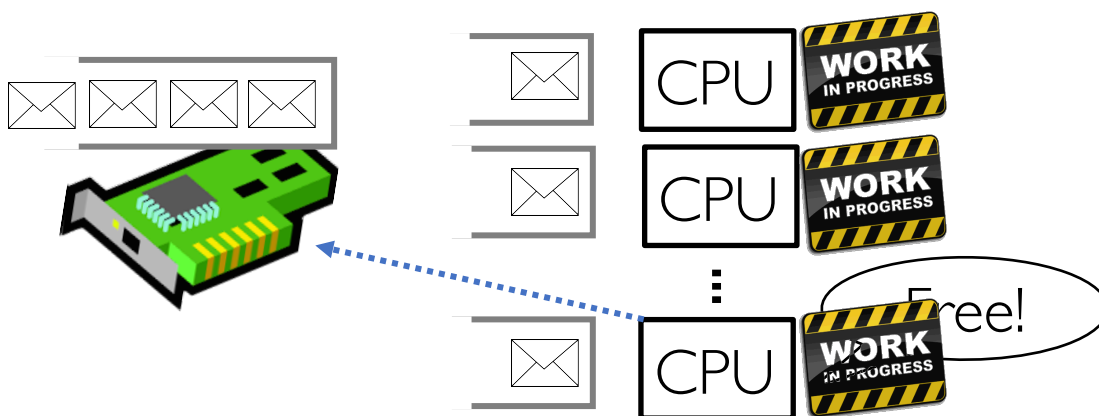
Co-design NIC with compute

- Direct interaction and load monitoring – dispatch work when compute available

[ASPLOS'19]

Simple greedy approach works even for μ s-scale services due to integration

- Nanosecond-scale on-chip latencies

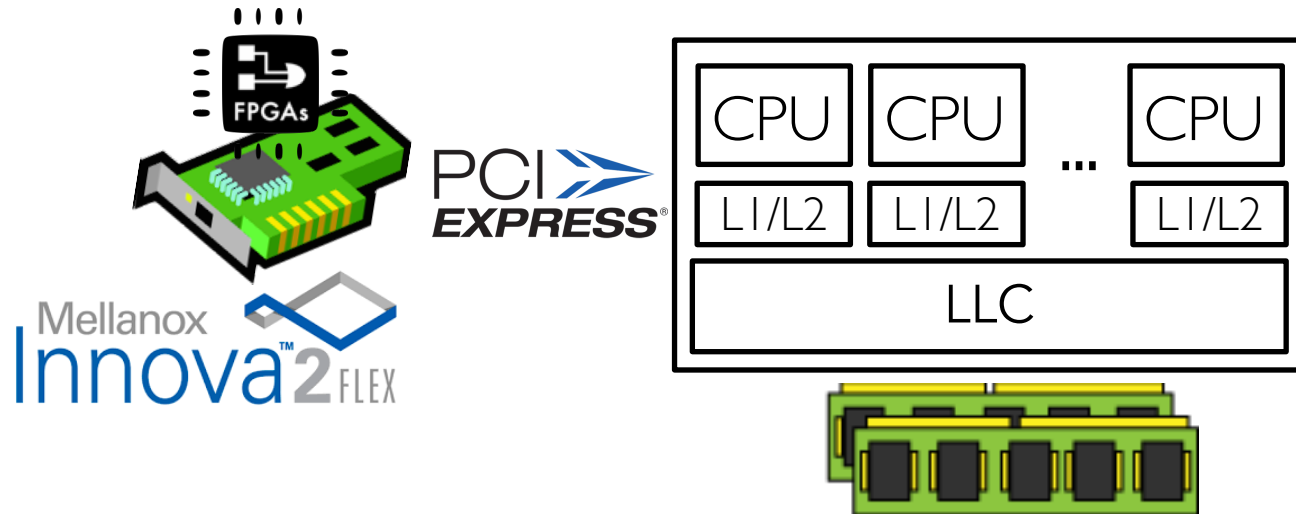


20-40% higher throughput under SLO for μ s-scale services

NIC-driven Load Balancing Extensions

Is NIC-driven load balancing applicable to existing smartNICs?

- PCIe latency precludes greedy approach
- But can learn and dynamically approximate per-core load



Decisions under workload diversity – can NIC predict service time?

Advanced Interactions via Co-Design

New Interfaces

Richer Operations

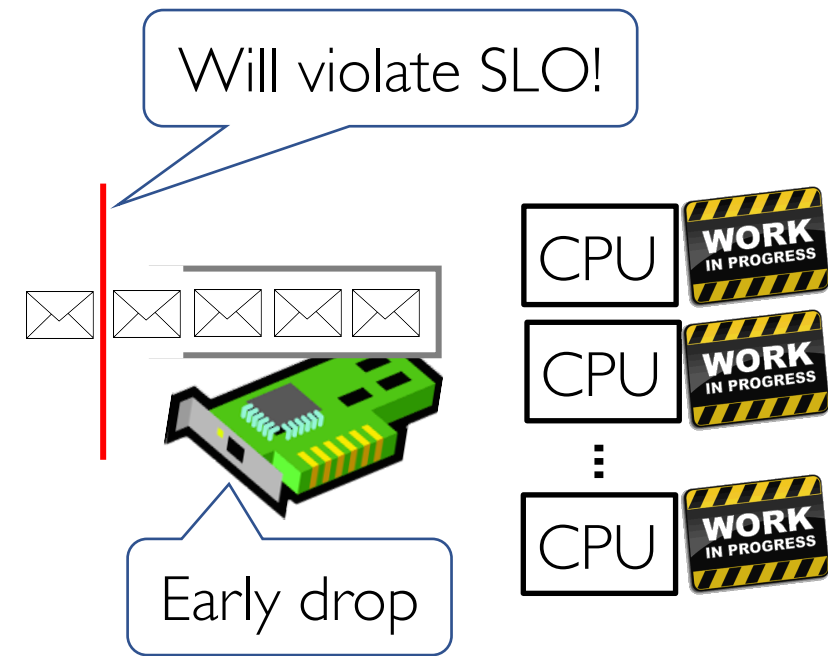
Advanced Interactions

Software hints enable data movement optimizations

Expose application service times and SLO to NIC

Enable SLO-aware packet management [ISCA'20]

- Minimize data movement under high contention
- Prevent spill of latency-sensitive traffic to DRAM



Up to 2x throughput with SLO-aware packet management

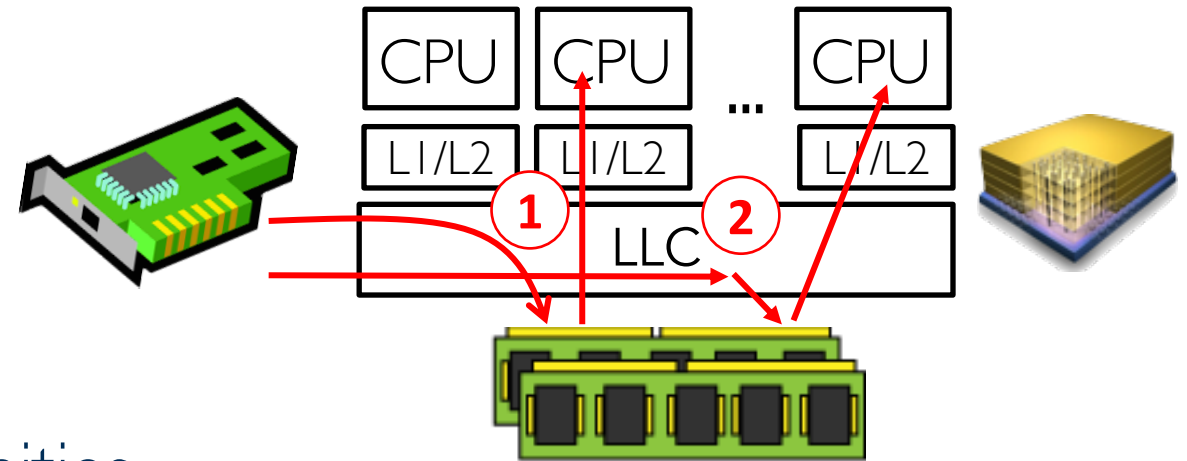
Judicious Data Movement

Incoming data placement policies are static – and suboptimal

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Mainstream approaches:

- ① Data into DRAM
- ② Data into subset of LLC (DDIO)



Data movement optimization opportunities

- Application-driven dynamic placement decision: DRAM, LLC, or private upper-level caches [ISCA'20, CAL'20]
- Even more interesting in heterogeneous, accelerator-rich architectures
- Header/payload splitting and separate manipulation

Ample opportunities in smarter data steering decisions

Conclusion

Evolution of online services puts network communication in spotlight

Advancements in networking technologies and protocols aligned with needs
... but also need architectural rethink for the “last mile”

Optimize network-compute-memory interactions via co-design

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