A Library for Automated Adiabatic Circuit Generation

Gibran Essa[1], Jeff Young[1], Tom Conte[1]

School of Computer Science [1]

Georgia Tech Center for Research into Novel Computing Hierarchies

Landauer's Limit

Rolf Landauer proposed in 1961, that, as a consequence of the second law of thermodynamics, erasing one bit of data would release energy. He determined a theoretical lower limit for that energy dissipation as follows:

$$E = nk_BT \ln 2$$

Where E is the energy dissipated by lost information, n is the number of bits of information that are lost, k_B, is the Boltzmann constant, and T is the temperature read from the heat sink of the device in kelvin.

Using this principle, we have an absolute lower limit for energy dissipated in a computer, and we can use this information to get as close to this lower limit as possible.

Adiabatic Logic

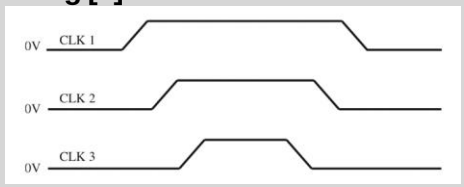
Adiabatic logic is uses entirely reversible logic operations in order to preserve data, and therefore energy. Standard CMOS logic is not reversible. Your standard AND gate in CMOS is not reversible, as by passing those values through, you lose the information supplied by the input values, which

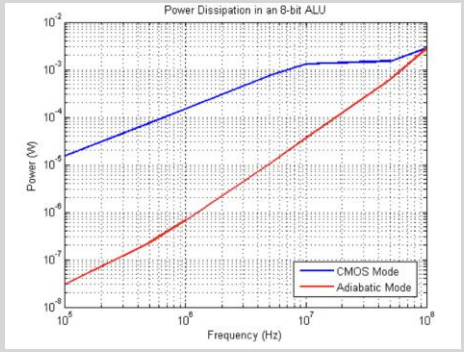
In addition, there are some rules to prevent power loss in transistors, for example, one should never power a transistor when there is already a voltage across it, and one should never un-power a transistor when there is current flowing through it, and no use of diodes.

Adiabatic Logic Methods/Families

Bennet Clocking [2]

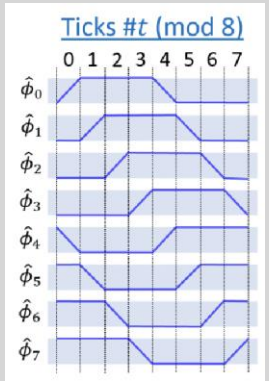
- Used most notably by a group led by Greg Snider at Notre Dame University
- Uses multiple trapezoidal clocks, that sequentially power sequential logic gates, then de-power them in reverse order, effectively reversing the computation.
- Each sequential logic gate needs a power and ground, as well as a positive and negative clock signal.
- Can function in CMOS mode or adiabatic mode
- Used and tested a 60% adiabatic processor vs a fully CMOS processor.
- At low frequencies, the power dissipation in adiabatic mode was significantly lower





Static 2 Level Adiabatic Logic [1]

- Proposed by Mike Frank at Sandia National Labs as a follow up to his dynamic logic family 2LAL
- Fully adiabatic circuitry with ability to form a fully reversible pipeline.
- Uses an 8 ”tick” system to sequentially power items
- Negative ticks can be pulled from a signal 4 spaces away



Planned Work

- We want to create a system to make it easier for people to use these logic systems, specifically S2LAL.
- Creating a standard cell library for use in hardware description languages.
- Allow people to easily use reversible circuits for whatever cause.
- Automatically generate reversible pipelines for arbitrarily large sequential logic circuits.
- Work towards creating a fully adiabatic processor.

References

[1] M. P. Frank, R. W. Brocato, B. D. Tierney, N. A. Missert, and A. H. Hsia, “Reversible Computing with Fast, Fully Static, Fully Adiabatic CMOS,” *CoRR*, vol. abs/2009.00448, 2020, [Online]. Available: https://arxiv.org/abs/2009.00448

[2] C. O. Campos-Aguillón, R. Celis-Cordova, I. K. Hänninen, C. S. Lent, A. O. Orlov and G. L. Snider, "A Mini-MIPS microprocessor for adiabatic computing," 2016 IEEE International Conference on Rebooting Computing (ICRC), 2016, pp. 1-7, doi: 10.1109/ICRC.2016.7738678.

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