# Modeling and Design for Magnetoelectric Random-access Memory based Ternary Content Addressable Memory (ME-TCAM)

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## ME-TCAM Operation

| | WL | SL | SL' | BL | BL' | Cell 1 | Cell 2 |
|---|---|---|---|---|---|---|---|
| **Writing '1'** | $V_{dd}$ | $V_{wr}$ | 0 | $V_{wr}$ | 0 | HRS | LRS |
| **Writing '0'** | $V_{dd}$ | 0 | $V_{wr}$ | 0 | $V_{wr}$ | LRS | HRS |
| **Writing 'X'** | $V_{dd}$ | $V_{wr}$ | $V_{wr}$ | 0 | 0 | HRS | HRS |

- To store binary bits to a TCAM cell, complementary logic values are stored into the two MTJs by applying the required voltage across the BFO layer.
- To store a don't care bit, both MTJs are set to anti-parallel state.

| | Cell1 data | Cell2 data | SL | SL' | $V_{fix}$ | ML |
|---|---|---|---|---|---|---|
| **Searching '1'** | 1 (HRS) | 0 (LRS) | $V_s$ | 0 | $kV_s$ | High |
| | 0 (LRS) | 1 (HRS) | $V_s$ | 0 | $(1-k)V_s$ | Low |
| | X (HRS) | X (HRS) | $V_s$ | 0 | $V_s/2$ | High |
| **Searching '0'** | 1 (HRS) | 0 (LRS) | 0 | $V_s$ | $(1-k)V_s$ | Low |
| | 0 (LRS) | 1 (HRS) | 0 | $V_s$ | $kV_s$ | High |
| | X (HRS) | X (HRS) | 0 | $V_s$ | $V_s/2$ | High |
| **Searching 'X'** | 1 (HRS) | 0 (LRS) | 0 | 0 | 0 | High |
| | 0 (LRS) | 1 (HRS) | 0 | 0 | 0 | High |
| | X (HRS) | X (HRS) | 0 | 0 | 0 | High |

$k=R_p/(R_p+R_{ap})$, $R_p$ = LRS and $R_{ap}$ = HRS

- To perform search, WL and BL/BL' are grounded and search voltages ($V_s$) are applied to SL/SL' which gets divided between the two MTJs
- $V_{fix}$ is used to control the gate of the discharge transistor (T3 in Figure).
- T3 discharges ML in case of a mismatch. ML stays high in case of a match.
- $V_s/2$ is adequately lower than the threshold voltage of the transistor.

## ME-TCAM Performance and Benchmarking

- Our design is variation tolerant. We show search error rates lower than 0.01% using Monte-Carlo simulations.
- Previous MTJ based TCAM designs required complex designs to overcome the issue of variation that leads to high search error rates while using 'x' bits.
- Our design is much more compact in their comparison and uses only 3 transistors.
- Possible due to the use of higher search voltages.
- In our case write and read paths are independent, hence higher $V_s$ values can be used.
- Increasing voltages not an option for two terminal STT devices where larger voltages can lead to a read disturb.

| | ME-MRAM | PMA | SRAM |
|---|---|---|---|
| **Search Delay(ps)** | 407 | 537 | 420 |
| **Search Energy(fJ)** | 563 | 680 | 723 |
| **Search EDP(ns*fJ)** | 22.9 | 36.5 | 30.3 |
| **Cell area($um^2$)** | 0.131 | 0.159 | 0.21 |
| **Write Energy(pJ)** | 0.66 | 10.3 | 1.59 |
| **Write Delay(ns)** | 1.90 | 1.00 | 0.14 |

- We use SPICE simulations to model search performance using 14 nm PTM ASU MOSFET models.
- We consider TMR degradation due to bias voltage in our simulations.