Thermal Modeling of 3D Polylithic Integration

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Motivation

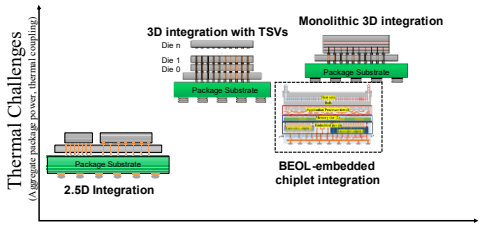


Figure 1: Motivation

- 3D integration of functional chiplets is primarily realized via TSV-based 3D stacking or monolithic 3D integration.
- However, there is a performance gap between TSV-based 3D and 3D monolithic ICs in terms of bandwidth and interconnect density.

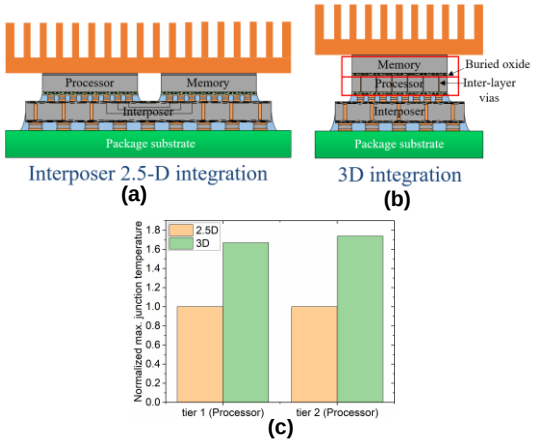
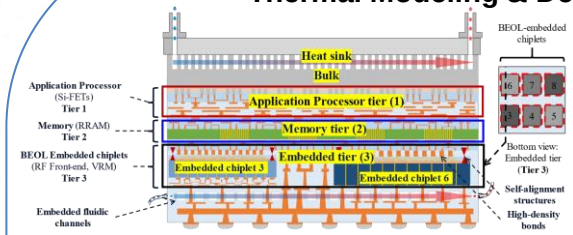


Figure 2: (a) Interposer-based 2.5-D and (b) 3D integration examples. (c) Maximum junction temperatures: Tier powers: 1. processor (150W), 2. processor (150W).

Thermal Modeling & Design Parameter Study



Tier / Chiplet		Power Density (W/cm²)	Dimensions (mm×mm×μm)	Bulk Material
Tier 1 (base) (AP)		100	10×10×157	Silicon
Tier 2 (RRAM)		5	10×10×8	Silicon
Tier 3 (with embedded chiplets)	Chiplet 3	5/50	2.5×3×12	Silicon
	Chiplet 4	5/50	2.5×3×12	Silicon
	Chiplet 5	5/50	2.5×3×12	Silicon
	Chiplet 6	5/50	2.5×3×12	Silicon
	Chiplet 7	5/50/500	2.5×3×12	Silicon
	Chiplet 8	5/50	2.5×3×12	Silicon

(b)

Figure 3: (a) 3D Seamless off-chip Connectivity (SoC+) concept: BEOL-embedded chiplet integration. (b) thermal simulations: design specifications & assumptions

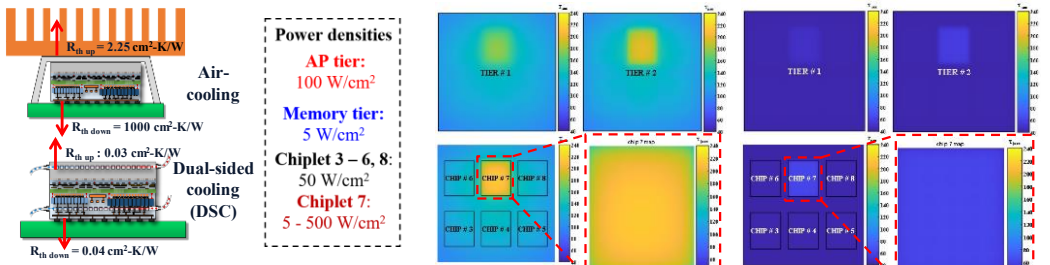


Figure 4: Considered cooling techniques and tier power densities for thermal evaluation and steady state evaluation

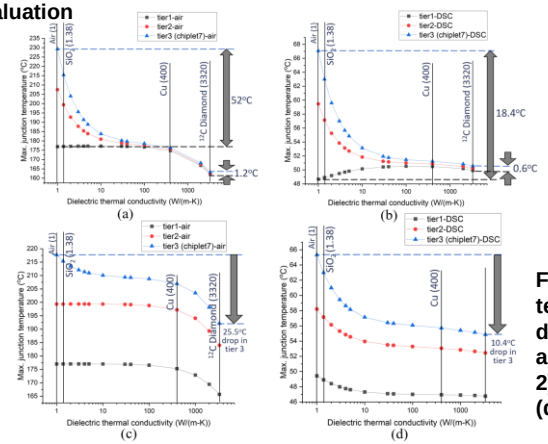
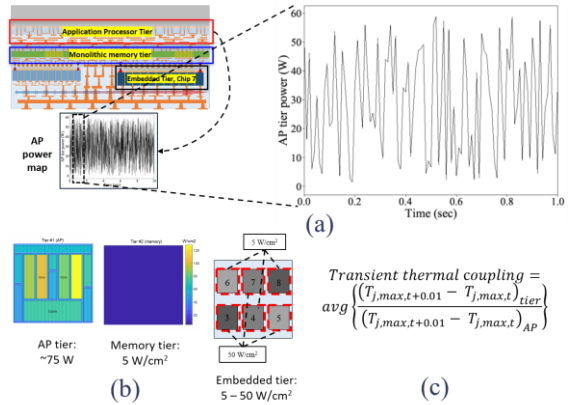


Figure 5: Maximum junction temperatures as a function of varying dielectric thermal conductivity in 1) all tiers with (a) air and (b) DSC and 2) just embedded tier with (c) air and (d) DSC.

Transient Thermal Analysis



$$Transient\ thermal\ coupling = avg\left\{\frac{\left(T_{j,max,t+0.01} - T_{j,max,t}\right)_{tier}}{\left(T_{j,max,t+0.01} - T_{j,max,t}\right)_{AP}}\right\}$$

Figure 6: Transient state thermal evaluation

Conclusion

We have presented a thermal study for 3D polylithic integration as a function of tier power density, dielectric thermal conductivity, and transient power variation to identify thermal limits and challenges in such integration approaches.

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