Sharc Lab
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Graph Neural Network Accelerators for FPGAs

GenGNN and Future Research Directions

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Ultra-fast Small Graph Accelerator

Motivation

- Small graphs: graphs that fit entirely within on-chip memory, e.g., tens of nodes and edges
- Example: molecular graphs

Goal

- Extend GenGNN to enable **high throughput** for thousands of small graphs

Key points

- Parallelization across nodes & edges
- Batched processing of graphs
- Quantization with minimal loss of accuracy

Scalable Large Graph Accelerator

Motivation

- Large graphs: graphs too large to fit into on-chip memory, e.g., millions of nodes and edges
- Example: social network graphs

Goal

- Extend GenGNN to optimize latency for large graphs, keeping **scalability** in mind

Key points

- Reordering nodes & edges on-the-fly
- Smart caching of nodes & edges
- Scalable to any embedding dimension
- Design-space exploration for different graph types

1

2

GenGNN: A Generic FPGA Framework for Graph Neural Network Acceleration

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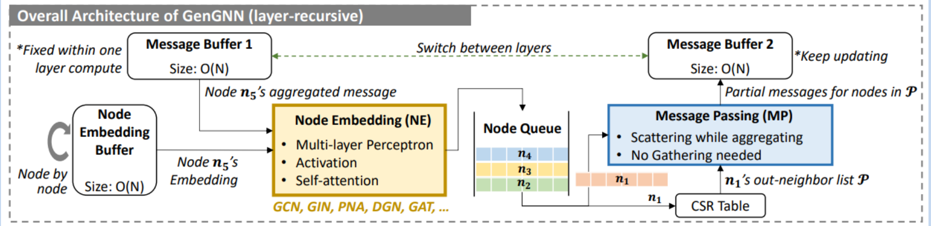
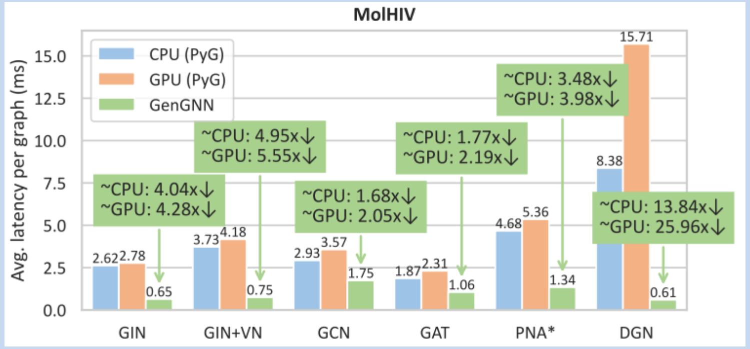
(Submitted to FCCM 2022)



Two-fold goals

- Ultra-fast GNN inference with zero graph pre-processing for real-time requirements
- Support for diverse set of GNN models with extensibility to adapt to new models

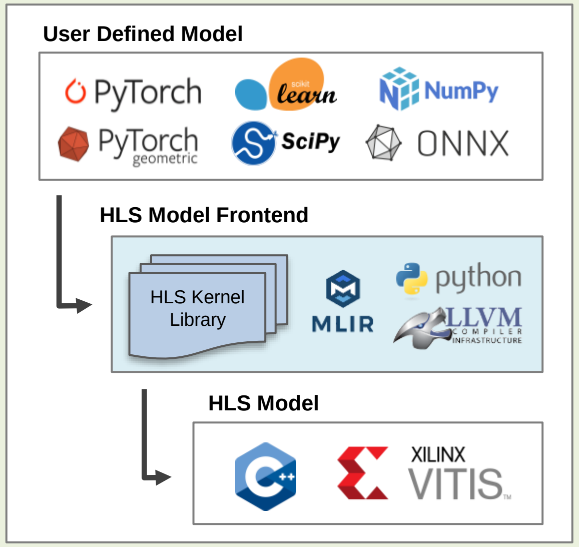


Implemented on Xilinx Alveo U50

- Up to 25x faster than CPU baseline
- Up to 13x faster than GPU baseline

3

Automated Accelerator Construction



Motivation

- GNN accelerators lack similar optimizations and repetition of same kernels across all models
- Programming effort high compared to design exploration

1 2 3

Ongoing directions based on GenGNN