

## Vortex Open GPU Research Platform



Georgia Tech College of Computing
Center for Research into
Novel Computing Hierarchies

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#### Motivation

## Research in GPU Hardware Architecture

- Hardware research beyond simulation
- A robust framework for prototyping
- Lack of open-source full-system GPU

#### The advent of RISC-V

- Open ISA for accessibility
- Frozen ISA for compatibility
- Extensible ISA for customization
- Ideal for architecture research!

#### The advent of RISC-V

- Large-scale RTL designs now possible
- What about complex GPU designs?

#### **Vortex System Architecture**

Vortex Processor

Core Core Core

Core Core Core

Core Core Core

Core Core Core

#### Open-source Toolchain

- POCL: OpenCL Compiler
- OPAE: FPGA Driver API
- Verilator: RTL simulation
- Yosys: FPGA Synthesis
- Gem5: CAS Simulation

#### Software Support

- OpenCL
- CUDAOpenGL
- Vulkan

#### Hardware

Configurable multi-core SIMT architecture

CUDA OpenCL

OpenGL

Applications

OpenCL Run-time API

Common Device Interface

Device

**POCL Runtime** 

- PCIe host-device interface
- Up to 32-cores @ 230 Mhz

#### **Vortex Processor Microarchitecture**

#### **Command Processor**

CPU-GPU communication

#### DCRs

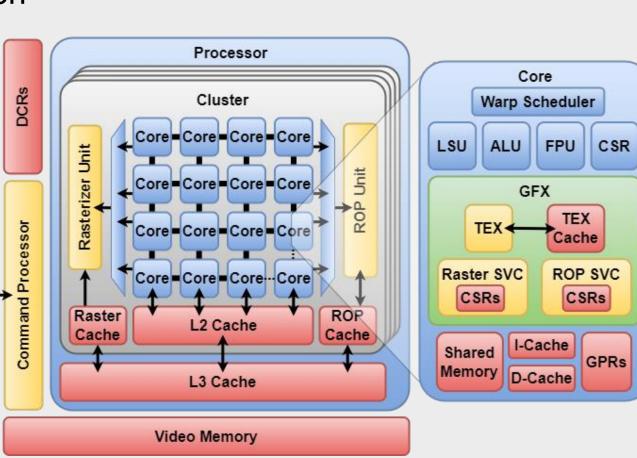
- Configuration registers
- CPU driven

#### Raster Unit

- Triangle rasterizer
- Tile-based

#### ROP Unit

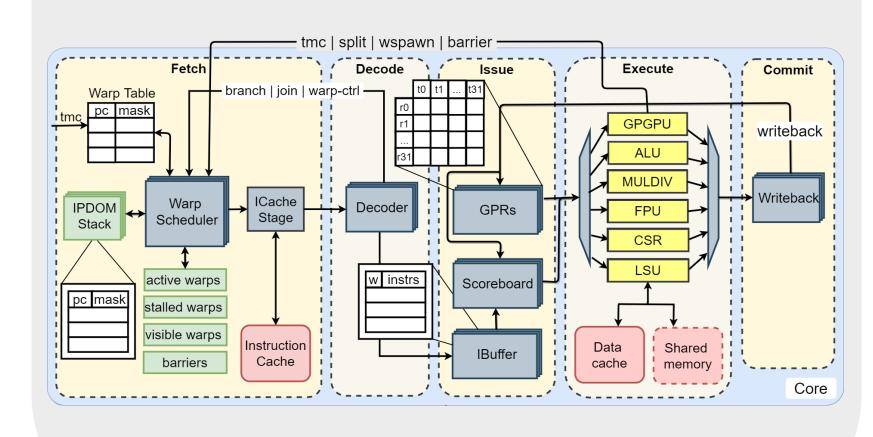
- Depth/Stencil
- BlendingLogic Op
- Texture Unit
- Texture sampling



### **Vortex Single Core Microarchitecture**

#### Five-stage RISC-V Pipeline

- In-order issue, out-of-order commit
- Warp scheduler
- Per-thread general-purpose register file
- Per-wavefront instruction buffer
- GPGPU Unit



#### **OpenCL Software Stack**

#### **OpenCL Runtime**

LLVM

Compiler

**GPU** 

Research

FPGA

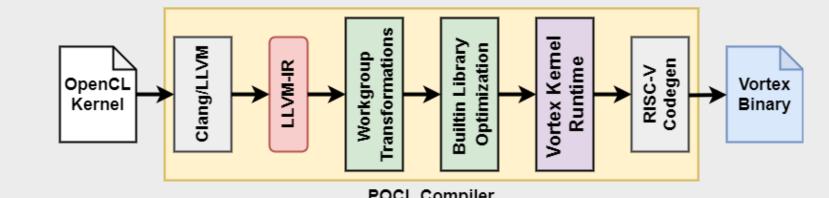
OpenCL

Vulkan

- Use POCL Runtime framework [1]
- Added new device target for Vortex
- FPGA Driver uses Intel OPAE API [2]

#### OpenCL Compiler

- Use POCL Compiler framework
- Added Vortex Kernel Runtime Pass
  - Work items => Vortex threadsWavefront invocations



[1] Pekka Jääskeläinen et al "pocl: A Performance-Portable OpenCL Implementation" [2] Open Programmable Acceleration Engine: https://opae.github.io

#### **Graphics Benchmark**

Instruction Cache

Fetch Decode

Register File

L1 cache / Shared Memory

ALU CSR LSU

#### **Evaluation Setup**

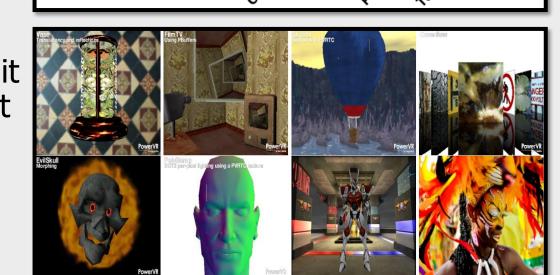
- Intel PAC Stratix
   10 FPGA
- Intel Xeon E5-1650 3.5 Ghz CPU

#### **FPGA**

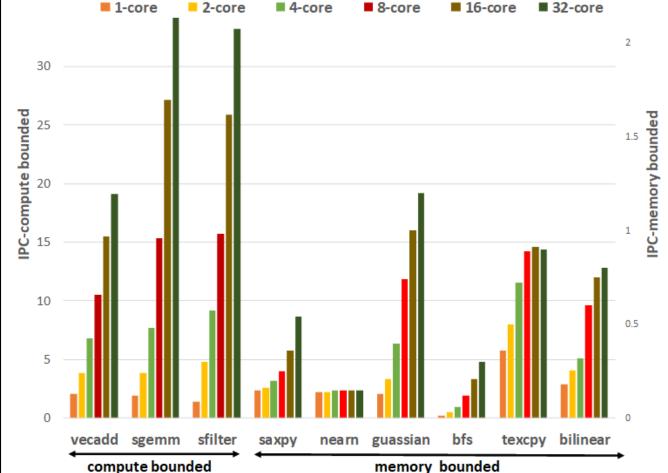
#### Performance

- 32 GPU cores
- 1 Rasterizer unit4 render output
- units8 texture units
- Texture Fill Rate: 7.4 GTexels/s
- Pixel Fill Rate:3.7 GPixels/s

# 1 core 2 cores 4 cores 8 cores 16 cores 32 cores



#### **GPGPU Benchmark**



#### **Evaluation Setup**

- Intel PAC Arria 10 FPGA
- Intel Xeon E5-1650 3.5 GHz CPU

#### | OpenCL Performance

- Rodinia benchmark
- Compute vs. memory bound
- Scaling across many applicationsThroughput: 29 Gflops