



Boolean Signals	
LD.MAR	GateMARMUX
LD.MDR	GateMDR
LD.REG	GatePC
LD.CC	GateALU
LD.PC	LD.IR
MEM.EN	

Signal Name	Possible Values
ALUK	ADD, AND, NOT, PASSA
ADDR1MUX	PC, BaseR
ADDR2MUX	ZERO, offset6, PCOffset9, PCOffset11
PCMUX	PC+1, ADDER, BUS
MARMUX	ZEXT, ADDER
SR2MUX	SR2, SEXT
R.W	R (0), W (1)

CS2110 Reference Sheet

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADD	0001				DR		SR1		0	00		SR2				
ADD	0001				DR		SR1		1	imm5						

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AND	0101				DR		SR1		0	00		SR2				
AND	0101				DR		SR1		1	imm5						

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NOT	1001				DR		SR		111111							

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BR	0000				N	Z	P	PCoffset9								

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
JMP	1100				000		BaseR		000000								
JSR	0100				1	PCOffset11											
JSRR	0100				0	00		BaseR		000000							

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LD	0010				DR		PCoffset9									
LDI	1010				DR		PCoffset9									
LDR	0110				DR		BaseR		offset6							
LEA	1110				DR		PCoffset9									

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ST	0011				SR		PCoffset9									
STI	1011				SR		PCoffset9									
STR	0111				SR		BaseR		offset6							

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRAP	1111				0000				trapvect8							

Trap Vector	Assembler Name
x20	GETC
x21	OUT
x22	PUTS
x23	IN
x25	HALT

Device Register	Addr
Keybd Status Reg	xFE00
Keybd Data Reg	xFE02
Display Status Reg	xFE04
Display Data Reg	xFE06

Mnemonic	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
*ADD	0	0	0	1	DR			SR1			0	0	0	SR2		
*ADD	0	0	0	1	DR			SR1			1	imm5				
*AND	0	1	0	1	DR			SR1			0	0	0	SR2		
*AND	0	1	0	1	DR			SR1			1	imm5				
BR	0	0	0	0	n	z	p	PCOffset9								
JMP	1	1	0	0	0	0	0	BaseR			0	0	0	0	0	0
JSR	0	1	0	0	1	PCOffset11										
JSRR	0	1	0	0	0	0	0	BaseR			0	0	0	0	0	0
*LD	0	0	1	0	DR			PCOffset9								
*LDI	1	0	1	0	DR			PCOffset9								
*LDR	0	1	1	0	DR			BaseR			offset6					
LEA	1	1	1	0	DR			PCOffset9								
*NOT	1	0	0	1	DR			SR			1	1	1	1	1	1
reserved	1	1	0	1	-	-	-	-	-	-	-	-	-	-	-	-
RTI	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ST	0	0	1	1	SR			PCOffset9								
STI	1	0	1	1	SR			PCOffset9								
STR	0	1	1	1	SR			BaseR			offset6					
TRAP	1	1	1	1	0	0	0	0	trapvect8							

* modifies condition codes NZP