The Story of the LC-3 Datapath

...Starting with Only 16 Wires

LC-3 datapath taken from Patt & Patel 3rd ed.
Edited by Austin Adams and Pulkit Gupta

16

MEMORY

MEM.EN

GatePC

LD.PC→ PC

+1

/16

[15:12]

FINITE
STATE
MACHINE

/16

LD.IR→ IR

/16

GateMDR

16/

MDR ←LD.MDR

MAR ←LD.MAR

/16

/16

MEMORY

16

MEM.EN

github.com/gt-cs2110/lc3-datapath

github.com/gt-cs2110/lc3-datapath

GatePC

LD.PC → PC

+1

/16

REG FILE

/16

DR /3

LD.REG →

SR2 /3 → SR2 OUT

SR1 OUT ← /3 SR1

/16   /16

[15:12]

FINITE STATE MACHINE

/16

LD.IR → IR

ALUK 2

/16

B   A

ALU

/16

GateALU

GateMDR

16/

MDR ← LD.MDR

/16

/16

MAR ← LD.MAR

/16

MEMORY

16

MEM.EN

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GatePC

LD.PC → PC

+1

16

REG FILE

16

DR — 3

LD.REG →

SR2 — 3 → SR2 OUT   SR1 OUT ← 3 — SR1

16   16

SEXT   16

[4:0]

[5]

[15:12]

SR2MUX

FINITE STATE MACHINE

16

B   A
ALU

2
ALUK

16

LD.IR → IR

16

GateALU

16

GateMDR

16

MDR ← LD.MDR   MAR ← LD.MAR

16   16

16

MEMORY

16

MEM.EN

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GateAddr

GatePC

LD.PC→ PC

+1

REG FILE

DR 3

LD.REG→

SR2 3 SR2 OUT

SR1 OUT 3 SR1

16

16

16

16

16

+

16

16

SEXT

[8:0]

SEXT

[4:0]

SEXT

[5]

[15:12]

FINITE STATE MACHINE

SR2MUX

16

16

16

16

16

16

2

ALUK

B   A

ALU

16

GateALU

LD.IR→ IR

16

16

GateMDR

16

MDR ←LD.MDR

MAR ←LD.MAR

16

16

MEMORY

16

MEM.EN

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GateAddr

GatePC

LD.PC → PC

+1

GateALU

REG FILE

DR

LD.REG

SR2 OUT

SR1 OUT

SR1

SR2

+

SEXT

[8:0]

SEXT

[4:0]

SEXT

[5]

SR2MUX

[15:12]

FINITE STATE MACHINE

ALUK

B   A

ALU

LD.IR → IR

GateALU

GateMDR

MDR ← LD.MDR

MEM.EN

MEMORY

MAR ← LD.MAR

MEM.EN   MEM.RW

SR1MUX

IR[11:9]

IR[8:6]

SR1

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GateAddr

GatePC

16

16

LD.PC → PC

+1

2

PCMUX

16

16

DR 3

REG FILE

LD.REG →

SR2 3 → SR2 OUT SR1 OUT ← 3 SR1

16

16

16

16

+

16

16

ADDR2MUX 16 16 ADDR1MUX

2

16 16 16 16

0

SEXT 16

[8:0] SEXT [4:0]

[5]

[15:9]

SR2MUX

FINITE STATE MACHINE

16

[5:0] SEXT

3

2 ALUK

B A

ALU

16

LD.IR → IR

N Z P ← LD.CC

3

16

LOGIC

3

16

GateALU

16

GateMDR

16 16

MDR ← LD.MDR

MAR ← LD.MAR

16

SR1MUX

MEM.EN

16

MEMORY

IR[11:9] 3

3 → SR1

IR[8:6] 3

16 16

16

MEM.EN MEM.RW

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