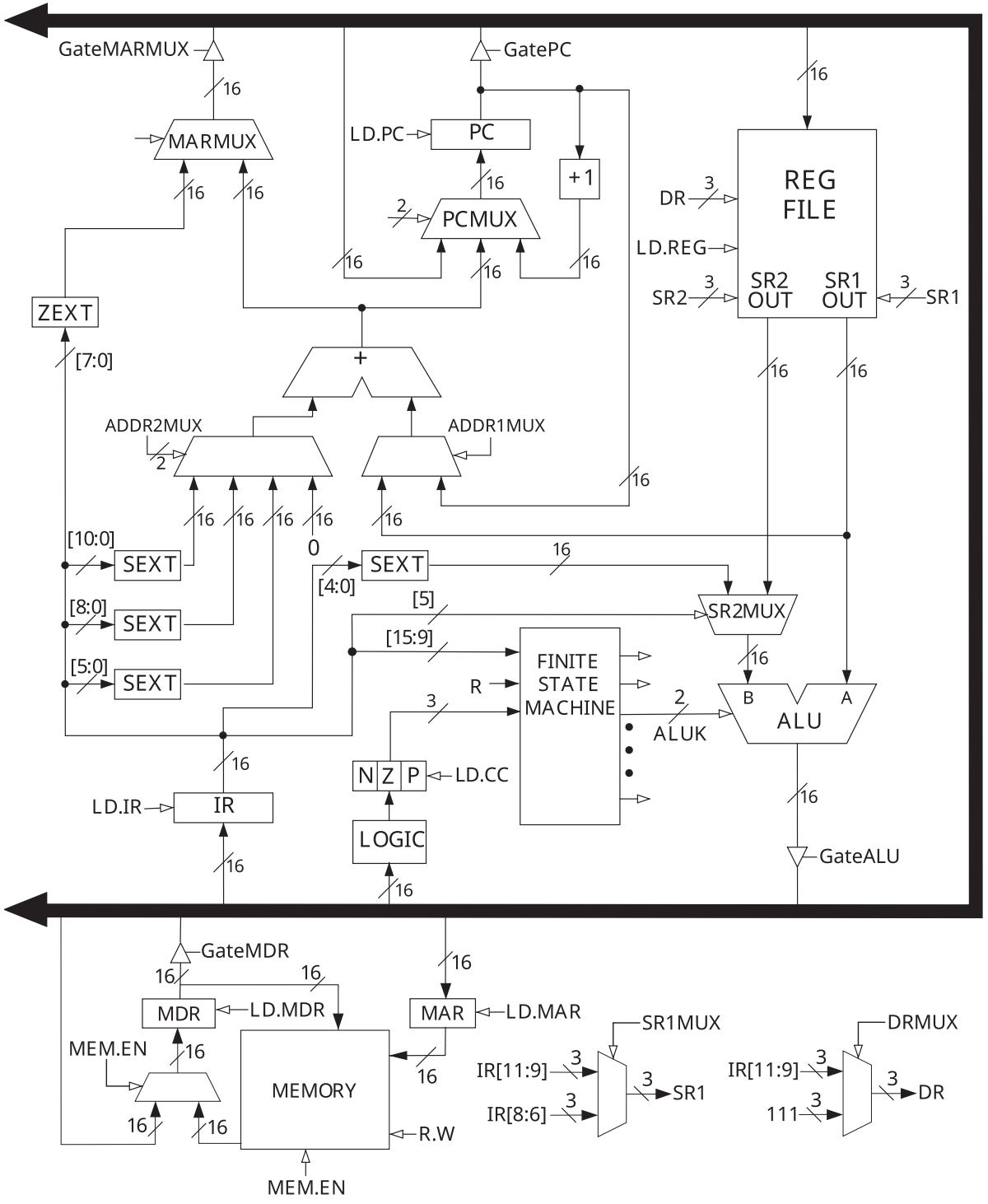

Boolean Signals	
LD.MAR	GateMARMUX
LD.MDR	GateMDR
LD.REG	GatePC
LD.CC	GateALU
LD.PC	LD.IR
MEM.EN	

Signal Name	Possible Values
ALUK	ADD, AND, NOT, PASSA
ADDR1MUX	PC, BaseR
ADDR2MUX	ZERO, offset6, PCoffset9, PCoffset11
PCMUX	PC+1, ADDER, BUS
MARMUX	ZEXT, ADDER
SR2MUX	SR2, SEXT
R.W	R (0), W (1)

Mnemonic	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
*ADD	0	0	0	1	DR			SR1			0	0	0	SR2		
*ADD	0	0	0	1	DR			SR1			1	imm5				
*AND	0	1	0	1	DR			SR1			0	0	0	SR2		
*AND	0	1	0	1	DR			SR1			1	imm5				
BR	0	0	0	0	n	z	p	PCoffset9								
JMP	1	1	0	0	0	0	0	BaseR			0	0	0	0	0	0
JSR	0	1	0	0	1	PCoffset11										
JSRR	0	1	0	0	0	0	0	BaseR			0	0	0	0	0	0
*LD	0	0	1	0	DR			PCoffset9								
*LDI	1	0	1	0	DR			PCoffset9								
*LDR	0	1	1	0	DR			BaseR			offset6					
LEA	1	1	1	0	DR			PCoffset9								
*NOT	1	0	0	1	DR			SR			1	1	1	1	1	1
reserved	1	1	0	1	-	-	-	-	-	-	-	-	-	-	-	-
RTI	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ST	0	0	1	1	SR			PCoffset9								
STI	1	0	1	1	SR			PCoffset9								
STR	0	1	1	1	SR			BaseR			offset6					
TRAP	1	1	1	1	0	0	0	0	trapvect8							

* *modifies condition codes NZP*

Trap Vector	Assembler Name
x20	**GETC**
x21	**OUT** or **PUTC**
x22	**PUTS**
x23	**IN**
x25	**HALT**

Character	ASCII Code
NUL	x00
A	x41
B	x42
C	x43
D	x44

Device Register	Addr
Keyboard Status Register	xFE00
Keyboard Data Register	xFE02
Display Status Register	xFE04
Display Data Register	xFE06