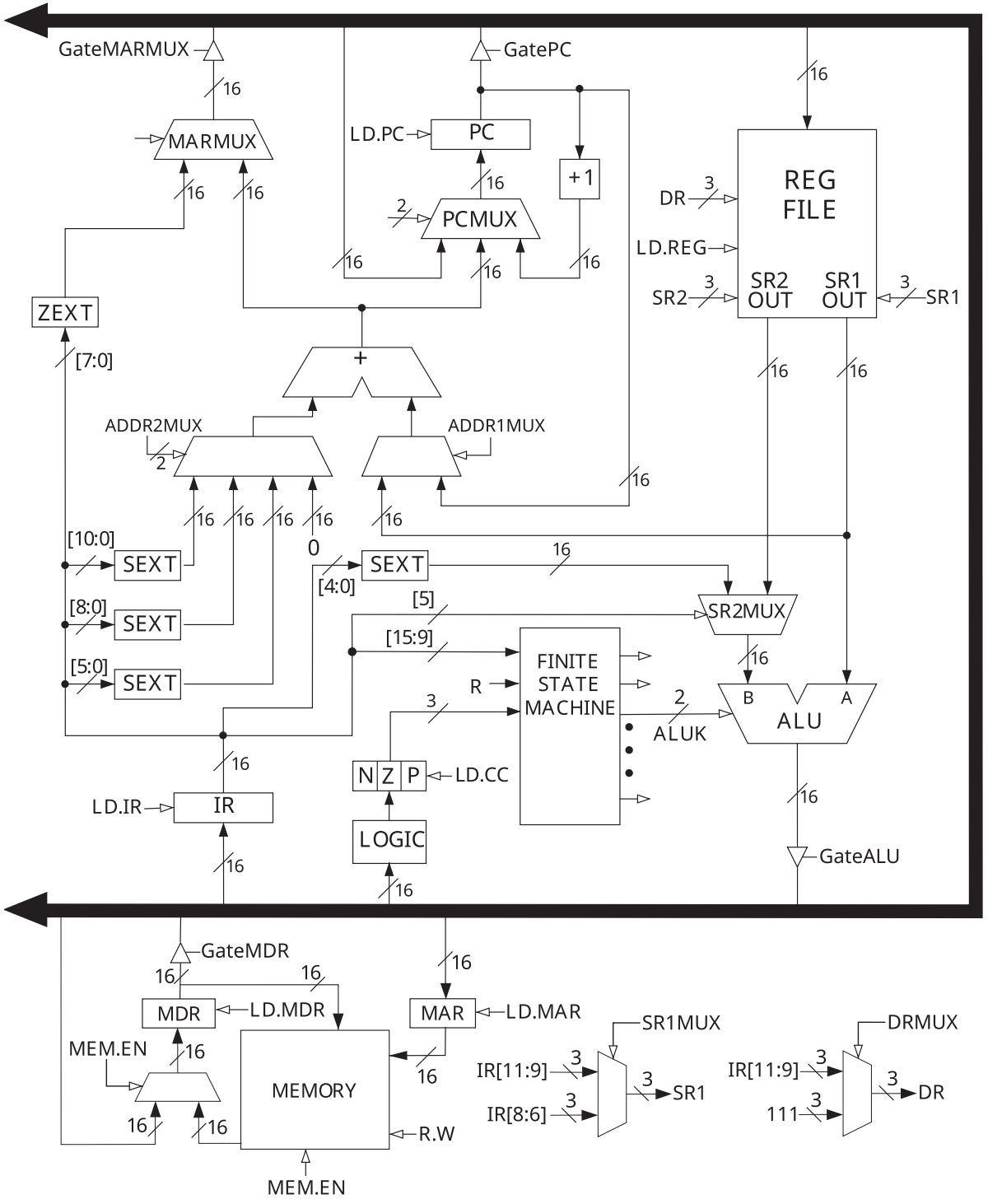

Boolean Signals	
LD.MAR	GateMARMUX
LD.MDR	GateMDR
LD.REG	GatePC
LD.CC	GateALU
LD.PC	LD.IR
MEM.EN	

Signal Name	Possible Values
ALUK	ADD, AND, NOT, PASSA
ADDR1MUX	PC, BaseR
ADDR2MUX	ZERO, offset6, PCoffset9, PCoffset11
PCMUX	PC+1, ADDER, BUS
MARMUX	ZEXT, ADDER
SR2MUX	SR2, SEXT
R.W	R (0), W (1)

CS2110 Reference Sheet

ADD

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0001				DR			SR1			0	00		SR2		
0001				DR			SR1			1	imm5				

AND

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0101				DR			SR1			0	00		SR2		
0101				DR			SR1			1	imm5				

NOT

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1001				DR			SR			111111					

BR

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0000				N	Z	P	PCoffset9								

JMP

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1100				000			BaseR			000000					

JSR

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0100				1	PCoffset11										

JSRR

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0100				0	00		BaseR			000000					

LD

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0010				DR			PCoffset9								

LDI

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1010				DR			PCoffset9								

LDR

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0110				DR			BaseR			offset6					

LEA

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1110				DR			PCoffset9								

ST

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0011				SR			PCoffset9								

STI

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1011				SR			PCoffset9								

STR

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0111				SR			BaseR			offset6					

TRAP

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1111				0000			trapvect8								

Trap Vector	Assembler Name
x20	**GETC**
x21	**OUT**
x22	**PUTS**
x23	**IN**
x25	**HALT**

Device Register	Addr
Keybd Status Reg	xFE00
Keybd Data Reg	xFE02
Display Status Reg	xFE04
Display Data Reg	xFE06