AT&T - CISCO

E3 issues on XR12K 3.6.3

5/4/2010

E3 ATM SER issue – SMU delivery

- 3.6.3 SMU (SER fix and packet capture for PLIM error)
  - Code review, unit test done
  - On track for delivery of SMU by 5/12
- 3.8.4 SMU (SER fix and packet capture for PLIM error)
  - SMU lineup created, patching the diffs now
  - Target delivery – 5/20 (trying to pull in the dates)

Error logs for SER invocation

- No Common message to catch all events triggering SER, some device specific messages listed below
- New string added to catch all occurrences in SMU

LC/0/1/CPU0:May 3 22:58:47.931 : hfa_main[56]: %L2-PSE-6-INFO_MSG : Info: **Invoking Soft Error Recovery**

- XBMA Errors:

LC/0/6/CPU0:Jan 7 18:35:08.745 : tx_xbma[83]: %L2-QM-**4-INTERRUPT** : EGRESSQ: ZBT parity error : reg value 0x2022bee

LC/0/6/CPU0:Jan 7 18:35:11.961 : rx_xbma[77]: %L2-E3INGRESSQ-**4-INTERRUPT** : PLIM error: reg 0x2000

- Alpha Errors:

LC/0/3/CPU0:May 3 11:37:48.228 : hfa_main[56]: %L2-ALPHA-**3-ERROR**_MSG : RX PSE: RX PSE:, CPU interrupt status, 0x40000, 0x0 RX PSE:, CPU_POST_CAM_INT, 0x1, 0x2 RX PSE:, POST_CAM_PARITY_ERR, 0x7c516110, 0x800 : 0x0 0x0

- PLIM Errors (multiple devices):

RP/0/0/CPU0:May 4 18:06:12.449 : gsr_prp_pm[60]: %LC-FAULT-3-LC_DEVICE : LC 2: Reset Device – PLIM

EFA Summary

- Total 9 cases of Engine3 card failures during XR migration
- 6 cases of Engine3 card failed to boot IOS-XR3.6.3
  - 3 Cards received with 256MB memory (Shipping configuration)
    - No issues found during FA
  - 1 case in FA process
  - 2 cases in transit
- 3 cases of PLIM 0x2000/ZBT Parity error
  - DDTS CSCtg47798 to track the issue
  - 1 case in FA process
  - 2 cases in transit
- FA timeline: 5 – 10 working days after board received at FA

EFA cases for E3 fail to boot XR (1 of 3)

EFA # TAC Case RMA#	Board Type & Serial #	Problem Description	EFA Status / Comments
FA-0096486 613694945 83193100	4OC12X/POS-I-SC-B= SAL1025S9VD	After migration from IOS (120-32.S6r) to XR3.6.3, slot 13 LC stuck in "Launching MBI" stage. It eventually timed-out and ended up in RESET. The router was brought back to 12.0(32)S6r due to this problem and the LC booted in IOS just fine.	Received at Cisco on 04/13/2010 The board received has 2x128MB memory which is not sufficient for XR booting. Board passed IOS booting with default memory. It could boot XR3.6.3 only after replacing memory with 2x512MB Case Closed as "FA Process Failure"
FA-0094547 613620981 83173058 83173064	4GE-SFP-LC= SAL11488QBJ MEM-LC-ISE-512A= (x2)	After migration from IOS (120-32.S6r) to XR3.6.3, slot 4 LC stuck in "Launching MBI" stage. It eventually timed-out and ended up in RESET.	Received at Cisco on 03/08/2010 The board received has 2x128MB memory which is not sufficient for XR booting. Board passed IOS booting with default memory. It could boot XR3.6.3 only after replacing memory with 2x512MB Memory in transit for FA Status "In FA process"

EFA cases for E3 fail to boot XR (2 of 3)

EFA # TAC Case RMA#	Board Type & Serial #	Problem Description	EFA Status / Comments
FA-0095907 613721487 83190040	4OC12X/POS-I-SC-B= SAD063600TV	After migration from IOS to XR3.6.3, slot 13 LC stuck in "MBI BOOT" stage. It eventually timed-out and ended up in RESET. Slot 1 had lower MBUS ROM version 2.42. Release Notes state that IOS to IOX3.6.3 upgrade requires MBUS ROM version 4.4.	Received at Cisco on 03/25/2010 The board received has 2x128MB memory which is not sufficient for XR booting. Board passed IOS booting with default memory. It could boot XR3.6.3 only after replacing memory with 2x512MB Case Closed as "FA Process Failure"
FA-0102597 613943445 83225112 83237454	4OC12/ATM-IR-SC= SAD113705KC MEM-ISE-512A-2PK	After migration from IOS (120-32.S11o) to XR3.6.3, slot 13 LC stuck in "Launching MBI" stage. It eventually timed-out and ended up in RESET.	Board received at Cisco on 04/30/2010 The board received has 512MB memory plus the TX PLU memory missing as part of visual inspection Status "In FA process"

EFA cases for E3 fail to boot XR (3 of 3)

EFA # TAC Case RMA#	Board Type & Serial #	Problem Description	EFA Status / Comments
FA-0102641 FA-0101287 614119857 83255648 83257823	4OC3X/ATM-IR-SC= SAD112501CY MEM-ISE-512A-2PK	After migration from IOS 32-S6r to XR3.6.3, slot 1 LC stuck in constant “IN RESET" loop. Hence customer had backed out of the upgrade but still the LC was down.	Board In transit Received 1GB (2x512MB) memory
FA-0101315 614120837 83255772	4OC3X/ATM-IR-SC= SAD1041085W	After migration from IOS 32-S6r to XR3.6.3, slot 5 LC crashed after booting XR and stuck in constant “IN RESET" loop. Hence customer had backed out of the upgrade but still the LC was down.	In transit

EFA cases for PLIM 0x2000 Error

EFA # TAC Case RMA#	Board Type & Serial #	Problem Description	EFA Status / Comments
FA-0102473 614172375 83267123	4OC3X/ATM-IR-SC= SAD083205PT	Engine 3 ATM sub-interface fails. L2 ping on ATM interface passes whereas L3 ping are getting dropped in the SAR. The issue happened on multiple VCs in slot 12 Problem cleared in MW, but ATT wants to replace the card	Received at Cisco on 04/30/2010 With 2x512MB memory 1 loose 512 dimm in a bag Status “In FA process”
FA-0102395 FA-0102396 614169037 83265027 83266057	4OC12X/ATM-IR-SC= SAD11010609 MEM-ISE-512A-2PK	Engine 3 ATM sub-interface fails. Ping on ATM interface are getting dropped in the SAR. The issue happened on multiple VCs in slot 5 Two cards failed, one sent for FA	Status “In transit”
FA-0102620 614199033 83269223	4OC12X/ATM-IR-SC= SAD121908HK MEM-ISE-512A-2PK	Engine 3 ATM sub-interface fails. L2 ping on ATM interface passes whereas L3 ping are getting dropped in the SAR. The issue happened on multiple VCs in slot 12	Status “In transit”

L3 Traffic – SER fix details

- Root cause fix
  - Do not replay “encap string” from Shared MEM into SDRAM during SER. Change classification of SDRAM errors to “Fatal”
  - Behavior would be at par with IOS with this change.
  - LOC < 10 line
  - Risk Analysis – No risk, change would get executed only when SER is invoked.
- Debug for finding the trigger for PLIM error, capture the packet which caused PLIM 0x2000 xbma error
  - LOC < 20 lines
  - Risk Analysis – No risk, this change would get executed when error handling interrupt is raised, before SER is invoked.

L3 Traffic – SER fix timelines

- Code changes, review, UT – 5/5
- Production SMU delivery – 5/12

Next Steps

- Why ping packets are taking CoS-Id 0 in 3.6.3 and CoS-Id 3 in 3.8.4?

L3 Traffic – RCA for SER issue

- **Root cause identified, working on fix**
- Sequence of events in XR
  1. When a policy map is attached, rewrite string is written into the Shared Memory (SW entry)
  2. ATM VC specific Encap-string is stored in SDRAM (HW entry) only for all the CoS-Ids. These CoS-Ids are NOT written in Shared Memory
  3. When SER is invoked, SW replays information stored in Shared Memory to SDRAM (part of recovery process)
  4. **rewrite string in Shared Memory is getting copied over into encap-string in SDRAM corresponding to first OI entry in HW**
  5. As a consequence, CoS-Id 0 gets overwritten with default value. When a packet comes for that OI pointer, it gets the encap-string as default, and packet gets dropped in SAR.
- In IOS, SDRAM is not re-inited as part of SER because PLIM and ZBT parity errors are treated as LOW_SEVERITY.
- In 3.8.x lab test, ping packets were going through CoS-Id 3 (not the CoS-Id 0), hence traffic was not impacted. **Problem does exist in 3.8.x and later releases, not getting exposed**

L3 Traffic – RCA for SER issue (cont..)

Proposed fix (Still in works..)

- Store encap string in Shared Memory as well, so that HW entries get reprogrammed correctly during SER

Next Steps

- Further analysis of proposed fix, and other possible solutions
- Behavior in IOS when SER is invoked for HIGH_SEVERITY errors
- Why ping packets are taking CoS-Id 0 in 3.6.3 and CoS-Id 3 in 3.8.4
- ETA for SMU – Would it be hitless?

L3 Traffic – SER issue

- Follow-up questions
  - Is the issue seen on 3.8.3 – **NO**
  - Check the “Humvee bug fix” that went in T5e - **RULED OUT**
    - •DDTS CSCeh61477, fix localized to the Humvee queue stuck (h/w errata).
    - •Fix is to update config registers correctly during humvee initialization to prevent humvee queue stuck-up.
    - •No change in packet formation or forwarding logic
- Root cause analysis
  - •rewrite string is wrong causing the pkt to be dropped in sar
  - •Fixed in 3.8.0, further analysis underway what changed between 3.7 and 3.8.0 release to explain this behavior
- Next Steps
  - •Provide 3.6.3 based SMU

L3 Traffic – Trigger for PLIM error

- Problem not consistent on one specific node in AT&T network, hard to draw any patterns wrt trigger
- Debug SMU
  - In E5, XBMA utility dumps all the information, including packets in the WIM and other modules. This will be written when LC crashes due to XBMA interrupt.
  - This utility not applicable for E3, the interrupt is non fatal and LC doesn't reload (SER is expected to recover).
  - Working on a E3 debug image to capture packet details before initiating SER (details in next slide)
- Next Steps
  - Identify any “pattern” in traffic type/config/event across multiple occurrences
  - Provide 3.6.3 based debug SMU for E3 to capture details.

PLIM error (reg 0x2000) – Debug SMU

- The "PLIM" portion of the message indicates that the condition encountered is associated with the PLIM (Alpha Interface) Module of the RADAR (queuing ASIC).
- The value of 0x2000 indicates that the condition causing the interrupt is E3_RADAR_PLIM_MAX_LEN_ERR.
- There is an "overflow_addr", which is loaded when an "MAX_LEN_ERR" occurs in the PLIM module that points to the base address in SDRAM.
- From the RADAR Hardware Spec

  Baddr Overflow Register: [55:32] This register captures the write address of the portion of the packet that exceeds the maximum length of the packet as determined by the QM.
- Using this base address in SDRAM, we can dump the packet buffer sitting at the pointed address in SDRAM.
- Knowing the packet we can narrow it down to the particular u-code forwarding path and hence debugging would be easier.

Upgrade failures (NO CHANGE)

- Suspect compatibility issues with memory used in failed E3 cards
  - Kernel crash pointing to “Invalid address access”
  - Once we are able to get memory used in AT&T, can proceed further
- Repro Update - Not yielding anything, need some ideas to proceed further
  - Upgrades were tried on 16-slot, 10-slot and 6-slot chassis, from 32S6r, 32S11n, 32S11o to 3.6.3 (+ SMU of CSCta18474 and CSCtd69603)
  - The 16-slot chassis is fully loaded with E3 cards (ATM and POS).
  - The RMAed card was also used (different memory)
  - MOP was followed (both power cycle and reload)
  - Rommon version, mbus version and fab loader version on some cards was same as that in failure case. (other cards had various versions – aim was to try upgrade with different versions)
  - Upgrades were done back to back several times
- Next Steps
  - Compare CI/GA MOP – Any changes exposing this issue?
  - Repro with RMAed boards – **WITH PHYSICAL MEM**
  - Debug in AT&T network during next upgrade cycle – DEs can join, live debug

L3 Traffic Issue - Follow-up

- Recap – What we discussed yesterday
  - rx_xbma errors seen on Vienna/Singapore (PLIM err 0x2000) and Brussels (ZBT Parity err) routers. Reproduced in Cisco lab by injecting HFA errors using test CLI, which invokes exactly same SER.
  - These errors are classified as non-fatal, does not trigger LC reload, system tries to recover thru SER (SW Error Recovery).
  - Suspect some issue in SER, which is messing up the data path causing L3 Ping failures
- What is ZBT error, PLIM Err 0x2000, and SER? **See backup slides**
- Is this issue specific to ATM cards only – **Similar issue is seen on GE as well, not an exact match (need more analysis)**
- Is this SER issue specific to XR – **Not able to repro on IOS in lab yet**
- Is SER processing diff in XR wrt IOS – **Logic is same, code is different**
- Do we suspect RPM upgrade causing Parity/PLIM error? **Transient Parity/PLIM errors have been seen in IOS before, impact in XR is severe due to SER bug.**

L3 Traffic Issue – Follow up (Cont..)

- Possible trigger for ZBT Parity error – **Suspect transient HW error conditions**
- Possible trigger for PLIM Error 0x2000 – **Specific GOOD packet received on wire, which results into invalid length in buffer header while processing in Alpha (SW error, internal to GSR)**
- Have ZBT parity errors been seen on IOS before? **YES**
- Have PLIM 0x2000 errors been seen on IOS before? **YES**
- How removal of QoS policy recovered from this issue on Singapore Node? **Rewrite structure getting reprogrammed after the policy is removal**
- Auto Detection and Recovery – **Scripts to search for PLIM/Parity error messages, re-add egress Qos Policy on all interfaces, OR Reload LC**

L3 Traffic Issue – SER Root Cause

- Problem NOT seen in 3.9 FCS image but could see with 3.7 image. Investigating further what code changes could have exposed this issue.
- The rewrite string is wrong causing the pkt to be dropped in sar
- Logs Analysis from local repro, highlighted portion below is the COSQ id

Packet Dump - Working case (Highlighted portion below is the COSQ id)

0001 0140 0002 0000 aaaa 0300 0000 0800 4500 0064 0001 0000 ff01 8b7d 0c0c 0c01

Packet Dump - Non working case

0125 0140 0002 0000 aaaa 0300 0000 0800 4500 0064 0004 0000 ff01 8b7a 0c0c 0c01

- Further investigation underway to nail down exact code change causing is issue

L3 Traffic Issue – Next Steps

- Identify exact trigger for PLIM error – What specific packet could cause this?
- Continue root cause investigation for SER issue, provide a SMU based upon 3.6.3 release

Problem Detection/Recovery

- Logs generated in XR

```
rx_xbma[77]: %L2-E3INGRESSQ-4-INTERRUPT :  PLIM error: reg
  0x2000

rx_xbma[77]: %L2-QM-4-INTERRUPT : INGRESSQ: ZBT parity error
```

- Logs generated in IOS

```
%EE48-4-QM_ZBT_PARITY_TRANSIENT

%EE48-3-BM_ERRS: ToFab BM PLIM error 2000
```

- The current recommendation based on our understanding of this issue is to reload the Line Card

Upgrade failures

- Suspect compatibility issues with memory used in failed E3 cards
  - Kernel crash pointing to “Invalid address access”
  - Once we are able to get memory used in AT&T, can proceed further
- Repro Update - Not yielding anything, need some ideas to proceed further
  - Upgrades were tried on 16-slot, 10-slot and 6-slot chassis, from 32S6r, 32S11n, 32S11o to 3.6.3 (+ SMU of CSCta18474 and CSCtd69603)
  - The 16-slot chassis is fully loaded with E3 cards (ATM and POS).
  - The RMAed card was also used (different memory)
  - MOP was followed (both power cycle and reload)
  - Rommon version, mbus version and fab loader version on some cards was same as that in failure case. (other cards had various versions – aim was to try upgrade with different versions)
  - Upgrades were done back to back several times
- Next Steps
  - Compare CI/GA MOP – Any changes exposing this issue?
  - Repro with RMAed boards – **WITH PHYSICAL MEM**
  - Debug in AT&T network during next upgrade cycle – DEs can join, live debug

E3 Issues – Post upgrade

Date	SR#	Node	Problem Category	Next Steps	Analysis
19-Apr	614172375	BEBRSL1001CR1	L3 traffic issue post upgrade, L2 traffic working fine **Problem reproduced in Cisco lab by injecting Parity error thru CLI.**	Check the behavior in IOS by injecting the same error MOP to ensure FPGA is upgraded before migration to XR Code review, comparison of IOS/XR error handling mechanism (SER – SW Error Recovery)	Rx_xbma INGRESSQ: ZBT parity error. Suspect some issue in SER triggered by this error
19-Apr	614169037	ATVINA1002CR1			Rx_xbma PLIM error (reg 0x2000), Suspect some issue in SER triggered by this error. Post RMA, FPGA version was old which resulted into other issues. Resolved after FPGA upgrade
22-Apr	614199033	SGSNGP1001CR1			Rx_xbma PLIM error (reg 0x2000), SER triggered. Suspect some issue in SER causing traffic halt

E3 Issues – During upgrade

Date	SR#	Node	Problem Category	Next Steps	Analysis
10-Feb	613620981	INCHNN1002CR1	Kernel crash during upgrade. No crash dump.	Repro in Cisco lab once cards/mem arrive. Scripts to do repeated upgrades, following same MOP, with exactly same configs and HW. Deep dive into what could lead to kernel crash without core dump	Suspect memory issue (HW) or illegal mem access (SW). 1G mem was removed before shipping the card to Cisco, not able to repro with local mem.
20-Feb	613694945	DEFRNK1002CR1			FA initiated, in transit
24-Feb	613721487	HUBDPS1002CR1			FA initiated, in transit. FW version <=1.13 not supported in XR, should not be related to this issue though

E3 Issues – During upgrade (cont..)

Date	SR#	Node	Problem Category	Next Steps	Analysis
19-Mar	613943445	FRPARI1002CR1	Continuous reboot during upgrade	Repro in Cisco lab once cards arrive. Scripts to do repeated upgrades, following same MOP, with exactly same configs and HW	No logs available for analysis. Provided restoration process and captures to be taken if issue is seen again.
12-Apr	614119857	CHGENV1002CR1			Suspect HW issue, LC went into XR run and then there was a PLIM reset
12-Apr	614120837	BRHORT1002CR1			Suspect HW failure since this didn't boot with IOS after downgrade.

SER - SW Error Handling

- As a part of handling the interrupt fired by RADAR, SER flushes the data path to clear/clean out the ASICs from the errors
  - Pausing rx alpha pipeline
  - Buffer recarve
  - Xbma, Alpha, PLIM re-init
- This is HIGH SEVERITY (but non-fatal) error, LC is not reloaded
- Impact
  - Temporary loss of traffic due to SER, while ASICs are being reset

ZBT Parity Error

- SSRAM (Connected to the QM only) - A ZBT memory, 4MByte, 64bit data bus.
- Each entry in the SSRAM represent one packet only and stores all the information needed for the RADAR to stream the packet through its blocks.
- Each entry contains the address of the buffer where the packet is stored - which is stable through out the life of the entry, and all packets represented by this entry will be stored in this location.
- The rest of the information is packet related and will be changed each time a new packet is being assigned to this entry.

ZBT Parity Error (Cont..)

- Whenever the QM detects bad parity from the external SSRAM it records which parity lane it was detected in, as well as the last address accessed.
- Error Reg value is 0x8000cb8e means – parity error QM_BAD_PAR_LANE_7 at address 0xcb8e.
- Bits 31:25 gives the SSRAM Bad Parity Location, which here is to be bit 31 set: SSRAM databits 63:56 (parity lane-7).
- Bits 18:0 gives the SSRAM address, which here is 0xcb8e.

PLIM error: reg 0x2000

- The "PLIM" portion of the message indicates that the condition encountered is associated with the PLIM (Alpha Interface) Module of the RADAR (queuing ASIC).
- The value of 0x2000 indicates that the condition causing the interrupt is E3_RADAR_PLIM_MAX_LEN_ERR.
- This indicates that a packet was received and placed into a buffer of insufficient length. This interrupt is indicative of a software problem where the microcode has somehow chosen a buffer that is too short for the packet that it is handling.

E3 HW FA Summary

- SR #613620981, 613694945, 613721487, 613943445, 614119857
  - Card failed to boot XR due to unknown memory detected
  - FA-0094547, FA-0095907 and FA-0096486 reported 256MB memory on the returned card
- SR #614120837
  - Card stuck in WAITRTRY even though correct memory is detected
- SR #614172375, 614169037, 614199033
  - Related to PLIM/Parity errors on Vienna/Brussels/Singapore Nodes
- Status of the FA cases:
  - FA-0094547 - The UUT failed to boot in IOX, so we tried booting with IOS. The unit booted without issues. During a show diag dump, we noticed that the processor memory for this LC was reading 256MB. After replaced them with two 512MB DIMMs, to give the LC 1GB of processor memory, we then booted the LC in IOX 3.6.3, and it booted without issues
  - FA-0096486 - Redirected for BU FA. The boards received has 2x128MB memory which is not sufficient for XR booting
  - FA-0095907 - Redirected by FA team to SJ from warehouse. In SJ, the LC received had MEM-LC-ISE-256 and hence after replacing with 1G memory on the LC , the LC has booted IOS and IOX without issues. But not sure how the memory got changed in the transit process
  - FA-0102597, FA-0101287, FA-0101315, FA-0102473, FA-0102395, FA-0102396 – In transit