Report Generated From Altium Designer

Name	Priority	Enabled	Type	Category	Scope	Attributes
AssemblyTestpoint	1	True	Assembly Testpoint Style	Testpoint	All	Under Comp - Allow Sides - Top, Bottom Pref Size = 1.524mm Pref Hole Size = 0.813mm Using Grid = Yes Grid = 0.025mm Grid Tolerance = 0mm
AssemblyTestPointUsage	1	True	Assembly Testpoint Usage	Testpoint	All	Testpoint - One Required Multiple - Not Allowed
BoardOutlineClearance	1	True	Board Outline Clearance	Manufacturing	All	Board Clearance = 0.4mm
Clearance_topbotPoly	1	True	Clearance	Electrical	InPolygon - (OnLayer('Multi-Layer') and IsPad) or OnLayer('L 01') or OnLayer('L 06')	Clearance = 0.2mm
ComponentClearance_J2PM"	1	True	Component Clearance	Placement	(InComponent('J2')) - (InComponent('PM2'))	Horizontal Clearance = -4mm Vertical Clearance = -1mm
DiffPairsRouting	1	True	Differential Pairs Routing	Routing	All	Pref Gap = 0.1mm Min Gap = 0.1mm Max Gap = 0.15mmPref Width = 0.1mm Min Width = 0.1mm Max Width = 0.15mm
Direct_J2	1	True	Polygon Connect Style	Plane	HasFootprint('STIFTLEISTE2_54 OG 1R-14') - All	Style - Relief Connect Width = 0.254mm Angle = 45 # Entries = 4 Air Gap = 0.254mm
Fanout_Small	1	False	Fanout Control	Routing	All	Style - Auto Direction - Alternating In and Out Via Grid = 0.025mm
Height	1	True	Height	Placement	All	Pref Height = 12.7mm Min Height = 0mm Max Height = 25.4mm
HoleSize	1	True	Hole Size	Manufacturing	All	Min = 0.2mm Max = 4mm
HoleToHoleClearance	1	True	Hole To Hole Clearance	Manufacturing	All - All	Hole To Hole Clearance = 0.254mm
LayerPairs	1	True	Layer Pairs	Manufacturing	All	Layer Pairs - Enforce
Lendht22mm	1	True	Length	High Speed	(InDifferentialPairClass('Lendht22mm'))	Min Length = 21.8mm Max Length = 22.2mm
MinimumAnnularRing	1	True	Minimum Annular Ring	Manufacturing	All	Min = 0.124mm
MinimumSolderMaskSliver	1	True	Minimum Solder Mask Sliver	Manufacturing	All - All	Minimum Solder Mask Sliver = 0.2mm
NetAntennae	1	True	Net Antennae	Manufacturing	All	Net Antennae Tolerance = 0mm
PasteMaskExpansion	1	True	Paste Mask Expansion	Mask	All	Expansion = 0mm
PermittedLayers-CAP3225	1	True	Permitted Layers	Placement	(HasFootprint('CAPC3216N'))	Permitted Layers - Top,
PlaneClearance	1	True	Power Plane Clearance	Plane	All	Clearance = 0.25mm
PlaneConnect_Via	1	True	Power Plane Connect Style	Plane	IsVia	Style - Direct Connect
RoutingCorners	1	True	Routing Corners	Routing	All	Style - 45 Degree Min Setback = 2.54mm Max Setback = 2.54mm
RoutingLayers	1	True	Routing Layers	Routing	All	TopLayer - Enabled MidLayer2 - Enabled MidLayer1 - Enabled MidLayer3 - Enabled MidLayer6 - Enabled BottomLayer - Enabled
RoutingPriority	1	True	Routing Priority	Routing	All	Priority = 0
RoutingTopology	1	True	Routing Topology	Routing	All	Topology - Shortest
RoutingVias	1	True	Routing Via Style	Routing	All	Pref Size = 0.5mm Pref Hole Size = 0.2mm
Schematic Supply Nets_4	1	True	Supply Nets	Signal Integrity	InNet('3.3V')	Voltage = 0.000
ShortCircuit	1	True	Short-Circuit	Electrical	All - All	Short Circuit - Not Allowed
SilkscreenOverComponentPads	1	True	Silk To Solder Mask Clearance	Manufacturing	IsPad - All	Silk To Solder Mask Clearance = 0.01mm
SilkToSilkClearance	1	True	Silk To Silk Clearance	Manufacturing	All - All	Silk to Silk Clearance = 0.01mm
SMDNeckDown_80%	1	True	SMD Neck-Down	SMT	All	Percent = 95%
SMDToPlane	1	True	SMD To Plane	SMT	All	Distance = 0.1mm
SolderMaskExpansion_Via	1	True	Solder Mask Expansion	Mask	IsVia	Expansion = -0.15mm
Testpoint	1	True	Fabrication Testpoint Style	Testpoint	(IsPad And (OnTopLayer Or OnBottomLayer))	Under Comp - Allow Sides - Top, Bottom Pref Size = 1.524mm Pref Hole Size = 0.813mm Using Grid = Yes Grid =

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						0.025mm Grid Tolerance = 0mm
TestPointUsage	1	True	Fabrication Testpoint Usage	Testpoint	All	Testpoint - One Required Multiple - Not Allowed
UnpouredPolygon	1	True	Modified Polygon	Electrical	All	Allow modified - No Allow shelved - No
UnRoutedNet	1	True	Un-Routed Net	Electrical	All	(No Attributes)
Width_S40	1	True	Width	Routing	InNetClass('S50')	Pref Impedance = 50.00ohms Min Impedance = 50.00ohms Max Impedance = 50.00ohms
Clearance	2	True	Clearance	Electrical	All - All	Generic clearance = 0.099mm, and 3 value(s) for objects
ComponentClearance_H3U7	2	True	Component Clearance	Placement	(InComponent('H3')) - (InComponent('U7'))	Horizontal Clearance = -0.5mm Vertical Clearance = -1mm
Fanout_Default	2	True	Fanout Control	Routing	All	Style - Auto Direction - Alternating In and Out Via Grid = 0.025mm
Logo	2	True	Width	Routing	(InComponent('LOGO*'))	Pref Width = 0.254mm Min Width = 0.001mm Max Width = 0.254mm
PlaneConnect	2	True	Power Plane Connect Style	Plane	All	Style - Relief Connect Expansion = 0.5mm Width = 0.2mm Gap = 0.25mm # Entries = 4
PolygonConnect_TopRilief	2	True	Polygon Connect Style	Plane	InPolygonClass('TopConnect') - All	Style - Relief Connect Width = 0.254mm Angle = 90 # Entries = 4 Air Gap = 0.2mm
Schematic Supply Nets_3	2	True	Supply Nets	Signal Integrity	InNet('1.8V')	Voltage = 0.000
SolderMaskExpansion	2	True	Solder Mask Expansion	Mask	All	Expansion = 0mm
All	3	True	Width	Routing	All	Pref Width = 0.2mm Min Width = 0.1mm Max Width = 3mm
ComponentClearance_-0.5mm	3	True	Component Clearance	Placement	HasFootprint('FIDU-DOT - small') OR HasFootprint('NetTieTOP_D35mm')or HasFootprint('MHole3_2mm') - All	Horizontal Clearance = -0.5mm Vertical Clearance = -0.013mm
Fanout_SOIC	3	False	Fanout Control	Routing	All	Style - Auto Direction - Alternating In and Out Via Grid = 0.025mm
PolygonConnect_Direct	3	True	Polygon Connect Style	Plane	(HasFootprint('MHole2_7mm')) or IsVia or InComponent('H1') or InComponent('H2') or InComponent('H3') or InComponent('H4') - All	Style - Direct Connect
Schematic Supply Nets_2	3	True	Supply Nets	Signal Integrity	InNet('5V')	Voltage = 0.000
ComponentClearance	4	True	Component Clearance	Placement	All - All	Horizontal Clearance = -0.05mm Vertical Clearance = 0.5mm
Fanout_BGA	4	False	Fanout Control	Routing	All	Style - Auto Direction - Alternating In and Out Via Grid = 0.025mm
PolygonConnect_Direct_TP	4	True	Polygon Connect Style	Plane	HasFootprint('TP_0.8mm') - All	Style - Direct Connect
Schematic Supply Nets_1	4	True	Supply Nets	Signal Integrity	InNet('GND')	Voltage = 0.000
Fanout_LCC	5	False	Fanout Control	Routing	All	Style - Auto Direction - Alternating In and Out Via Grid = 0.025mm
PolygonConnect	5	True	Polygon Connect Style	Plane	All - All	Style - Relief Connect Width = 0.2mm Angle = 90 # Entries = 4 Air Gap = 0.2mm
Schematic Supply Nets	5	True	Supply Nets	Signal Integrity	InNet('1.0V')	Voltage = 0.000