

ELEC 2210 LABORATORY REPORT COVER PAGE  
Complete and attach this page to the front of your lab report.

Meeting # 10      CMOS Logic  
*Title of Lab Experiment*

Student Name: Emerson, Gabriel  
*Name (Last, First, MI)*

Student Email: gfe0032  
*AU 7-character username*

GTA: Paul Atilola  
*Name of your GTA*

Section you are enrolled in: (Circle One): 1 2 3 4 5 6 7 8

Date experiment performed (dd / mm / yy): 03/23/21

Date report submitted: (dd / mm / yy): 04/05/21

If you performed this experiment at a time other than your regularly scheduled section meeting:

Section # of the section you sat in on (Circle One): 1 2 3 4 5 6 7 8 Makeup

Name of the GTA who supervised your work: \_\_\_\_\_

I hereby certify that the contents of this report are true and complete to the best of my ability.  
The lab work was performed by me exclusively, and this report was written by me exclusively.

  
Student signature

04/05/21  
Date signed

Gabriel Emerson  
ELEC 2210 – T 11:00  
Experiment #10 CMOS Logic Circuits  
03/23/2021

### Introduction:

The goal of this lab is to experiment with NMOS and PMOS transistors and understand how to connect them to form CMOS inverters. CD4007 chips will be used to form inverter chains, transmission gates, and D-latches. This lab will provide further experience on the NI Elvis Board and knowledge of CMOS inverter characteristics.

### Step 1: CMOS Inverter Chain

Using a CD4007 chip and the connections provided in the manual, an inverter chain was constructed on the wiring board. Using probes, the output of each inverter was taken and displayed on the oscilloscope. As expected, the signal inverted after going through the inverter. The square wave also became more defined after passing through each inverter, having sharper transitions. These changes can be observed in the figures below.

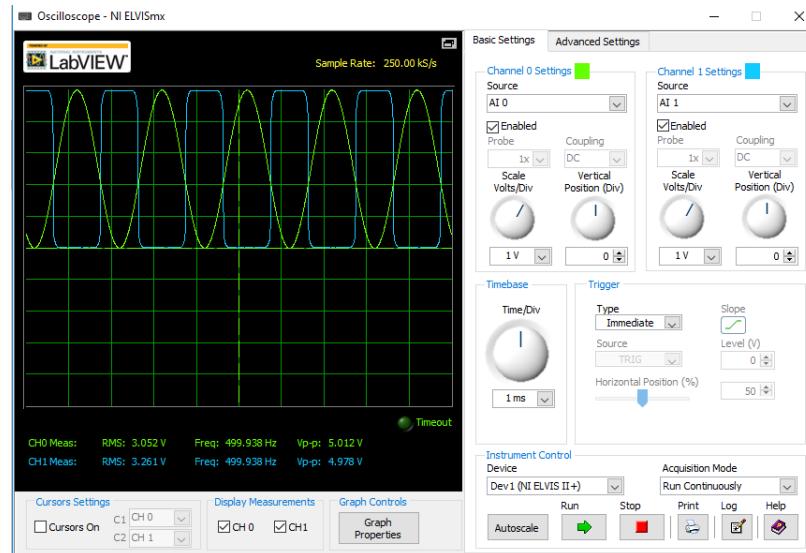


Figure 1: First Inverted Output

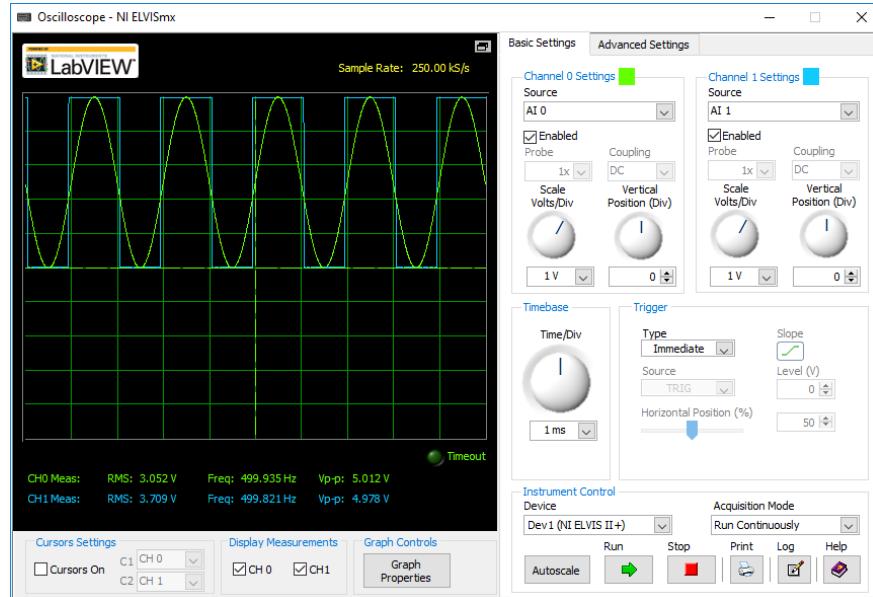


Figure 2: Second Inverted Output

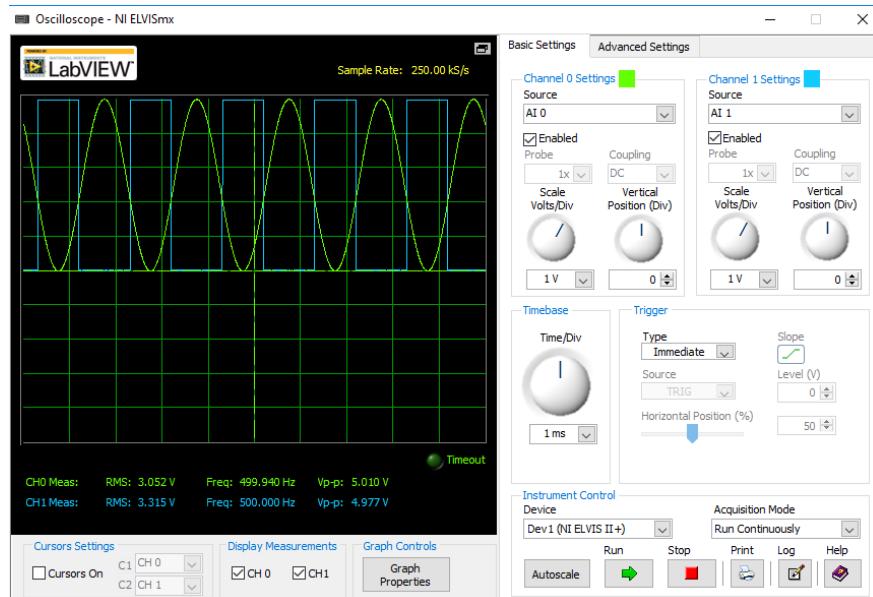


Figure 3: Third Inverted Output

## Step 2: CMOS Transmission Gates

Using a new CD4007 chip, the diagram, and the connections provided in the lab manual, a transmission gate was constructed on the wiring board. The function generator was used to produce a 500Hz square wave with a 5V peak to peak value. To test functionality, the Digital Writer was used to simulate clock pulses and the waveforms were evaluated on the oscilloscope. Screenshots of the results can be seen below.

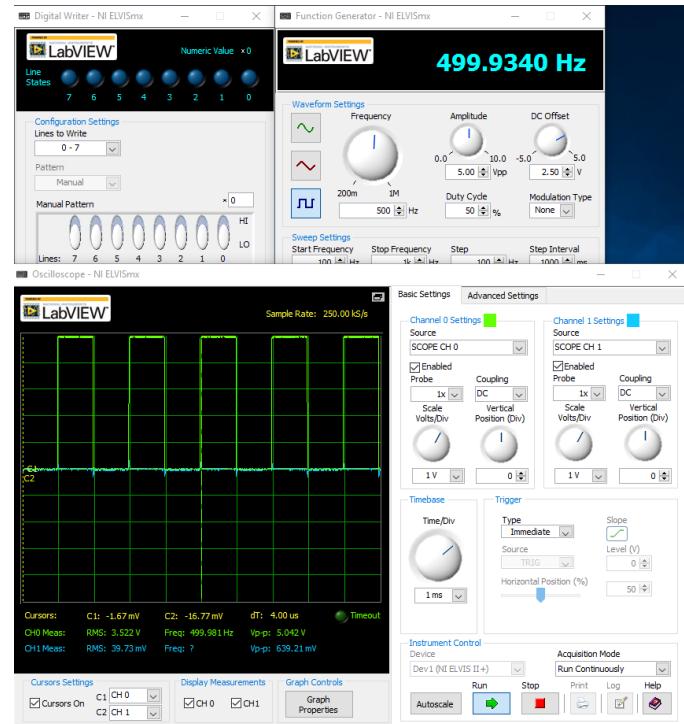


Figure 4: Clock = 0

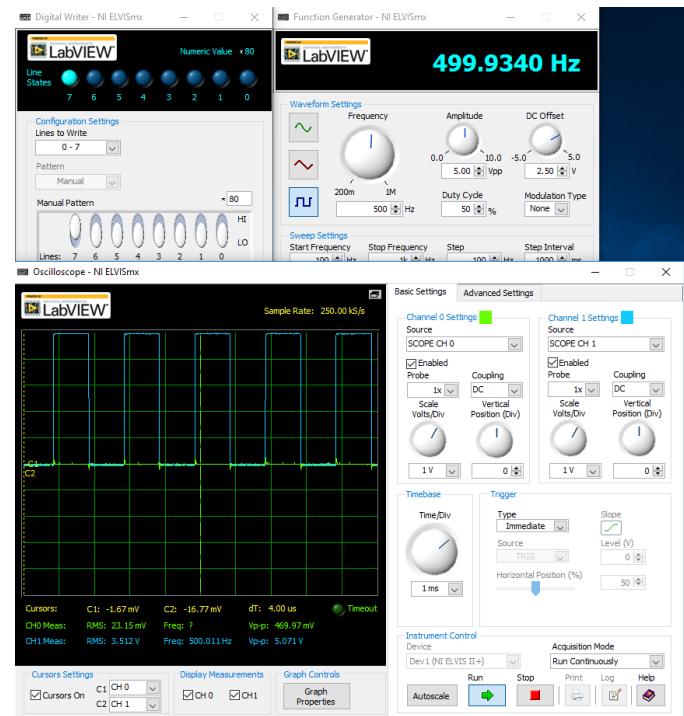


Figure 5: Clock = 1

### Step 3: D-Latch

Combining the circuits from Step 1 and 2, a D-Latch was created. When the clock signal was logic low, the latch was in a transparent phase. This means that the input to the latch would also be the output. When the clock was logic high, whatever value was in the latch previously would be held. These results can be seen below.

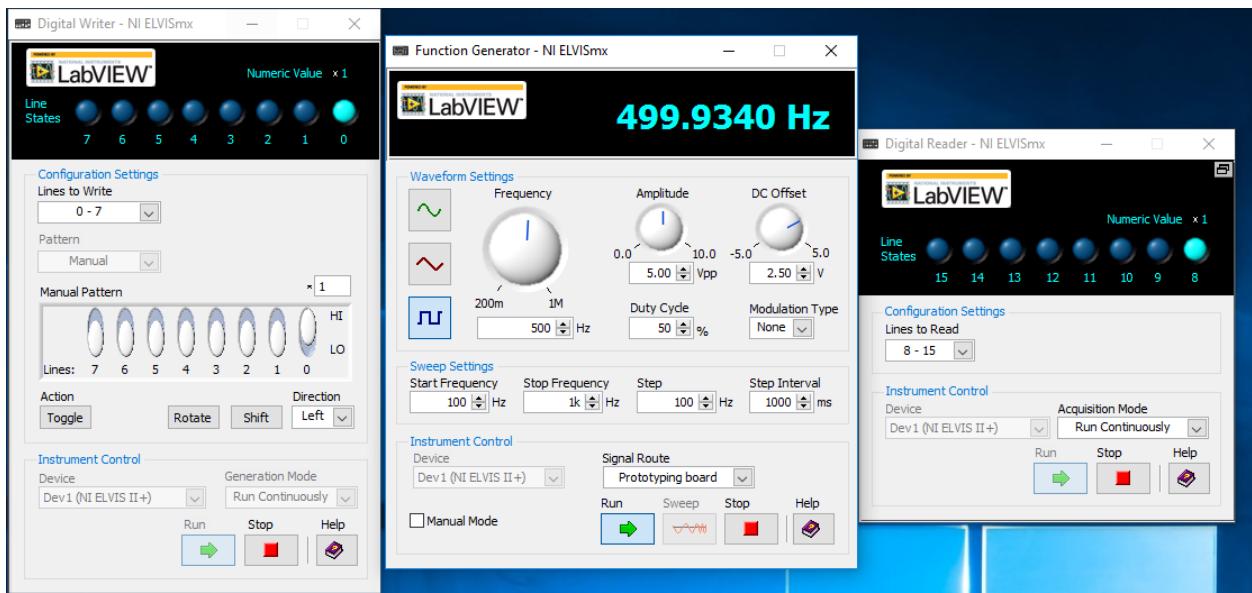


Figure 6: Input High – Output High

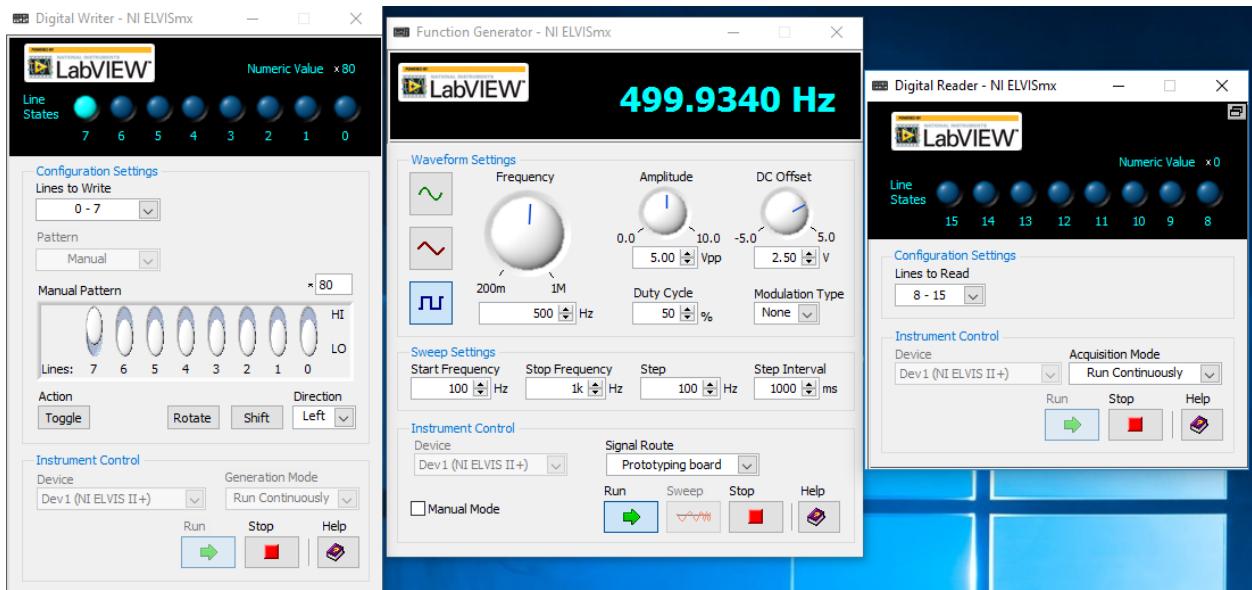


Figure 7: Holding Previous Output

### Bonus: Master-Slave D Flip-Flop

To convert the D-Latch to a D Flip-Flop, a copy of the Step 3 circuit was created with an inverted clock signal. If correctly assembled, one should be able to determine if it is rising edge or falling edge triggered as well as test the Flip Flop logic for functionality. Below I have figure 8, which shows the output voltage of the second inverter and voltage across the capacitor. In figure 9, it shows the output voltage of the second inverter and the voltage at node C.

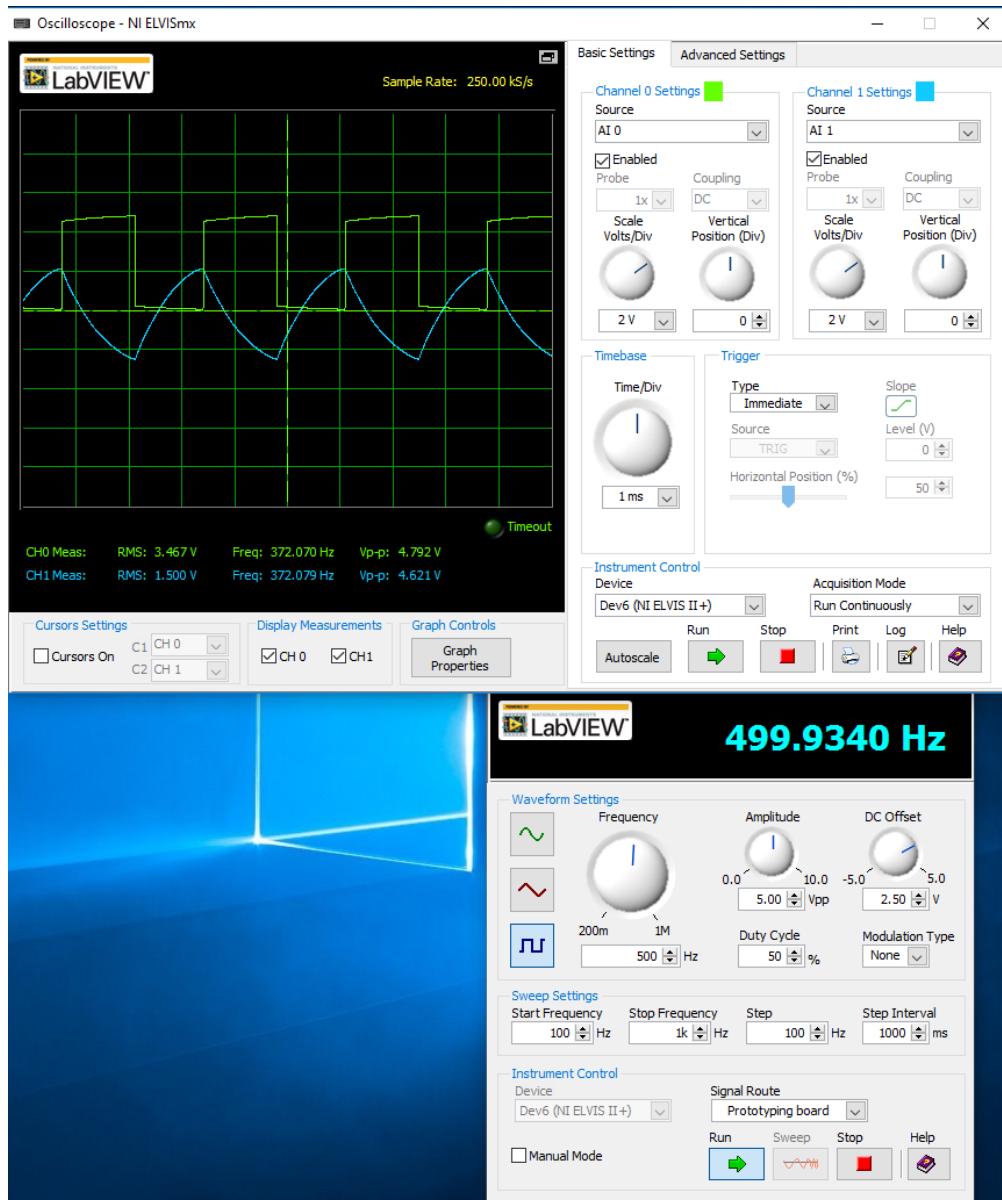


Figure 8: Master-Slave D Flip Flop

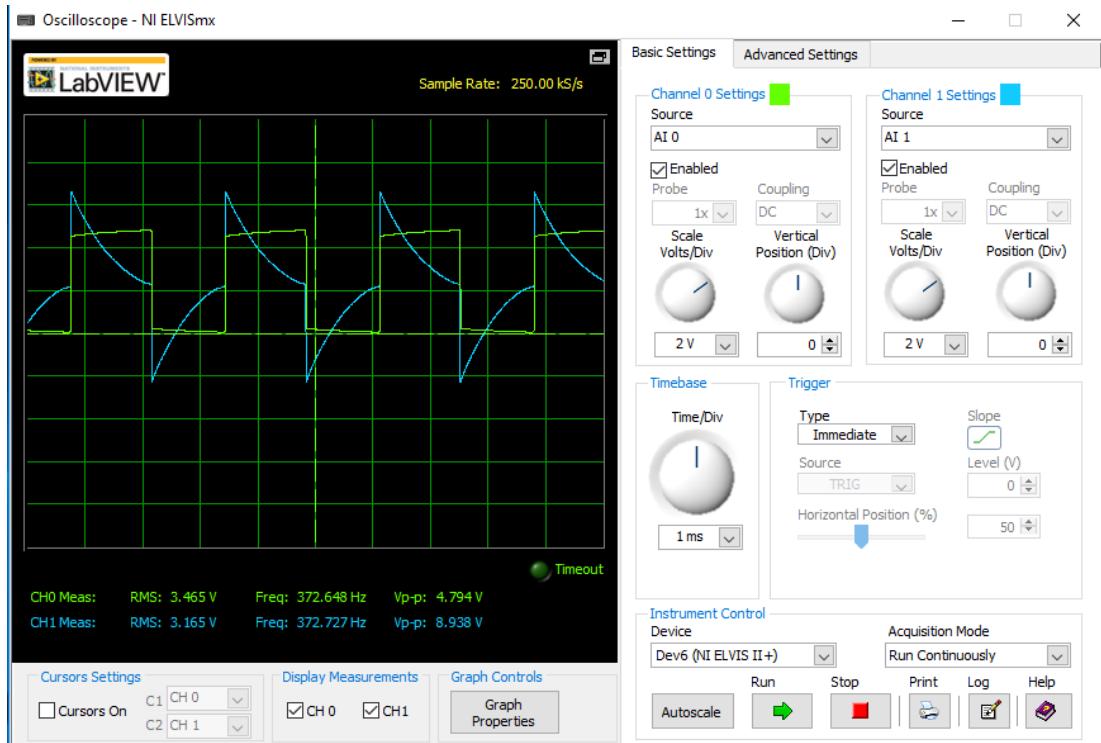


Figure 9: Master-Slave D Flip Flop

### Conclusion:

After completing this lab, I am more confident on how to use a CD4007 as a CMOS inverter and how to use multiple chips to create a chain of inverters. I can see how this might come in handy during the final lab design. I also learned how to create a D-latch which will help in the future for logic diagrams. I was slightly confused at first when assembling the flip flop in the bonus. However, I think that I gained a lot from this lab and that it was good preparation for the wiring difficulty that will be on our lab final.

ELEC 2210 Lab Checklist

Student Name Gabriel Emerson

Meeting Date & Time 11:00 T GTA Name Paul Atilola

Section # 001 Station # \_\_\_\_\_

Meeting # & Title 10 CMOS Logic

Student Instructions: Fill in the items to be checked off by the GTA. When you are ready for checking off, notify the GTA. Include this sheet in your lab report.

GTA Instructions: Initial the student activities as requested in the experiment. Include comments as appropriate.

Part 1 CMOS inverter Chain GTA Initials P·O·A

Comments (GTA / Student):

Part 2 CMOS Transmission Gates GTA Initials P·O·A

Comments (GTA / Student):

Part 3 D-latch GTA Initials P·O·A

Comments (GTA / Student):

Part 4 Bonus GTA Initials P·O·A\*

Comments (GTA / Student):

Cleanup Inspection

GTA Initials P·O·A