

ELEC 2210 LABORATORY REPORT COVER PAGE
Complete and attach this page to the front of your lab report.

Meeting # 5 Switch Debounce Circuit
Title of Lab Experiment

Student Name: Emerson, Gabriel
Name (Last, First, MI)

Student Email: gfe0002
AU 7-character username

GTA: Paul Atilola
Name of your GTA

Section you are enrolled in: (Circle One): 1 2 3 4 5 6 7 8

Date experiment performed (dd / mm / yy): 02/09/21

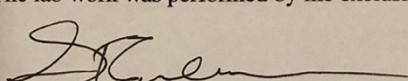
Date report submitted: (dd / mm / yy): 02/15/21

If you performed this experiment at a time other than your regularly scheduled section meeting:

Section # of the section you sat in on (Circle One): 1 2 3 4 5 6 7 8 Makeup

Name of the GTA who supervised your work: _____

I hereby certify that the contents of this report are true and complete to the best of my ability.
The lab work was performed by me exclusively, and this report was written by me exclusively.



Student signature

02/15/21

Date signed

Gabriel Emerson
ELEC 2210 – T 11:00
Experiment #5: Switch Debounce Circuits
02/09/21

Introduction

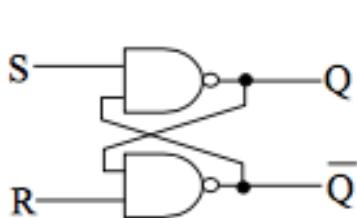
The purpose of this lab is to refresh students on latches from digital logic circuits and introduce them to the bounce that occurs from using electromechanical buttons. The signal from this type of button is not reliable unless the bounce is accounted for. The students will use a counter, NAND gates, and an oscilloscope to build and verify a latching circuit that can bypass the bounce of a button. After completing this lab, students should realize the significance of having clear digital signals.

Step 1:

A single pole double throw (SPDT) pushbutton switch was connected to a power source, LED 6, and LED 7. LED 6 and 7 were also connected to DIO 14 and 15 so the state could be seen by the Digital Reader. If it was operating properly, LED would be on until the button was pressed. Once this occurred, it would turn off and LED 6 would turn on in its place.

Step 2:

Using the prelab schematic and the 7400 IC, the RS Latch was created on the breadboard. Output Q was connected to LED 5 and DIO 13 while Qbar was connected to LED 4 and DIO 12. The inputs to the NAND gates were connected to DIO 1 and 2, therefore being able to be tested using the Digital Writer. The latch inputs were changed, and the LED outputs were checked with the truth table to make sure the latch was working properly.



S	R	Q^+	Function
1	1	Q	storage (hold) state
1	0	0	reset state
0	1	1	set state
0	0	1	indeterminate

Figure 1: SR Latch and Truth Table

Step 3:

DIO 1 and 2 were disconnected and the SPDT was installed with reference to ground. The NO position was connected to R and the NC position was connected to S. Two 10k resistors were added in series with a 5V power supply to the latch inputs. Two channels were measured using the oscilloscope: latch input R and latch output Q. After ten uses, the result with the worst input bounce was compared to the debounced output. This can be seen below.

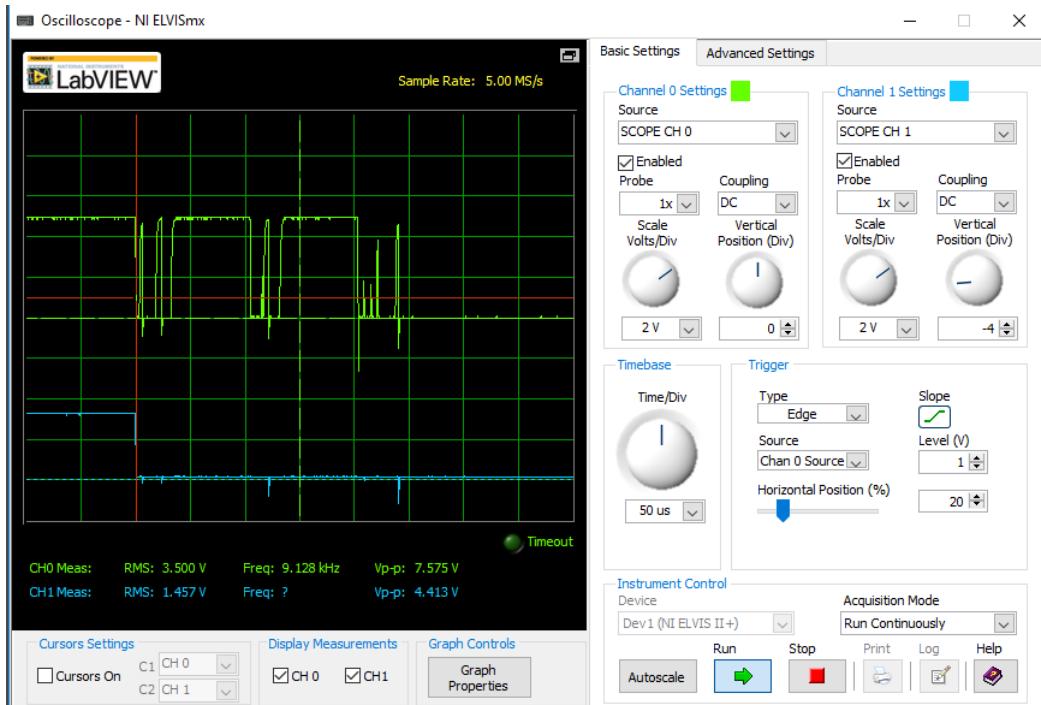


Figure 2: Oscilloscope Results

Step 4:

Using the prelab schematic, the 74161 counter was added to the circuit by connecting the latch output Q to the clock input of the counter. The counter outputs were connected to LEDs 0-3 and DIO 8-11 to be easily monitored. Once the setup was complete, pressing the pushbutton of the SPDT would increment the counter by one. If the debounce was implemented, the counter worked as expected. However, once it was bypassed, the counter acted erratically and the next state could not be determined, as there was no telling how many times the bounce incremented the counter.

Conclusion:

This lab taught me the importance of grasping circuit design techniques. On paper, things like debounce do not come into play. The circuit design should work as expected with no unexpected bumps along the way. However, in reality, debounce is a very real issue that is our job to overcome as the designer. So I think it is very important for us to be introduced to problems like this and learn ways to overcome them. This lab was similar to a project I had in Computer Systems and I really enjoyed seeing how the circuit was actually designed. This lab also did a good job of reminding me about logic latches and the concepts behind how they work. I did not run into trouble this lab and I think it excelled at teaching the importance of proper circuit design.

ELEC 2210 Lab Checklist

Student Name Gabriel Emerson

Meeting Date & Time T 11:00 GTA Name Paul Atilola

Section # 001 Station # _____

Meeting # & Title 5 Switch Debounce Circuits

Student Instructions: Fill in the items to be checked off by the GTA. When you are ready for checking off, notify the GTA. Include this sheet in your lab report.

GTA Instructions: Initial the student activities as requested in the experiment. Include comments as appropriate.

Part 1 Step 1 GTA Initials P.O.A.

Comments (GTA / Student):

Part 2 Step 2 GTA Initials P.O.A

Comments (GTA / Student):

Part 3 Step 3 GTA Initials _____

Comments (GTA / Student):

Part 4 Step 4 GTA Initials P.O.A.

Comments (GTA / Student):

Cleanup Inspection GTA Initials P.O.A.