Gabriel Emerson gte0002 | CMOS HW1 | Due 3/12

1.) NMOS
$KP = 300 \frac{mA}{V^2}$
$V_{TO} = 0.5V$

PMOS
$KP = 150 \frac{mA}{V^2}$
$V_{TO} = -0.5V$

0.25mm CMOS

$V_{DD} = 3V$

$\frac{W_P}{L_P} = \frac{300}{150} \cdot 2 = \frac{4}{1}$

NMOS	PMOS
W = 0.5mm	W = 1mm
L = 0.25mm	L = 0.25mm

2.) For CMOS:

a.) $V_L = 0V$ $V_H = 3V$

b.) Standby power consumption = 0V

c.) V_L and V_H will be the same.

d.) $V_{DD} \rightarrow 4V$: Standby power consumption = 0V

e.) $V_{IL} = 1.25V$ $V_{IH} = 1.75V$

$V_{OH} = 2.75V$ $V_{OL} = 0.25V$

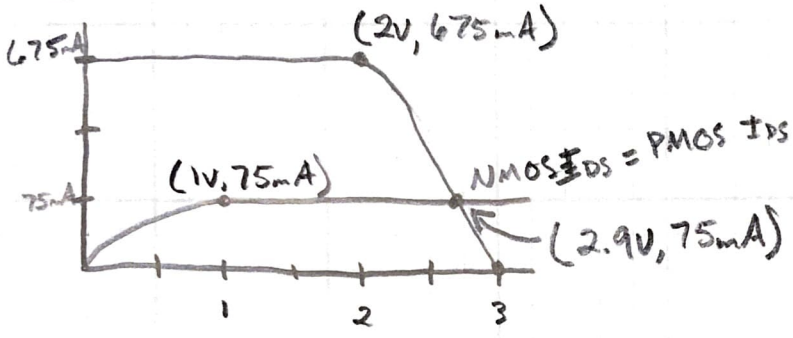
f.) Noise Margin Low → 1
Noise Margin High → 1

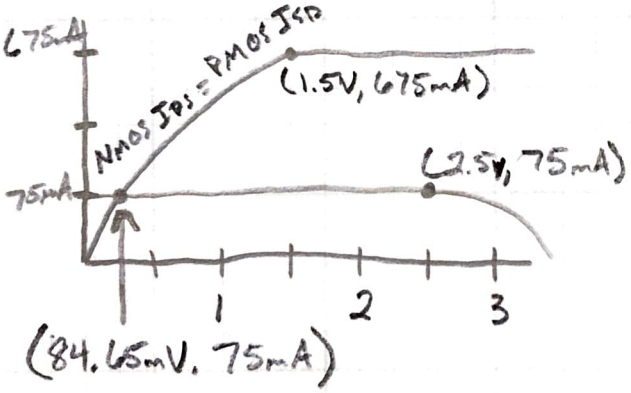
g.) Symmetry remains but it is shifted to 2v due to V_{DD} being 4V. The circuit does still work like an inverter. However the NML and NMH will increase which is something we do not want.

3a) $V_{in} = 1V$, $V_{in} = 2V$

1V
$\frac{1}{2}(300)(2)(1-0.5)^2 = 75mA \rightarrow I_{DS}$, NMOS
$I_{SD} = \frac{1}{2}(150)(4)(-2-(-0.5))^2 = 675mA$, PMOS

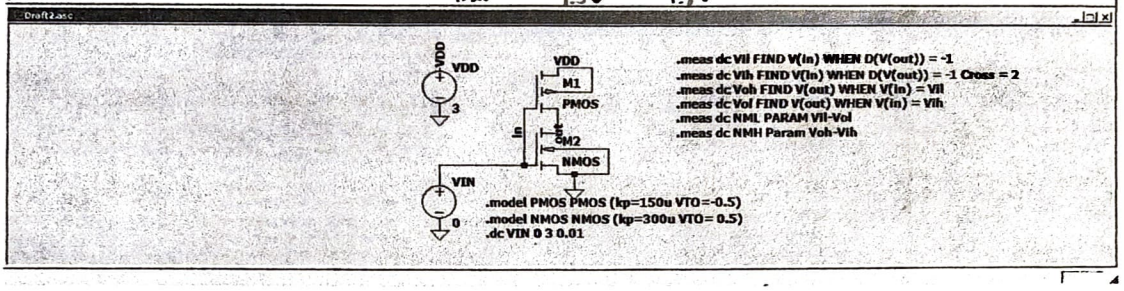
2V
$I_{DS\,sat} = \frac{1}{2}(300)(2)(2-0.5)^2 = 675mA$, NMOS
$I_{DS\,sat} = \frac{1}{2}(150)(4)(-1-(-0.5))^2 = 75mA$, PMOS

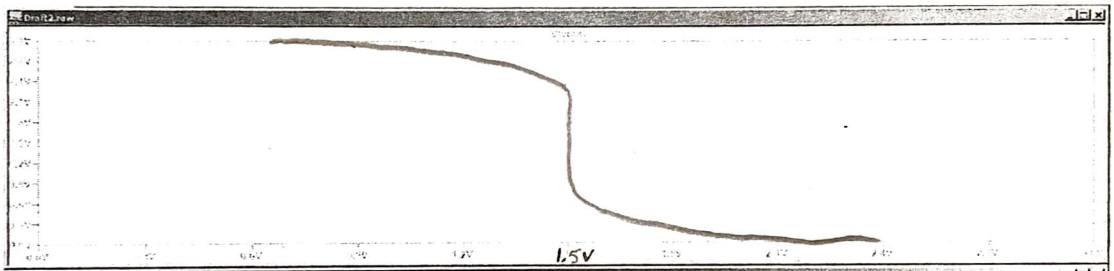


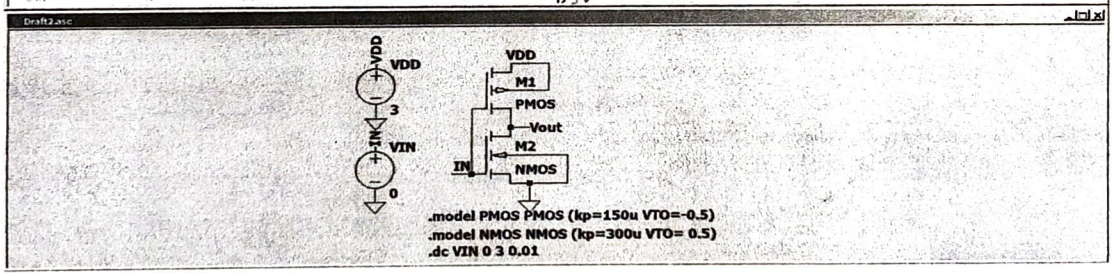


yes hand calculations are close to simulations.


Draft2.raw
1.2v
1.5v
1.9v


Draft2.asc
VDD
3
VIN
0
M1
PMOS
M2
NMOS
Vout
IN
.meas dc Vil FIND V(In) WHEN D(V(out)) = -1
.meas dc Vih FIND V(In) WHEN D(V(out)) = -1 Cross = 2
.meas dc Voh FIND V(out) WHEN V(in) = Vil
.meas dc Vol FIND V(out) WHEN V(in) = Vih
.meas dc NML PARAM Vil-Vol
.meas dc NMH Param Voh-Vih
.model PMOS PMOS (kp=150u VTO=-0.5)
.model NMOS NMOS (kp=300u VTO= 0.5)
.dc VIN 0 3 0.01


Draft2.raw
1.5V


Draft2.asc
VDD
3
IN
VIN
0
M1
PMOS
Vout
M2
NMOS
.model PMOS PMOS (kp=150u VTO=-0.5)
.model NMOS NMOS (kp=300u VTO= 0.5)
.dc VIN 0 3 0.01

```
Instance "M2": Length shorter than recommended for a level 1 MOSFET.
Instance "m2": Width narrower than recommended for a level 1 MOSFET.
Instance "m1": Length shorter than recommended for a level 1 MOSFET.
Instance "m1": Width narrower than recommended for a level 1 MOSFET.

vil: v(in)=1.24998 at 1.24998
vih: v(in)=1.75002 at 1.75002
voh: v(out)=2.75002 at 1.24998
vol: v(out)=0.24998 at 1.75002
nml: vil-vol=0.999999
nmh: voh-vih=1


Date: Thu Feb 28 11:38:56 2019
Total elapsed time: 0.102 seconds.

tnom = 27
temp = 27
method = trap
totiter = 637
traniter = 0
tranpoints = 0
accept = 0
rejected = 0
matrix size = 5
fillins = 0
solver = Normal
Matrix Compiler1: 132 bytes object code size  0.1/0.1/[0.1]
```