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ELEC 4200 – Lab 9
10/28/21

Lab 9: XDC Macros

Goals:

The goal for this lab is to understand and design circuits with Macros. This means to become familiar with RTL design, and how the Synthesis of circuits can be helpful for the design. We also have to design two Ring Oscillator circuits using Gate-Level modeling. The Macros are very important in the design of circuits because they add a new level of realism to the simulation of these circuits created in Verilog. This also makes the simulation of circuits more ideal in all instances of circuit design.

Design Process:

Task 1 and 2 are very similar in design. For task 1, we will design a 5 Ring Oscillator using AND gates. Then we will use the tools given in Vivado to synthesize the circuit and view the design. Then we will simulate the design. The simulation expected result should look like the one given in Figure 1.

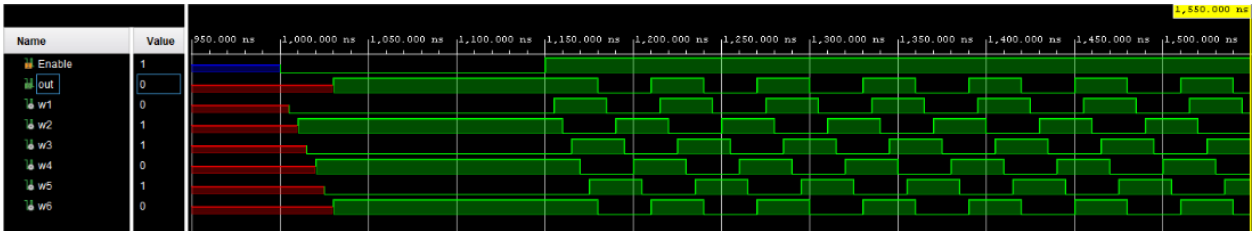

Figure 1

Task 2 is very similar to that of task 1. Instead of creating a 5 stage Ring Oscillator, we modify the circuit to be a 9 Ring Oscillator. Besides the change of the circuit design, everything else matches that of the previous task. The simulation results should match the previous in Figure 1, except with more wires in the same pattern of task 1. See Figure 1 above to verify.

Detailed Design:

Task 1 and 2 are very similar in the design, synthesis, and simulation of the circuit. The code for both will change slightly by simply adding more NOT gates to create more ring oscillators. The code for Task 1 and 2 are shown in Figures 2 and 3 respectively.

```
module Lab9_1(enable,out);
    input enable;
    output out;
    (* ALLOW_COMBINATIONAL_LOOPS = "TRUE" *)
    (* DONT_TOUCH = "TRUE" *) wire w1, w2, w3, w4, w5, w6;

    and #5(w1, enable, out );
    not #5(w2, w1);
    not #5(w3, w2);
    not #5(w4, w3);
    not #5(w5, w4);
    not #5(w6,w5);
    assign out = w6;
endmodule
```

Figure 2

```
module Lab9_2(enable,out);
    input enable;
    output out;
    (* ALLOW_COMBINATIONAL_LOOPS = "TRUE" *)
    (* DONT_TOUCH = "TRUE" *) wire w1, w2, w3, w4, w5, w6, w7, w8, w9, w10;

    assign out = w10;
    and #5(w1, enable,out );
    not #5(w2, w1);
    not #5(w3, w2);
    not #5(w4, w3);
    not #5(w5, w4);
    not #5(w6,w5);
    not #5(w7,w6);
    not #5(w8,w7);
    not #5(w9,w8);
    not #5(w10,w9);
endmodule
```

Figure 3

After the creation of the circuit, we are to synthesize the design and use the TCL commands to add our circuit in the device view. The commands used to do this for Task 1 and Task 2 are shown in Table 1. Then after adding to the device view, the device will look like the one shown in Figures 4 and 5 for Task 1, and Figures 6 and 7 for Task 2.

Task	TCL Command
Task 1	create_macro RO update_macro RO {w1_inferred_i_1 X0Y0 w2_inferred_i_1 X0Y0 w3_inferred_i_1 X0Y0 w4_inferred_i_1 X0Y1 w5_inferred_i_1 X1Y0}
Task 2	create_macro update_macro RO {w1_inferred_i_1 X0Y0 w2_inferred_i_1 X0Y0 w3_inferred_i_1 X0Y0 w4_inferred_i_1 X0Y0 w5_inferred_i_1 X1Y0 w6_inferred_i_1 X1Y0 w7_inferred_i_1 X1Y0 w8_inferred_i_1 X1Y0 w9_inferred_i_1 X0Y1 w10_inferred_i_1 X0Y1}

Table 1

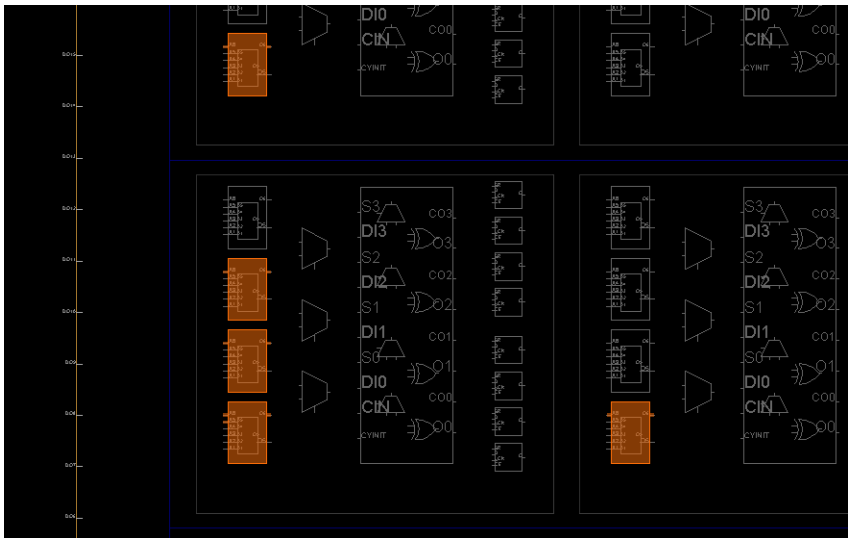

Figure 4

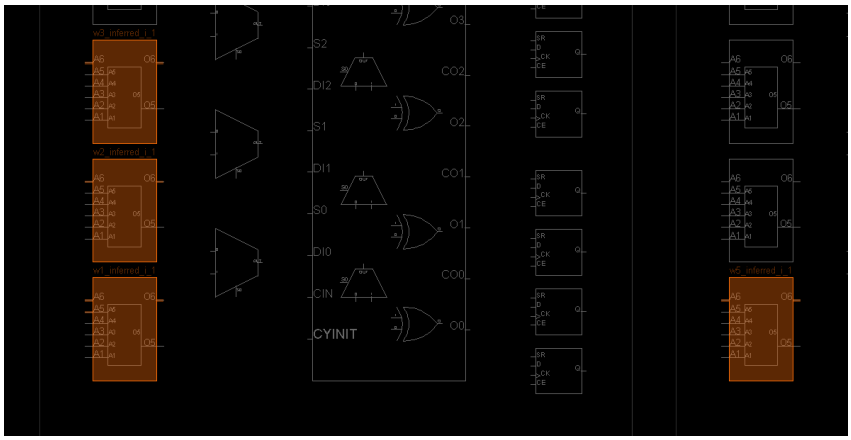

Figure 5

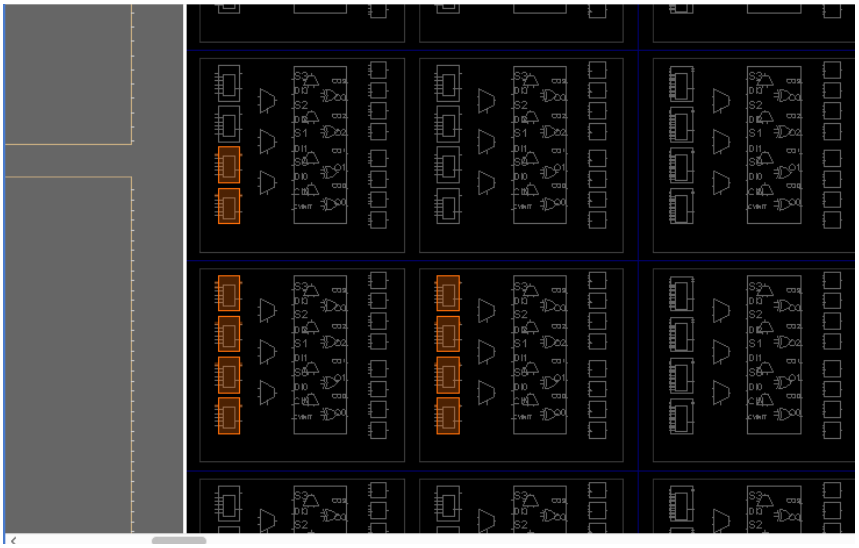

Figure 6

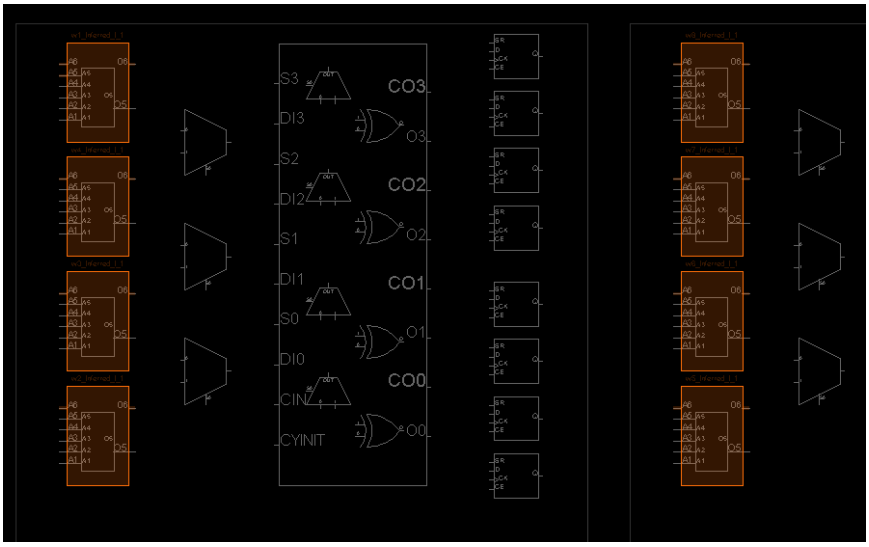

Figure 7

Verification:

Both of these tasks are verified by using a simulation testbench that is developed, since the two circuits are essentially the same in functionality, we can use the same testbench for both tasks, which looks like the one shown below in Figure 8.

```
module Lab9_1_tb();
    reg enable;
    wire out;

    Lab9_1 DUT ( .enable(enable), .out(out) );

    initial begin
        enable = 1'b0;
        #150 enable = 1'b1;
        #450 $stop;
    end
endmodule
```

Figure 8

After setting up the device in the synthesis menu, we can now run the simulation and compare the outputs of each to the expected result given at the beginning of the lab. The results for the simulation of Task 1 and 2 are shown below in Figures 9 and 10.

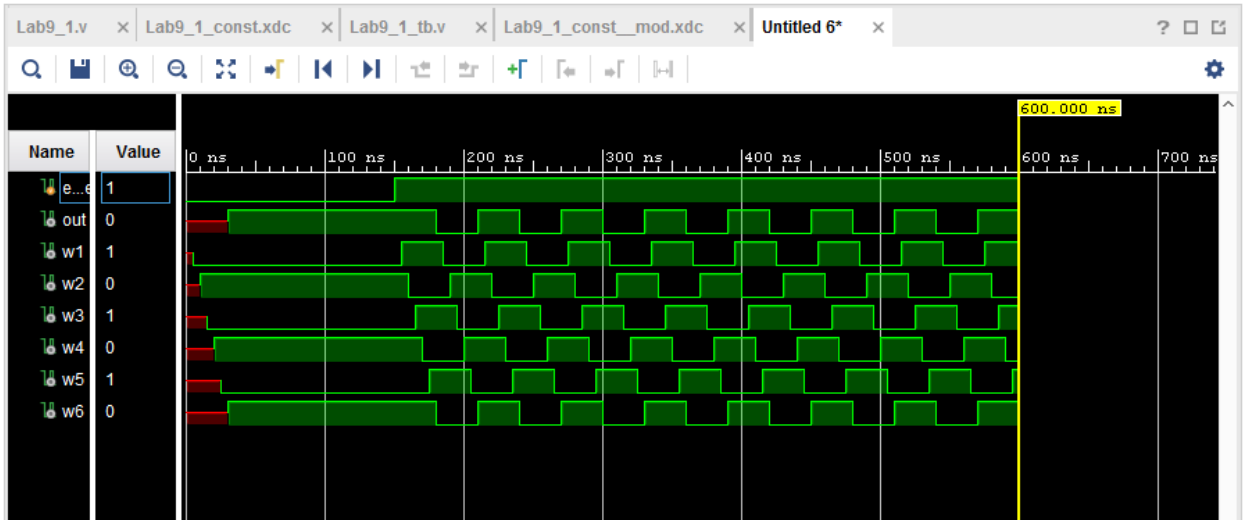

Figure 9

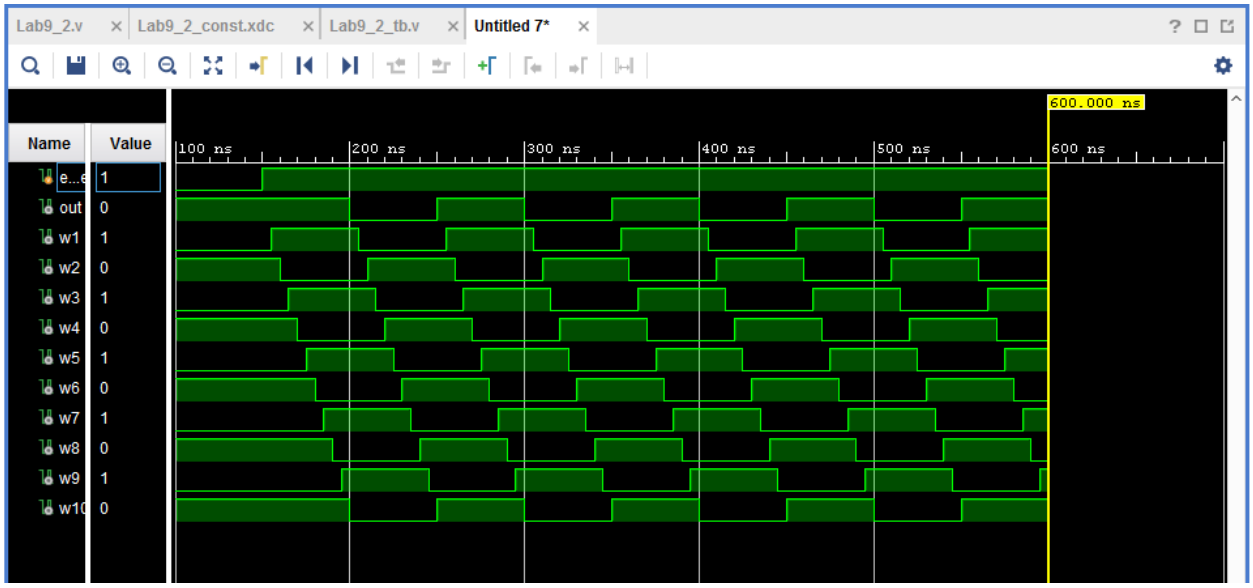

Figure 10

Conclusion:

What I learned in this lab is how effective the RTL design tools are that are given in Vivado. Macros can be a powerful tool for the complete design of a system and help to ensure the correct design. I also learned what a Ring Oscillator circuit is, and how it can be used to measure the delay of a gate using the simulation. This lab also helped to enforce ideas of writing our own testbench and using Gate-Level Modelling. This lab went well since I was well prepared at the start of the lab which made the overall lab time go much faster.