Sistemi Operativi

Corso di Laurea in Informatica

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SAPIENZA
UNIVERSITÀ DI ROMA

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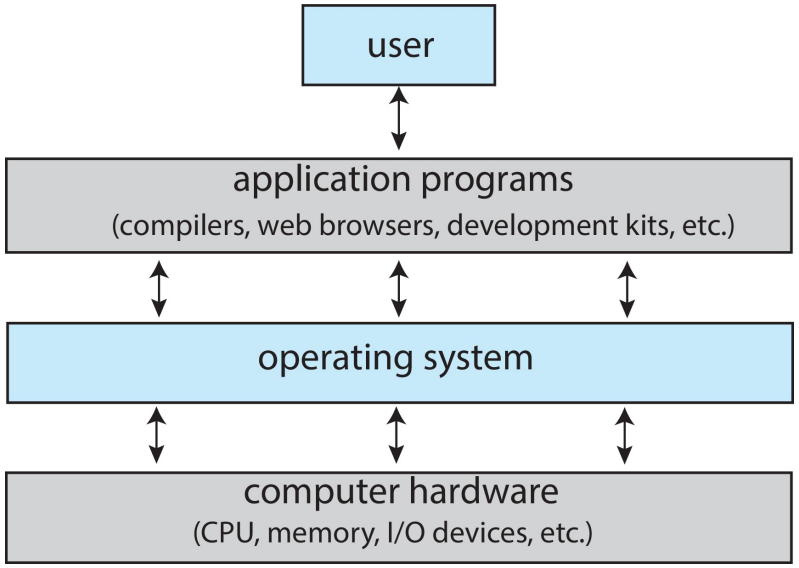
Recap from Last Lecture

- Operating System is a complex system which plays several roles:
  - resource manager
  - virtual machine
  - HW/SW interface



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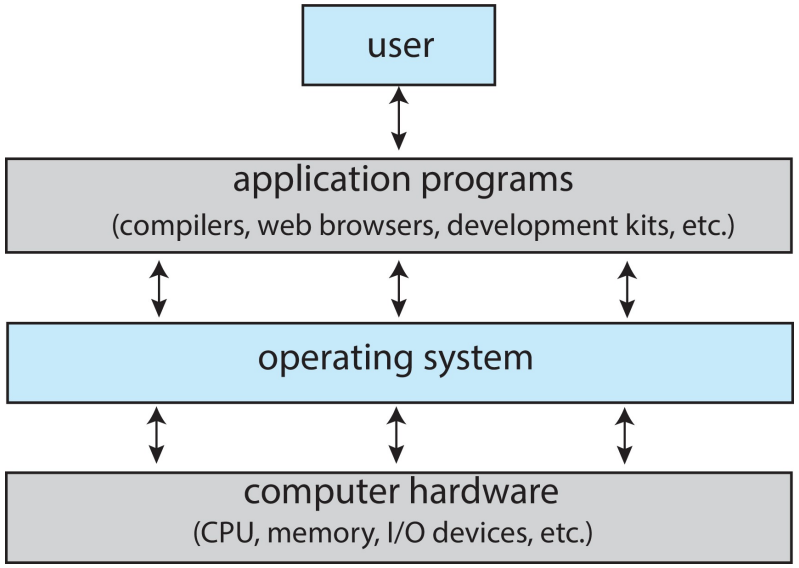

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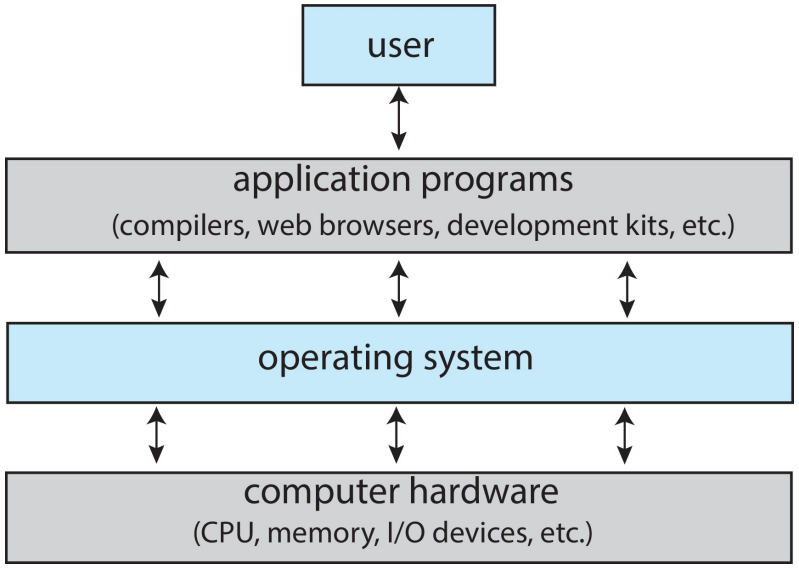
- Changes in HW may affect OS design



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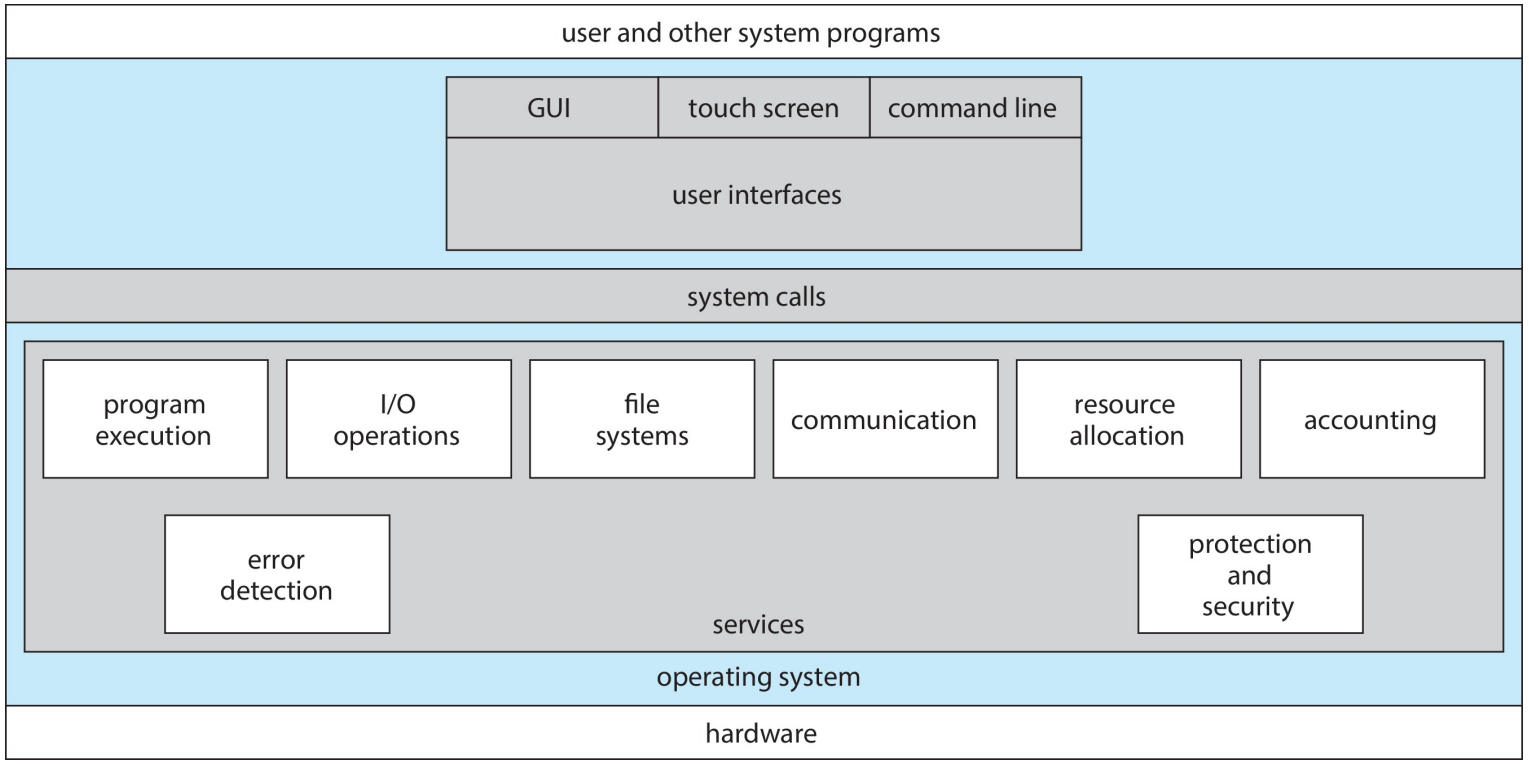
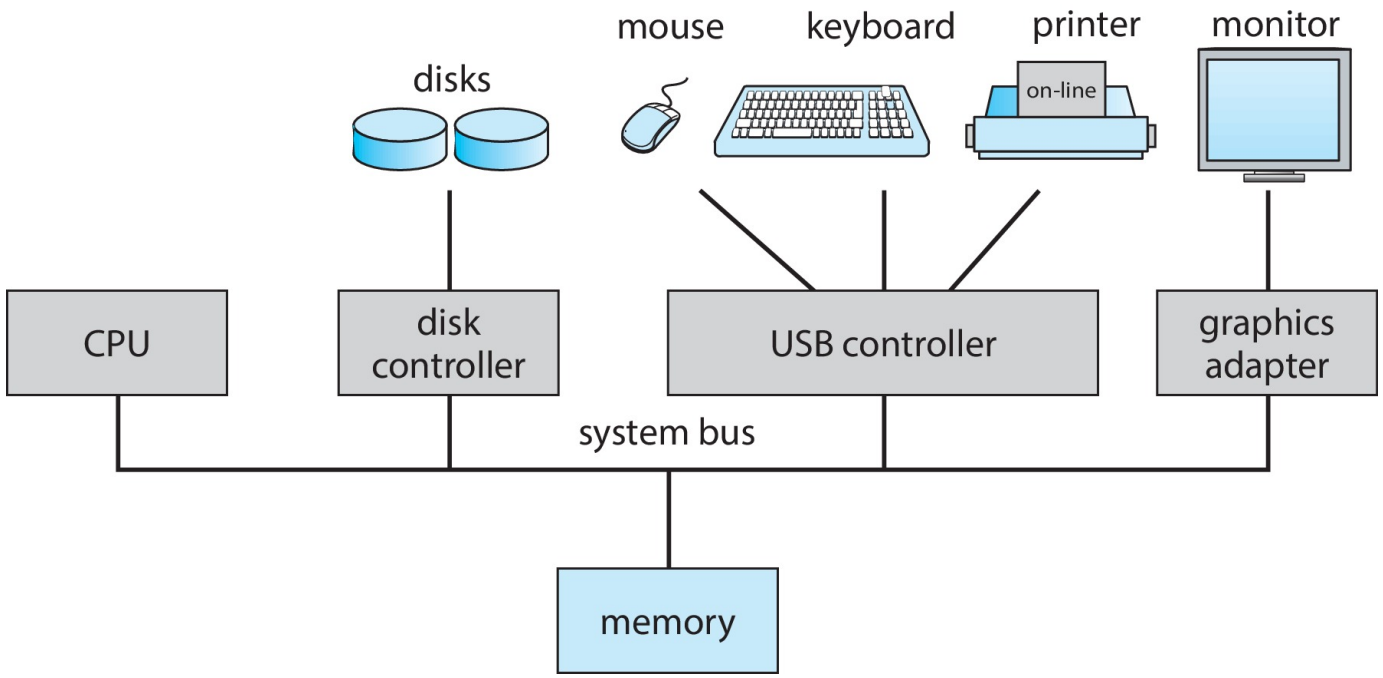
- Architectural support may significantly simplify or complicate the OS design

Modern OS Functionalities



Generic High-Level Computer Architecture



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  - associated with specific device controllers
- **System Bus** → communication medium between CPU, memory, and peripherals

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  - PCs/laptops
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John von Neumann

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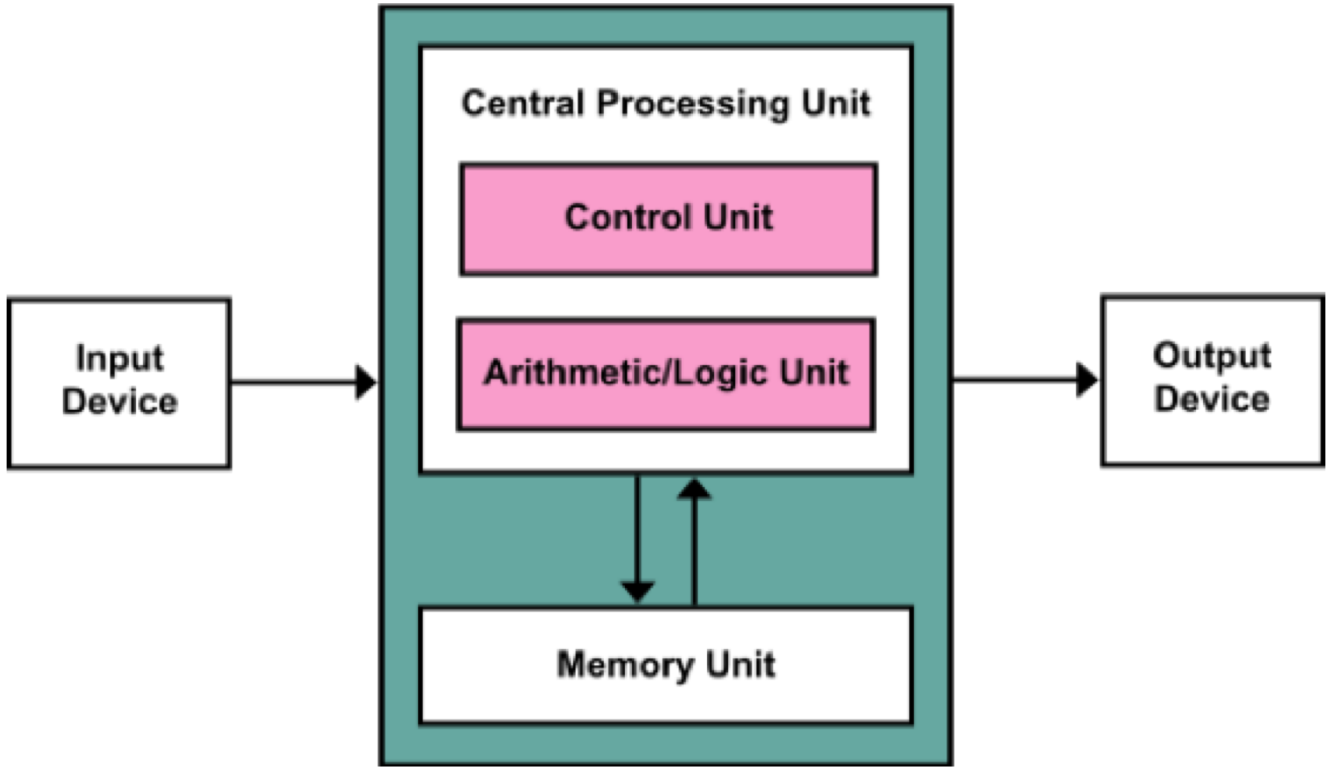
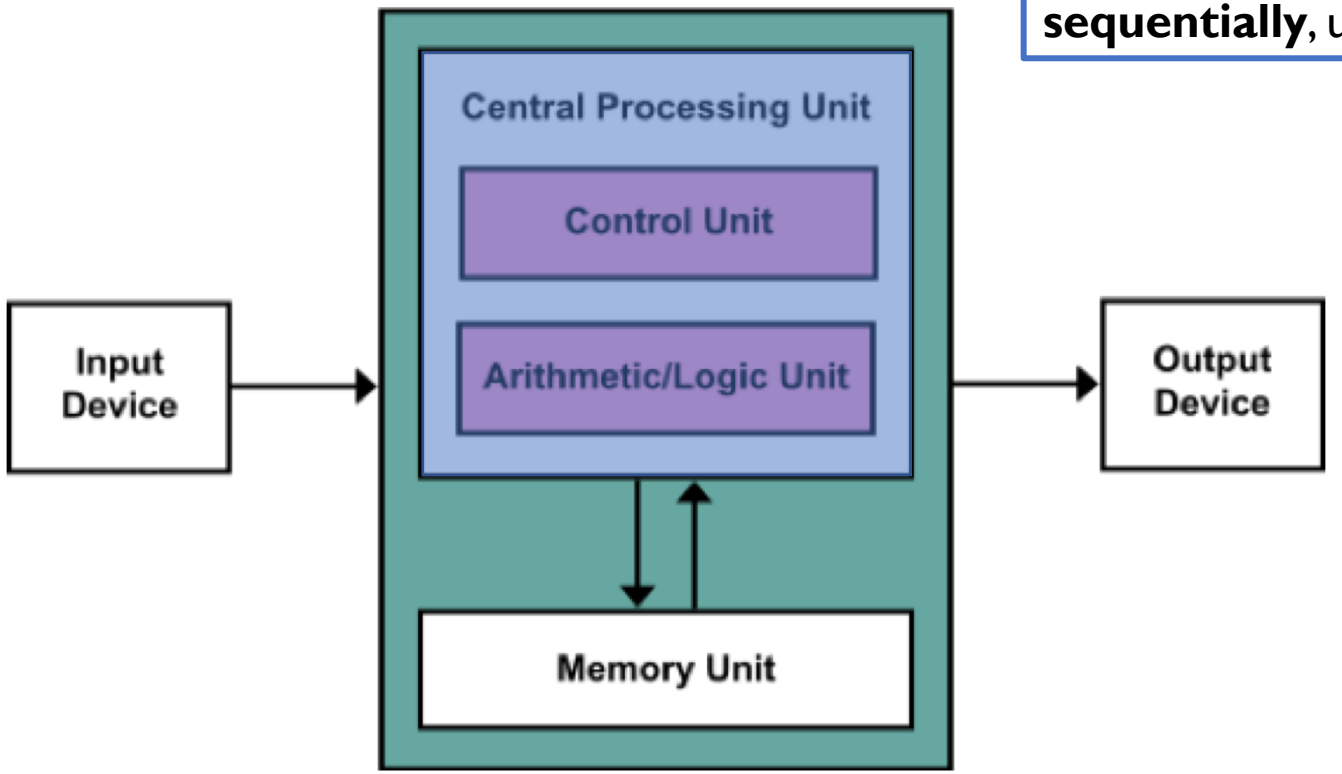


von Neumann Architecture

Executes **instructions** (i.e., basic arithmetical/logical computations) **sequentially**, using internal **registers**



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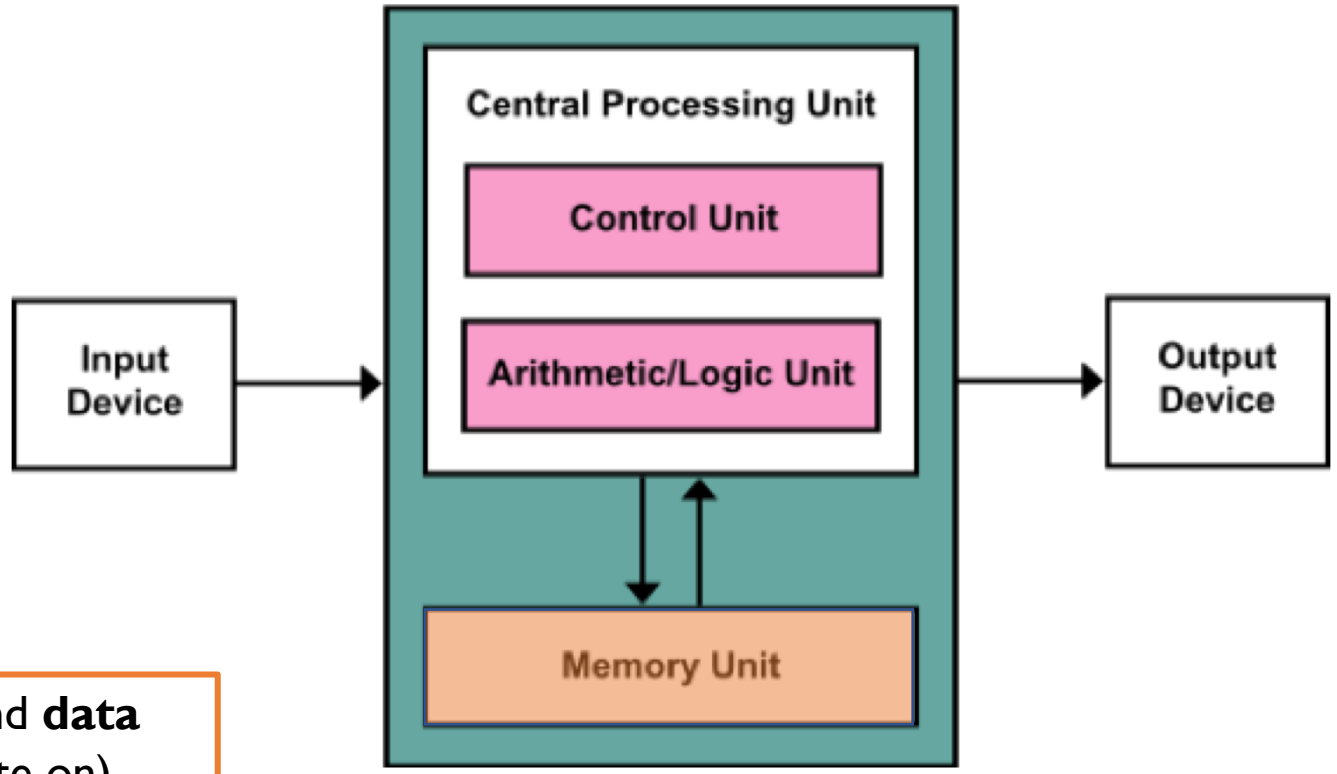

Contains **instructions** and **data** (which instructions operate on)

Central Processing Unit (CPU)

Instruction Cycle: Fetch-Decode-Execute

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  - **Execute:** runs the actual decoded instruction

Machine Language

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- Each instruction is encoded as a sequence of bits
  - A single bit is the smallest unit of (digital) information
  - It takes on two possible values: 0 or 1
- A **word** is the unit of data the CPU can directly operate on
  - today ranging from 32 to 64 bits

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- In base-10 system, each digit can only take one out of 10 possible values: 0, 1, …, 9

1	0	1
10^2	10^1	10^0

$1*10^0 + 0*10^1 + 1*10^2 = 101$

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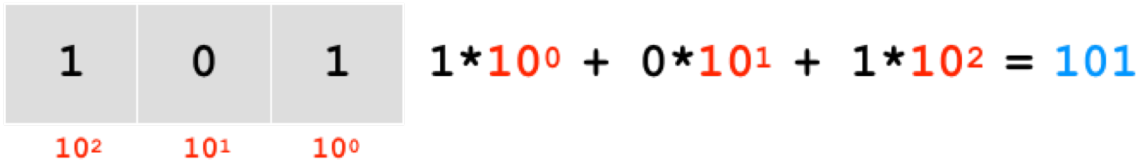
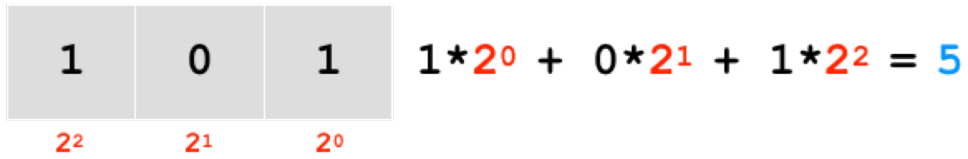


- In binary system (base-2), each digit is a bit



A Side Note on Units

Prefixes for multiples of bits (bit) or bytes (B)

Decimal				Binary				
Value		SI		Value		IEC		JEDEC
1000	10^3	k	kilo	1024	2^{10}	Ki	kibi	K kilo
1000^2	10^6	M	mega	1024^2	2^{20}	Mi	mebi	M mega
1000^3	10^9	G	giga	1024^3	2^{30}	Gi	gibi	G giga
1000^4	10^{12}	T	tera	1024^4	2^{40}	Ti	tebi	–
1000^5	10^{15}	P	peta	1024^5	2^{50}	Pi	pebi	–
1000^6	10^{18}	E	exa	1024^6	2^{60}	Ei	exbi	–
1000^7	10^{21}	Z	zetta	1024^7	2^{70}	Zi	zebi	–
1000^8	10^{24}	Y	yotta	1024^8	2^{80}	Yi	yobi	–

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- An abstraction of the underlying physical (hardware) architecture
  - x86, ARM, SPARC, MIPS, etc.
- Each realization of the same instruction set is an implementation of a physical architecture
  - x86 → Intel, AMD, Cyrix, etc.

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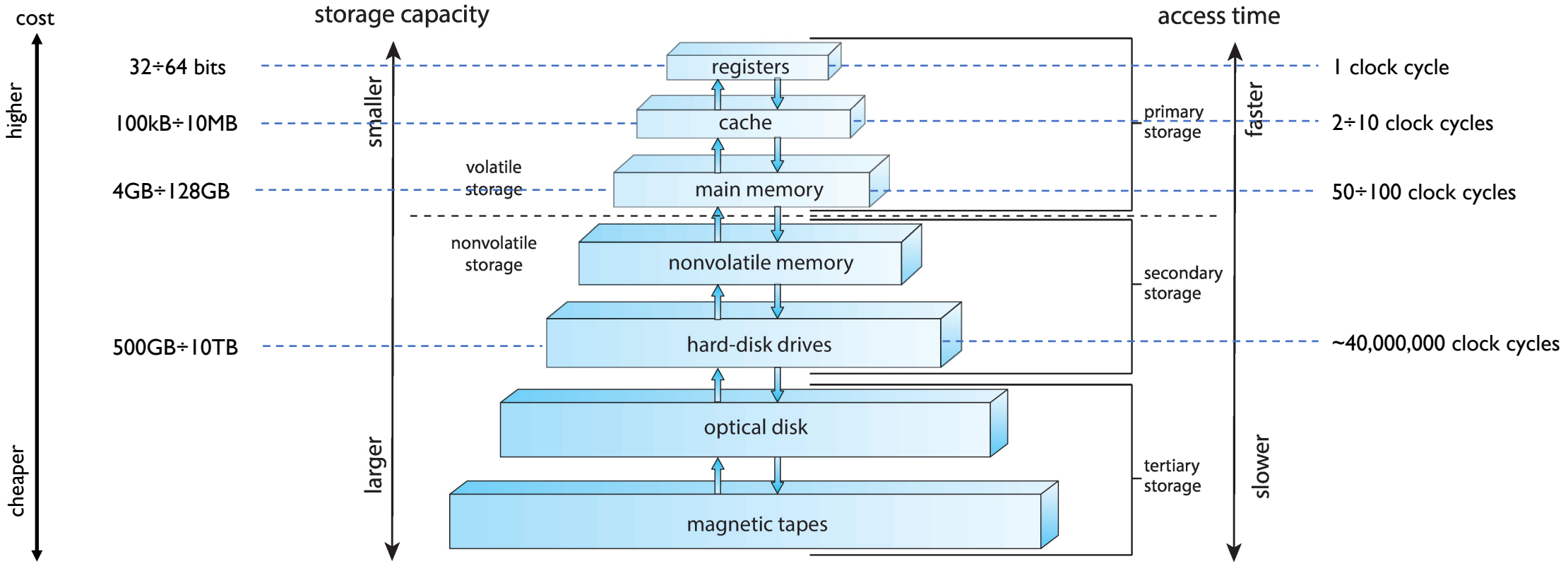
- Special-purpose (x86):
  - `esp` → Stack pointer for top address of the stack
  - `ebp` → Stack base pointer for the address of the current stack frame
  - `eip` → Instruction pointer, holds the program counter (i.e., the address of next instruction)

Memory

Memory Hierarchy



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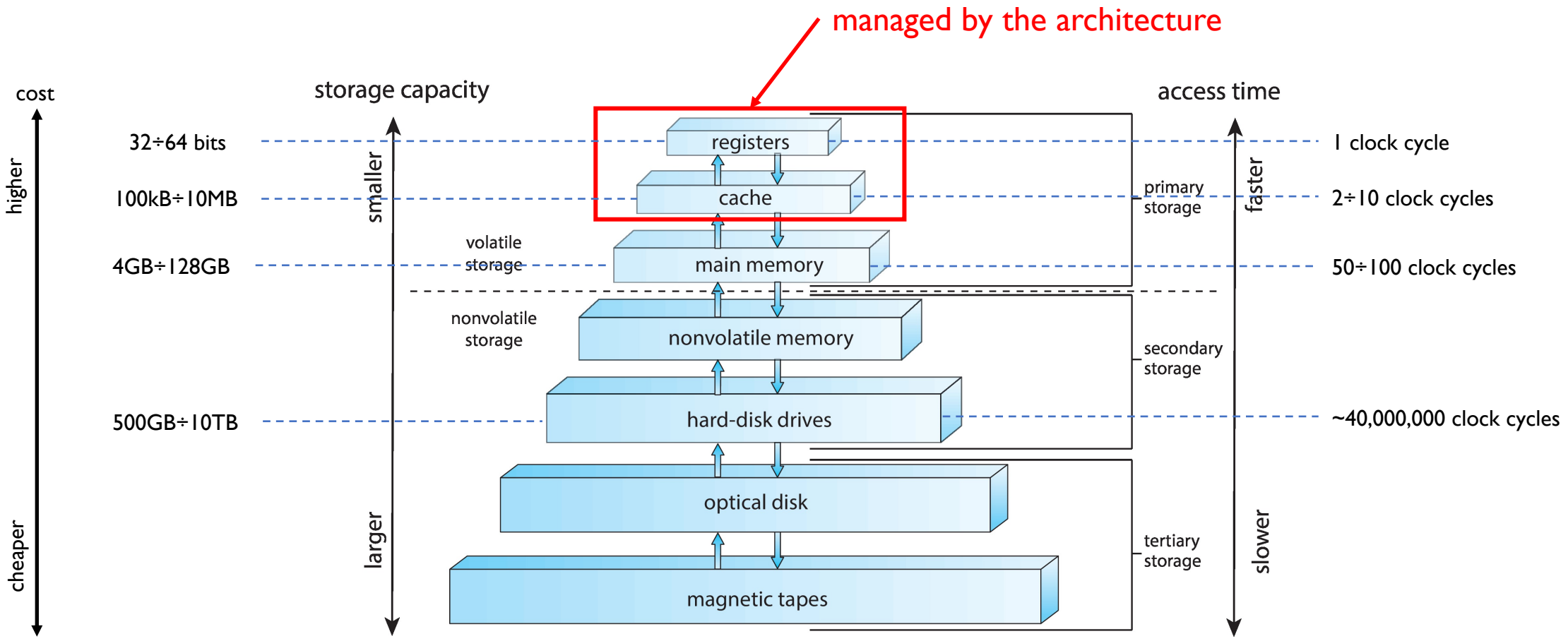

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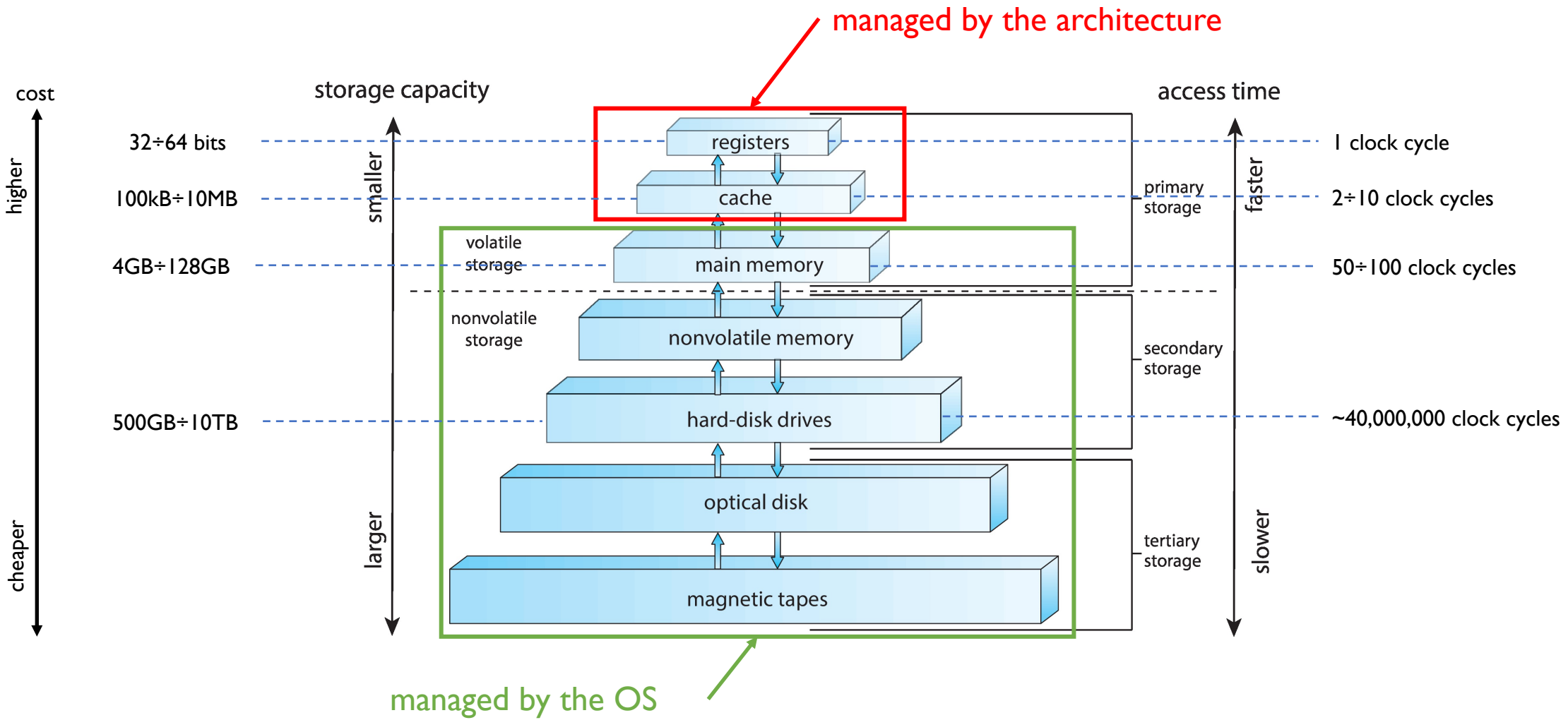

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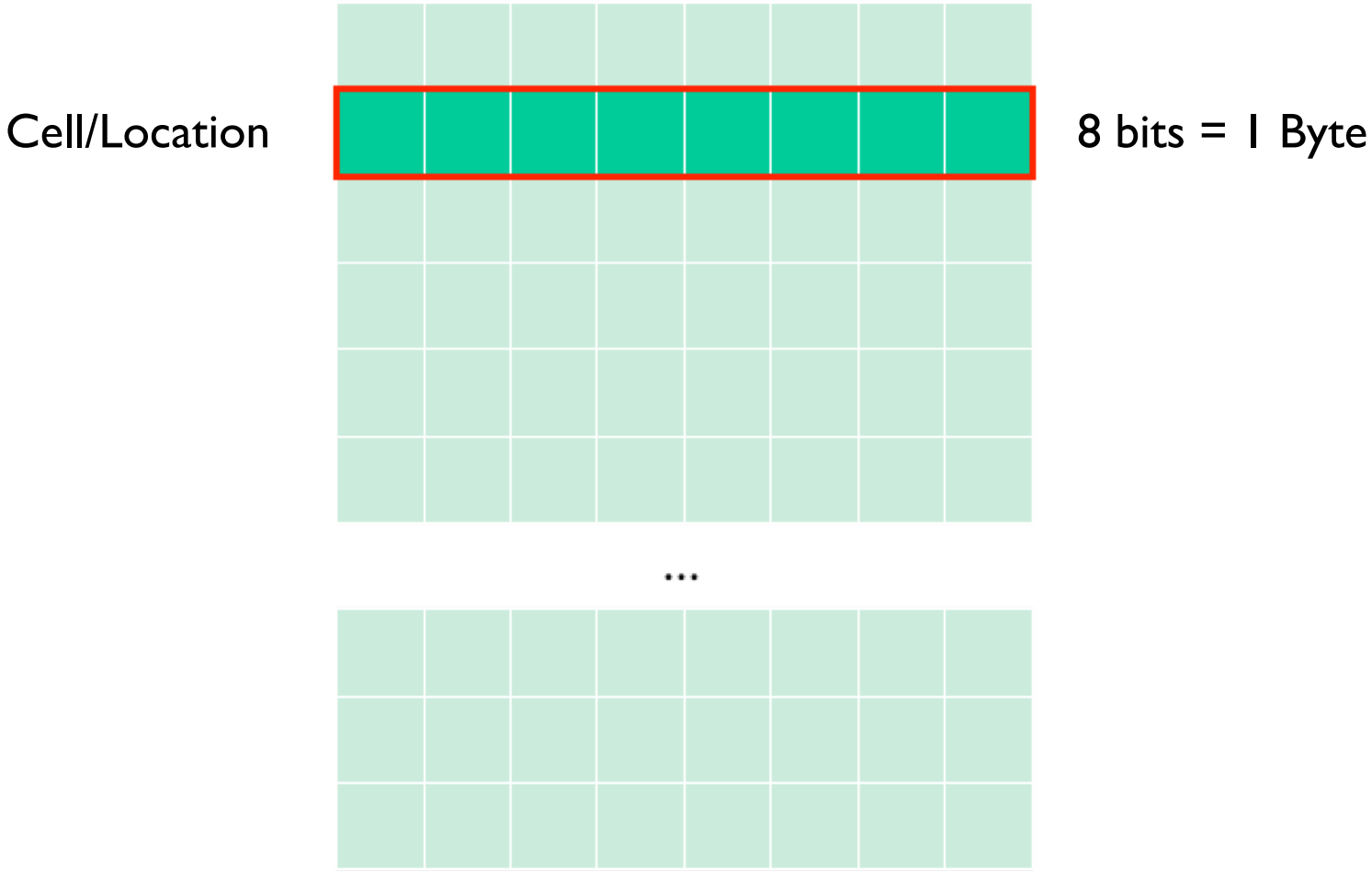
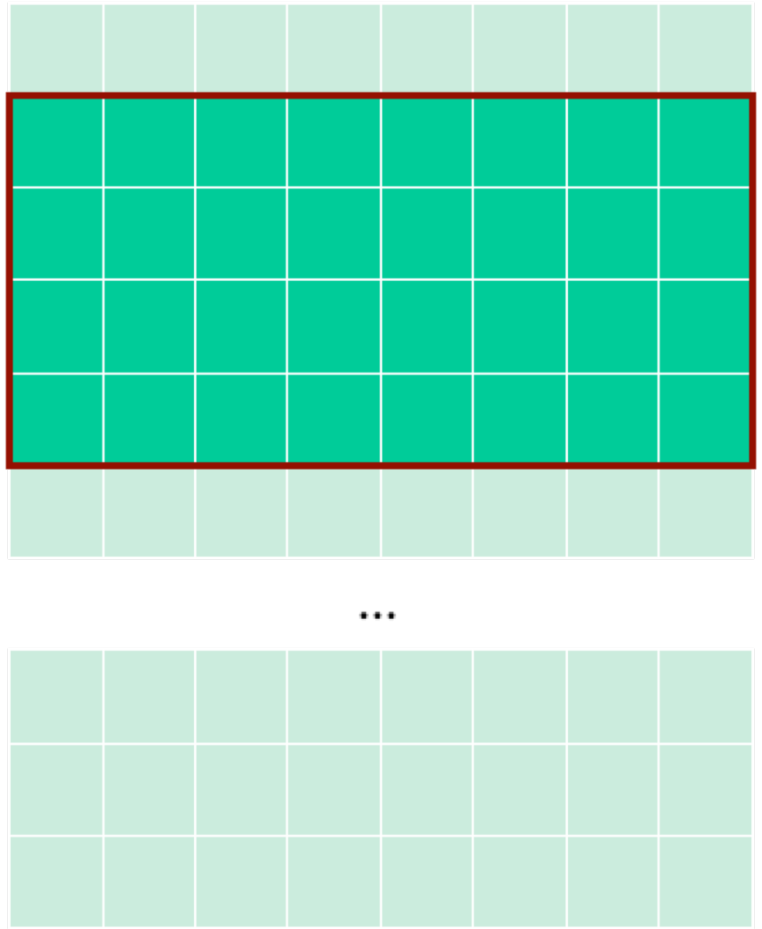
- The smallest addressable unit is usually 1 Byte

Memory Cell (1)



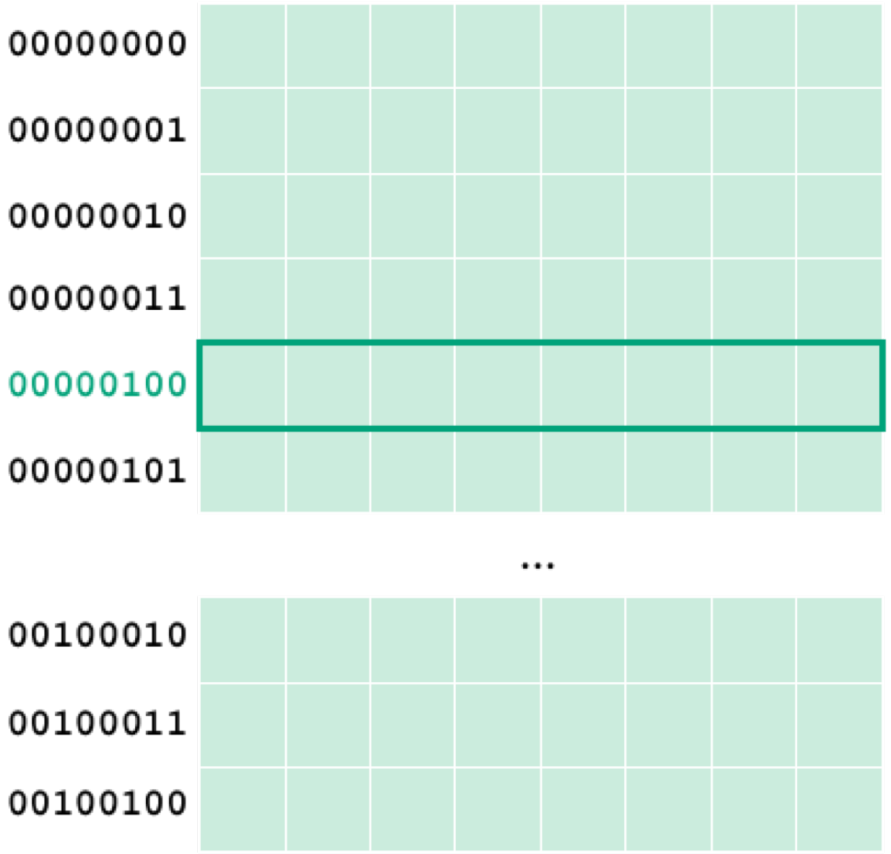
Memory Cell (2)

Cell/Location



32 bits = 4 Bytes

Memory Address (Single Byte)



Computer Buses

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- More dedicated buses have been added to manage CPU-to-memory and I/O traffic
  - PCI, SATA, USB, etc.

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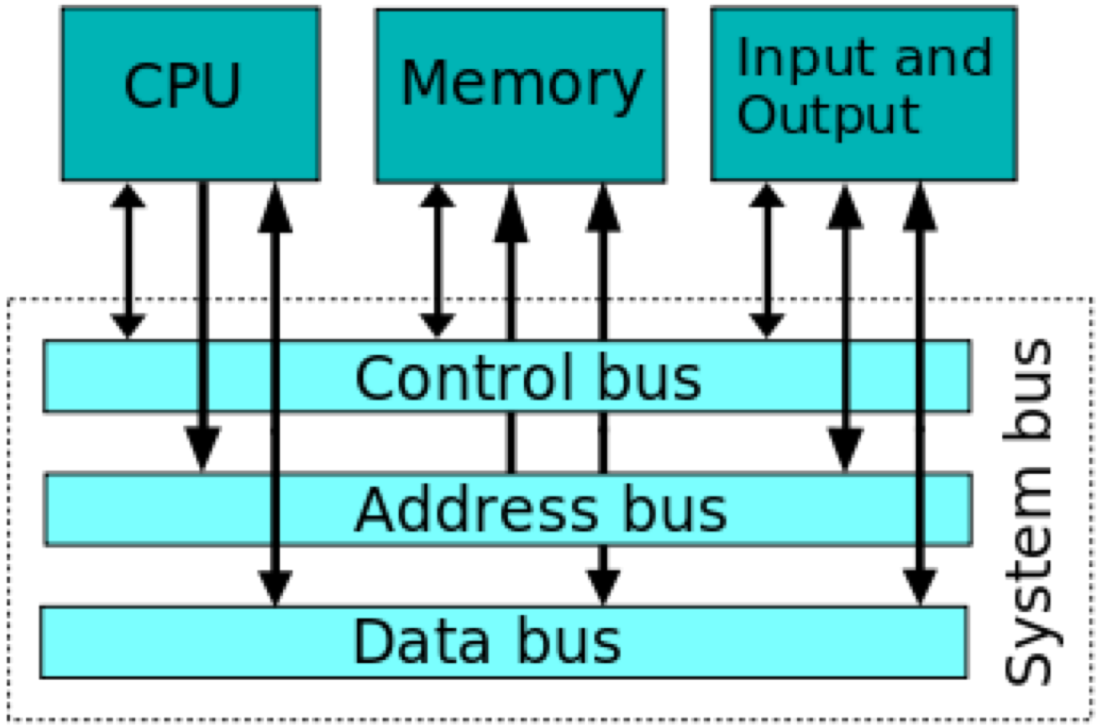
CPU
Memory
Input and Output
Control bus
Address bus
Data bus
System bus

I/O Devices

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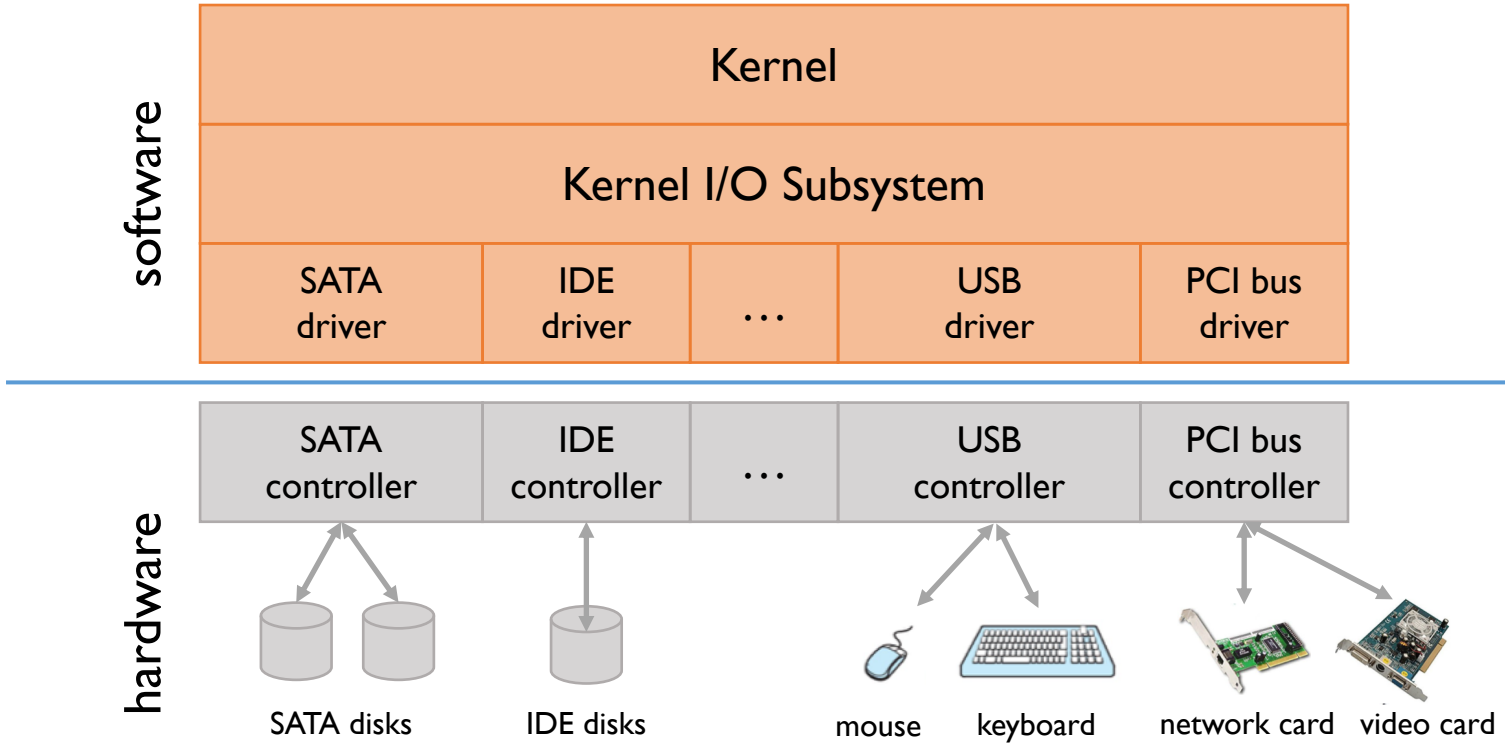
- OS talks to a device controller using a specific **device driver**

Device Drivers: OS Software Abstraction



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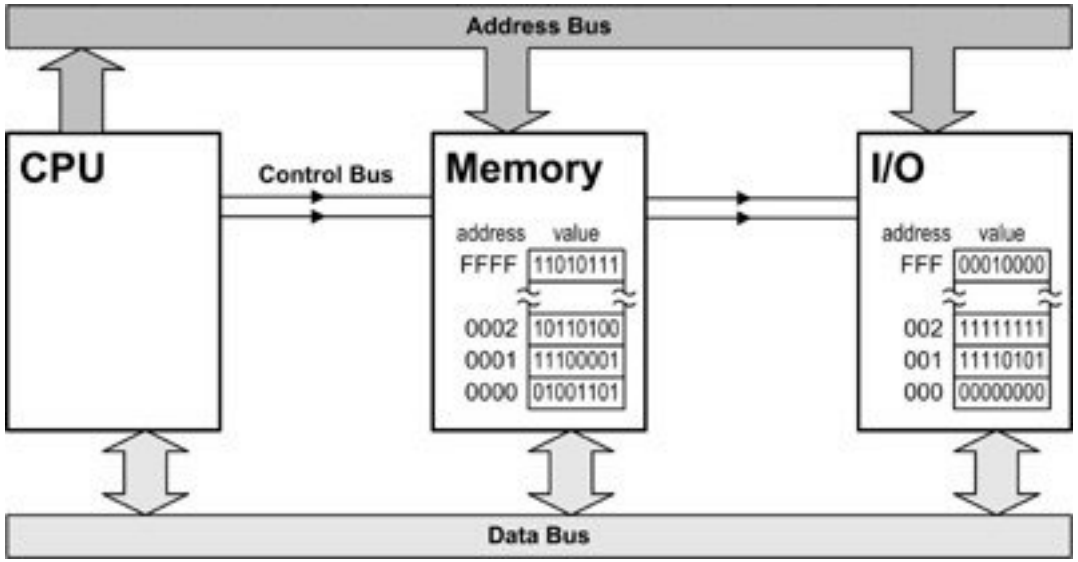
How does the CPU know how to address (registers of) I/O devices?

Addressing Using the System Bus



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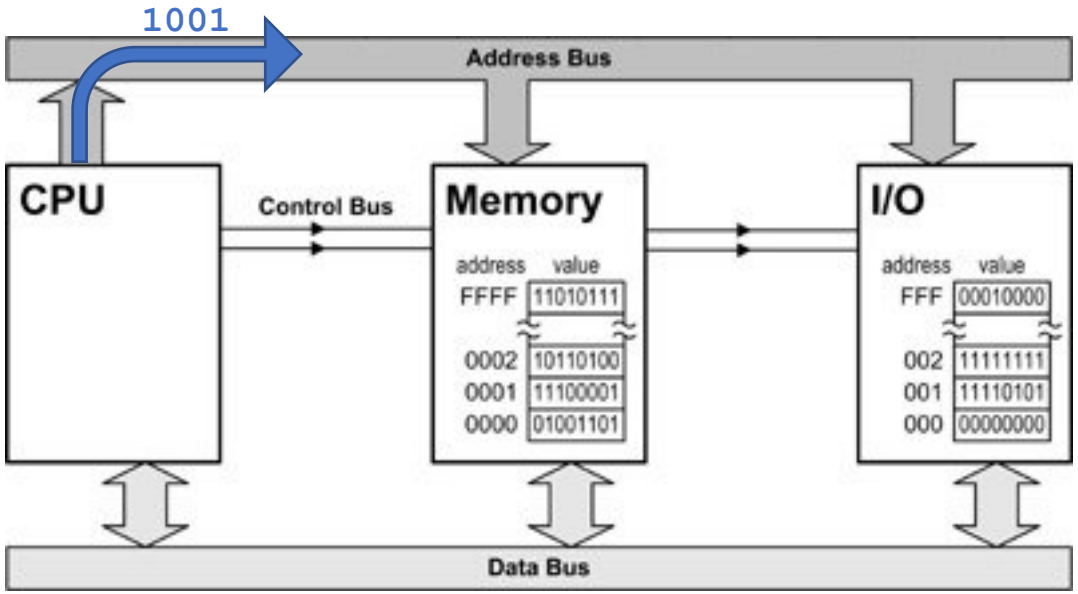

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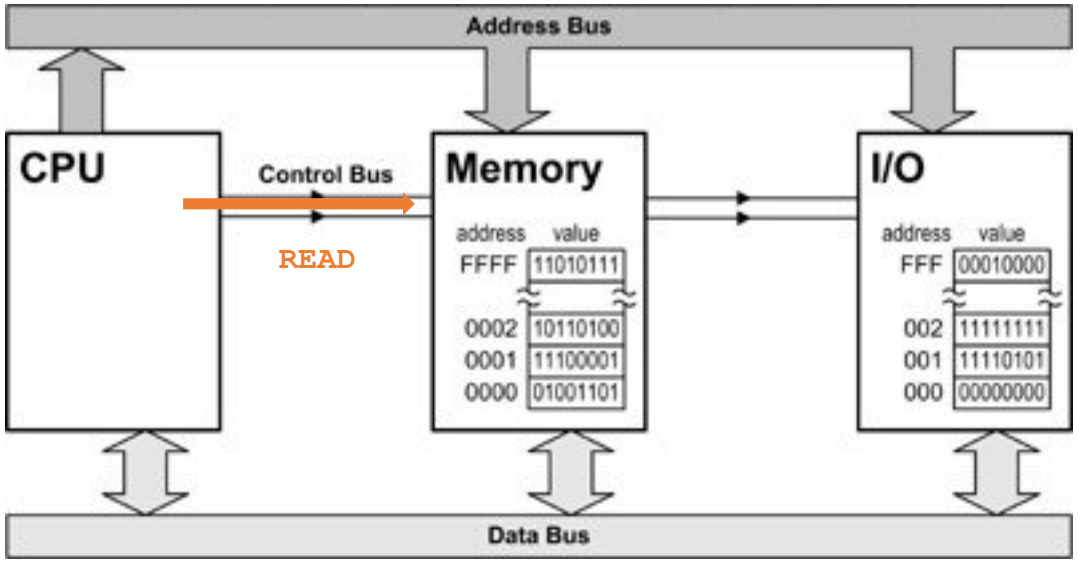

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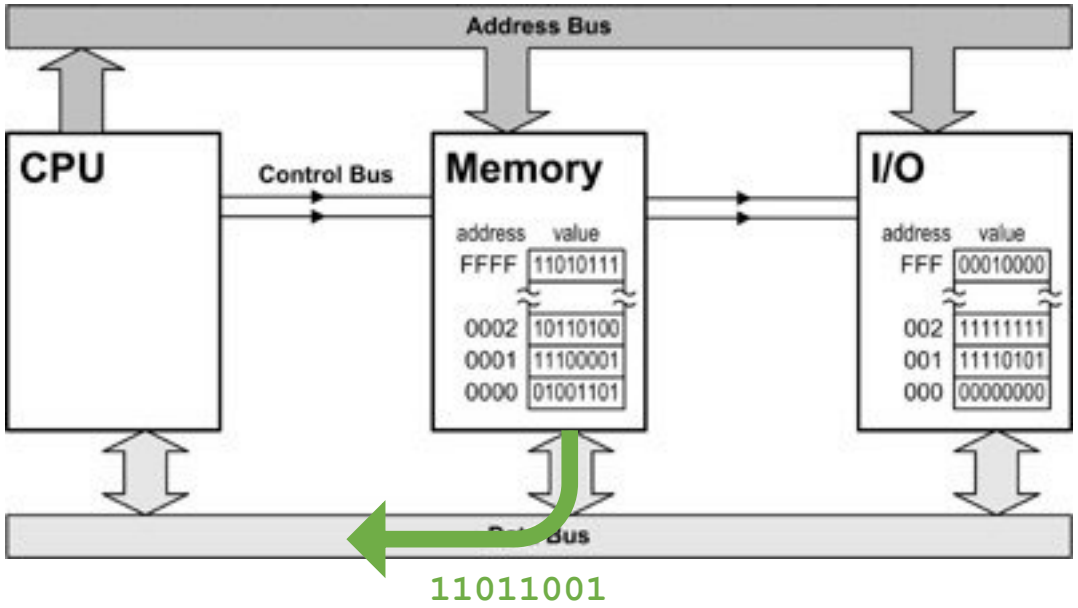

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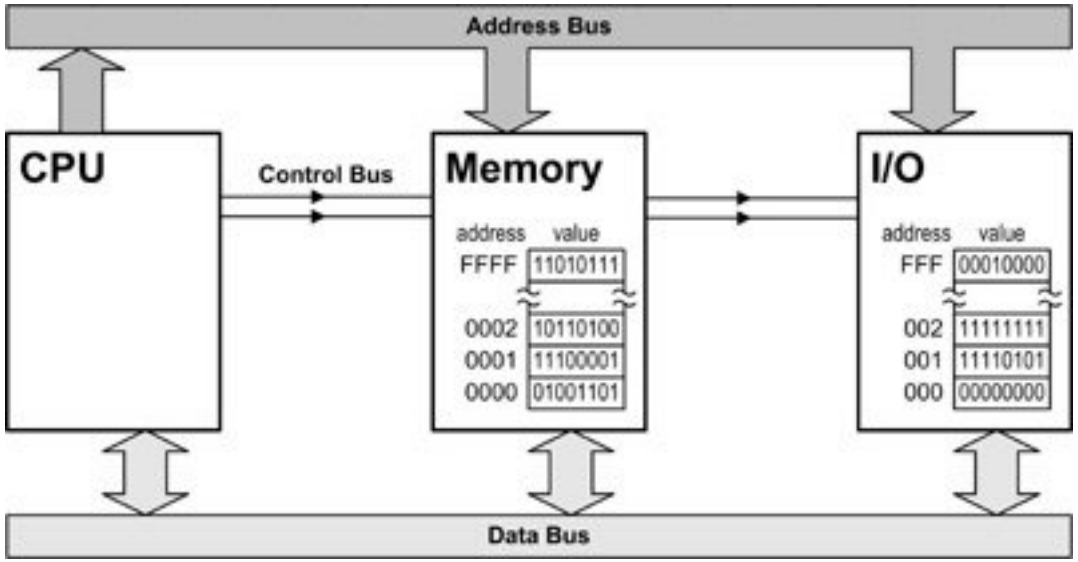

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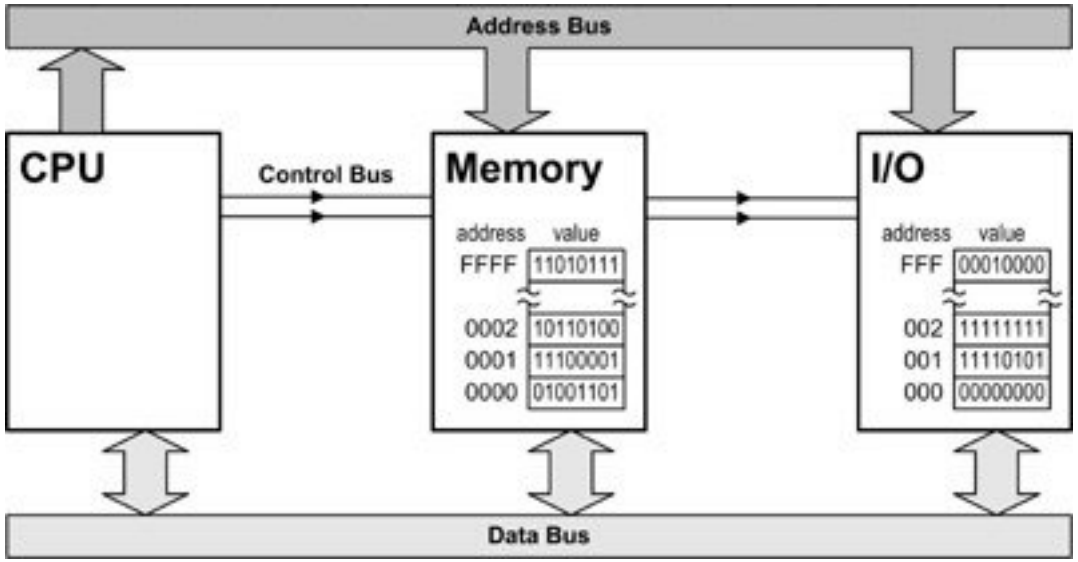

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The control bus has a special line called "**M/#IO**" which asserts whether the CPU wants to talk to memory or an I/O device

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  - **Port-mapped I/O** → referencing controller's registers using a separate I/O address space
  - **Memory-mapped I/O** → mapping controller's registers to the same address space used for main memory

Port-Mapped I/O

- Each I/O device controller's register is mapped to a specific port (address)
- Requires special class of CPU instructions (e.g., `IN`/`OUT`)
  - The `IN` instruction reads from an I/O device, `OUT` writes
- When you use the `IN` or `OUT` instructions, the **`M/#IO`** is not asserted, so memory does not respond and the I/O chip does

Memory-Mapped I/O

- Memory-mapped I/O "wastes" some address space but doesn't need any special instruction
- To the CPU I/O device ports are just like normal memory addresses
- The CPU use `MOV`-like instructions to access I/O device registers
- In this way, the **`M/#IO`** is asserted indicating the address requested by the CPU refers to main memory

Port- vs. Memory-Mapped I/O

```
MOV DX,1234h
MOV AL,[DX]     ;reads memory address 1234h (memory address space)
IN AL,DX        ;reads I/O port 1234h (I/O address space)
```

Both put the value **1234h** on the CPU address bus, and both assert a **READ** operation on control bus

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MOV DX,1234h
MOV AL,[DX]     ;reads memory address 1234h (memory address space)
IN AL,DX        ;reads I/O port 1234h (I/O address space)
```

The first one will assert **M/#IO** to indicate that the address belongs to memory address space

Port- vs. Memory-Mapped I/O

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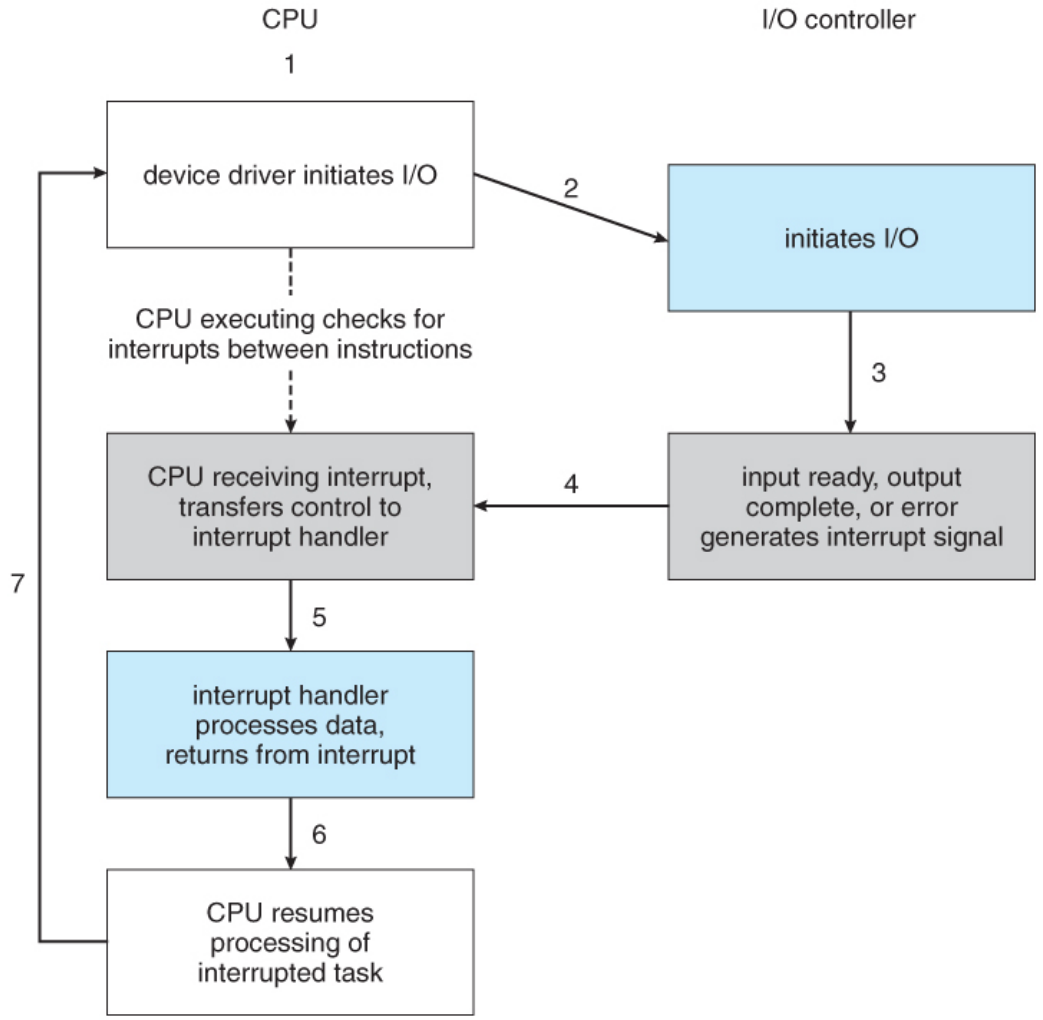
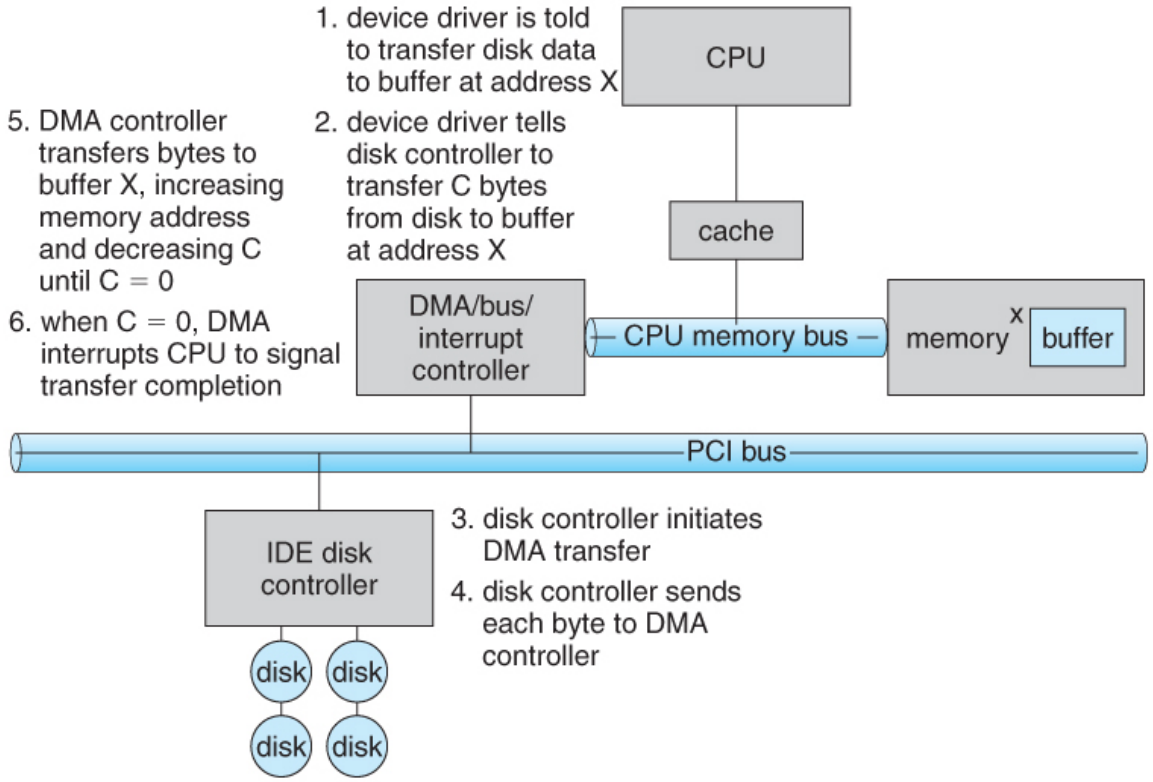
WHO?

Interrupt-driven I/O



Direct Memory Access (DMA)



Overcome the limitation of Programmed I/O

Maybe wasteful to tie up the CPU transferring data in and out of registers **one byte at a time**

Useful for devices that transfer large quantities of data (such as disk controllers)

Typically, used in combination with interrupt-driven I/O

Architectural Features Enabling OS Services

OS Service	HW Support
Protection and Security	Kernel/user mode, protected instructions, base/limit registers
System calls	Trap instructions and interrupt vectors
Exception handling	Trap instructions and interrupt vectors
I/O operations	Trap instructions, interrupt vectors, and memory mapping
Scheduling	Timer
Synchronization	Atomic instructions
Virtual memory	Translation Look-aside Buffer (TLB)

Protection and Security

Privileged Instructions

- Some CPU instructions are more sensitive than others
  - `MOV %eax, %ebx` → move the content of the register `ebx` into `eax`
  - `MOV %eax, [%ebx]` → move the content of memory indexed by register `ebx` to `eax`
  - `HLT` → halt the system
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Idea: sensitive (privileged) instructions can be executed only by the OS

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Implemented in HW!
A status bit stored in a protected CPU register
(0=kernel, 1=user)

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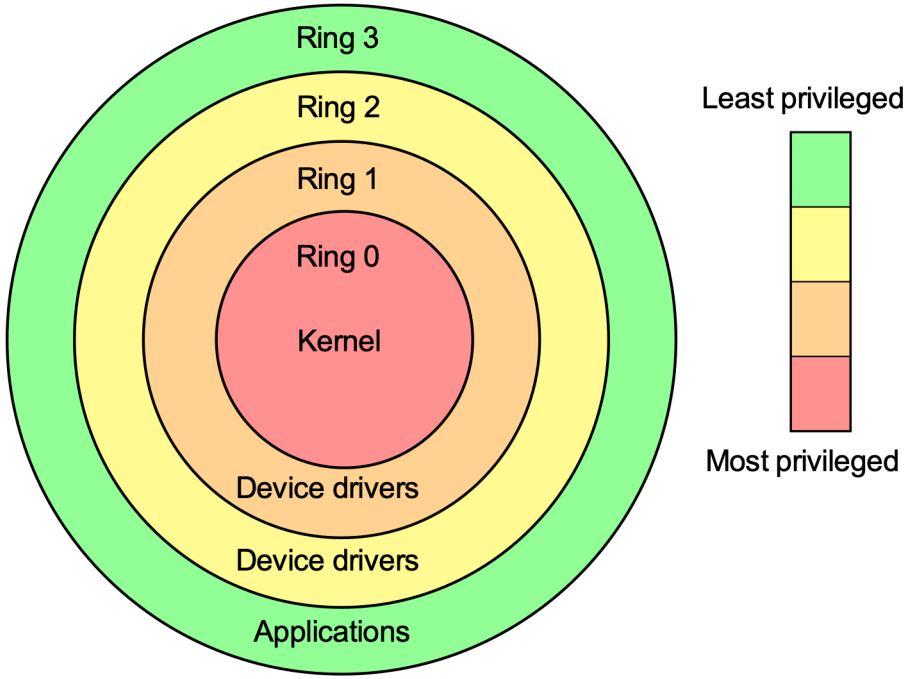
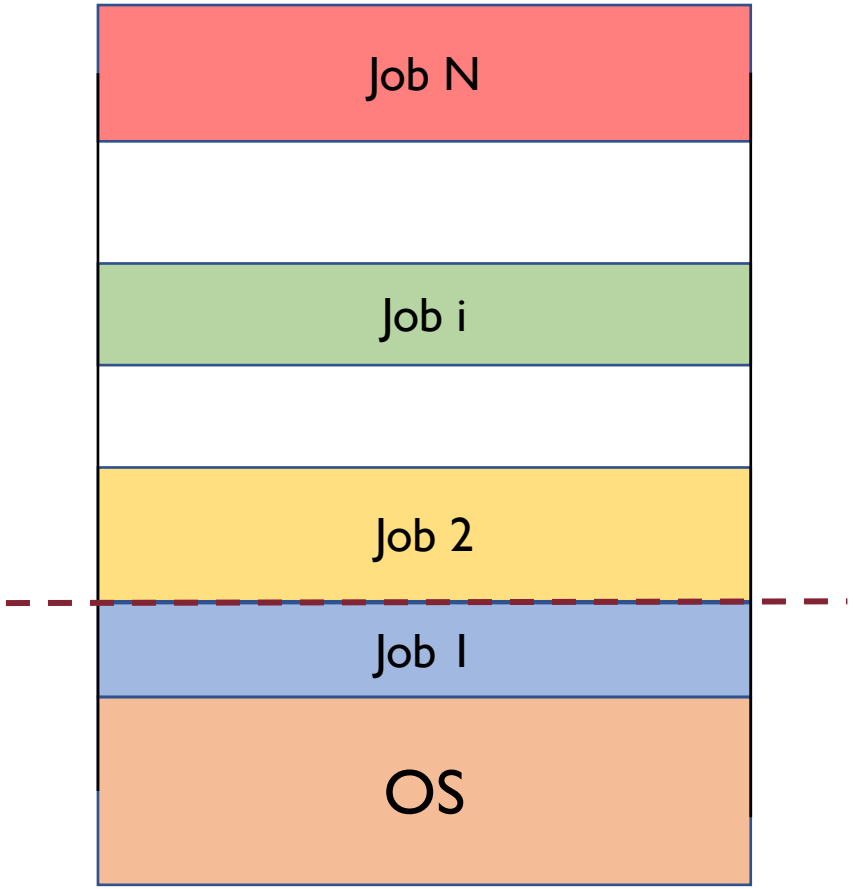
- **Protection Rings**
  - 4 different privilege levels {0, …, 3}
  - Still implementable in HW (2 bits)



Memory Protection

- Architecture must provide support for the OS to:
  - Protect user programs from each other



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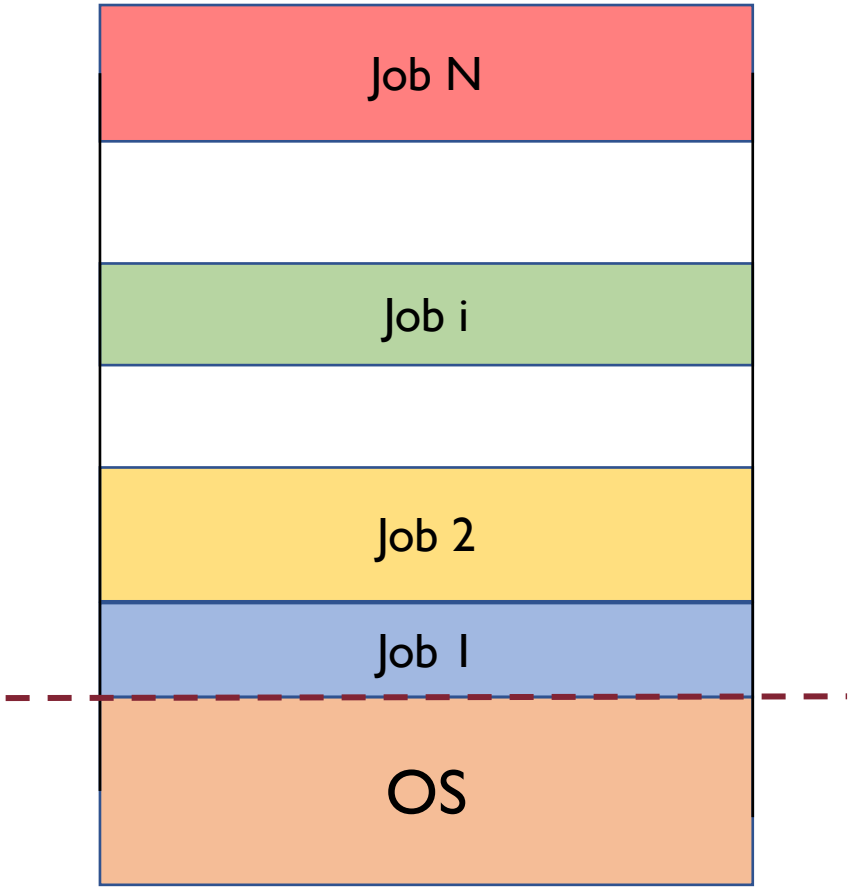

Memory Protection

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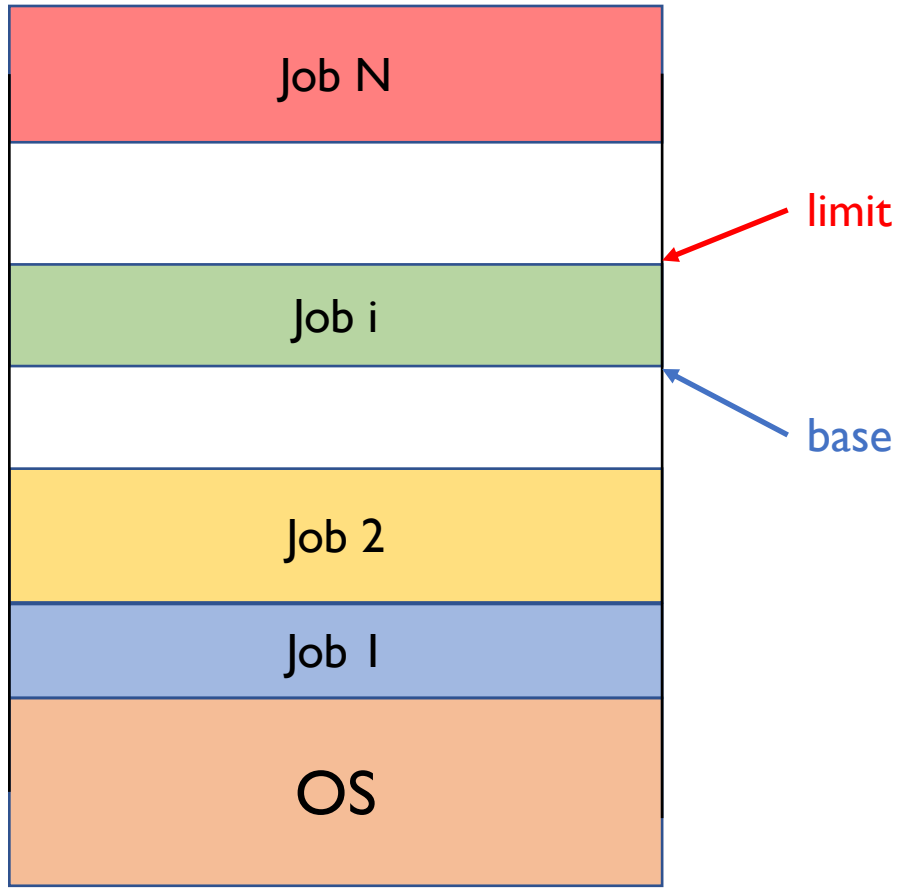
  - base → contains the starting valid memory address
  - limit → contains the last valid memory address



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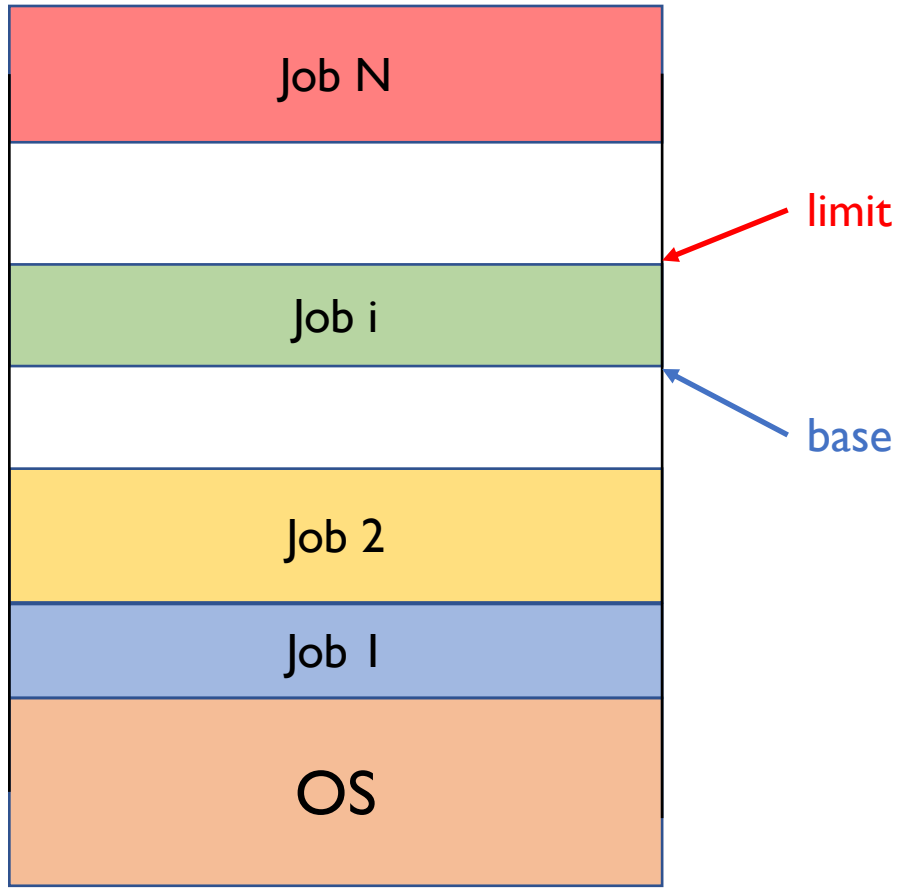

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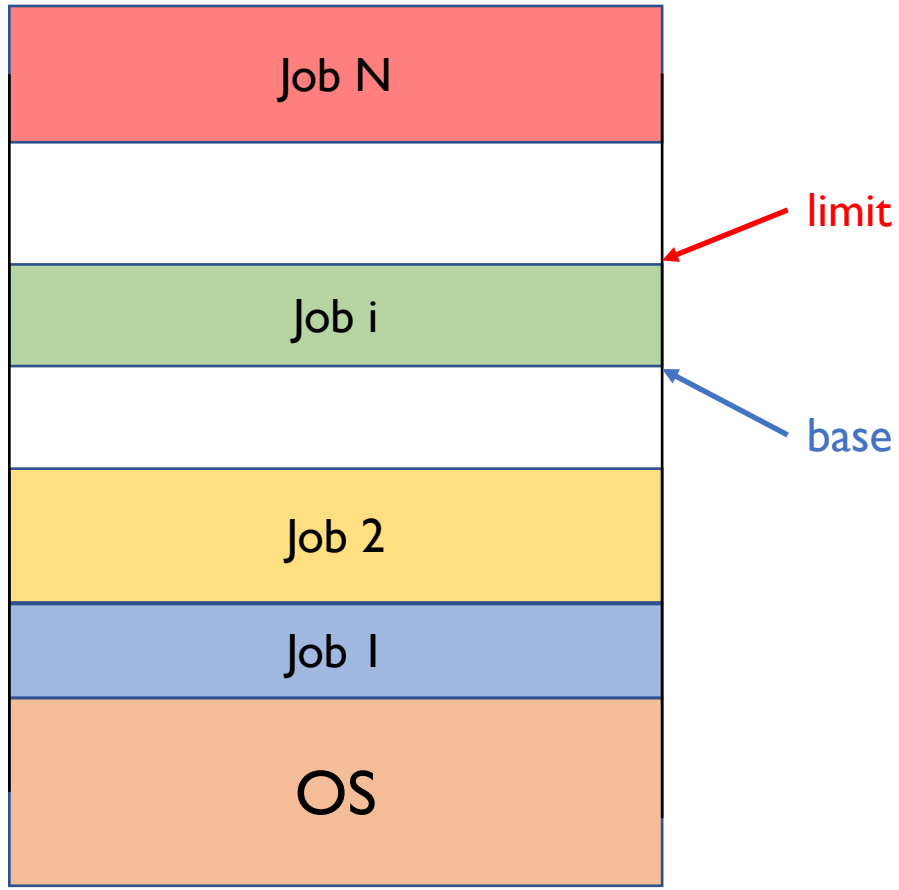
- The CPU checks each memory address referenced by user program falls between base and limit values



Program vs. Process

- A **program** is an executable file which resides on the persistent memory (e.g., disk),
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program → "static/passive" vs. process → "dynamic/active"

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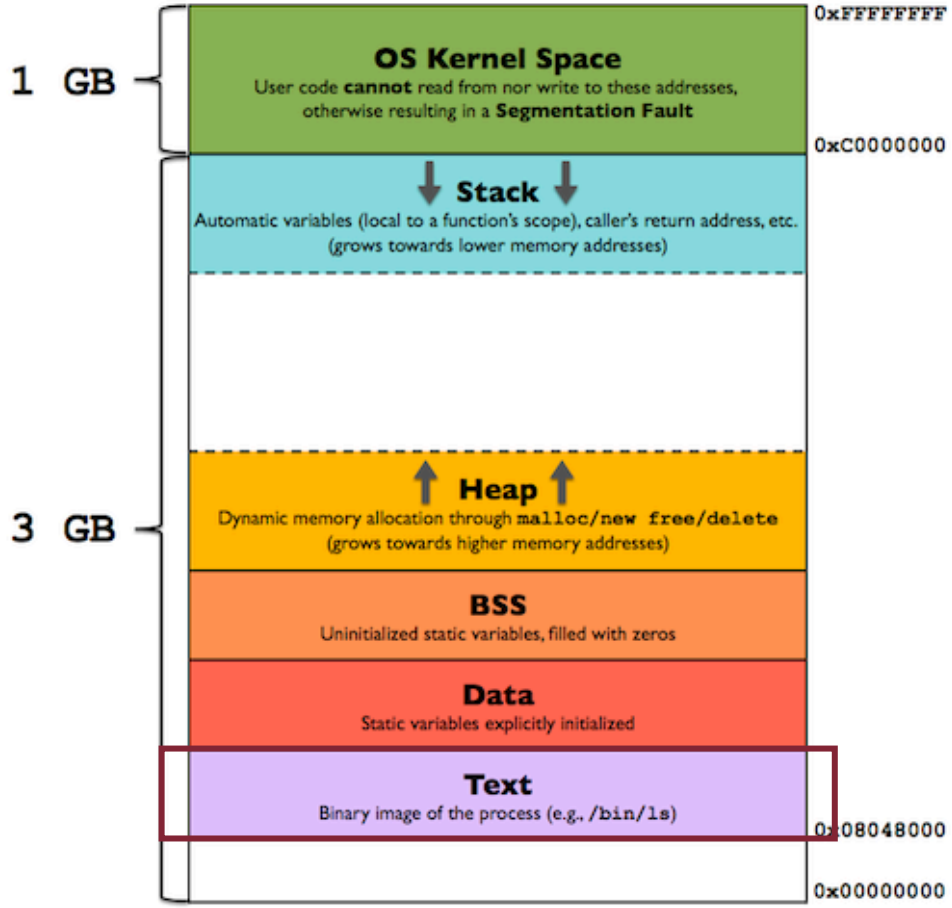

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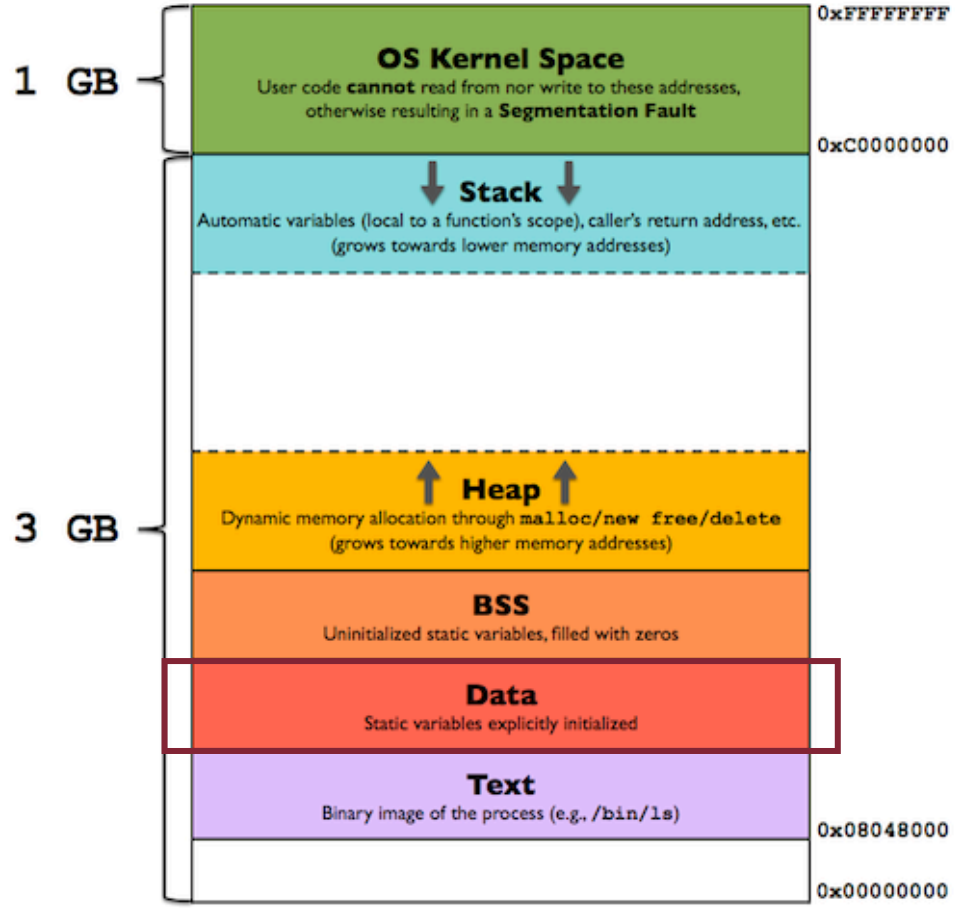

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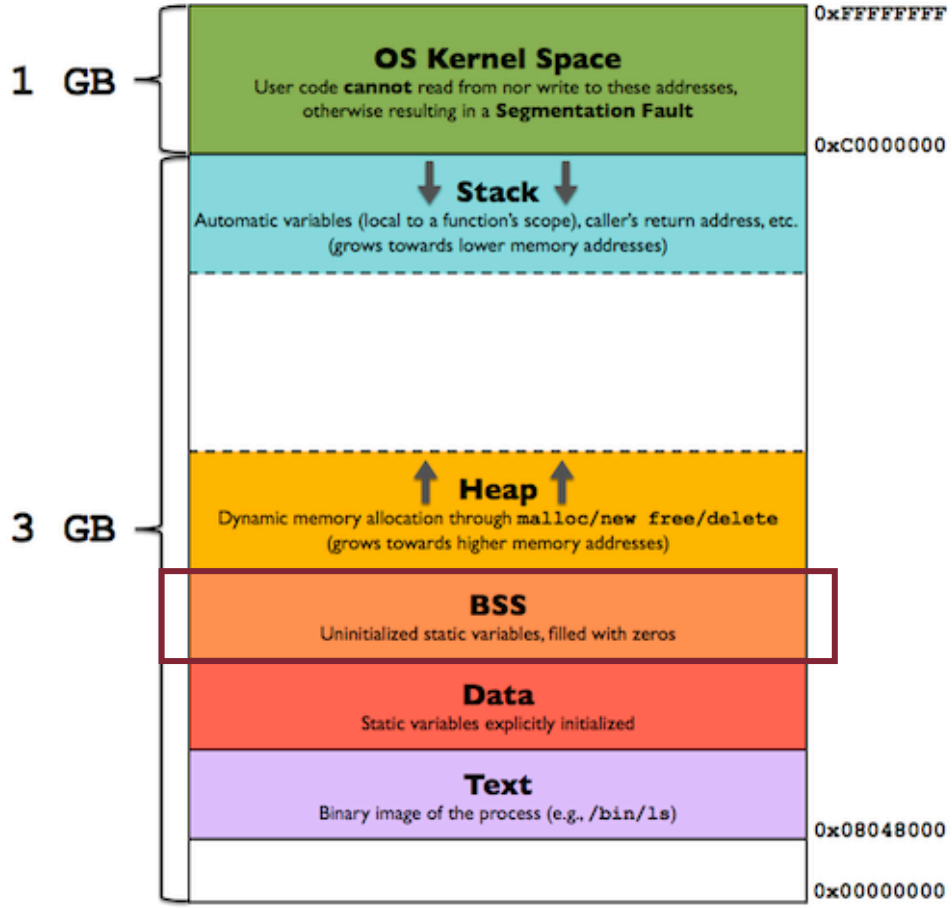

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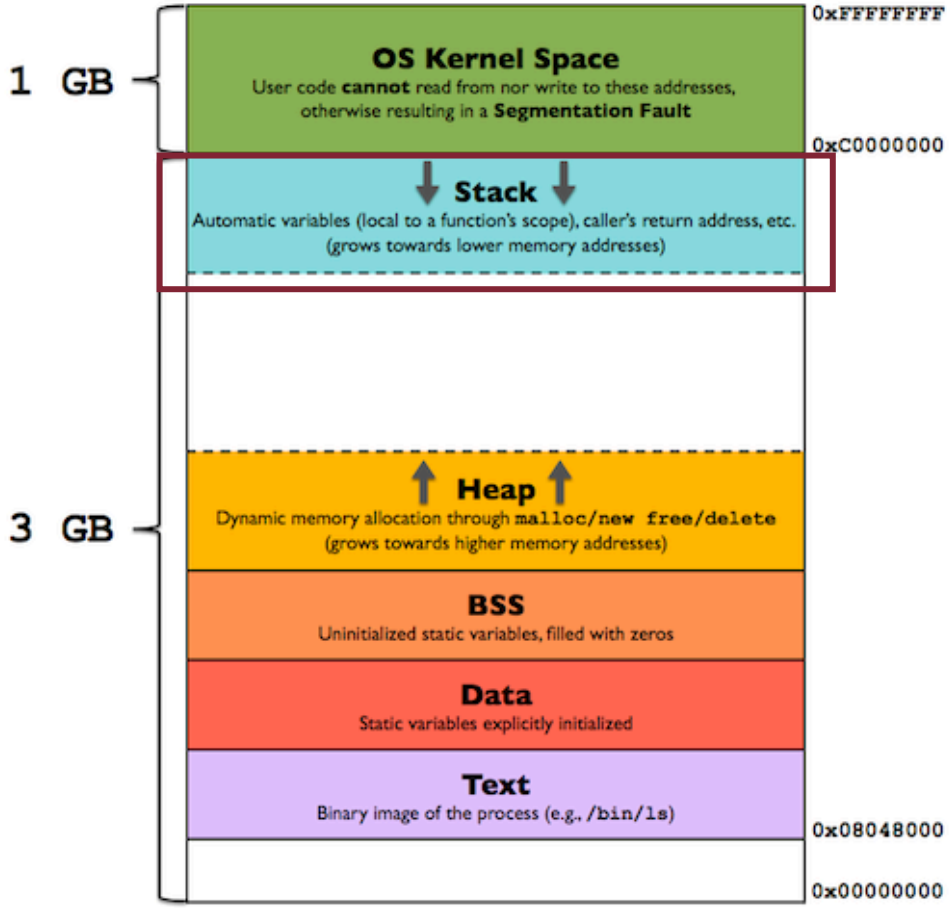

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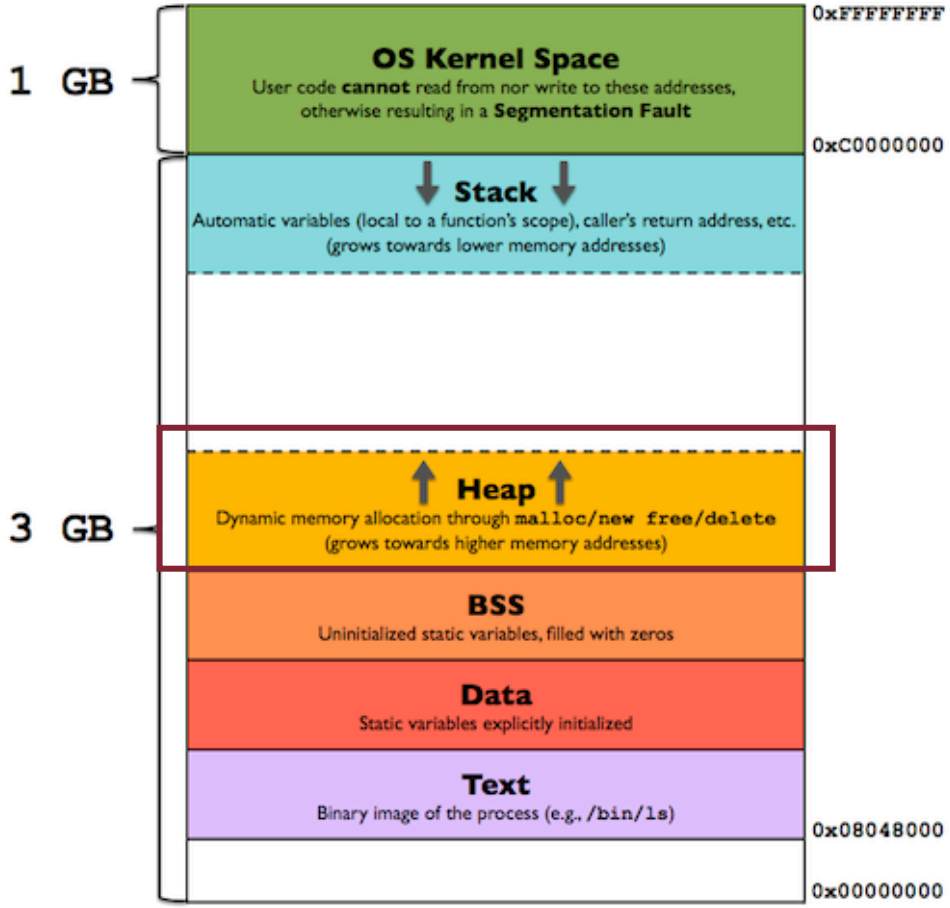
- **Heap** → used for dynamic allocation



Function Call: Stack Frame

- Each function uses a portion of the stack, and we call it a **stack frame**
- The stack frame for each function is divided into **3 parts**:
  - function parameters
  - back-pointer to the previous stack frame
  - local variables

Stack Frame: Function Parameters

- This part of a function's stack frame is set up by the **caller**
- **2 operations** are defined on a stack:
  - `push` → used to place items onto the stack
  - `pop` → user to remove items from the stack
- Different languages may push the parameters on in different orders

Stack Frame: Function Parameters

```
foo (a, b, c);
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- Each item is pushed onto the stack, the stack grows down
- The stack-pointer register (**`esp`**) is decremented by 4 bytes (in 32-bit mode), and the item is copied to the memory location pointed to by the stack-pointer register
- The **`call`** instruction will implicitly push the return address on the stack

```
[esp + 0]   - return address
[esp + 4]   - parameter 'a'
[esp + 8]   - parameter 'b'
[esp + 12]  - parameter 'c'
```

Stack Frame: Base Pointer

```
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This way of accessing parameters from the callee might get clumsy, especially when several local variables need to be stored

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Save the stack frame base pointer (**ebp**)!

```
push ebp        ; save previous stackbase-pointer register
mov  ebp, esp   ; ebp = esp
```

```
[ebp + 16]  - parameter 'c'
[ebp + 12]  - parameter 'b'
[ebp + 8]   - parameter 'a'
[ebp + 4]   - return address
[ebp + 0]   - saved stackbase-pointer register
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Stack Frame: Putting All Together

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Parameters (of the caller) are accessed through the stack frame base pointer (**ebp**)

```
[esp + (# - 4)] - top of local variables section
[esp + 0]       - bottom of local variables section
```

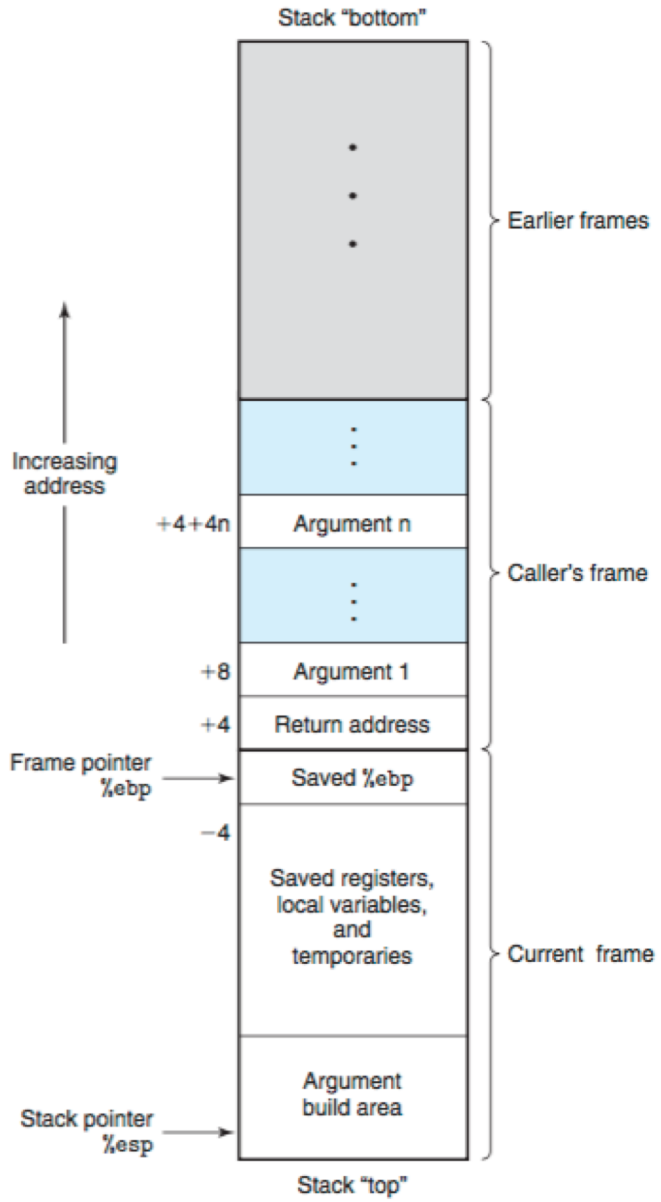
Local variables (of the callee) are accessed through the stack frame top pointer (**esp**)

Stack Frame: Cleanup

```
mov esp, ebp   ; undo the carving of space for the local variables
pop ebp        ; restore the previous stackbase-pointer register
```

The old stack frame base pointer is restored

Stack: Outline



System Calls, Exceptions, I/O Interrupts

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Crossing protection boundaries using **system calls**

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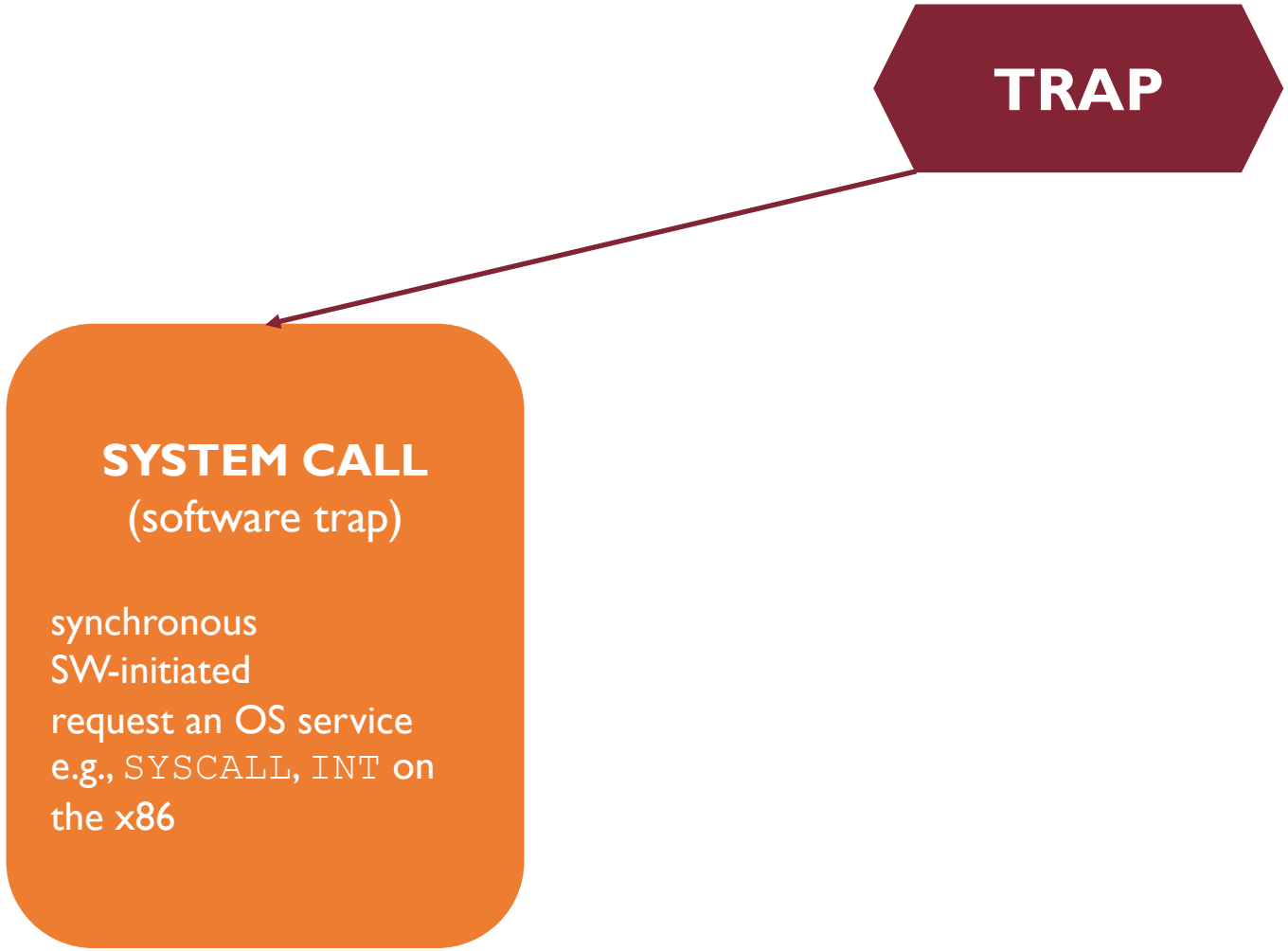
- **Interrupts**
  - hardware-generated (by external devices)
  - e.g., I/O completion or timer interrupt on a multi-tasking system

A Quick Note on Terminology

TRAP

We will refer to **trap** as any event that causes switch to OS kernel mode

A Quick Note on Terminology



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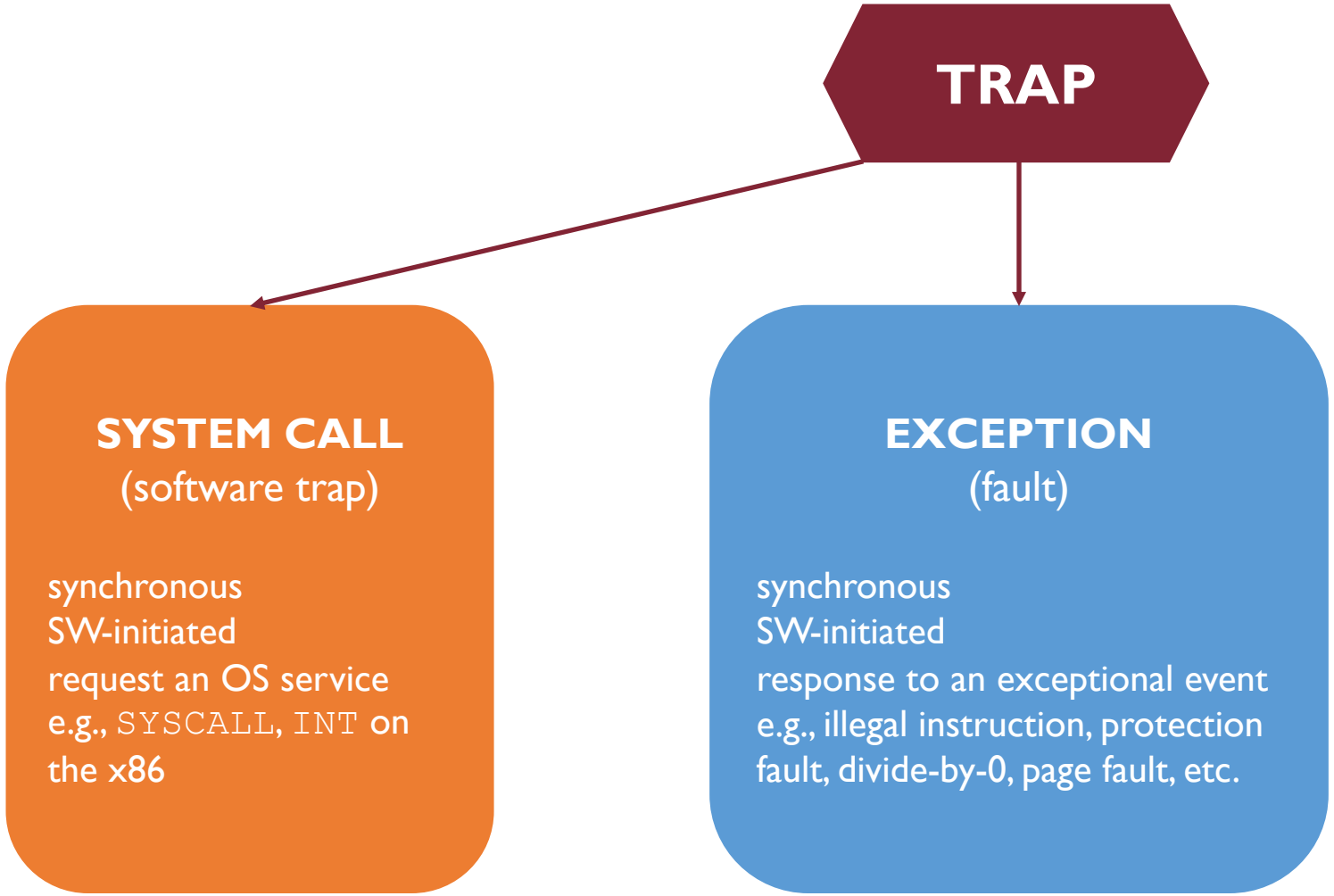

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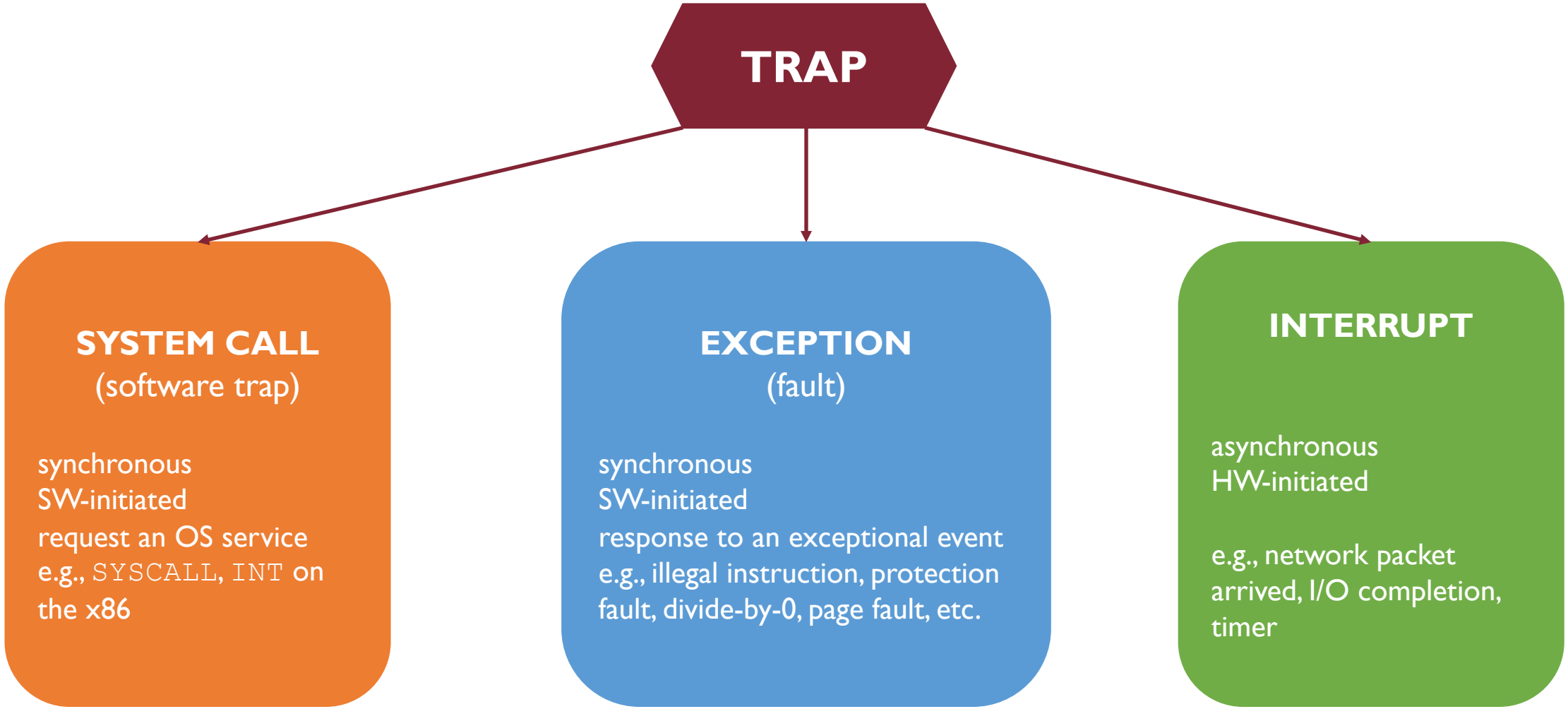

Scheduling and Synchronization

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- At each timer interrupt, the CPU scheduler takes over and decides which process to execute next

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- OS must be able to synchronize the activities of cooperating, concurrent processes
- Hardware must ensure that short sequences of instructions (e.g., read-modify-write) are executed **atomically** by either:
  - Disabling interrupts before the sequence and re-enable them afterwards

  or
  - Special instructions that are natively executed atomically

Virtual Memory

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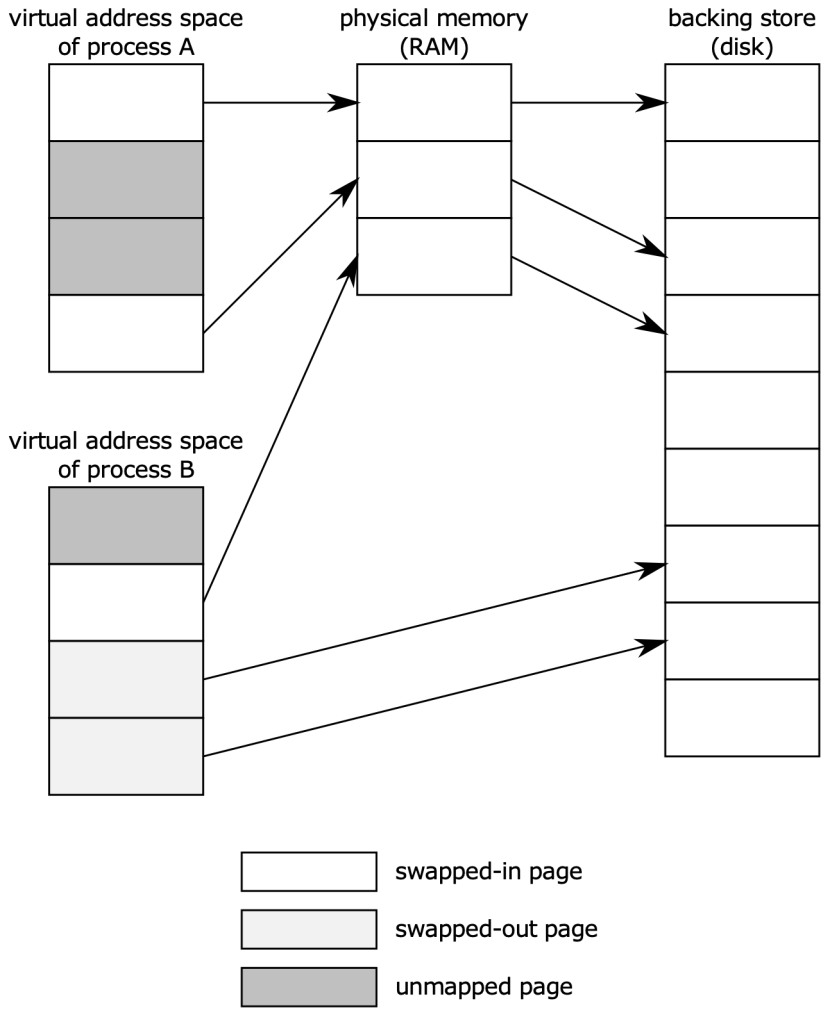
- It allows to run programs without them being entirely loaded in main memory
  - They are entirely loaded in virtual memory, though!
- Implemented both in HW (**MMU**) and SW (**OS**)
  - **MMU** is responsible for translating virtual addresses into physical ones
  - **OS** is responsible for managing virtual address spaces

Virtual vs. Physical Address Space

- On a 64 bit system the CPU is able to address 2^{64} bytes = 16 exbibytes (EiB)
- Virtual address space ranges from 0 to $2^{64} - 1$
- This is about a billion times more than main memory capacity currently available!
- Virtual address space is typically divided into contiguous blocks of the same size (e.g., 4 KiB), called **pages**
- Pages which are not loaded in main memory are stored on disk

Virtual vs. Physical Address Space



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- Uses a cache called **Translation Look-aside Buffer** (**TLB**) with "recent mappings" for quicker lookups
- The OS must be aware of which pages are loaded in main memory and which ones are on disk

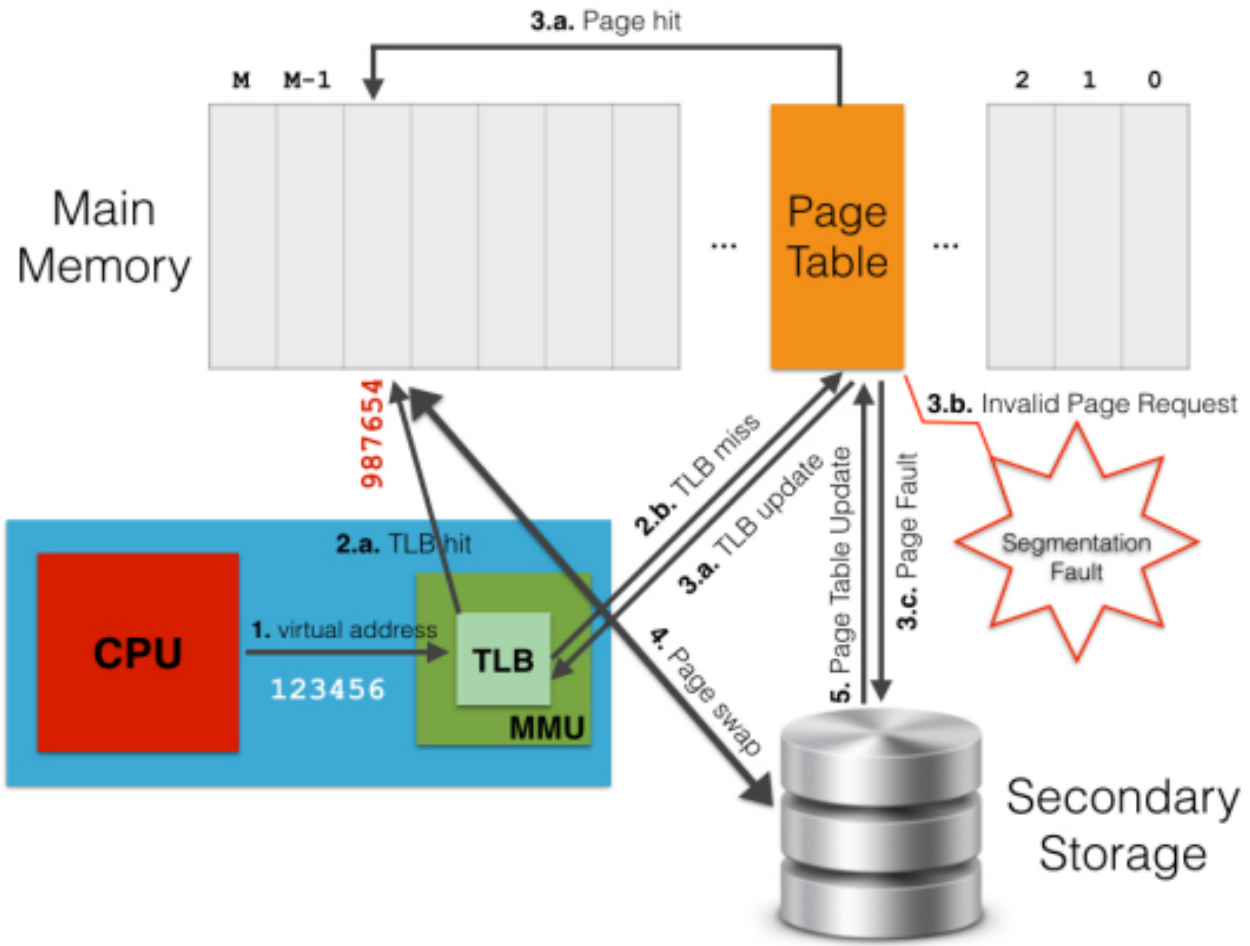
Lookup Fault

- Page lookup may fail due to **2 reasons**:
  - no valid mapping exists for a virtual address → **segmentation fault**
  - requested page is not in main memory → **page fault**
- Both cases the Page Supervisor (OS kernel) takes over

Lookup Fault Handling

- In case of a page fault the Page Supervisor:
  - checks if there is enough room in main memory
  - if not, it has to free some space by removing a page from main memory and storing to disk (**swapping**)
    - several page replacement algorithms (e.g., LRU)
  - retrieves the missing page from disk and stores it in main memory
  - updates the Page Table and the TLB cache

Lookup Fault Handling



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Summary

- Architecture support is key to OS design
- Most of the services provided by the OS to the applications rely on specific HW features
- The OS is tightly coupled to the HW of the host machine
- Advice: Keep your Computer Architecture book at hand!