

Sistemi Operativi

Corso di Laurea in Informatica

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SAPIENZA
UNIVERSITÀ DI ROMA

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 - Frequent compaction needed
- Process entirely loaded
 - Swapping helps but it may be too inefficient

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 - Internal fragmentation may still occur though

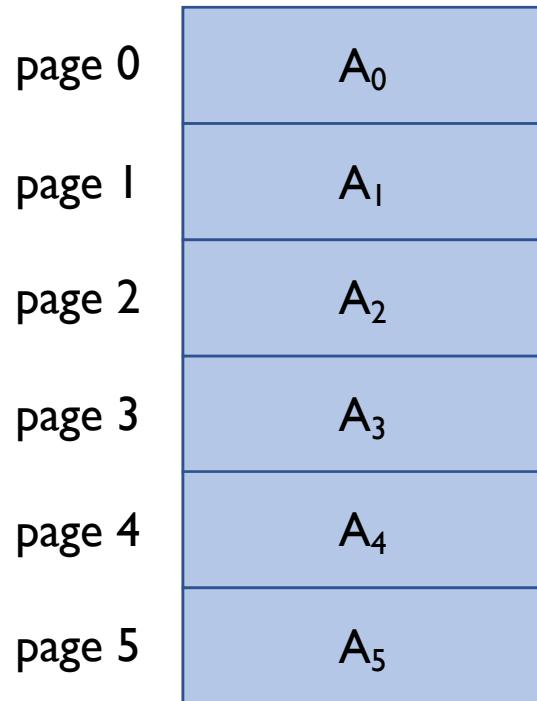
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- External fragmentation is eliminated because pages have fixed size
 - Internal fragmentation may still occur though
 - Keep only those frames that are actually being used by a process

90/10 Rule

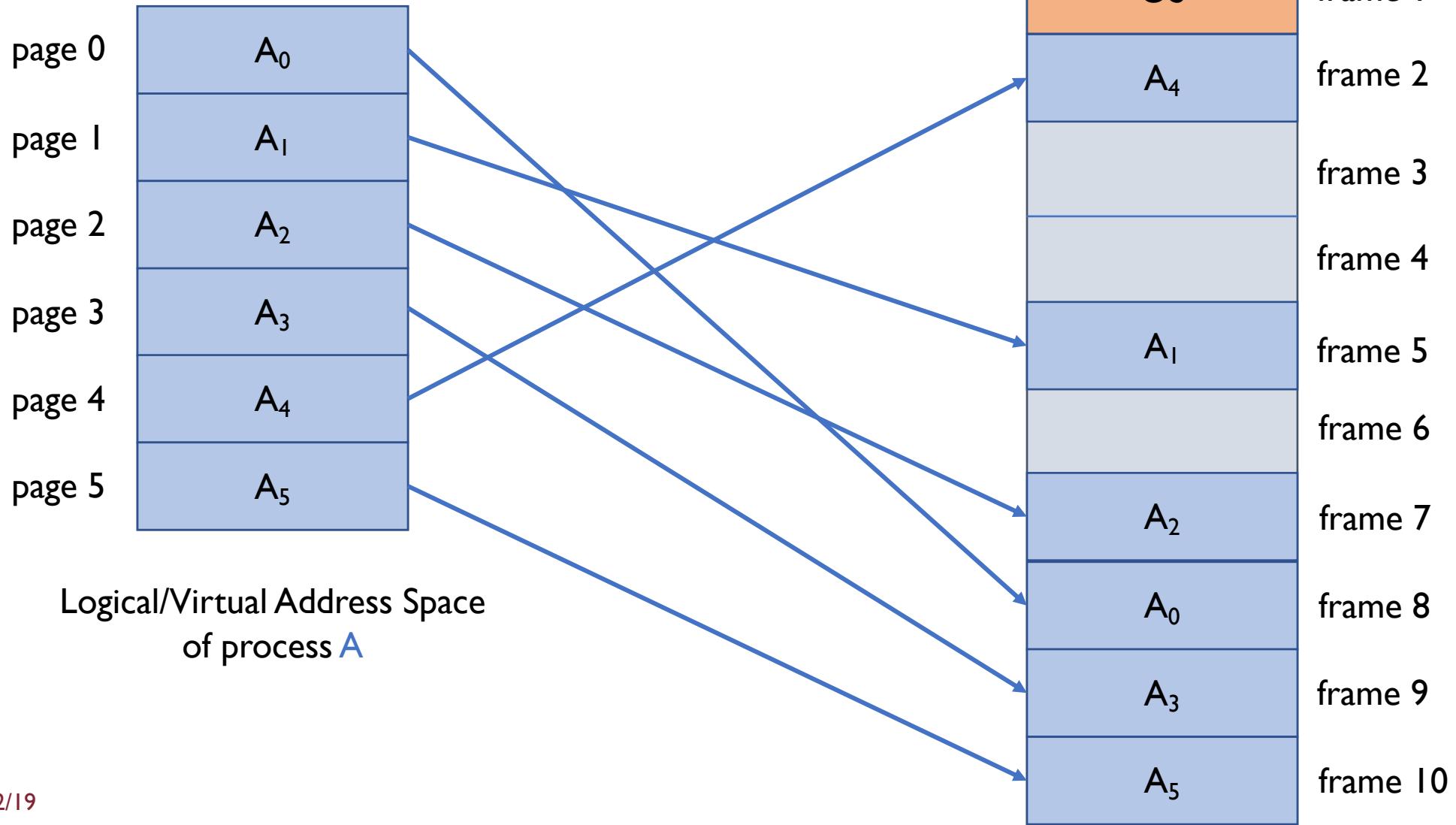
Processes spend **90%** of their time accessing only **10%** of their allocated memory space

Paging: The Big Picture



Logical/Virtual Address Space
of process A

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Basic OS Responsibilities for Paging

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- The OS has **2 main responsibilities**:
 - mapping between logical pages and physical frames
 - translating logical addresses to physical addresses
- All of this must be done efficiently!
 - Remember, memory addresses are referenced all the time
- OS needs dedicated support for doing it → **Page Table**

Page Table: Mapping Pages to Frames

0	A ₀
1	A ₁
2	A ₂
3	A ₃
4	A ₄
5	A ₅

OS	0
OS	1
A ₄	2
	3
	4
A ₁	5
	6
A ₂	7
A ₀	8
A ₃	9
A ₅	10

Page Table: Mapping Pages to Frames

Lookup table to efficiently retrieve what frame a page is stored in

0	A ₀
1	A ₁
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Page	Frame
0	8
1	5
2	7
3	9
4	2
5	10

OS	0
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So far, we have simply assumed **all** pages of a process is mapped to physical frames, but we will see this is not always the case

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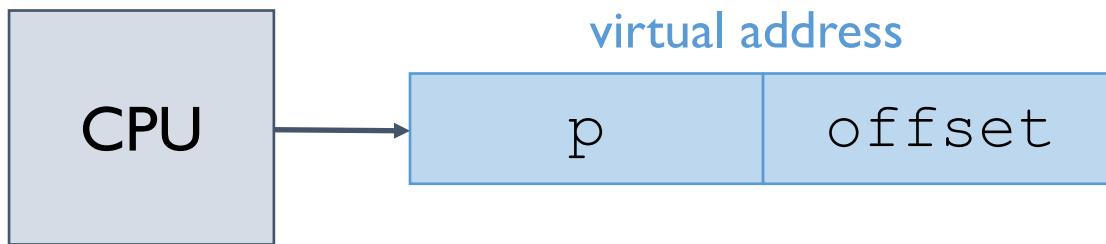
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- Processes use virtual (logical) addresses to refer to memory (not page number!)
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- Page table must ultimately translate virtual address to physical address

Page Table: Virtual to Physical Address

virtual address consists of 2 parts:

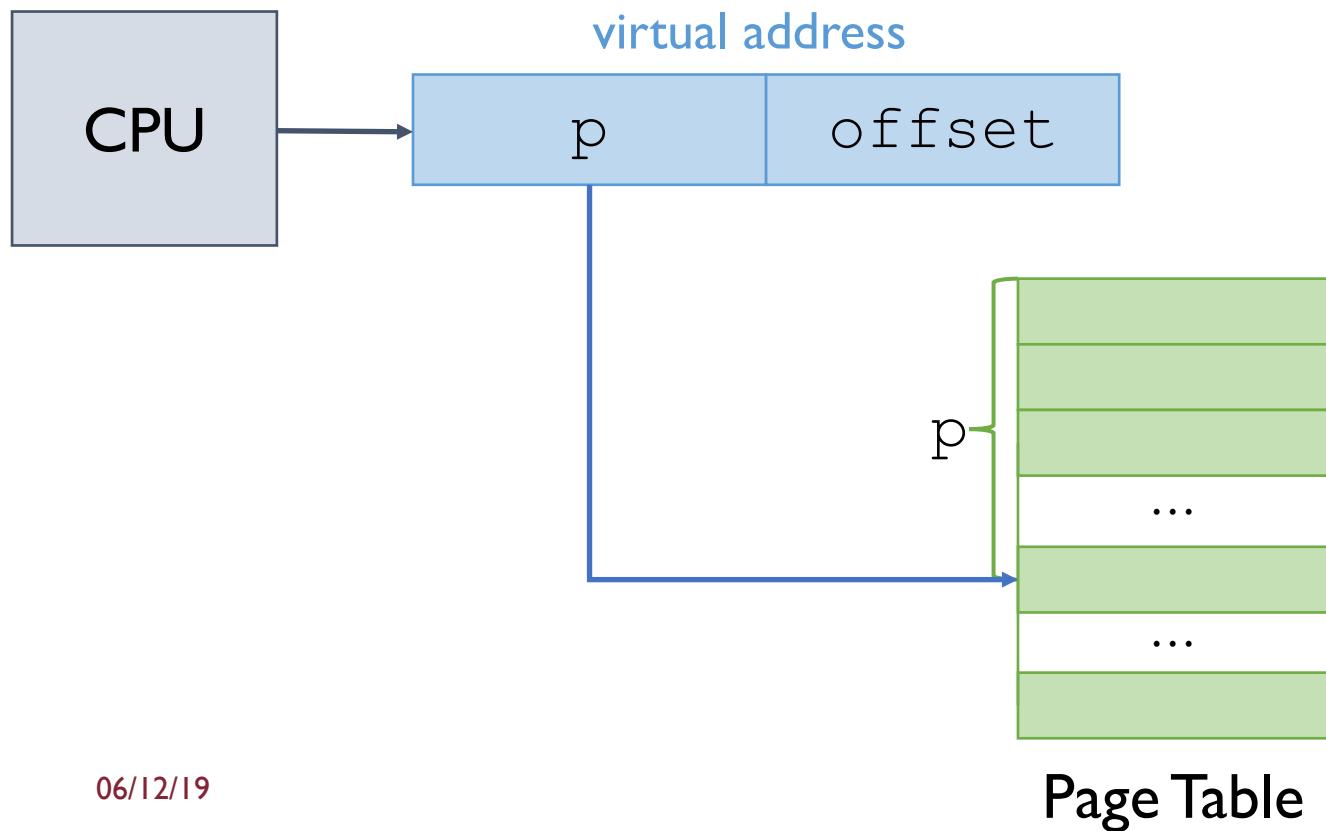
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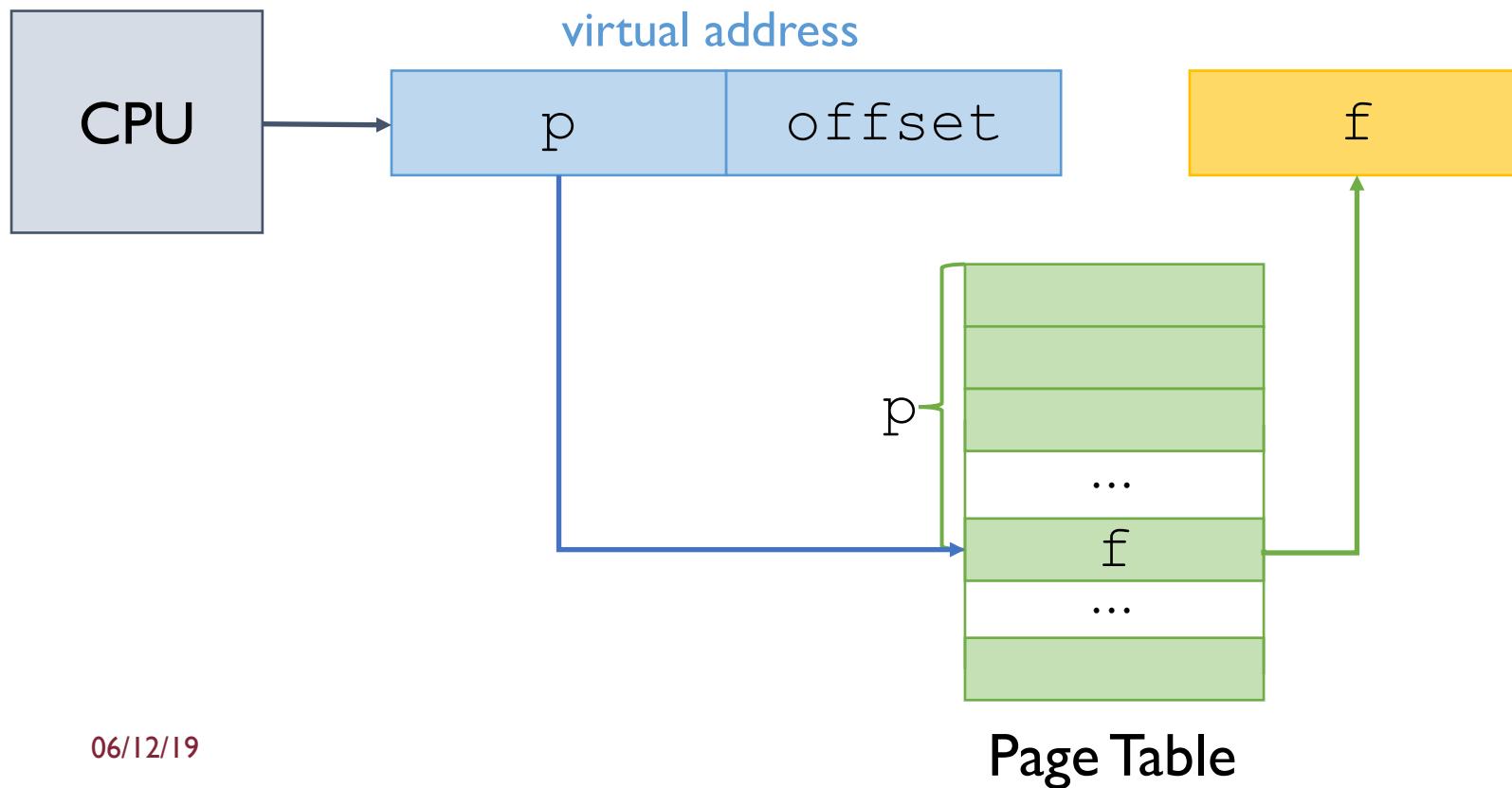
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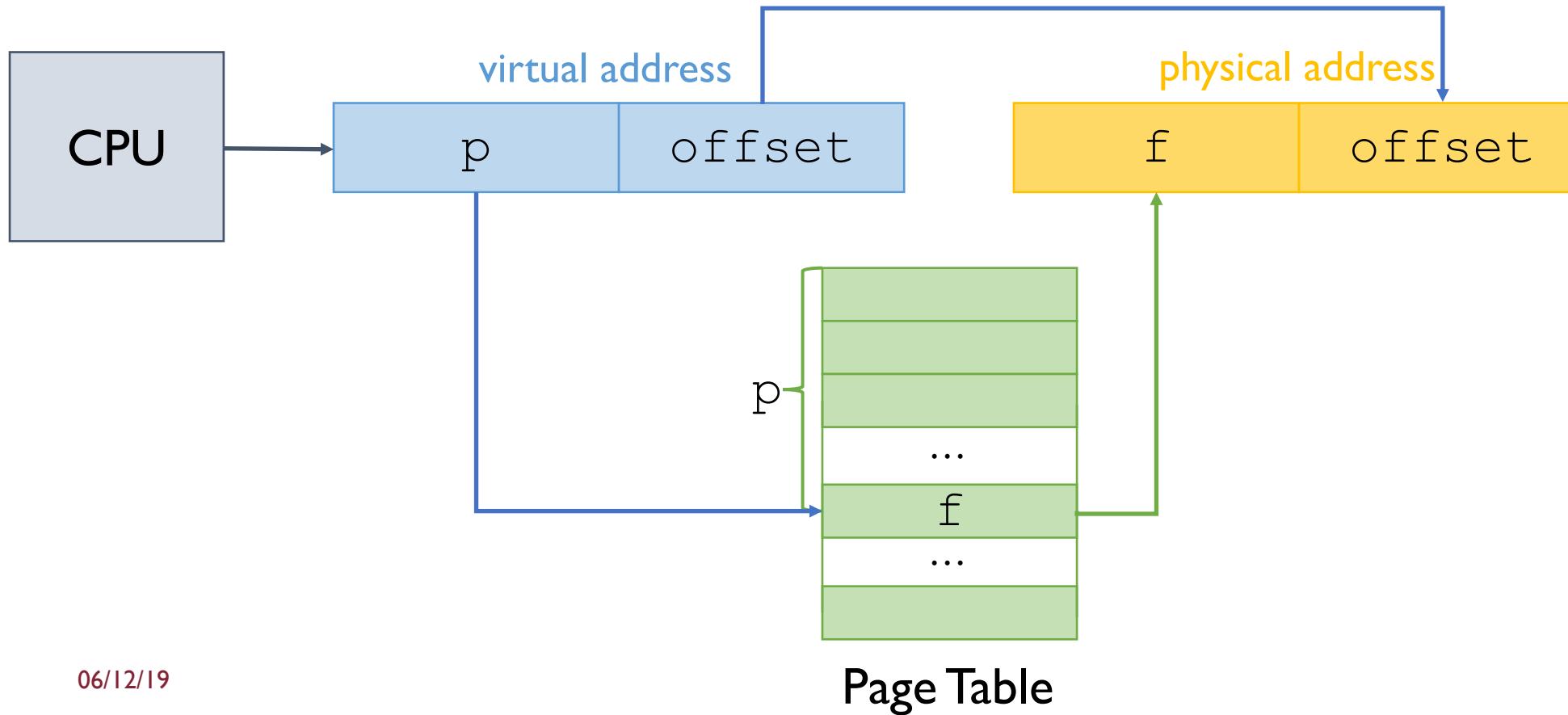
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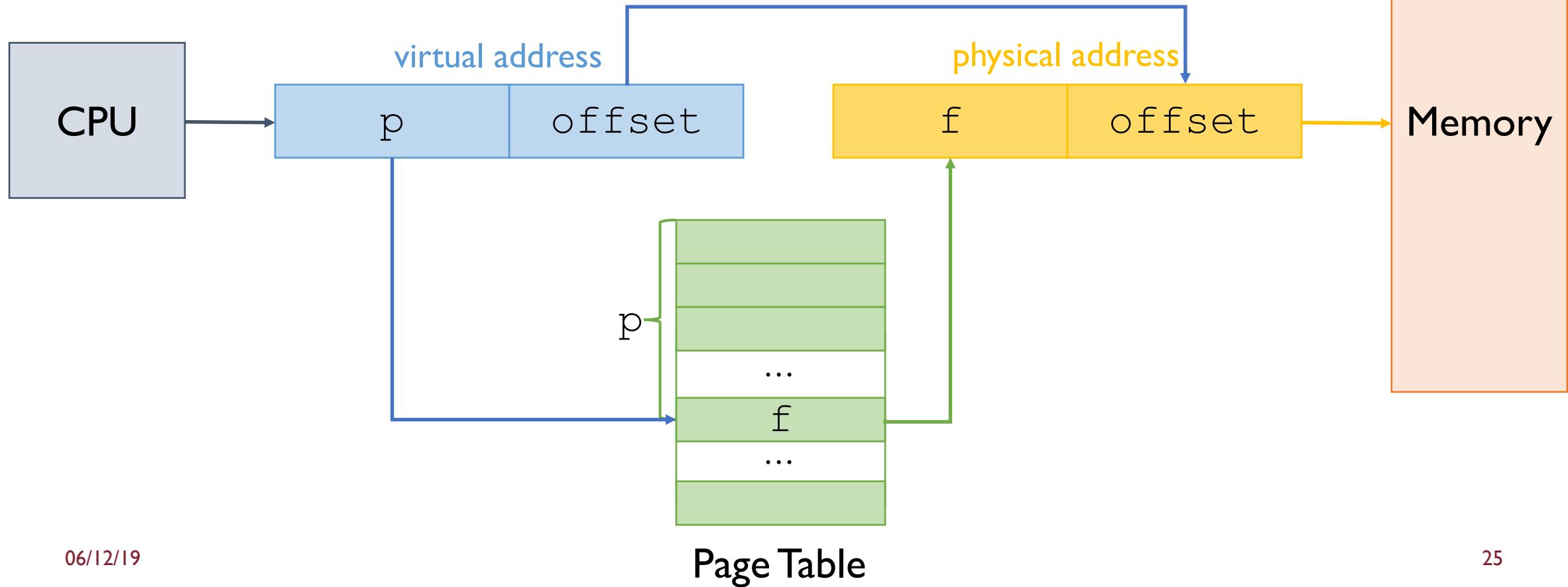
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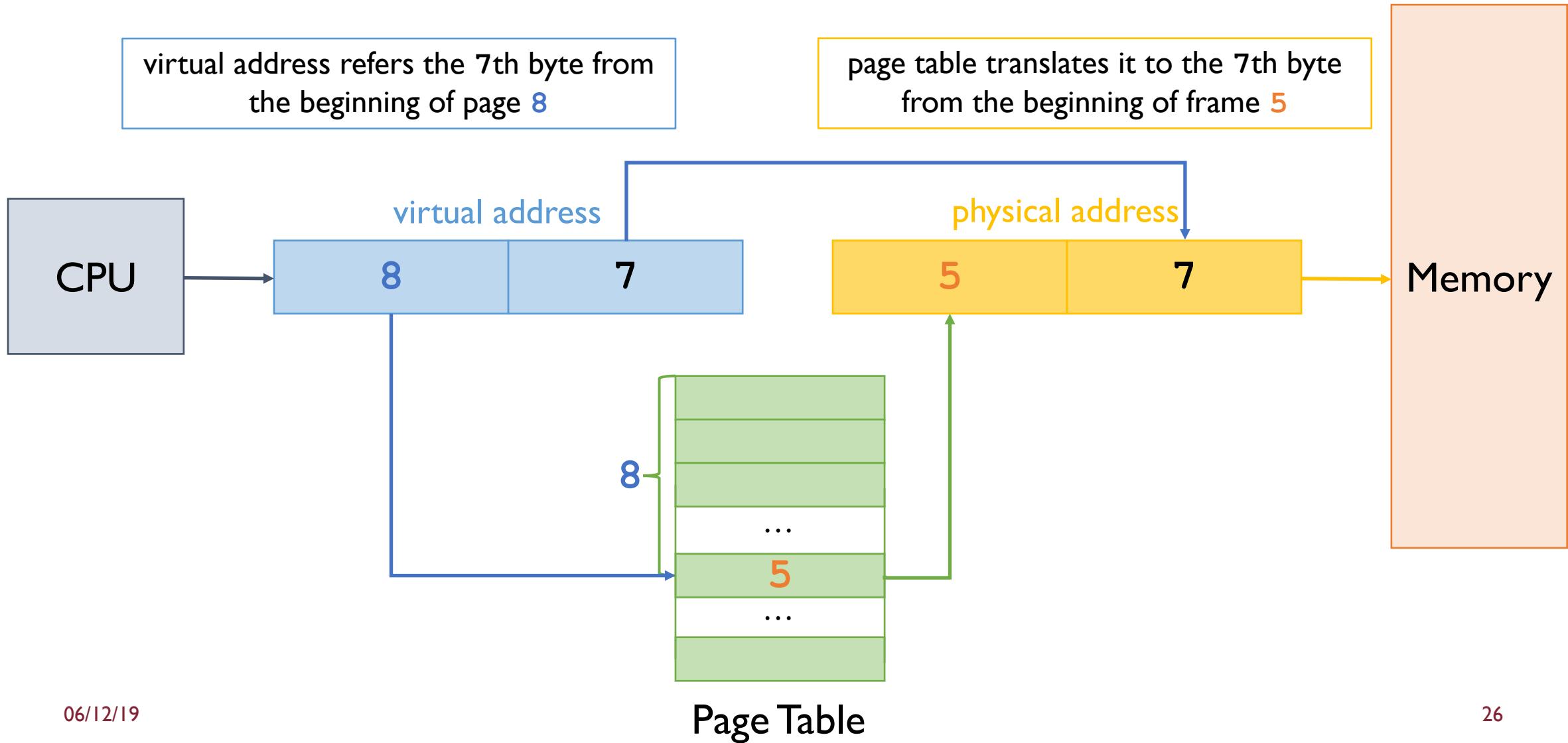
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physical address also consists of 2 parts:

- f: physical frame number
- offset: as above



Page Table: Example of Address Translation



Paging Hardware

- Paging can be a form of dynamic relocation
- Each virtual address is bound by the paging hardware (i.e., page table) to a physical address
- Page table can be seen just as a set of base (relocation) registers, one for each frame
- Mapping is invisible to the user process: the OS maintains the page table and translation happens in hardware
- Protection is provided similarly to dynamic relocation (limit register)

Paging Hardware: Steps

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- I. Get the page number (**p**) and the **offset** where the virtual address **x** resides
2. Use **p** to index into the page table to retrieve the frame number **f**
3. Combine **f** with **offset** to obtain the physical address **y**

Paging Hardware: Get **p** and offset from **x**

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Address translation requires a **div** and a **mod** operation

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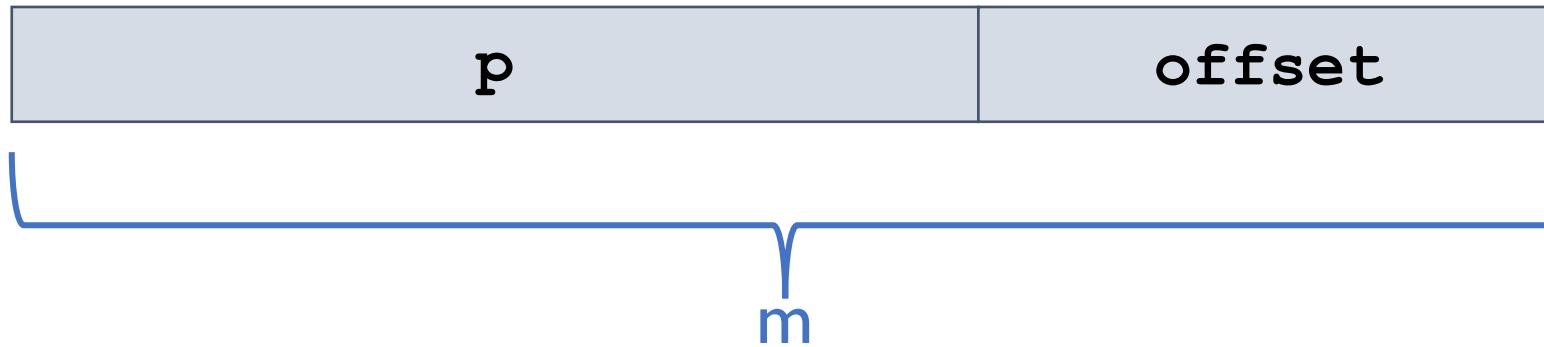
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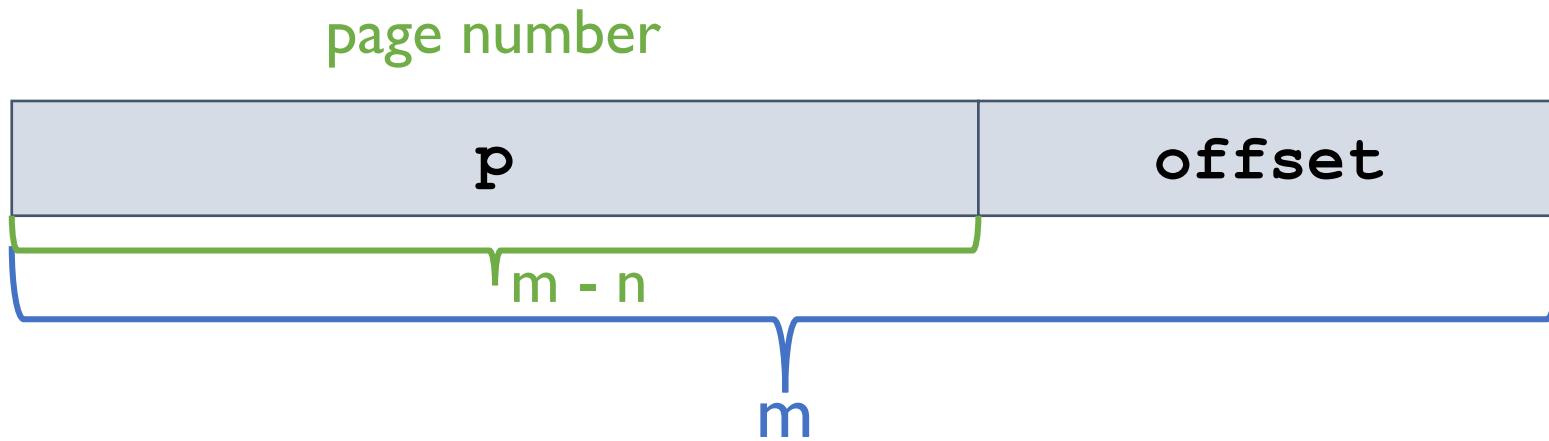
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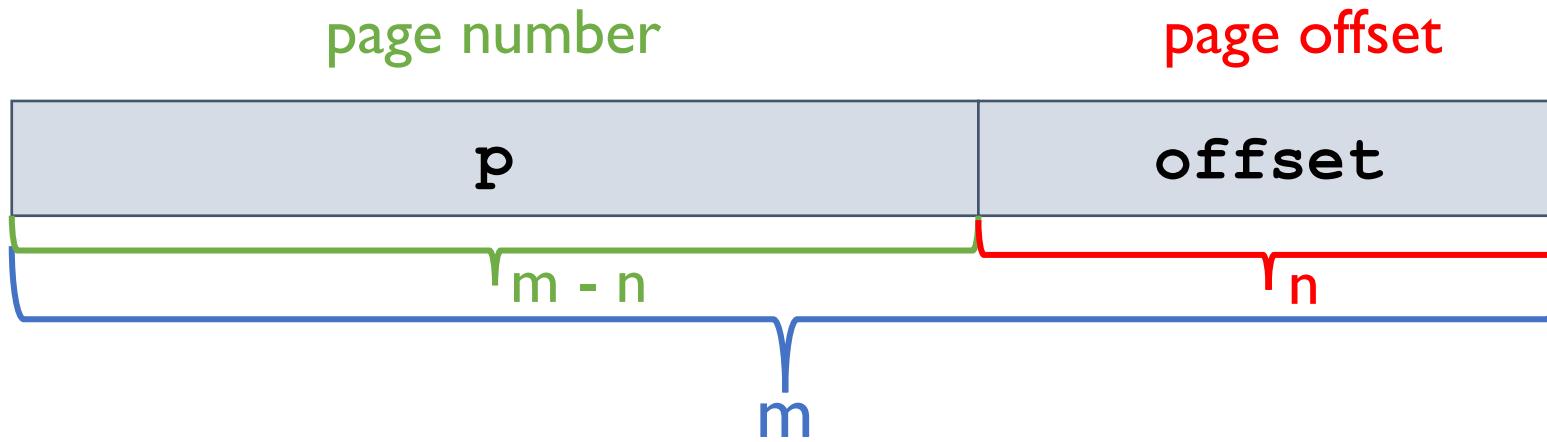
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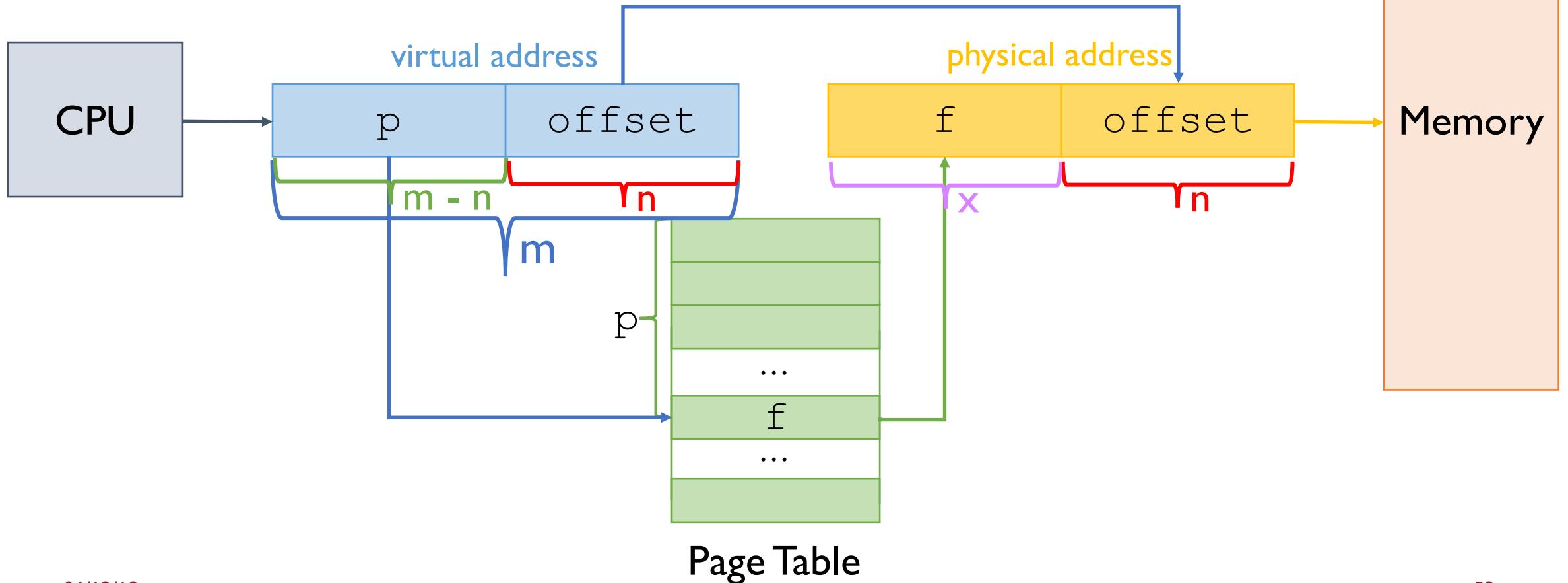
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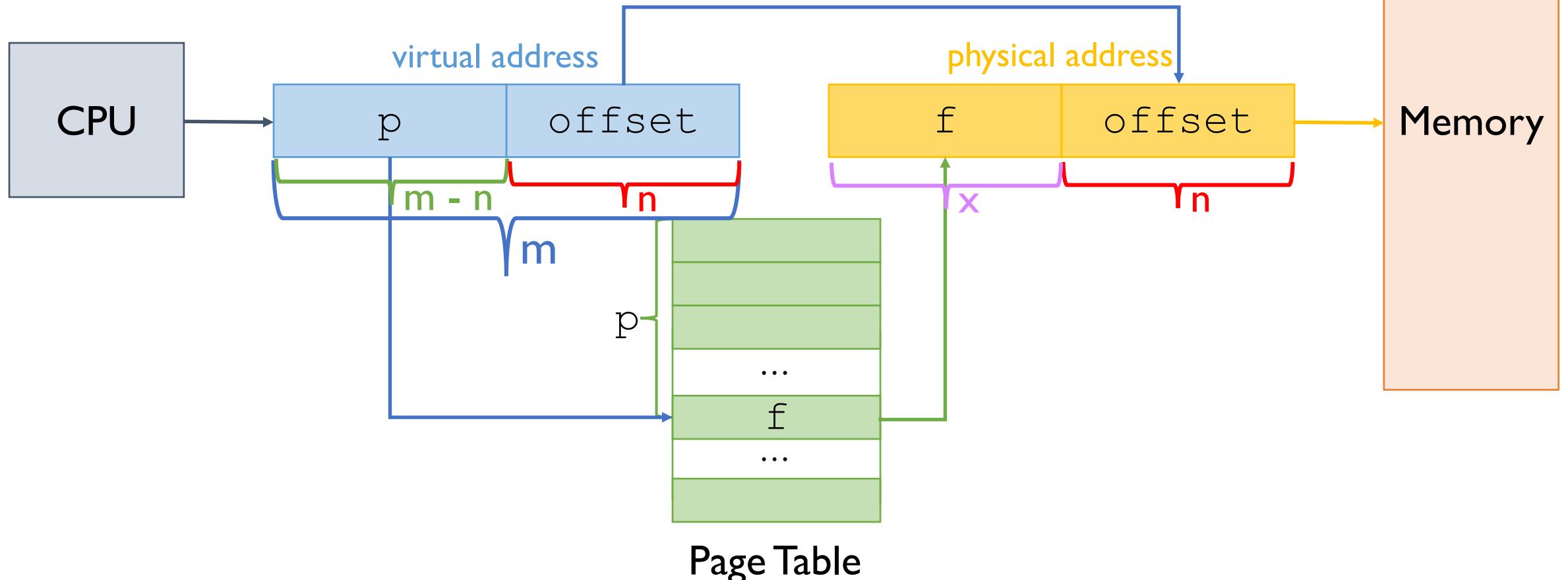
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NOTE

$m-n$ doesn't necessarily have to be equal to x



Paging Hardware: Practical Details

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 - That means each page/frame is $2^{12} = 4\text{KiB}$
- Assuming $m = 32$ bits, there are $2^{m-n} = 2^{20} = 1\text{MiB}$ pages/frames
 - That means page table has 2^{20} entries (i.e., one for each page/frame)

Paging Hardware: Practical Example

Suppose we have a virtual memory and a physical memory, both of size $M = 1024B$ (1KiB)

Q1

How many bits are needed for a virtual/physical address (assuming single-byte addressing)

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R1

10 bits to address $M = 1024$ bytes (both for virtual and physical address)

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$T = M / S = 1024 \text{ memory bytes} / 16 \text{ bytes per page} = 64 \text{ pages}$

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Q3

What is p and offset (i.e., how many bits for p and offset?)

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R3

Our logical address is made of $m = 10$ bits

$n = 4$ bits are used to represent the offset, as each page/frame is $S = 16$ bytes

$m-n = 6$ bits are used to represent page number p , as there are $T = 64$ pages

Paging Hardware: Practical Example

Q4

Translate the virtual address $x = 42$, assuming the following page table

page	frame
0	12
1	5
2	37
3	0
...	..
63	29

Paging Hardware: Practical Example

Q4

Translate the virtual address $x = 42$, assuming the following page table

page	frame
0	12
1	5
2	37
3	0
...	..
63	29

R4

$$p = x \text{ div } S = 42 \text{ div } 16 = 2$$

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R4

$$p = x \text{ div } S = 42 \text{ div } 16 = 2$$

$$\text{offset} = x \text{ mod } S = 42 \text{ mod } 16 = 10$$

10th byte from the beginning of frame 37

Paging Hardware: Practical Example 2

Suppose we still have a virtual memory and a physical memory, both of size $M = 1024B$

Q1

So far, we have assumed that computers work on single-byte (i.e., 8-bit architecture). Modern computers however operate natively on multiple of bytes (i.e., **words**) rather than single-byte. Typical values of word length is: 16, 32 or 64 bits.

If we assume 32-bit architecture (i.e., word = 32 bits = 4 bytes), virtual addresses refer to words instead of bytes

How many bits are therefore needed to address the number of words available on M?

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R1

8 bits to address $M = 1024/4 = 256$ 4-byte **words** (both for virtual and physical address)

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Now, assume we still use paging with page/frame size $S = 16B$

Q2

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$T = M / S = 1024 \text{ memory bytes} / 16 \text{ bytes per page} = 64 \text{ pages}$

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Q3

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R3

Our logical address is now made of $m = 8$ bits
 $n = 2$ bits are used to represent the offset, as each page/frame is:

$$S = 16 \text{ bytes} = 4 * 4\text{-byte words}$$

$m-n = 6$ bits are used to represent page number p, as there are still $T = 64$ pages

Paging Hardware: Practical Example 2

Q4

Translate the virtual address $x = 7$, assuming the following page table

page	frame
0	12
1	5
2	37
3	0
...	..
63	29

Paging Hardware: Practical Example

Q4

Translate the virtual address $x = 7$, assuming the following page table

page	frame
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Remember: now virtual address refers to a 4-byte word!

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$S = 16 \text{ bytes} = 4 * 4\text{-byte words}$

Must be expressed in terms of
number of words

R4

$$p = x \text{ div } S = 7 \text{ div } 4 = 1$$

Paging Hardware: Practical Example 2

Q4

Translate the virtual address $x = 7$, assuming the following page table

page	frame
0	12
1	5
2	37
3	0
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R4

$$p = x \text{ div } S = 7 \text{ div } 4 = 1$$

$$\text{offset} = x \text{ mod } S = 7 \text{ mod } 4 = 3$$

3rd word from the beginning of frame 5

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- Trade-off solution: **Translation Look-aside Buffer (TLB)**

Appendix: Registers and Main Memory

- All memory accesses are equivalent: the memory hardware doesn't know what a particular part of memory is being used for
- CPU can only access its registers and main memory (any access to other devices, e.g., hard drive, requires data to be moved into main memory first)
- Access to registers is very fast, generally one clock cycle
- Access to main memory is comparatively slow, and may take several clock cycles to complete

Appendix: Cache Memory

- Bridge the gap between fast registers and slower main memory
- Cache Memory: on-chip (thereby, fast!) intermediary memory built into most modern CPUs
- Several chunks of memory transferred from main memory to the cache
- Access individual memory locations one at a time from the cache rather than from memory directly

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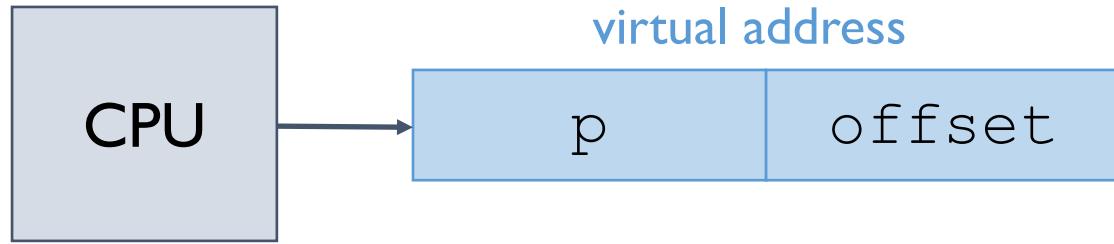
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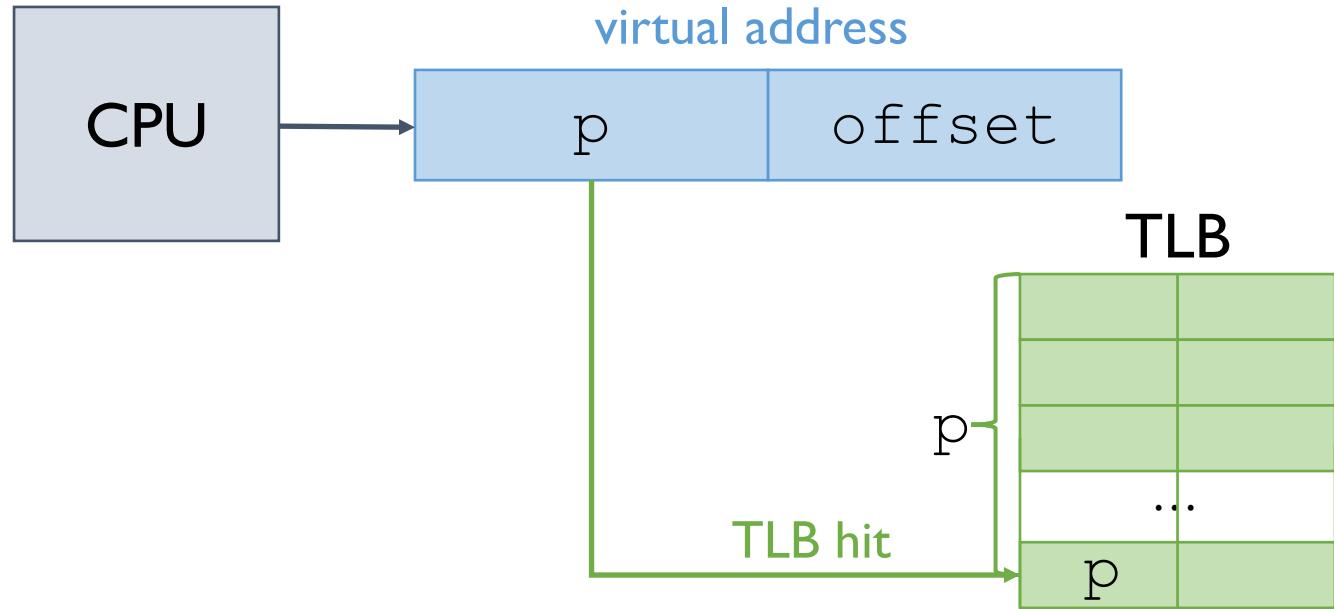
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- Locality still holds for address translation
- Typical TLB sizes range from 8 to 2048 entries

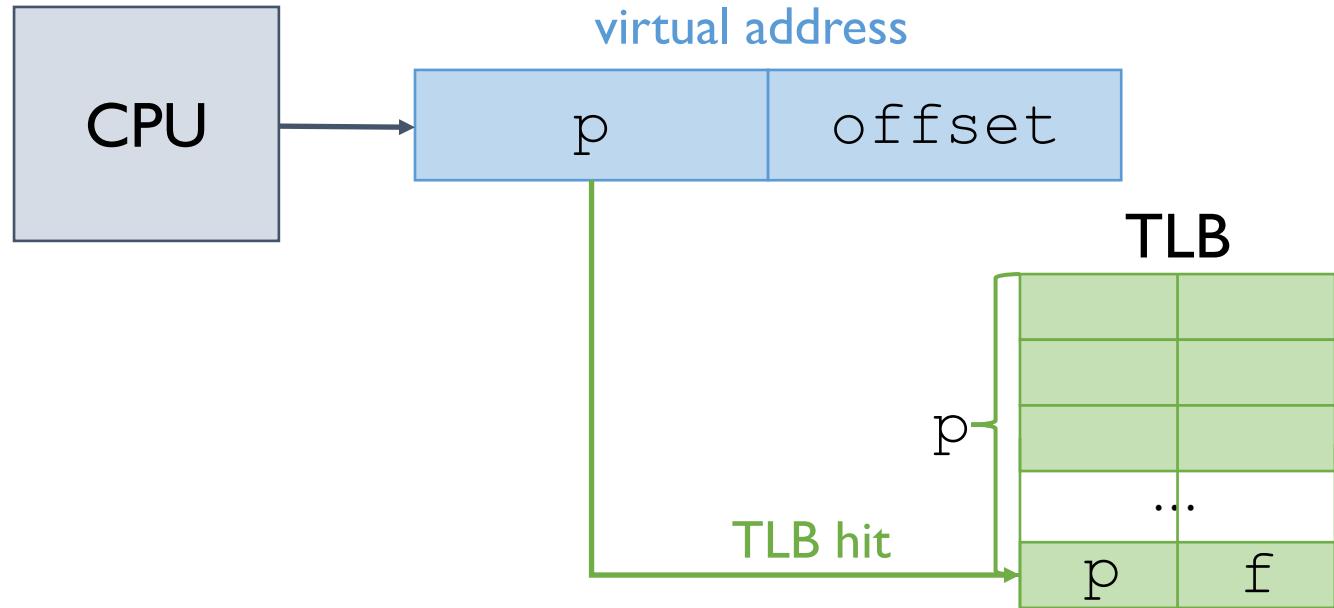
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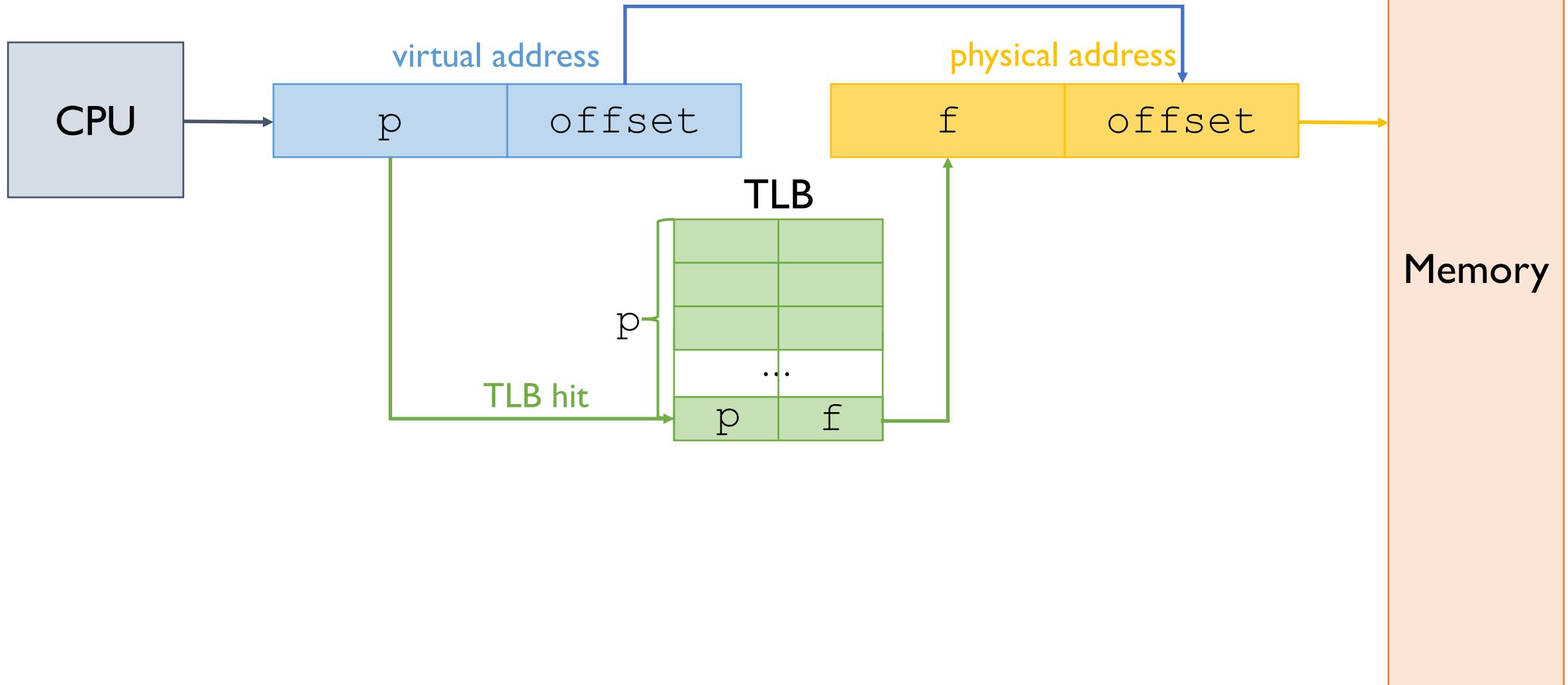
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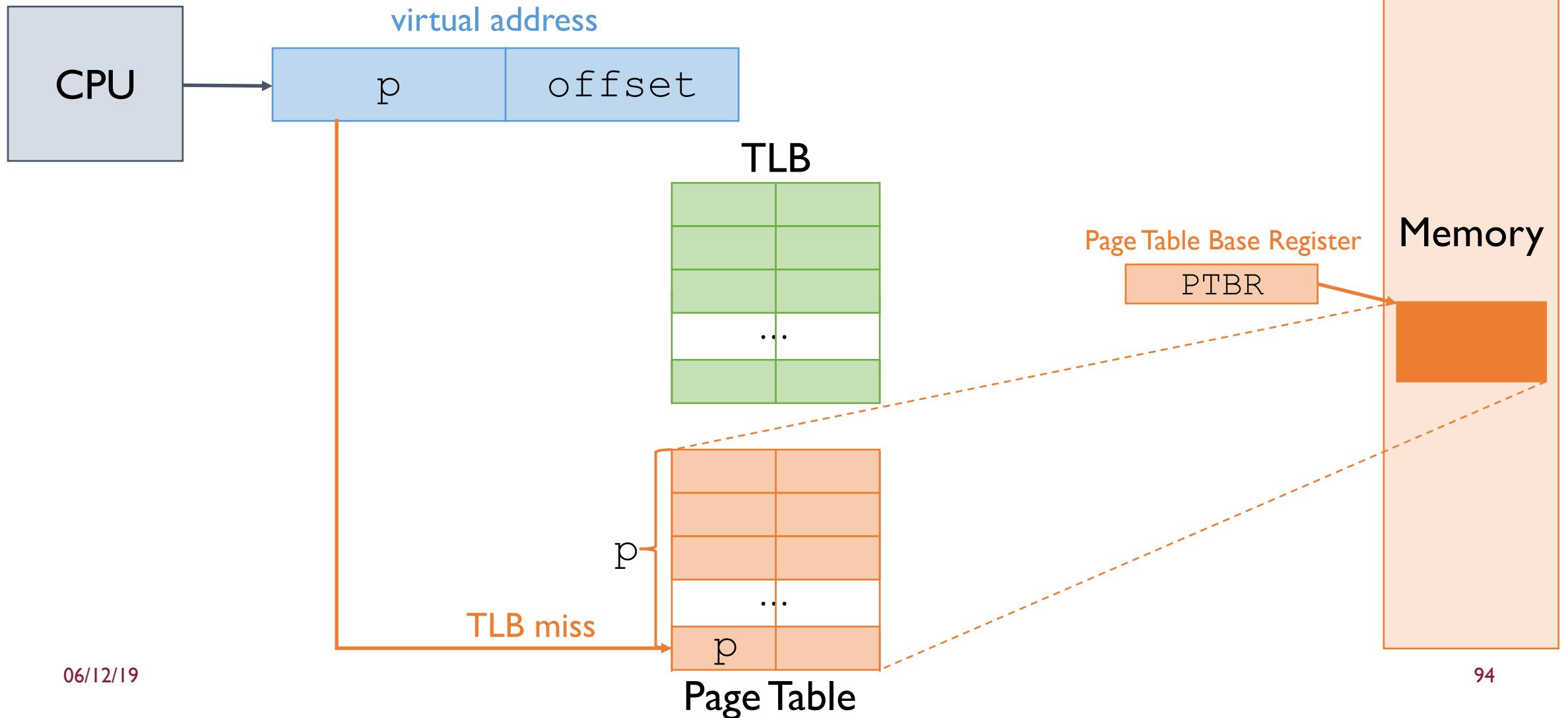
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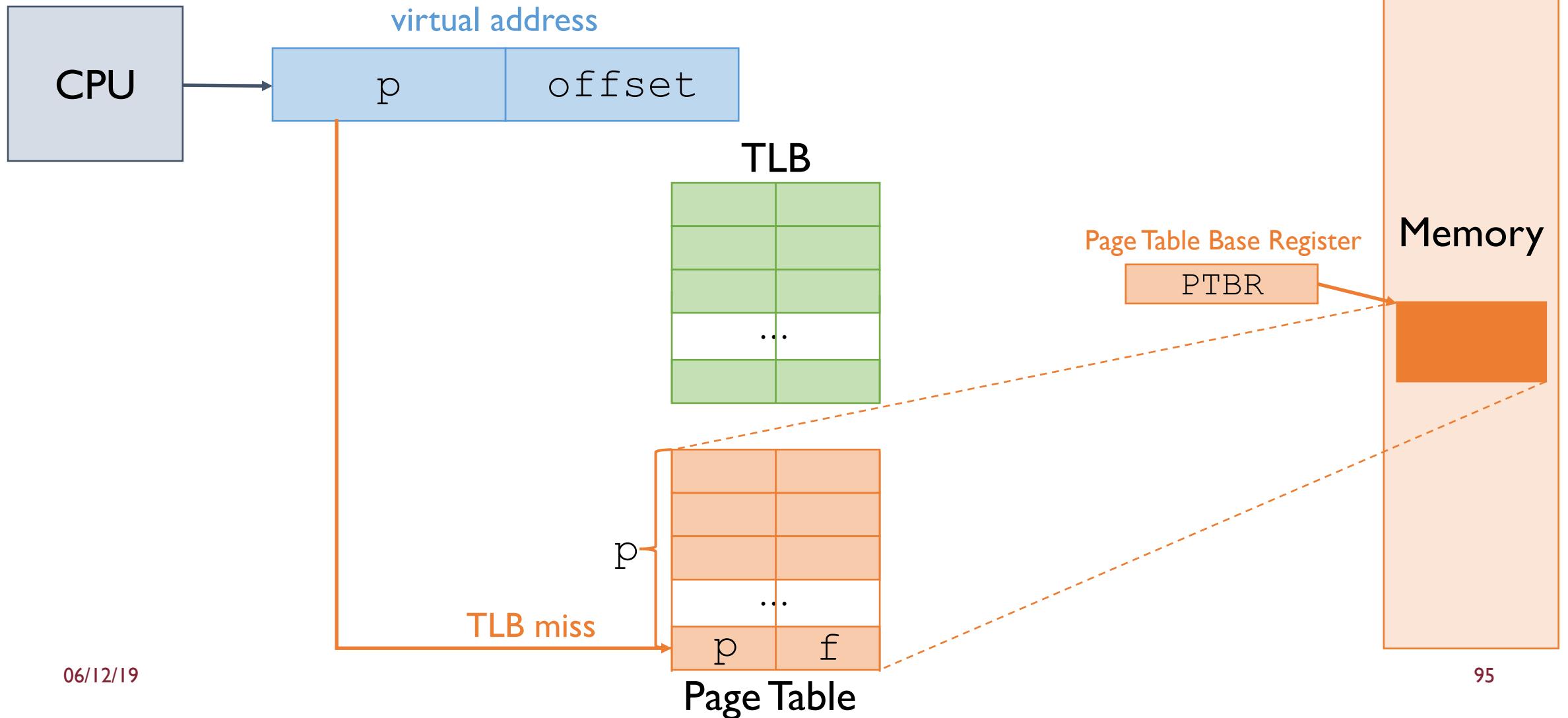
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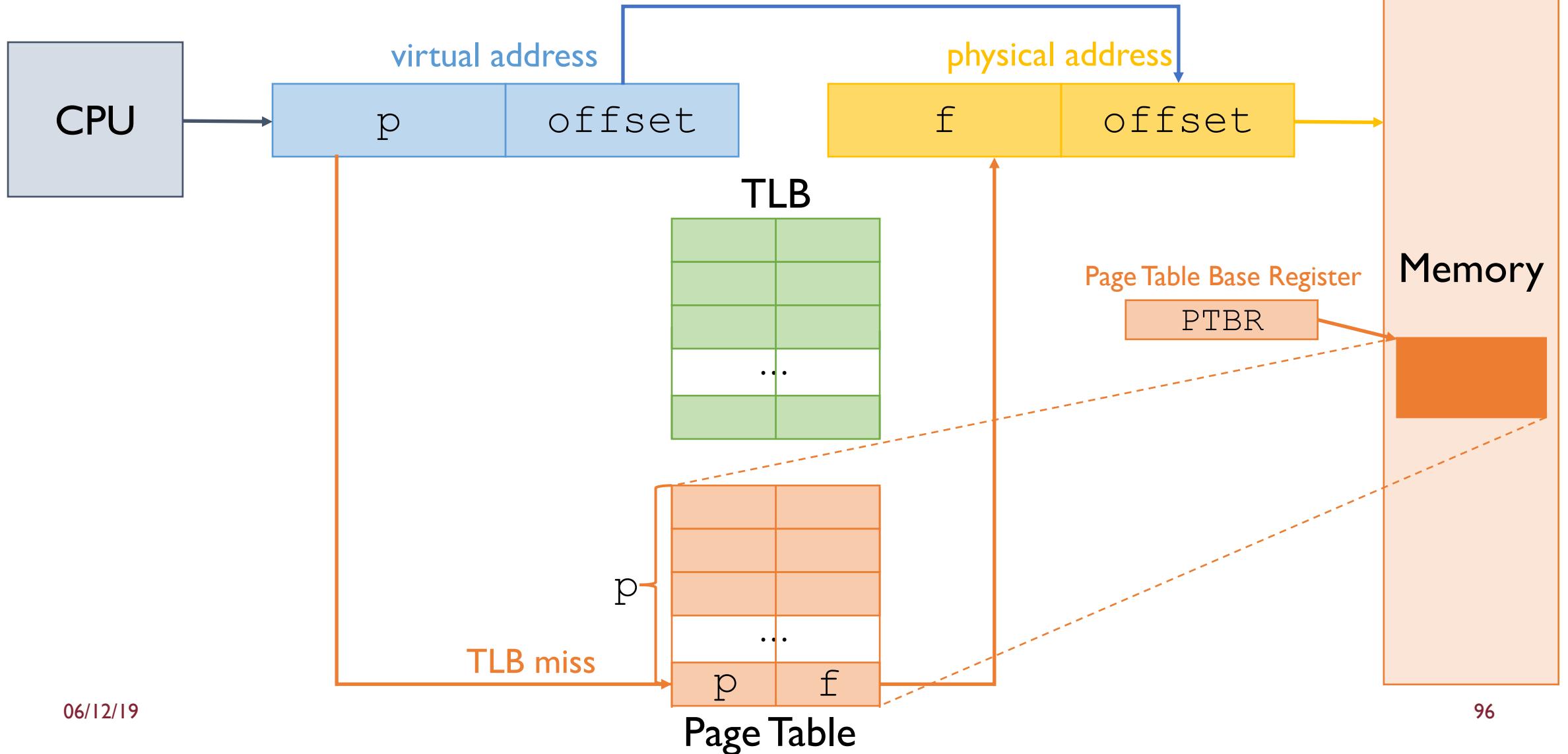
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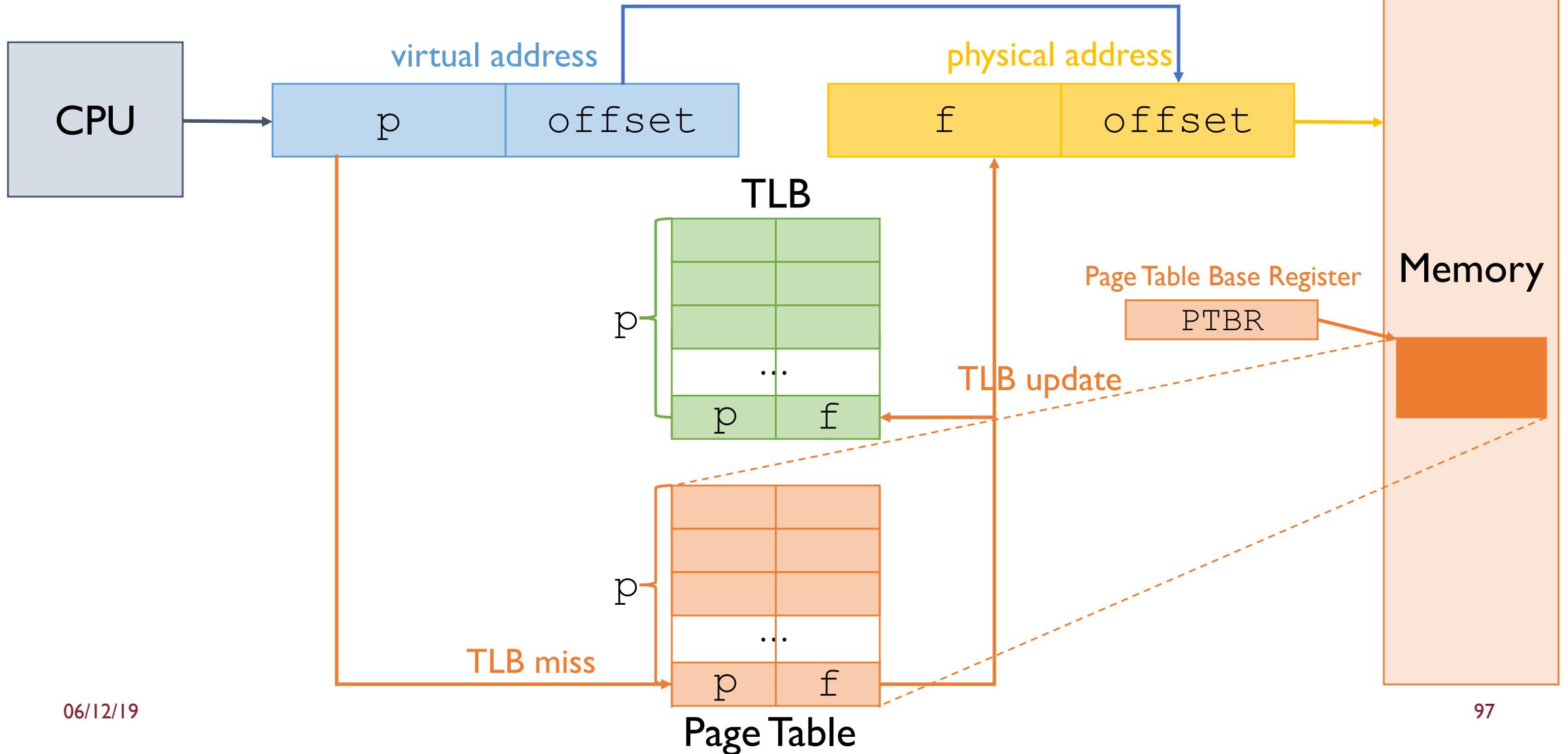
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 - **basic:** at each context switch the content of the TLB is fully flushed and cleaned (cold-start → the first accesses will generate all TLB misses)
 - **advanced:** TLB entries dumped and restored within the PCB or adding a so-called process context ID (PCID) to each entry (the CPU will use a TLB entry iff the PCID of that entry corresponds to the ID of the running process)

Memory Access Cost

t_{MA} = physical memory access time

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The larger the TLB the higher the probability p of hit ratio,
thereby decreasing the average memory access cost

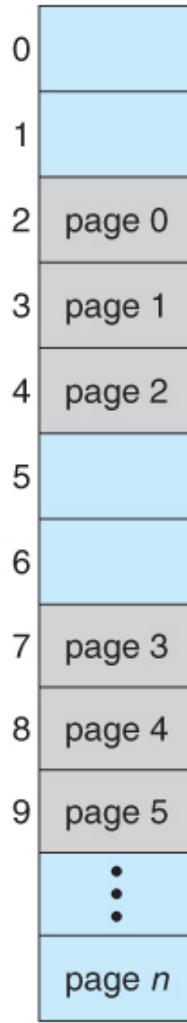
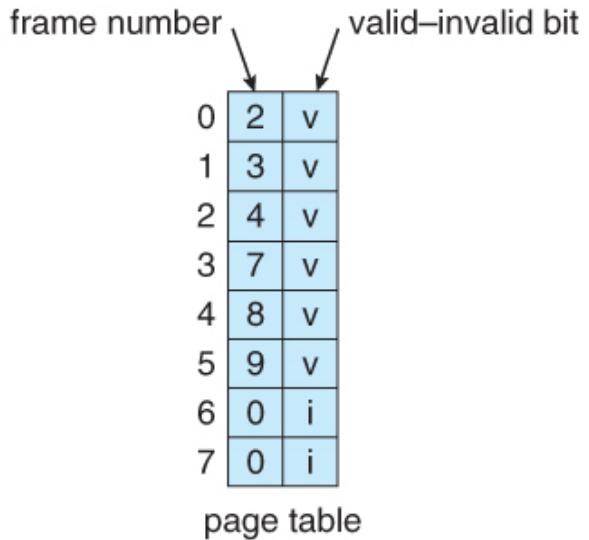
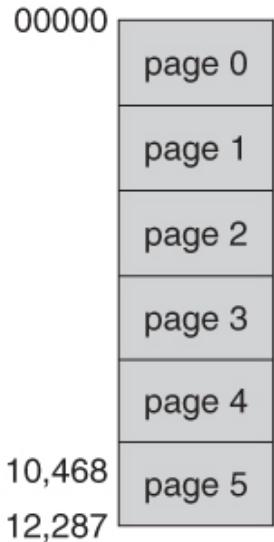
Additional Protection

- The page table can also help to protect processes from accessing memory they shouldn't, or their own memory in correct ways
- A bit or bits can be added to the page table to classify a page as read-write, read-only, read-write-execute, or combination of those
- Each memory reference can be checked to ensure it is accessing the memory in the appropriate mode
- Valid/invalid bits can be added to "mask off" entries in the page table that are not in use by the current process

Additional Protection

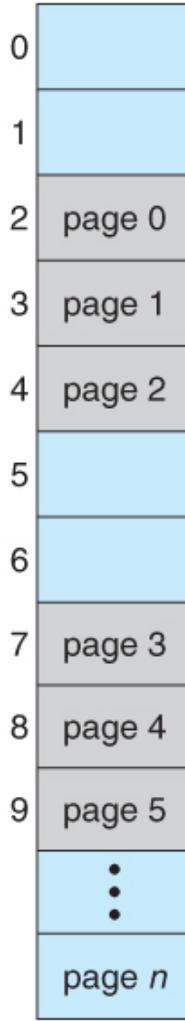
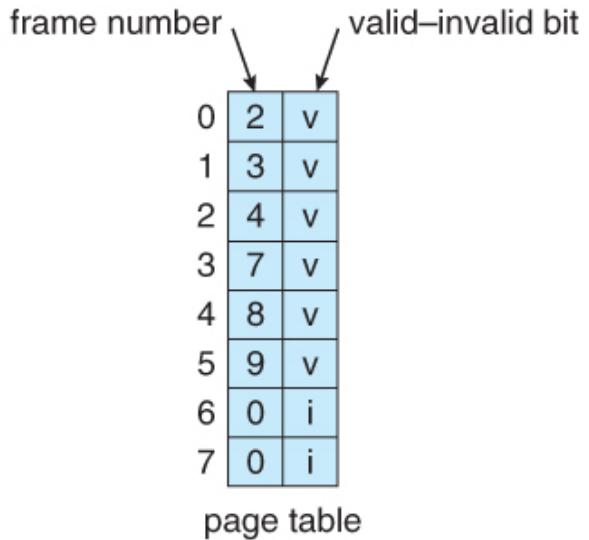
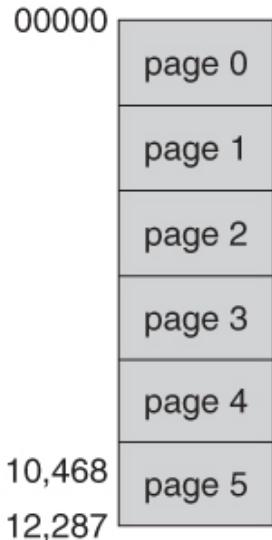
- valid/invalid bits cannot block all illegal memory accesses, due to the internal fragmentation
- Many processes do not use all of the page table entries available, particularly in modern systems with very large potential page tables
- Some systems use a page-table length register (PTLR) to specify the length of the page table

Additional Protection



valid/invalid bits can be used to flush TLB entries upon context switch if basic setup is used

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any entry whose invalid bit is set will be discarded (and updated)

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5. As process runs, OS loads TLB missed entries possibly replacing existing entries if TLB is full

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- On a context switch:
 - Copy the PTBR value to the PCB
 - Copy the TLB to the PCB (optional)
 - Flush the TLB (if TLB is not saved to/restored from the PCB)
 - Restore the PTBR (i.e., with the value of the new running process)
 - Restore the TLB (if it was previously saved)

Sharing Pages

- Paging systems can make it very easy to share blocks of memory, since memory doesn't have to be contiguous anymore

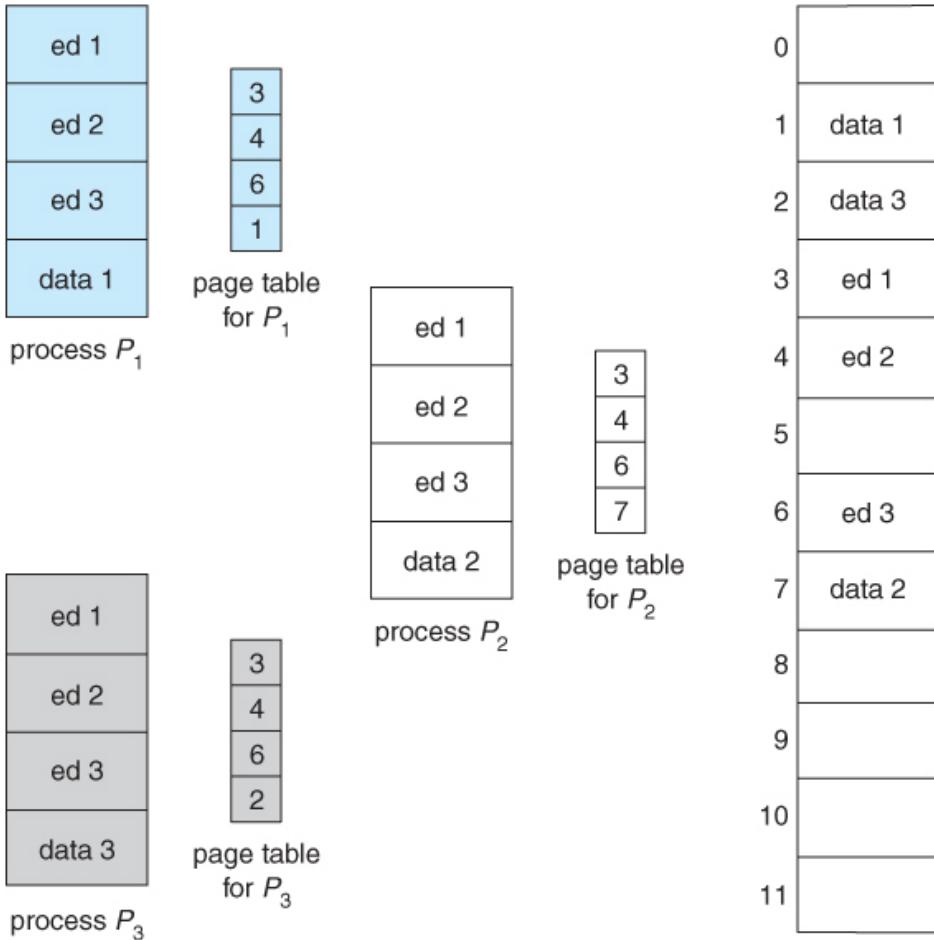
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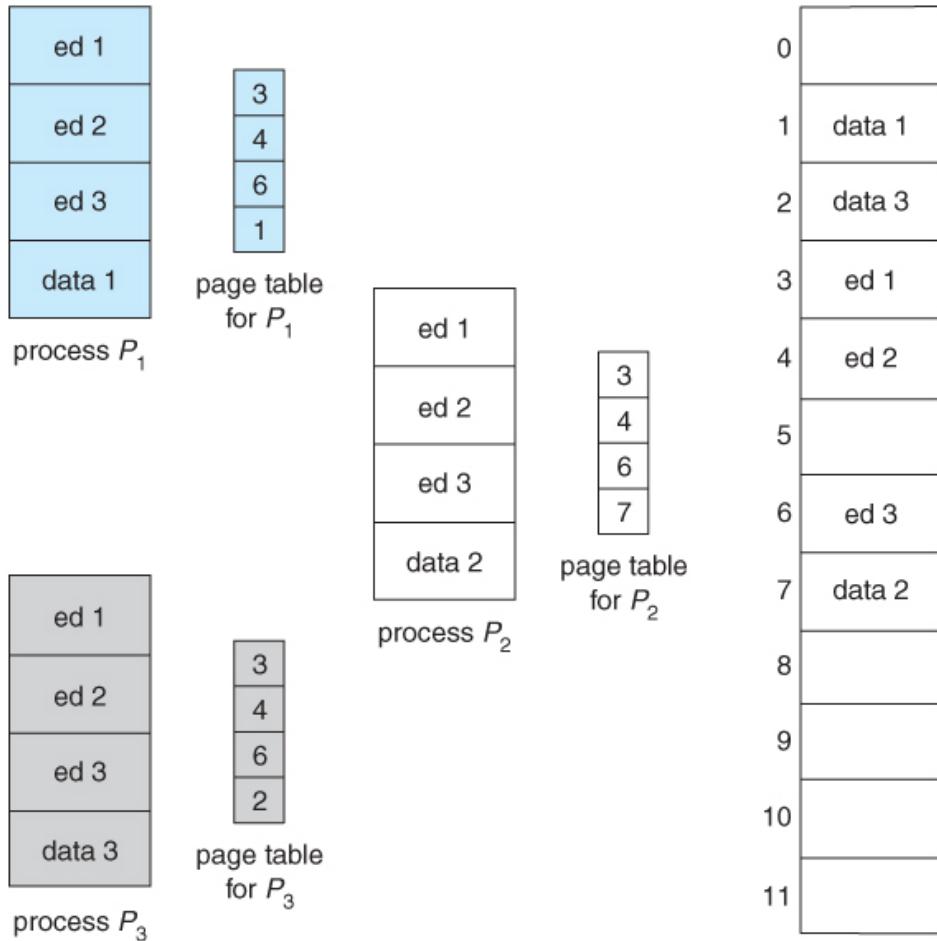
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- This can be done by simply duplicating page entries of different processes to the same page frames (both for code and data)
- Only if code is **reentrant**:
 - it does not write to or change the code (i.e., it is non self-modifying)
 - the code can be shared by multiple processes, as long as each has their own copy of the data and registers, including the instruction register

Sharing Pages: Example



3 user processes are using the editor program ed

Sharing Pages: Example



3 user processes are using the editor program **ed**

Only a **single copy** of the code of **ed** is actually loaded in main memory

Paging: Summary

- A big improvement over **relocation**
 - Eliminates the problem of external fragmentation and therefore the need for compaction
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- A big improvement over **relocation**
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 - Allows code sharing among processes, reducing memory footprint
 - Enables processes to run when they are partially loaded
- However, paging comes with its costs:
 - Virtual/Physical address translation may be time consuming
 - Hardware support like TLB cache is needed to make it efficient enough
 - OS has to be inevitably more complex

A Quick Step Back: Segmentation

- Most users (programmers) do not think of their programs as existing in one continuous linear address space

A Quick Step Back: Segmentation

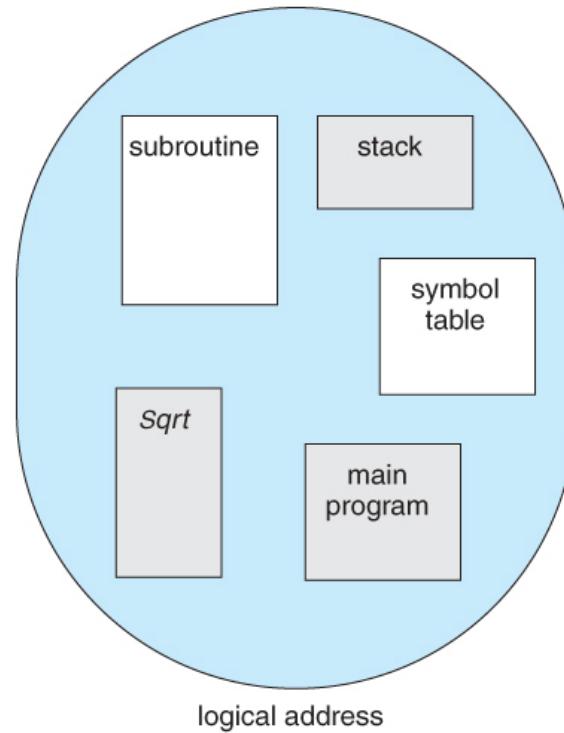
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- Most users (programmers) do not think of their programs as existing in one continuous linear address space
- Rather they think of memory divided in multiple **segments**, each dedicated to a specific use, such as code, data, stack, heap, etc.
- Memory segmentation supports this view by providing addresses with a **segment number** (mapped to a segment base address) and an **offset** from the beginning of that segment

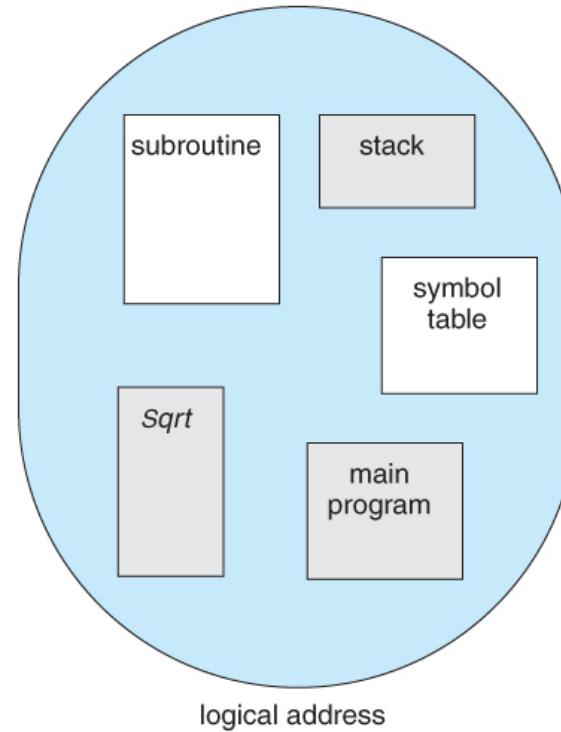
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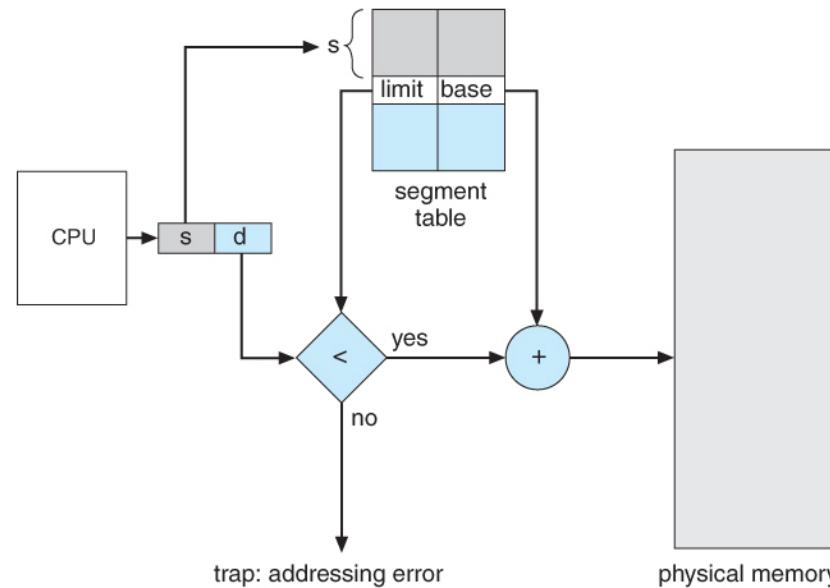
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The compiler generates addresses identifying segments and offset in those

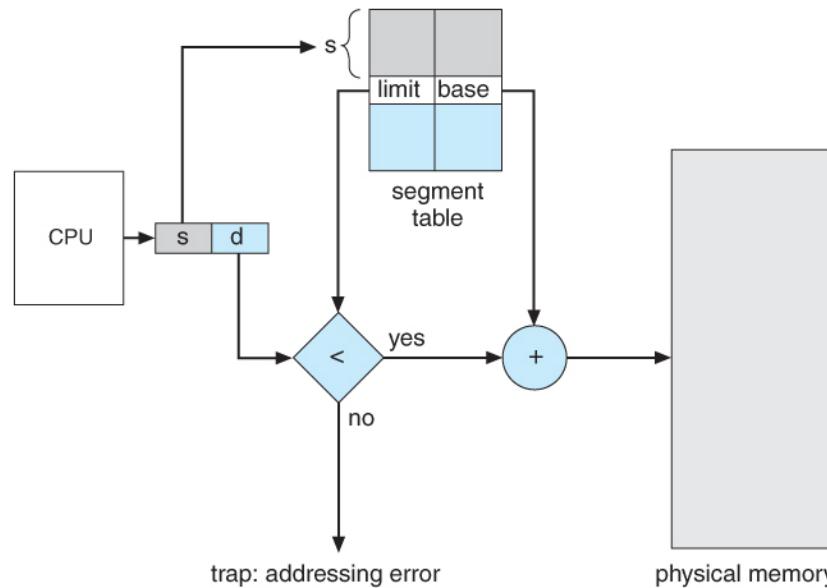
Segmentation Hardware

A **segment table** maps segment-offset addresses to physical addresses, and simultaneously checks for invalid addresses, using a system similar to the page tables and relocation base registers discussed previously



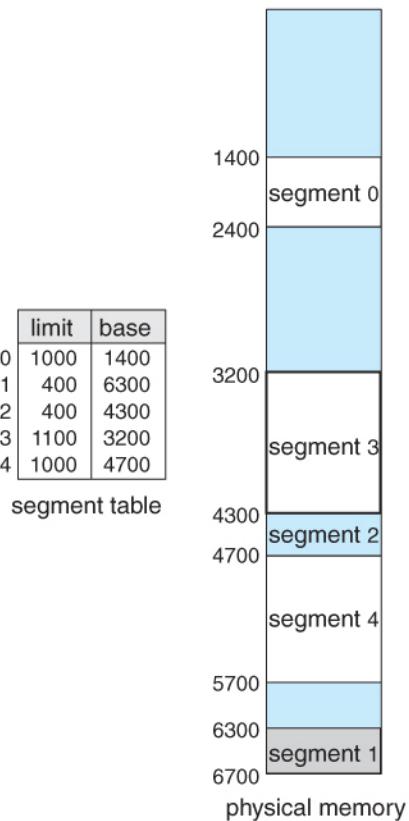
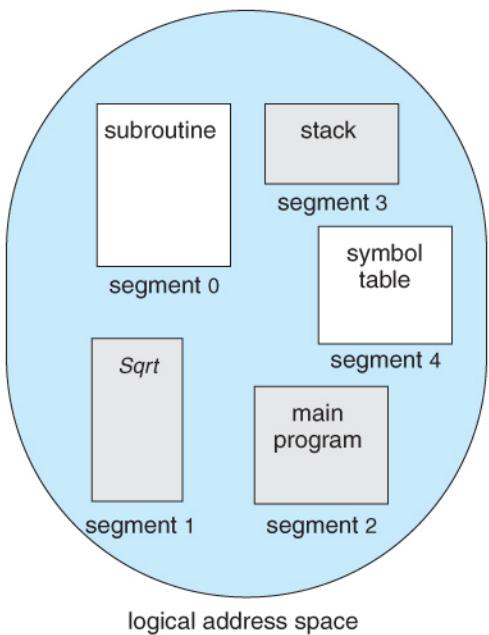
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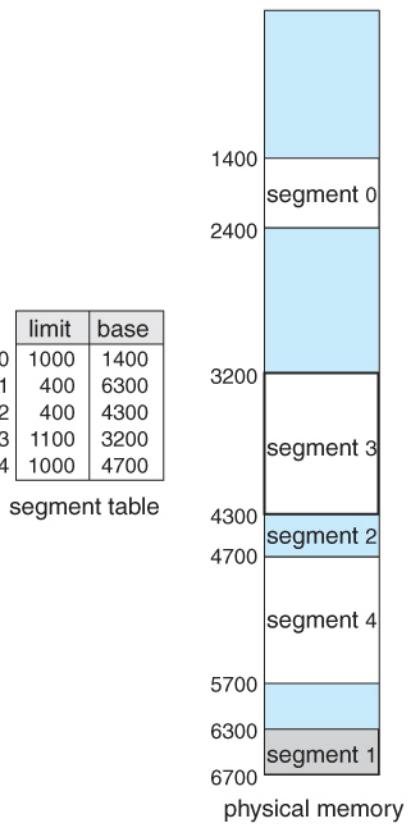
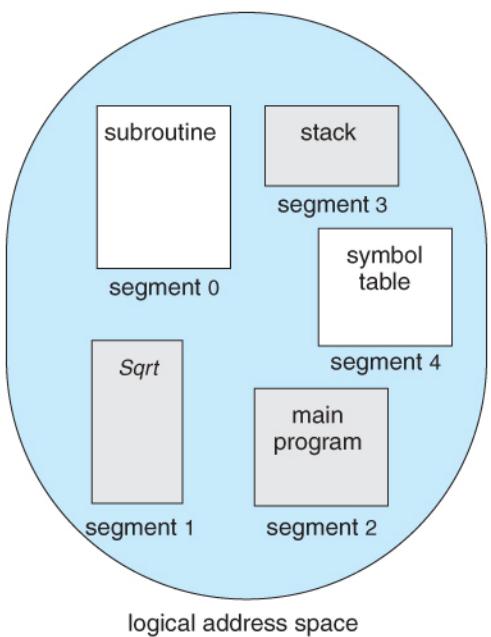
Note that we came back to the assumption that each segment is kept in **contiguous** memory and may be of different sizes...

Segment Table



Each entry contains a base address in memory, the length of the segment, plus additional protection information (e.g., sharing, read/write permissions)

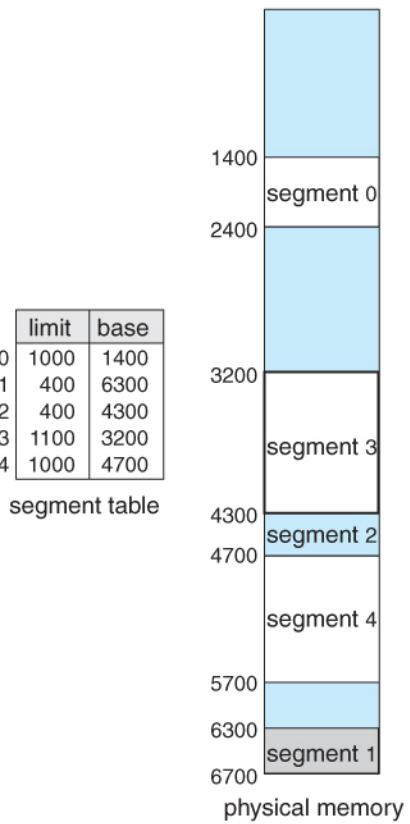
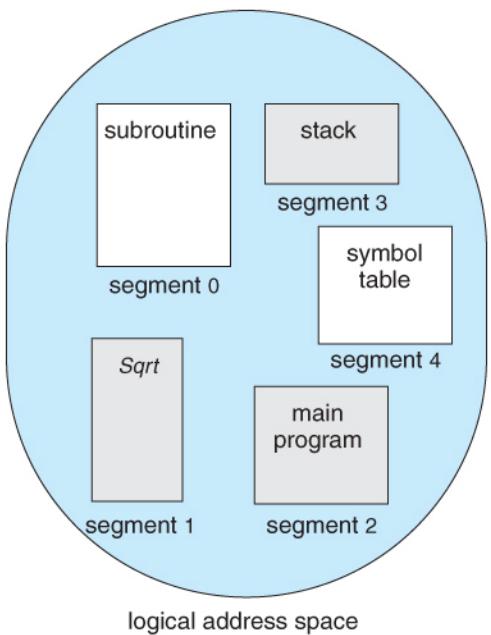
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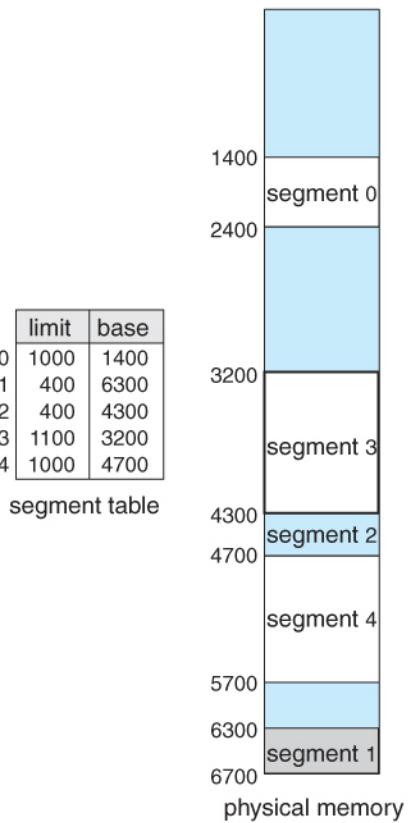
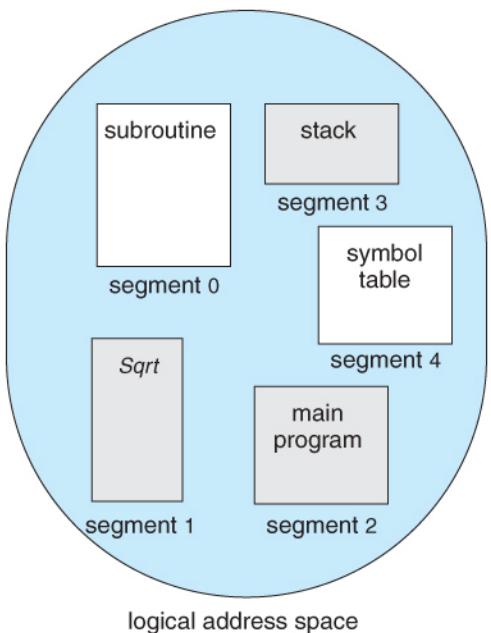


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Segment Table, instead, must store a very limited amount of segments per process (3÷5)

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Combine Segmentation with Paging

Try to get the best of both world

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How?

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How?

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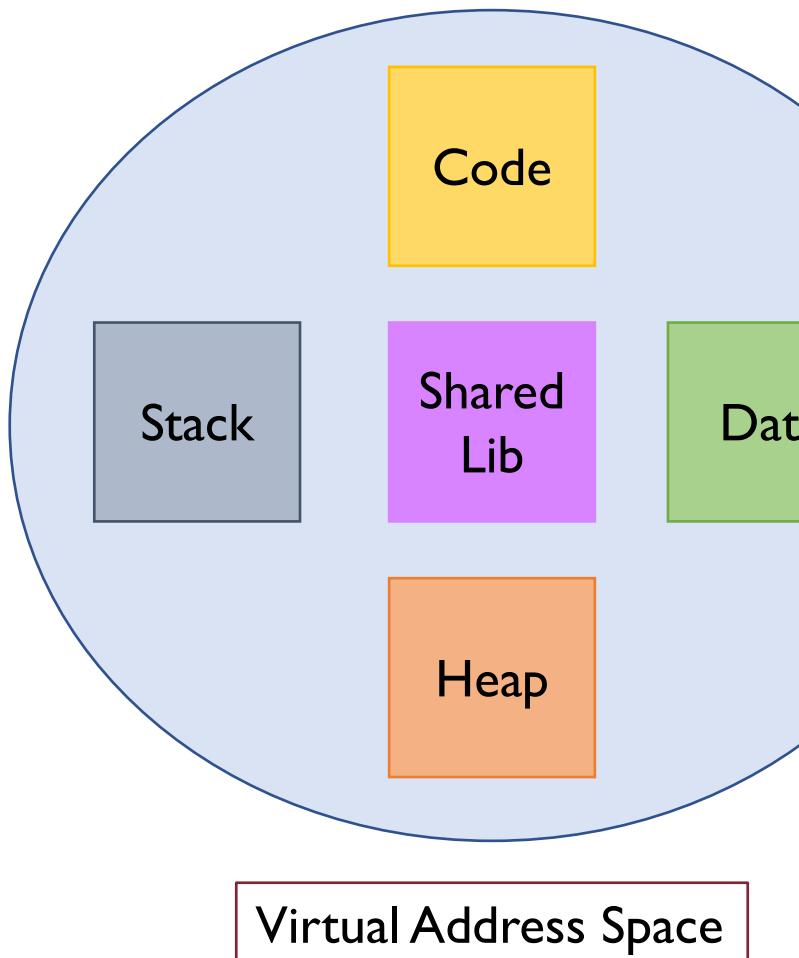
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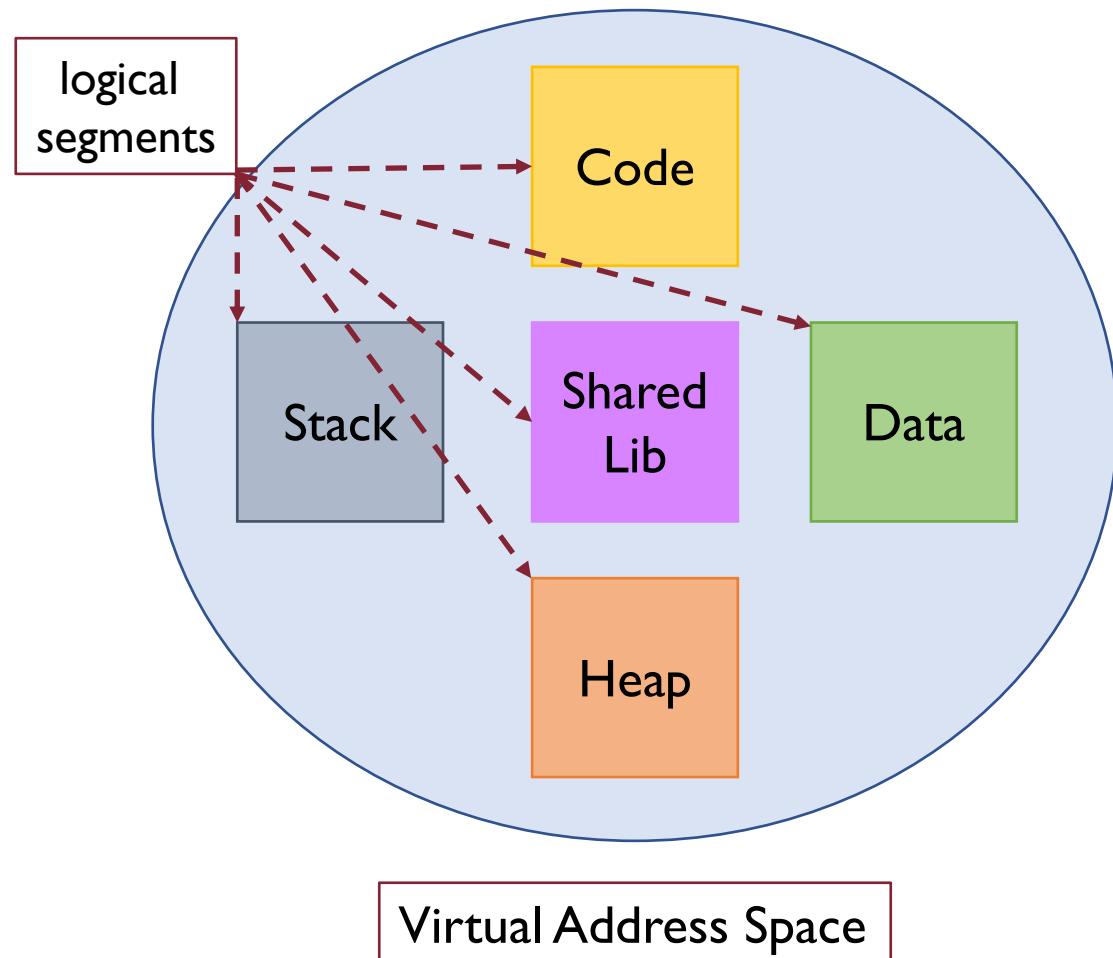


Map a logical segment onto multiple page frames

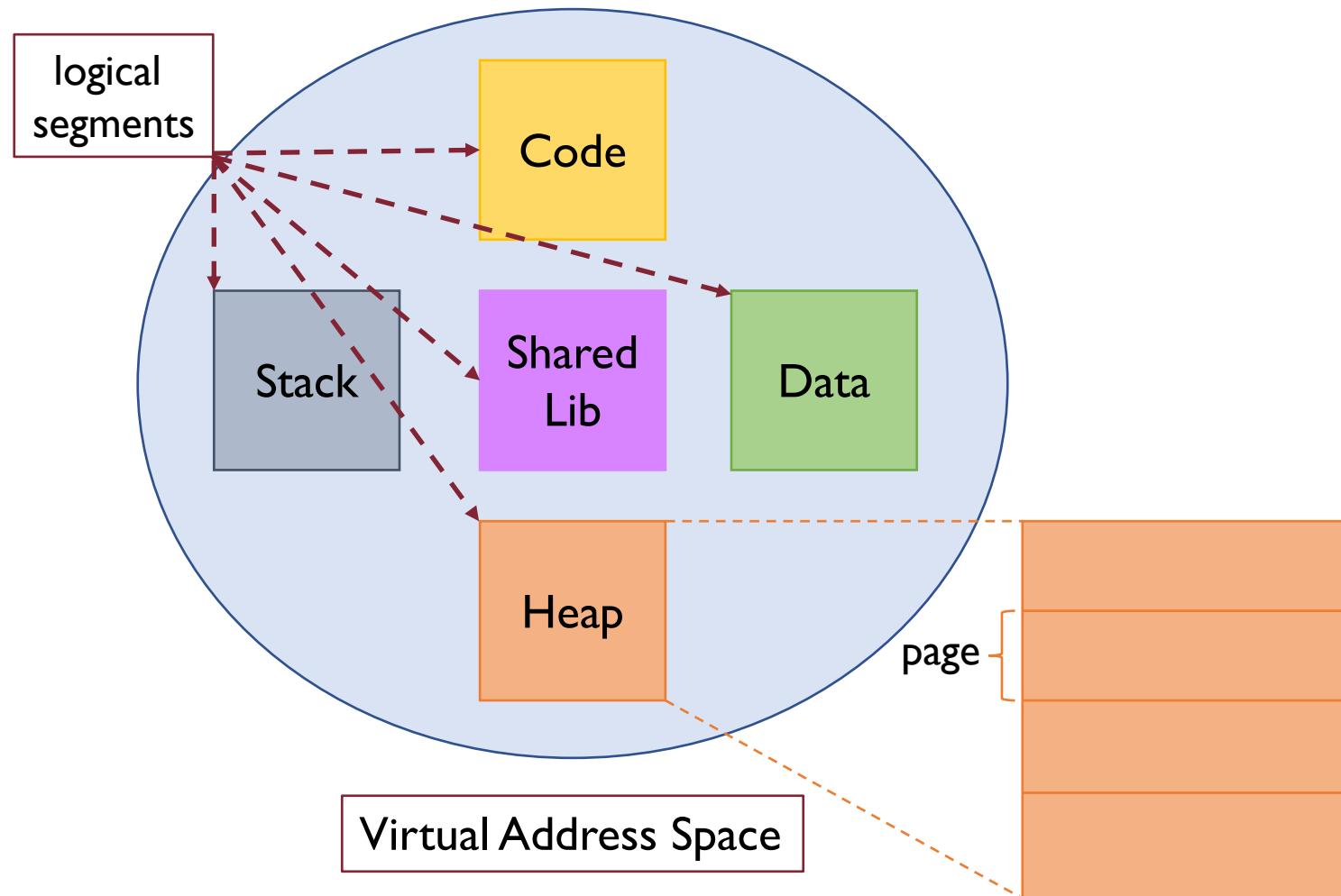
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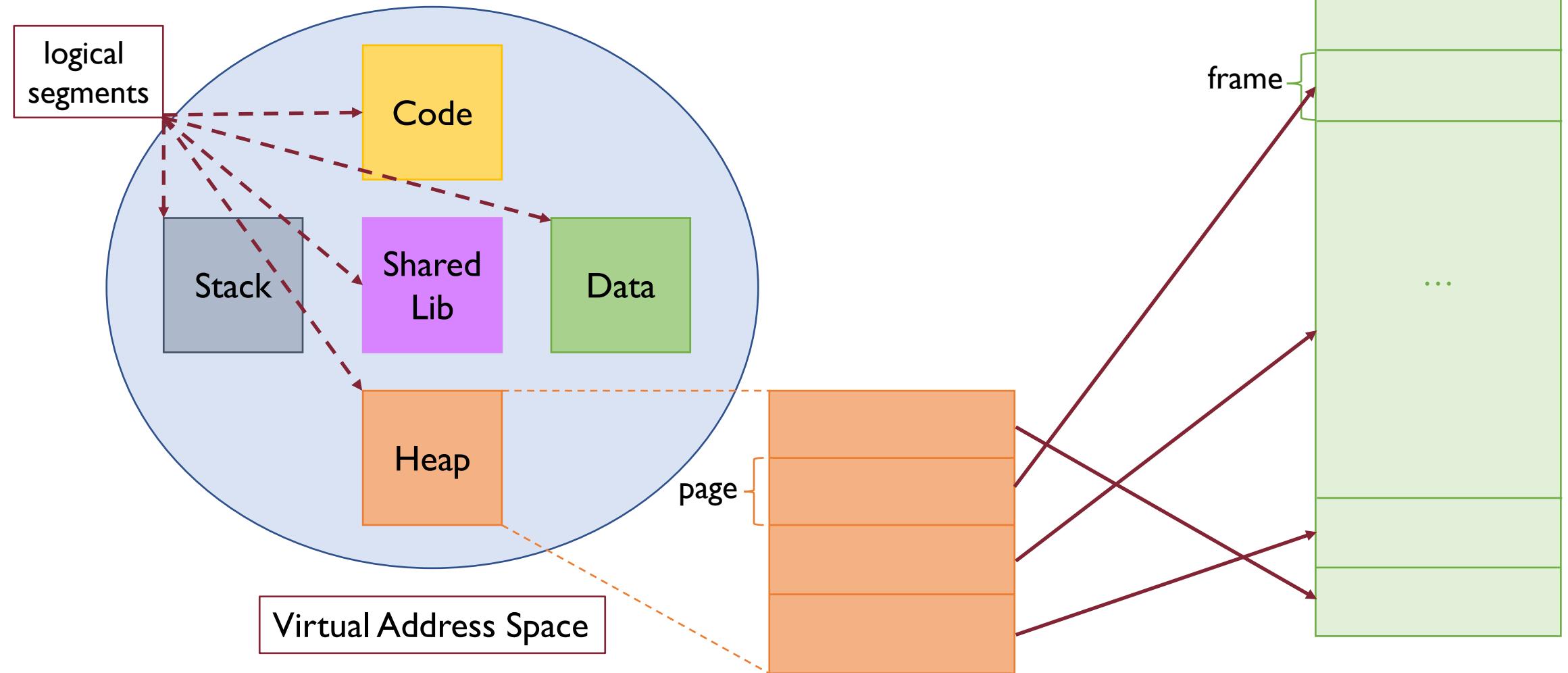
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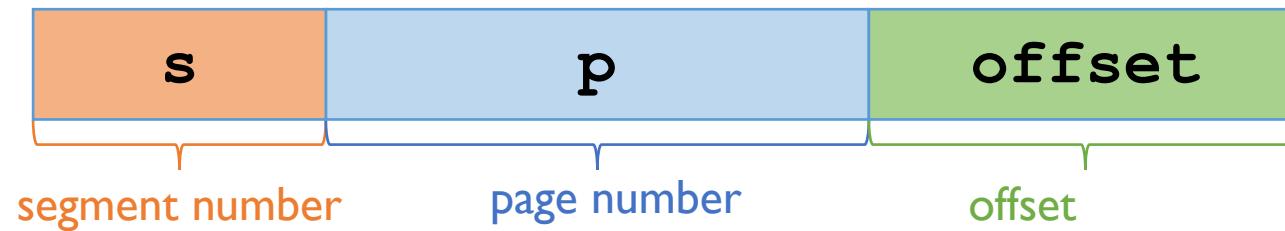


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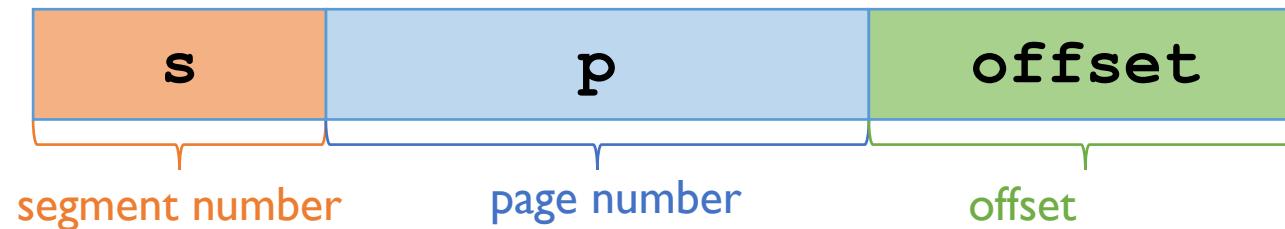
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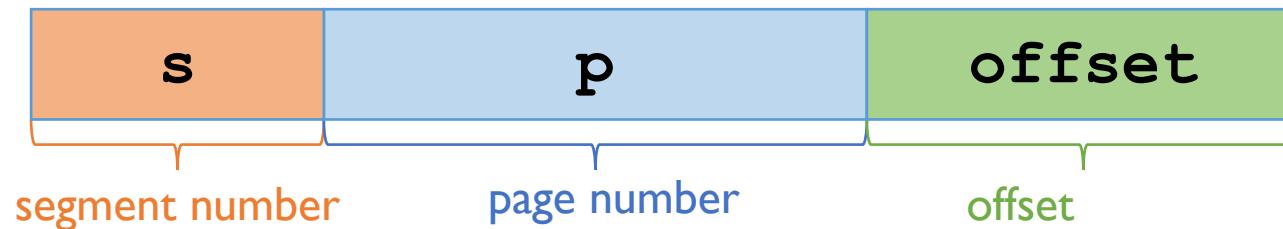
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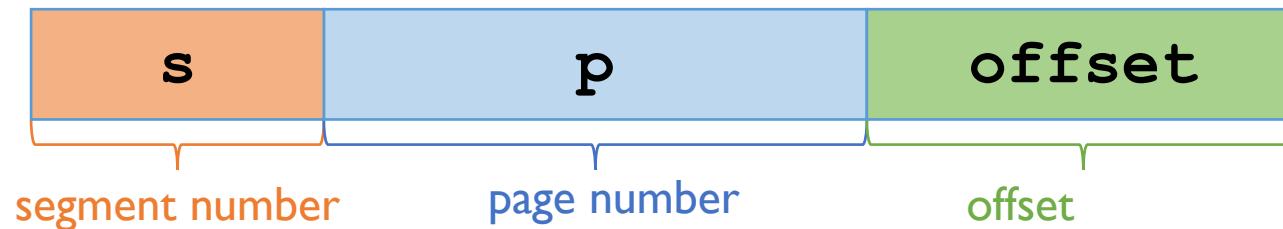
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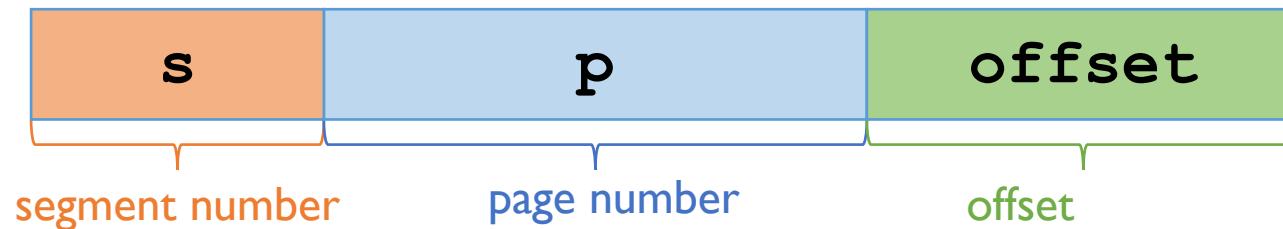
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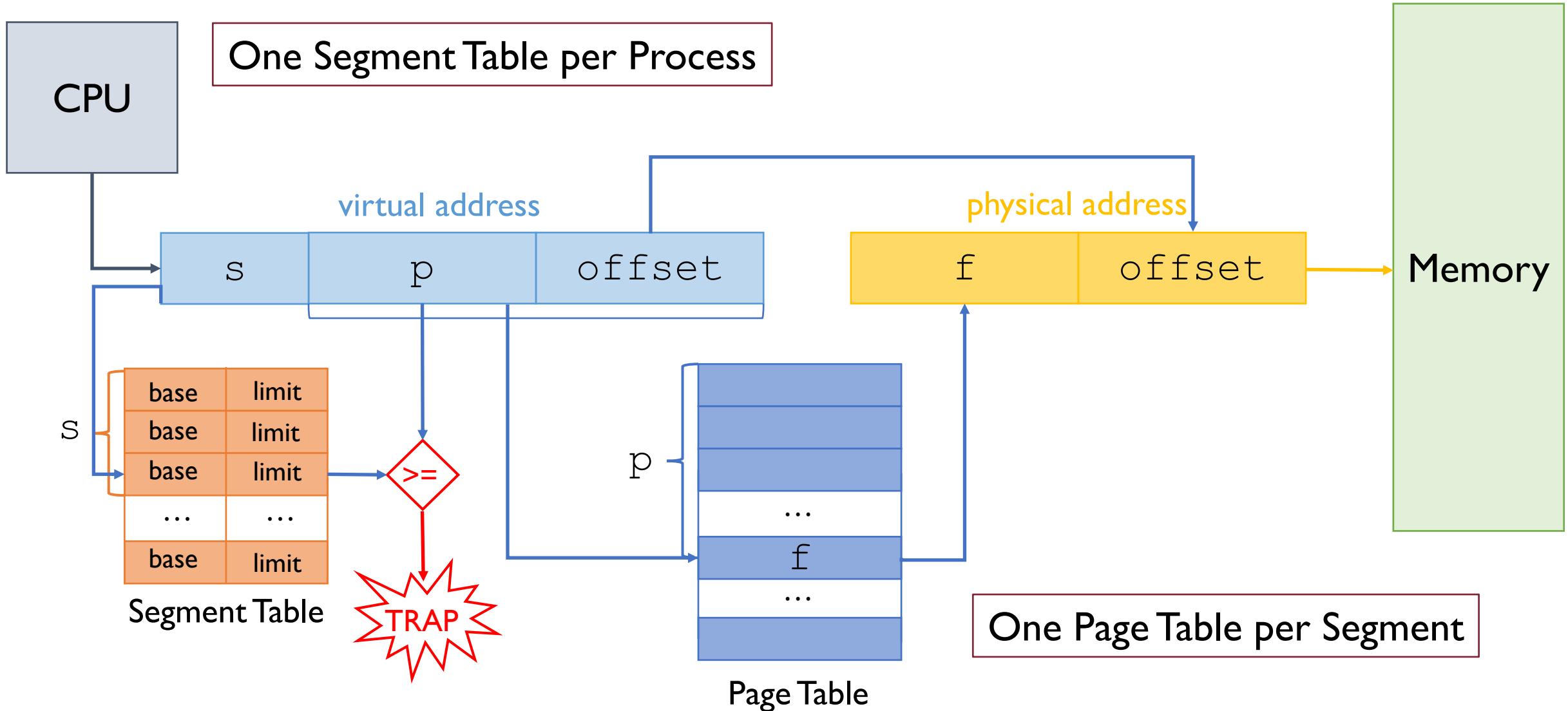
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Slower but more flexible

Segmented Paging Hardware: Practical Example 3

Suppose a physical memory of 1024 addressable words (assuming 1 word = 1 byte)

Frame size is 64 words (i.e., 64 bytes)

Page table size (i.e., number of entries) is thus $1024 \text{ bytes} / 64 \text{ bytes per frame} = 16$

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R2

3 bits to address 8 logical segments (s)

4 bits to address 16 entries of the page table

6 bits to address 64 individual words (i.e., bytes) within each page

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- Segments can also be shared by sharing segment table entries:
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 - Since there is one page table for each segment, we can share a segment by simply sharing the page table this points to
- Even more flexible!

Segmented Paging: Benefits and Costs

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- **Costs:**

- Slower context switches (why?)
- Slower address translation (why?)

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- On segmented paging, we can lose 0.5 page per process' segment
- The larger the page size the higher the chance of internal fragmentation

Advanced Paging

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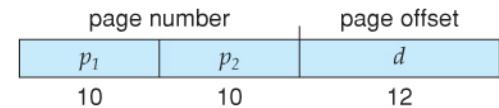
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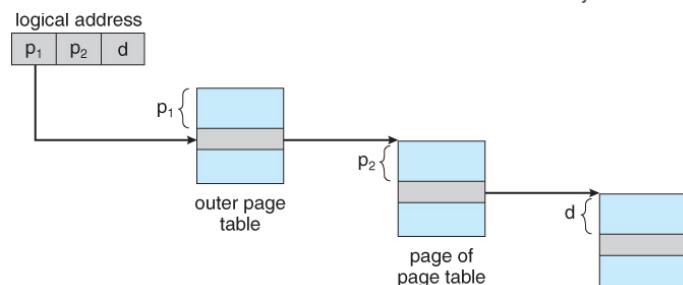
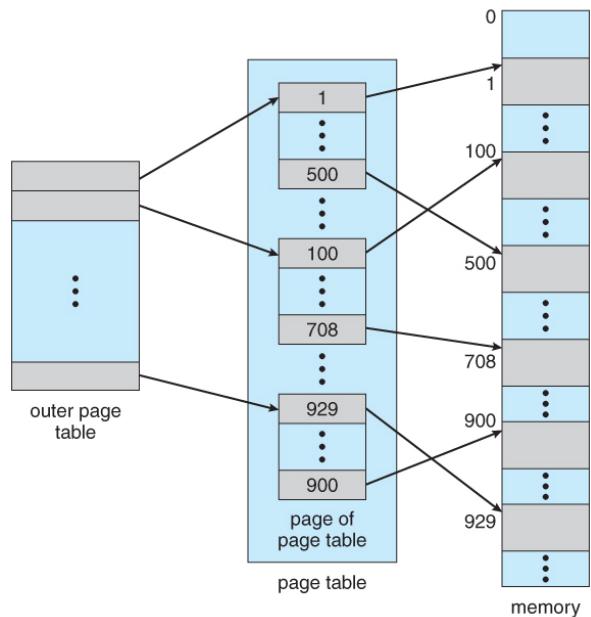


More advanced paging structures are needed!

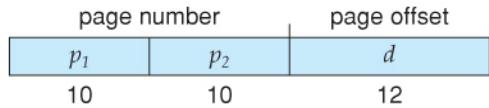
Advanced Paging: Two-Tier Page Table



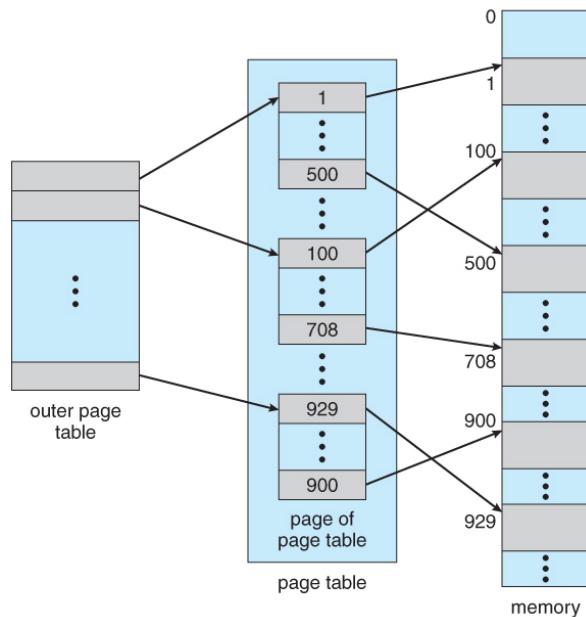
Let's page the page table!



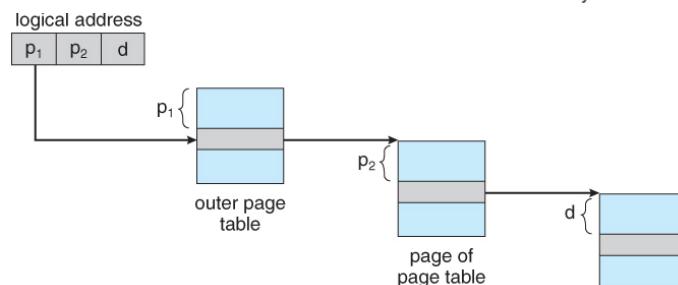
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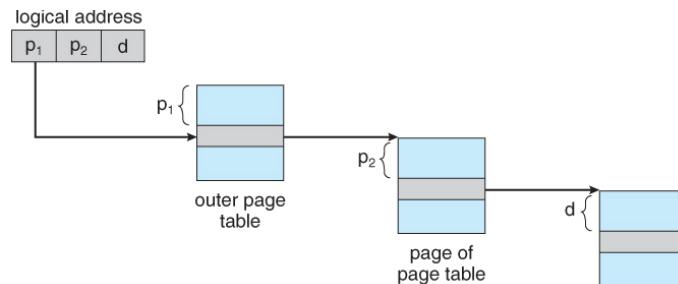
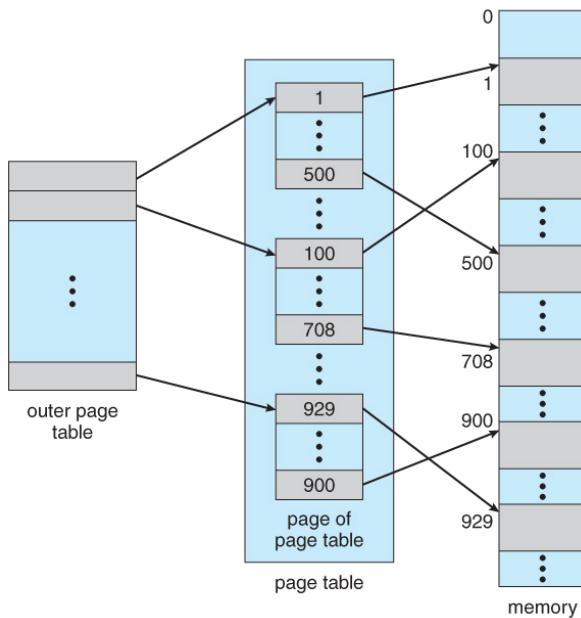
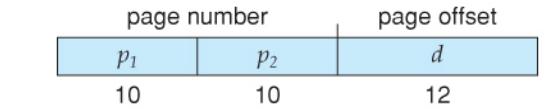
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20-bit page number broken into 2 10-bit page numbers



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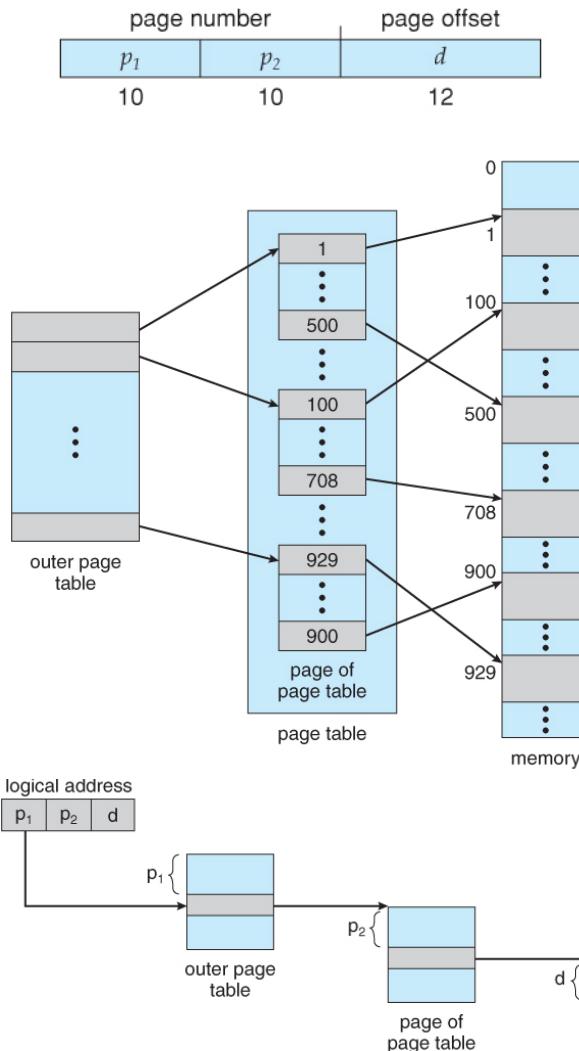


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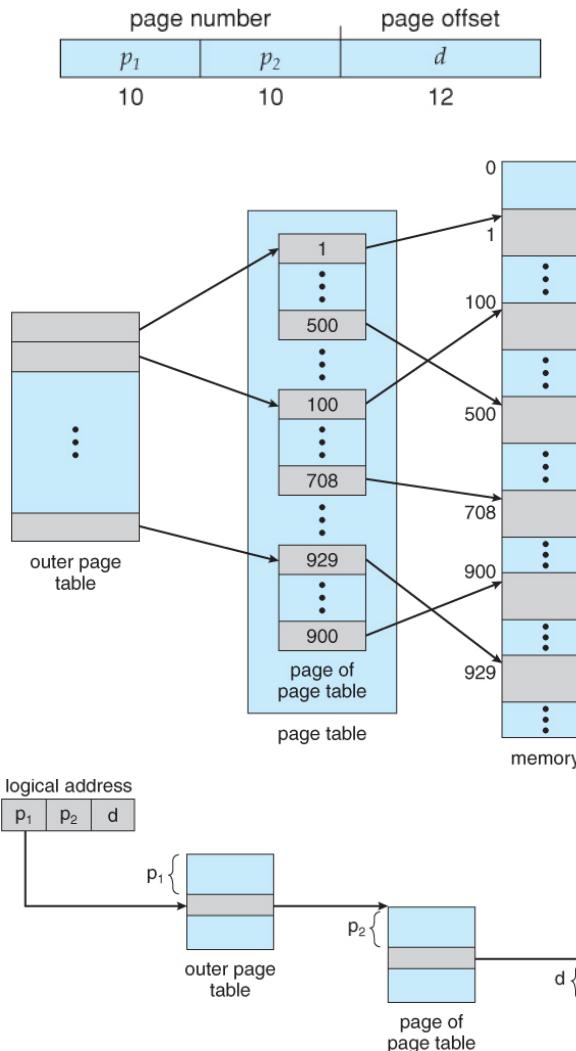
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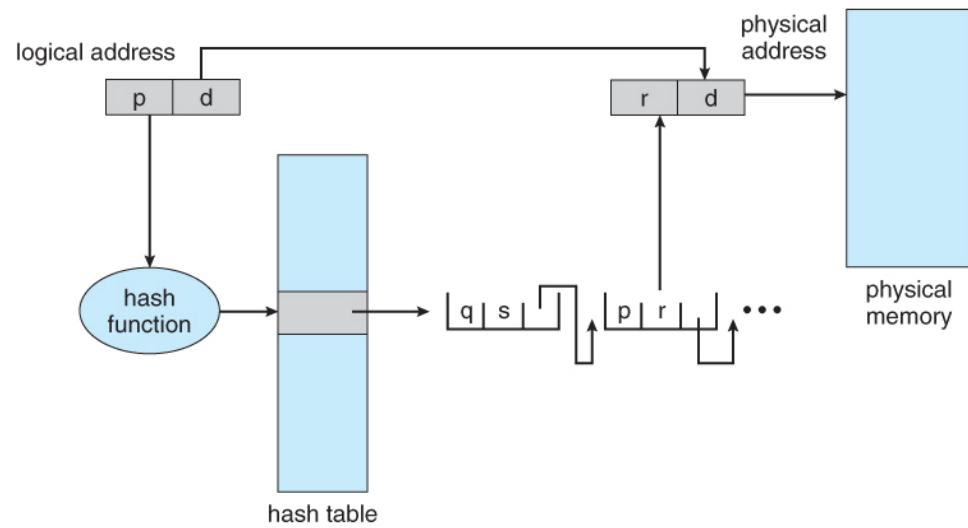
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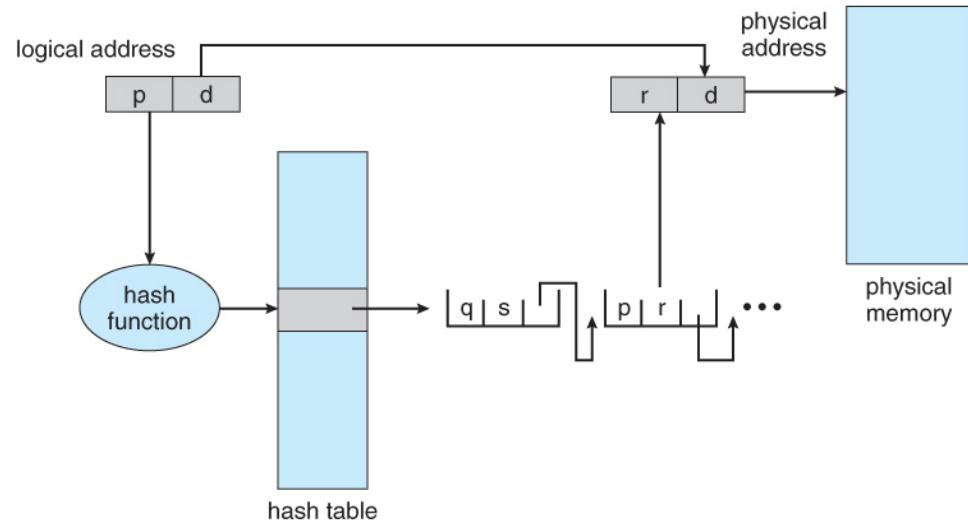
The remaining 12 bits of the 32-bit logical address are still the offset within the 4KiB frame

Advanced Paging: Hashed Page Table



Use **hash tables** to store highly sparse page tables

Advanced Paging: Hashed Page Table



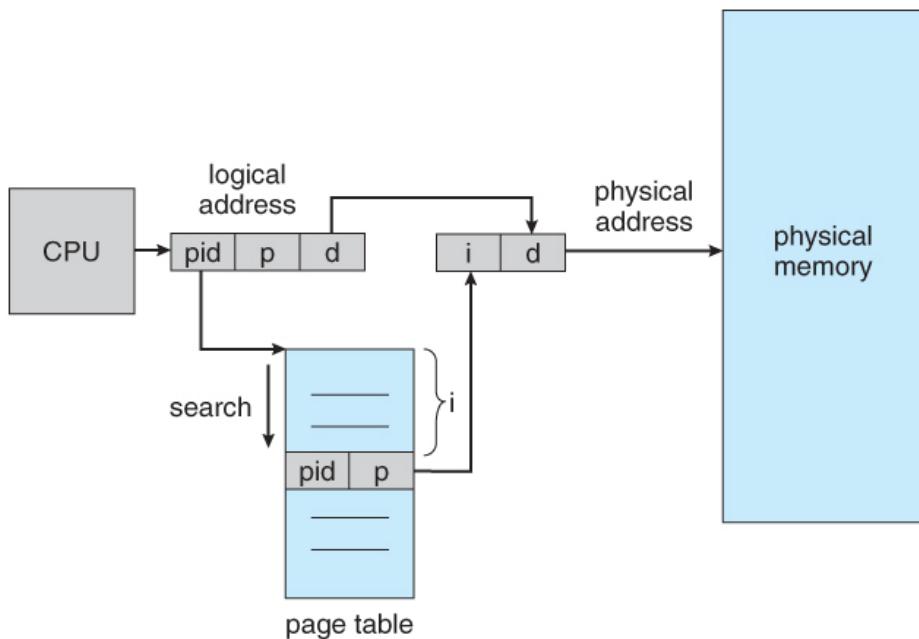
Use **hash tables** to store highly sparse page tables

Indexing via **hash function** rather than integers

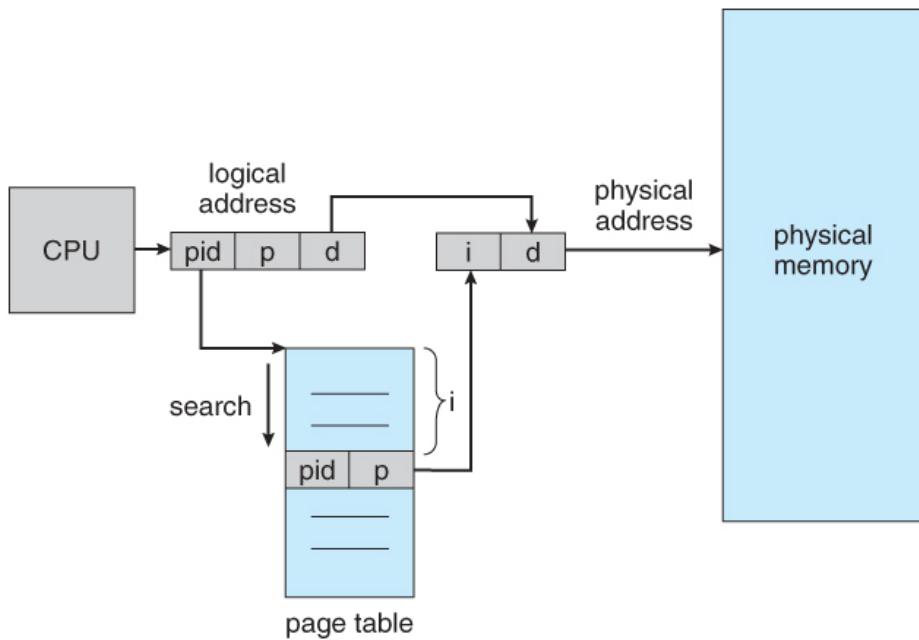
Advanced Paging: Inverted Page Table

An inverted page table lists all of the pages currently loaded in memory, for all processes

Instead of a table listing all of the pages for a particular process



Advanced Paging: Inverted Page Table



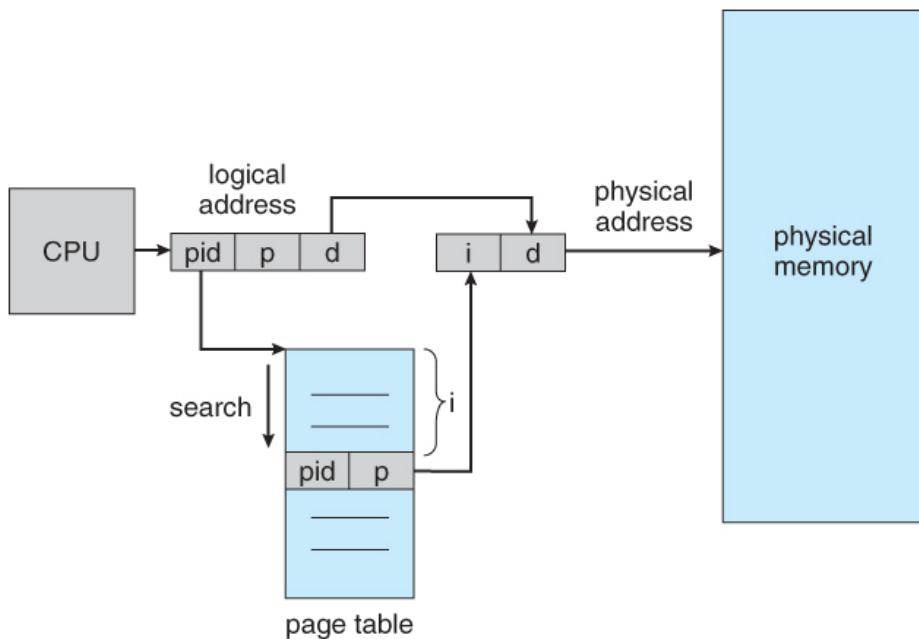
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Access to an inverted page table can be slow (linear search)

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Inverted page tables do not easily allow mapping multiple logical pages to a common physical frame (page sharing)

Each frame is mapped to exactly one process

Summary

- **Relocation** using base and limit registers
 - Simple yet inflexible

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- **Relocation** using base and limit registers
 - Simple yet inflexible
- **Segmentation**
 - Compiler's logical view of memory presented to the OS
 - Segment tables tend to be small enough to be stored in registers
 - Contiguous memory allocation is expensive and complicated (first-fit, best-fit, or worst-fit)
 - Compaction is needed to solve external fragmentation

Summary

- **Paging**
 - Simplifies memory allocation by relaxing contiguous assumption
 - Each logical page can be allocated to any physical frame
 - Page tables can be extremely large

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- **Segmentation + Paging**

- Only need to allocate as many page table entries as needed
- Sharing either at the segment or at the page level
- Might increase internal fragmentation over pure paging
- 2 lookups per memory reference are needed