Sistemi Operativi I

Corso di Laurea in Informatica

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SAPIENZA
UNIVERSITÀ DI ROMA

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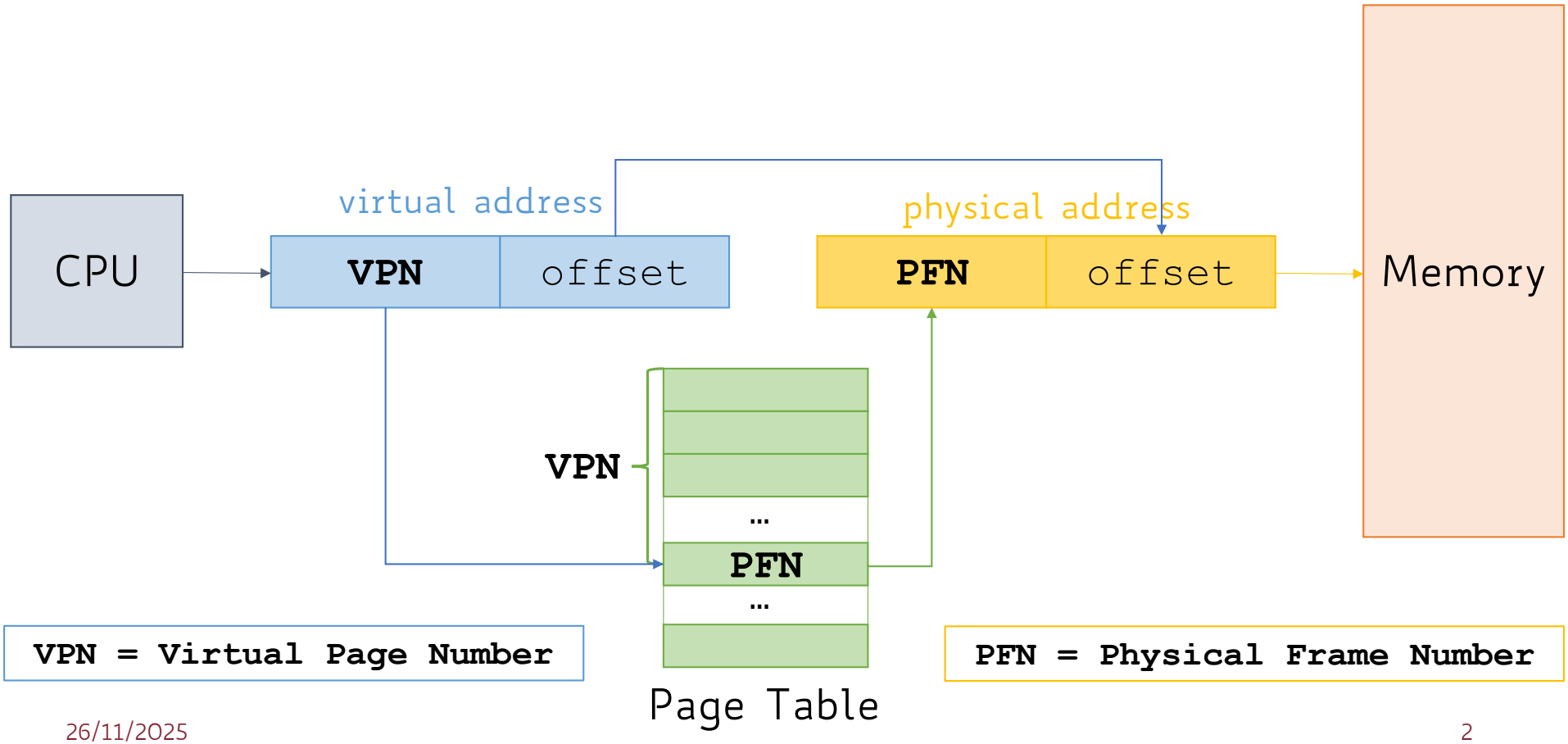
One-Slide Paging



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- To do so, the MMU must access the page table

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  - **Main Memory** → PRO: highest capacity CON: quite slow (every memory translation requires one extra memory access!)
  - **Trade-off** → Keep page tables in main memory and cache a subset of them into a **Translation Look-aside Buffer** (TLB)

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- Access individual memory locations one at a time from the cache rather than from memory directly

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- Typical TLB sizes range from 8 to 2048 entries

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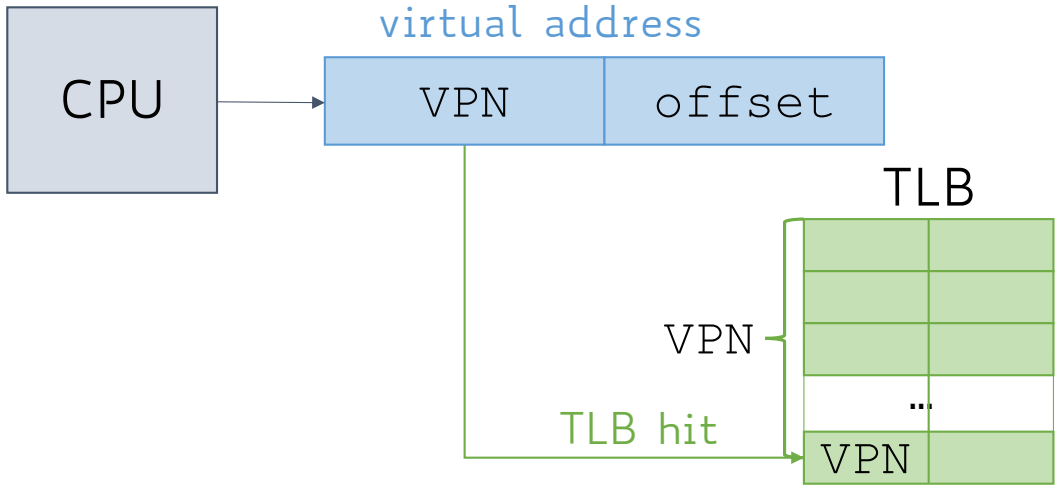

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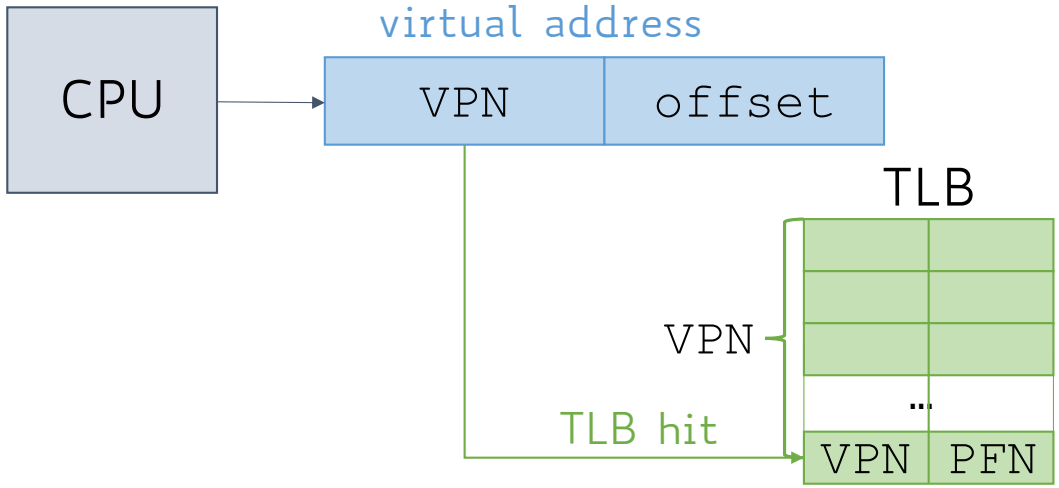

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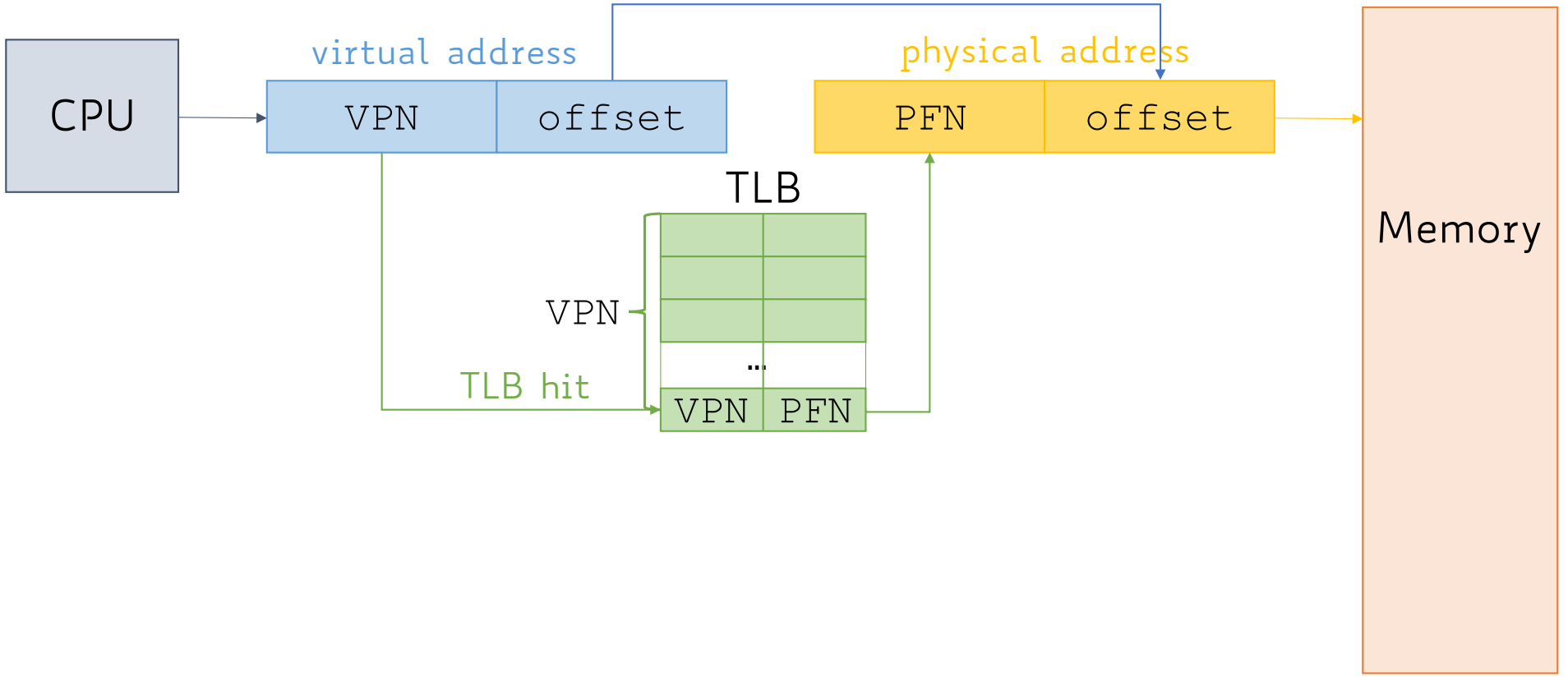

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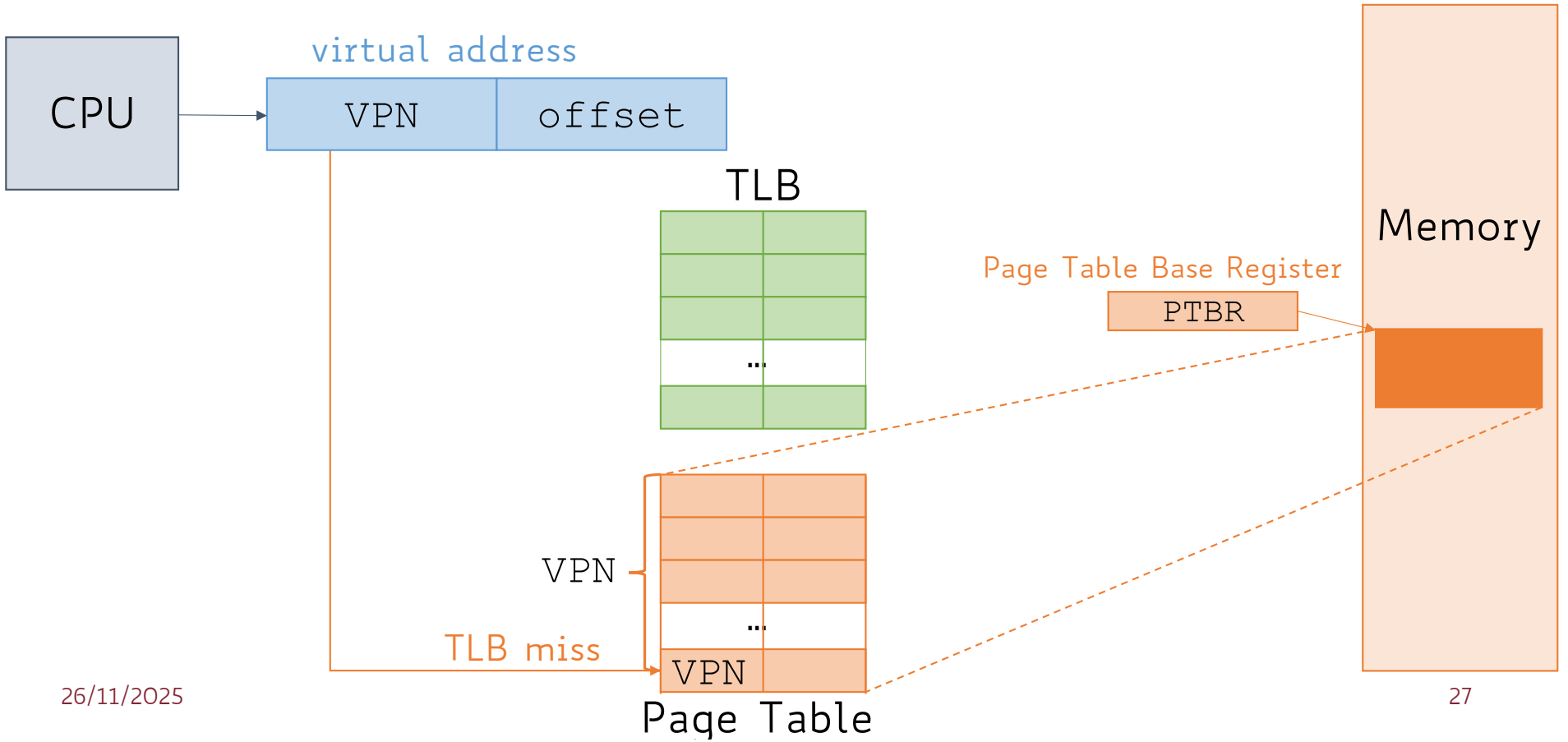

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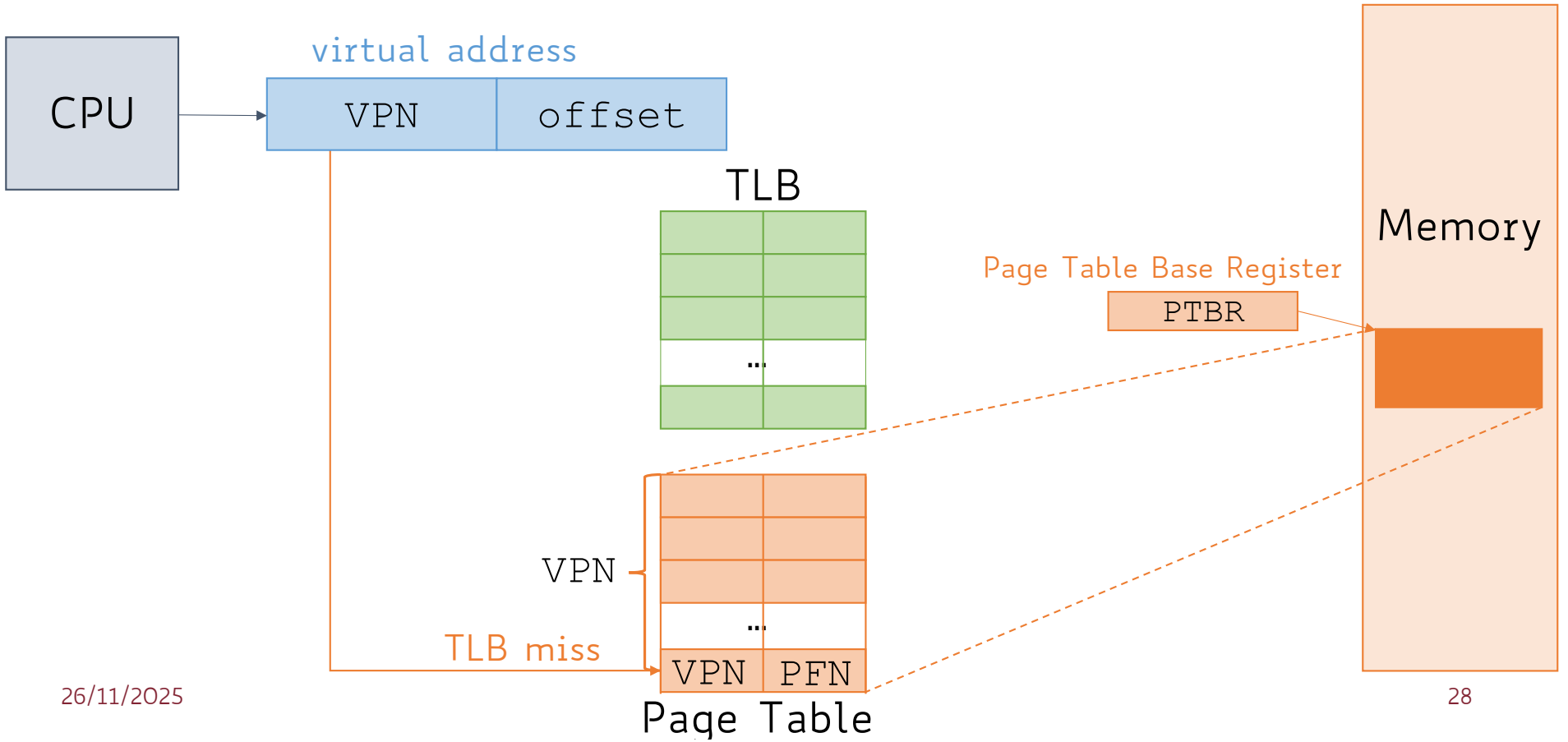

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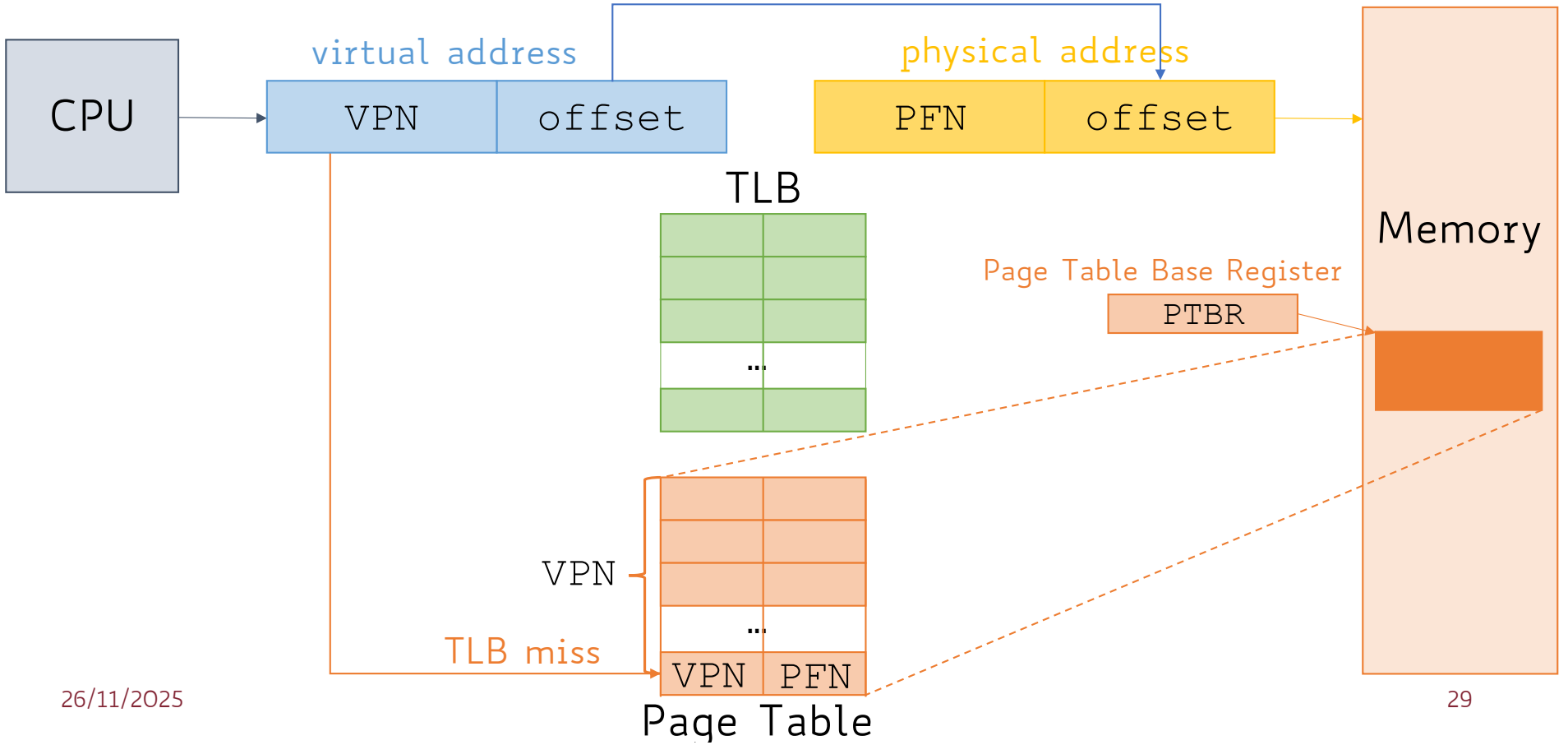

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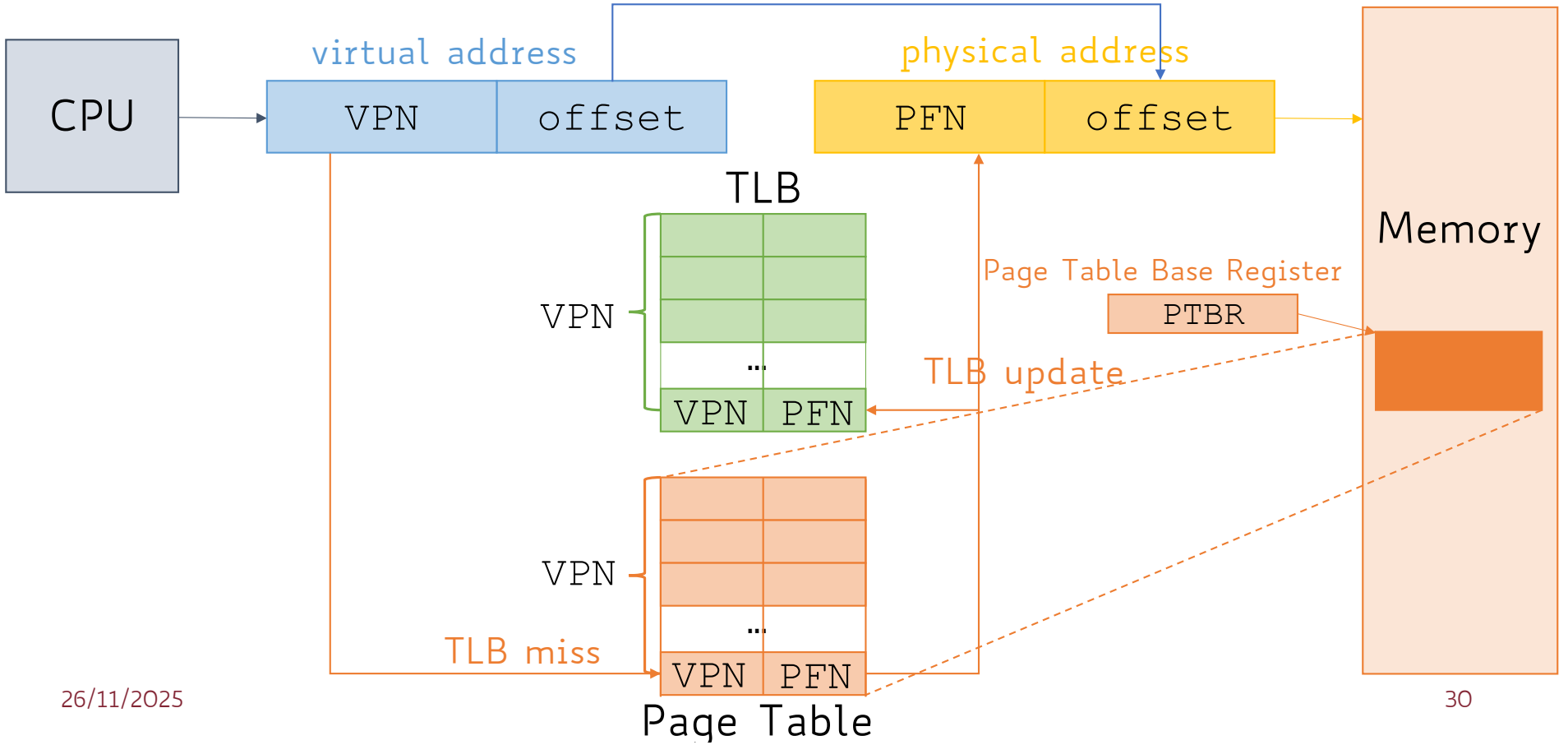

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- **2 setups:**
  - **basic:** at each context switch the content of the TLB is fully flushed and cleaned (cold-start → the first accesses will generate all TLB misses)
  - **advanced:** TLB entries dumped and restored within the PCB or adding a so-called process context ID (PCID) to each entry (the CPU will use a TLB entry iff the PCID of that entry corresponds to the ID of the running process)

Memory Access Cost

t_{MA} = physical memory access time
t_{TLB} = lookup time on the TLB cache
(NOTE: $t_{TLB} \ll t_{MA}$)
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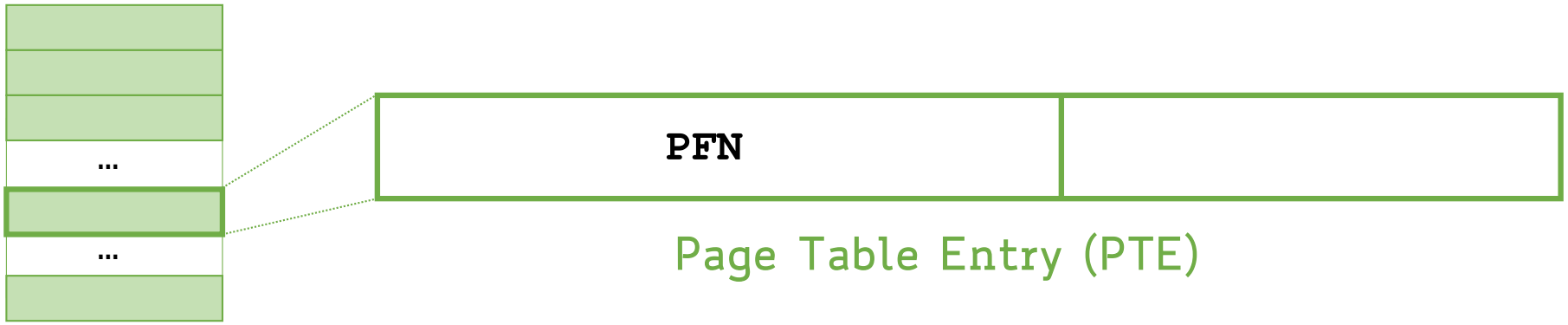
The larger the TLB the higher the probability p of hit ratio, thereby decreasing the average memory access cost

What's Inside the Page Table?



At least, the mapping to the Physical Frame Number (PFN)…

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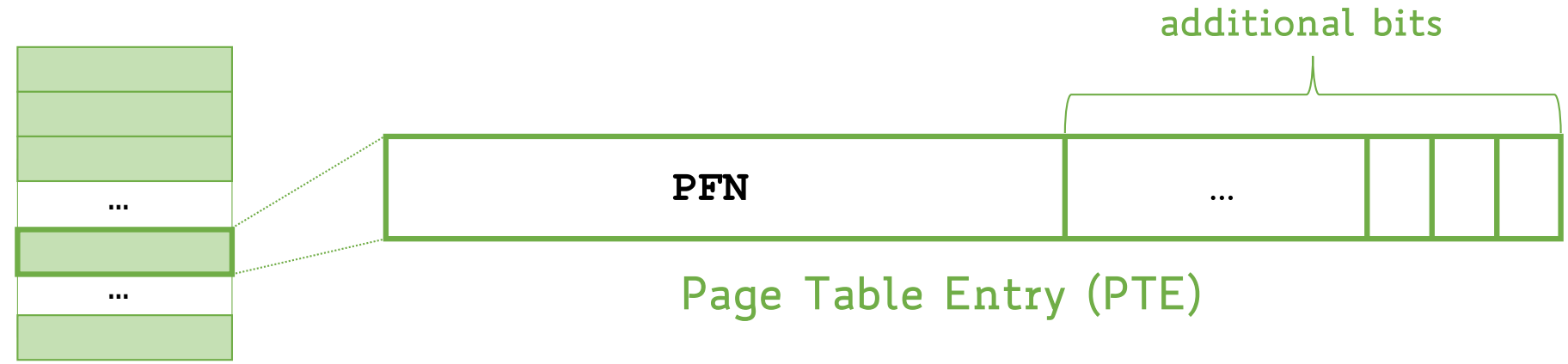


valid/invalid bit → check if the translation is legitimate

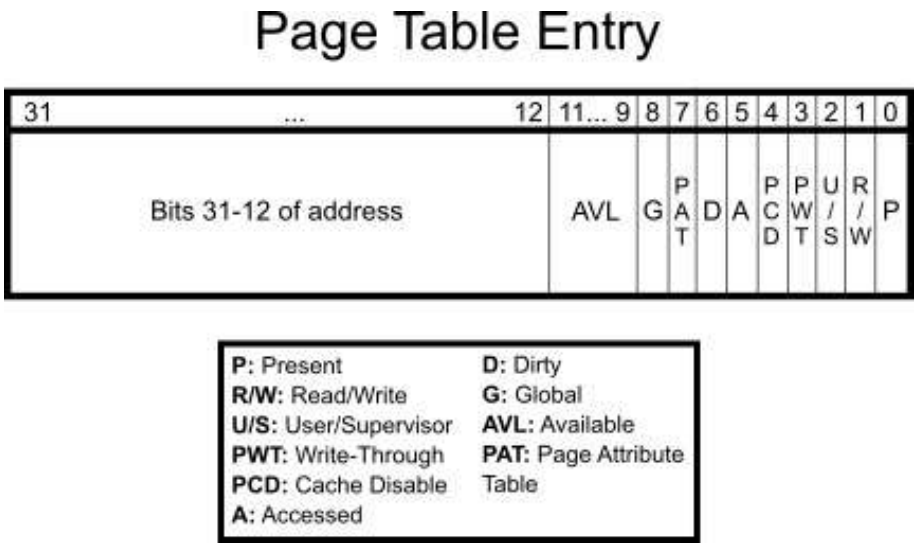
protection bits → read (R), write (W), execute (X)

present bit → the page is in RAM or swapped out to disk

reference bit → the page has been accessed (recently)

...

32-bit x86 PTE



source: https://wiki.osdev.org/Paging

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- Valid/invalid bits can be added to "mask off" entries in the page table that are not in use by the current process

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- Some systems use a page-table length register (PTLR) to specify the length of the page table

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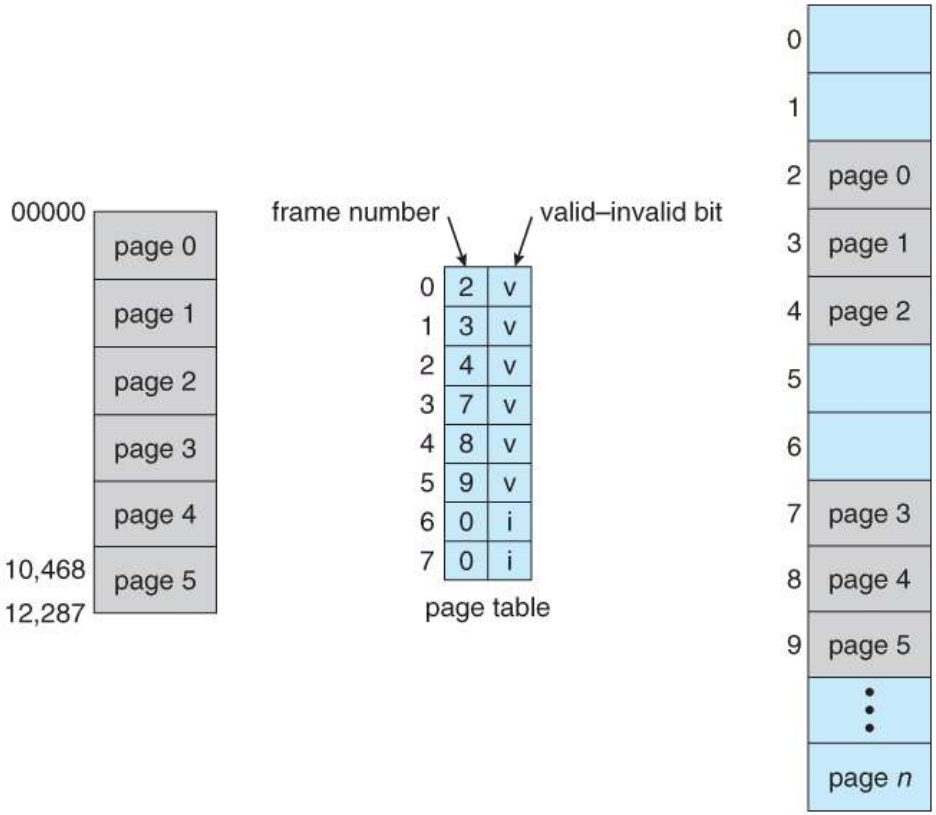

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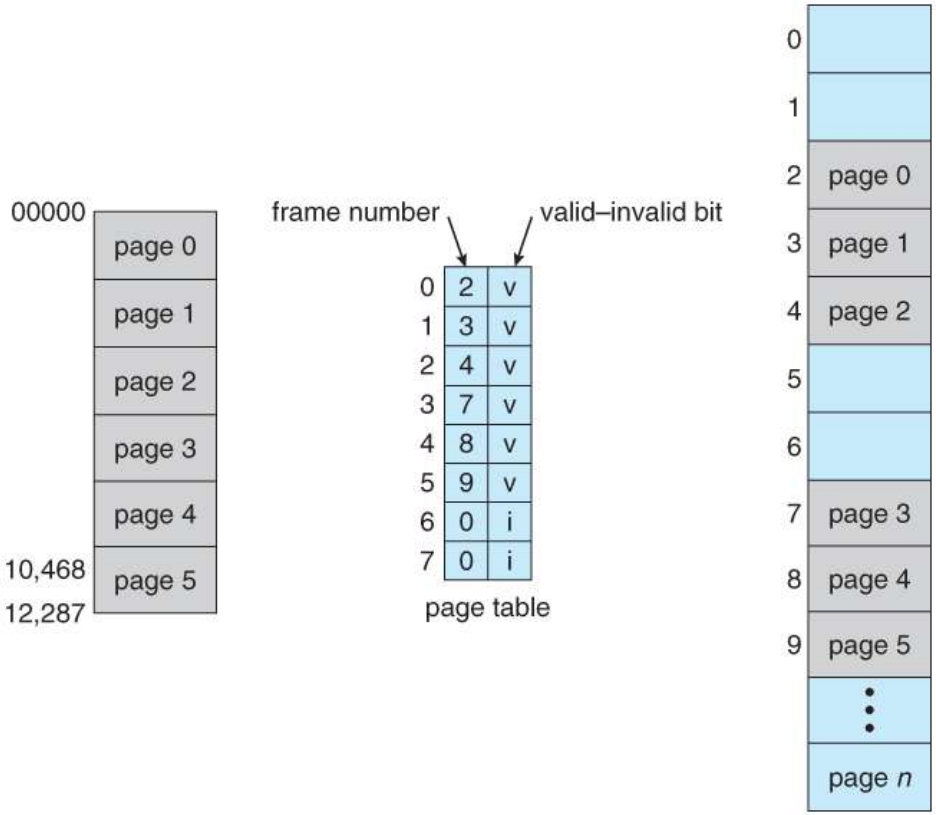

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any entry whose invalid bit is set will be discarded (and updated)

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- On a context switch:
  - Copy the `PTBR` value to the PCB
  - Copy the TLB to the PCB (optional)
  - Flush the TLB (if TLB is not saved to/restored from the PCB)
  - Restore the `PTBR` (i.e., with the value of the new running process)
  - Restore the TLB (if it was previously saved)

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- Just duplicate page entries of different processes to the same page frames (both for code and data)

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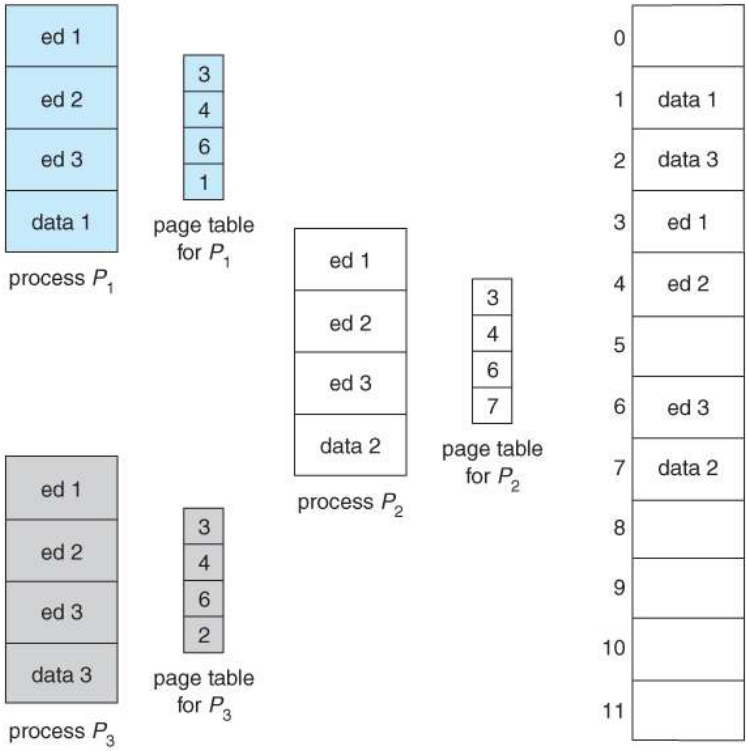
- The code can be shared by multiple processes, as long as each has their own copy of the data and registers, including the instruction register

Sharing Pages: Example



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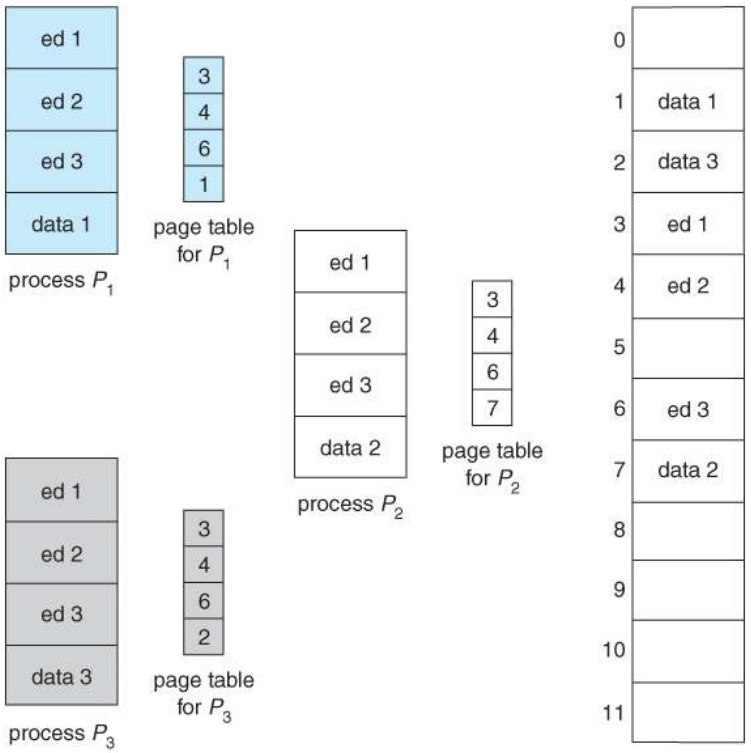

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Only a single copy of the code of `ed` is actually loaded in main memory

Paging: PROs

- A big improvement over **relocation**
- Eliminates the problem of external fragmentation and therefore the need for compaction
- Allows code sharing among processes, reducing memory footprint
- Enables processes to run when they are partially loaded (more on this later…)

Paging: CONs

- Virtual/Physical address translation may be time consuming
- Hardware support like TLB cache is needed to make it fast enough
- OS has to be inevitably more complex
- Simple linear page stored in (kernel) memory can be prohibitive for large and highly sparse VAS systems

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Plus, most of such space would be wasted as the process' VAS is sparse and only a fraction of its pages should be mapped to RAM

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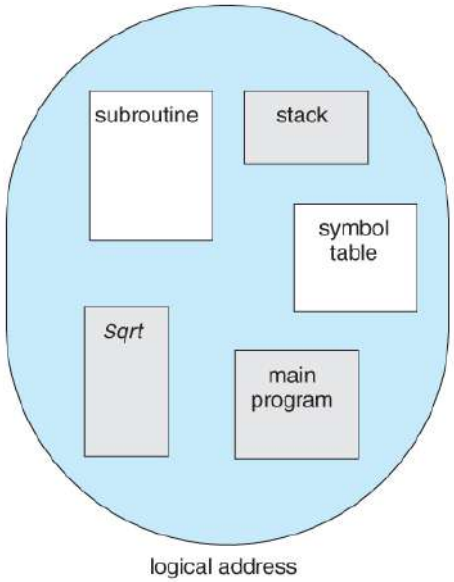
- Rather they think of memory divided in multiple **segments**, each dedicated to a specific use, such as code, data, stack, heap, etc.
- Memory segmentation supports this view by providing addresses with a **segment number** (mapped to a segment base address) and an **offset**

Segmentation: Example

A C compiler generating 5 segments for the user code, library code, global (static) variables, the stack, and the heap



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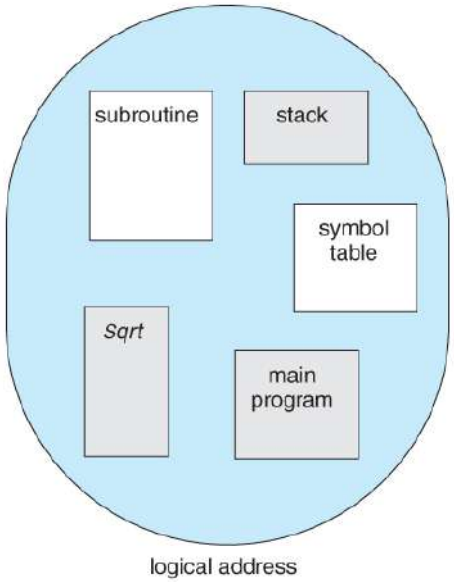
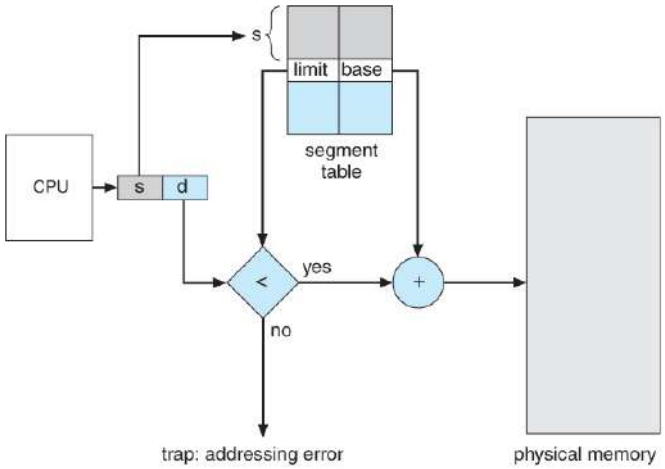


The compiler generates addresses identifying segments and offset

Segmentation Hardware

A segment table maps segment-offset addresses to physical addresses, and simultaneously checks for invalid addresses, using a system similar to the page tables and relocation base registers discussed previously



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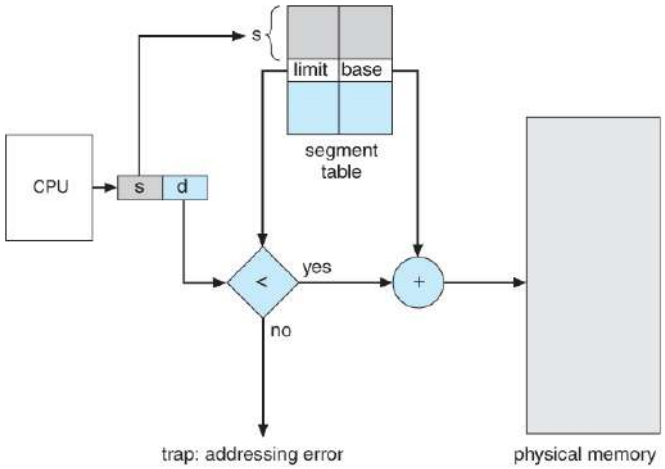
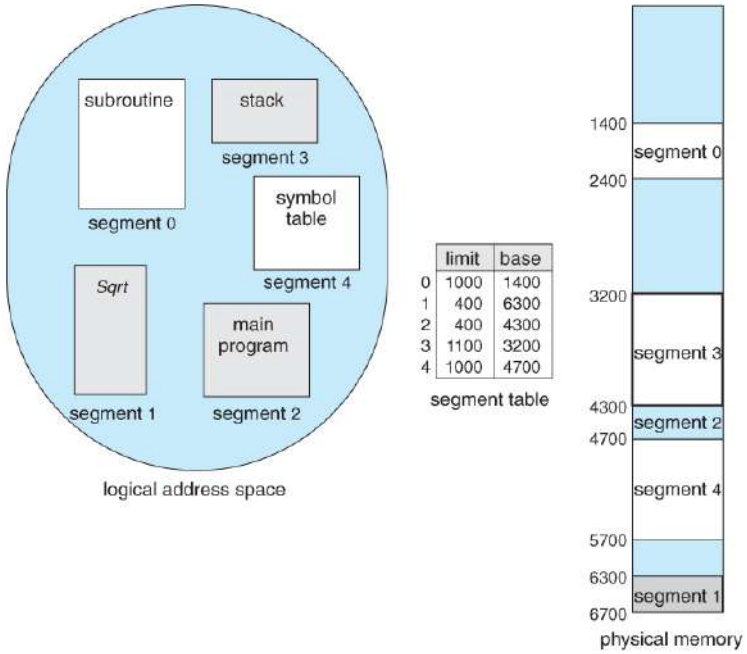


Note that we came back to the assumption that each segment is kept in contiguous memory and may be of different size…

Segment Table

Each entry contains a base address in memory, the length of the segment, plus additional protection information (e.g., sharing, read/write permissions)



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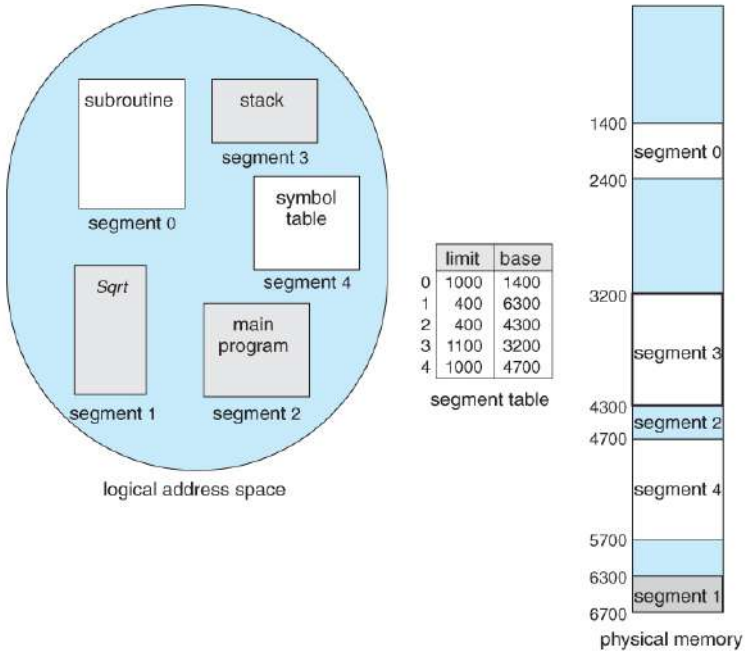

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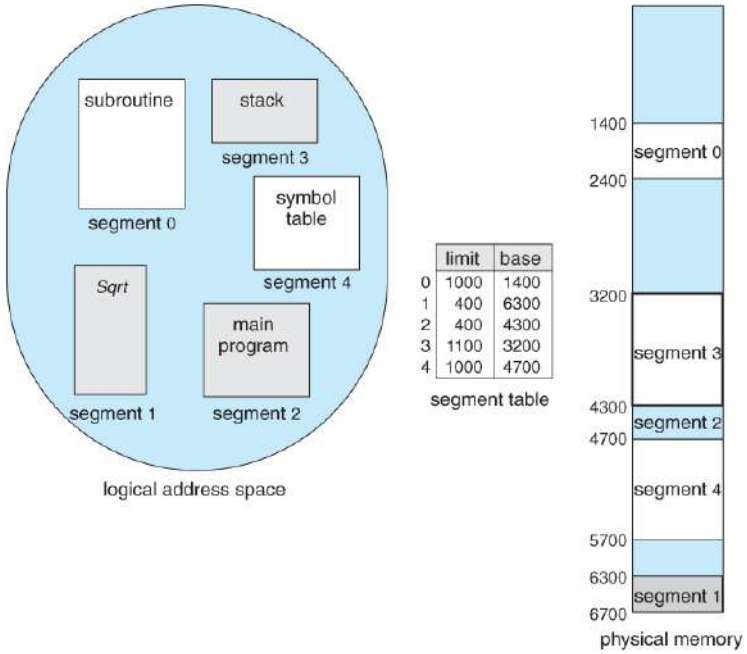

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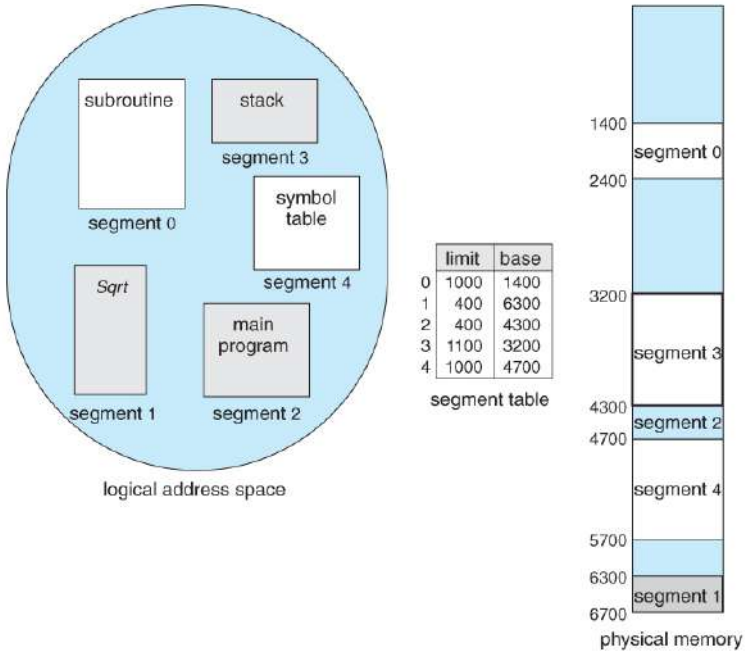

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Page Table cannot be stored using hw registers as there might be potentially too many page entries

Segment Table, instead, must store a very limited amount of segments per process (3÷5)

Implementing (Basic) Segmentation

- Compiler generates virtual addresses whose top-most significant bits indicate the segment number

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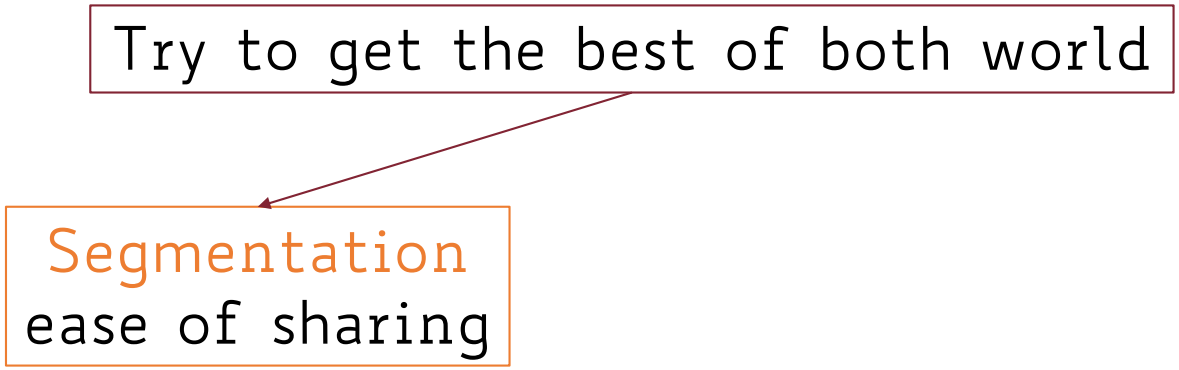
- Additional HW (like TLB cache) might be needed if programs use many logical segments

Combine Segmentation with Paging

Try to get the best of both world

Combine Segmentation with Paging



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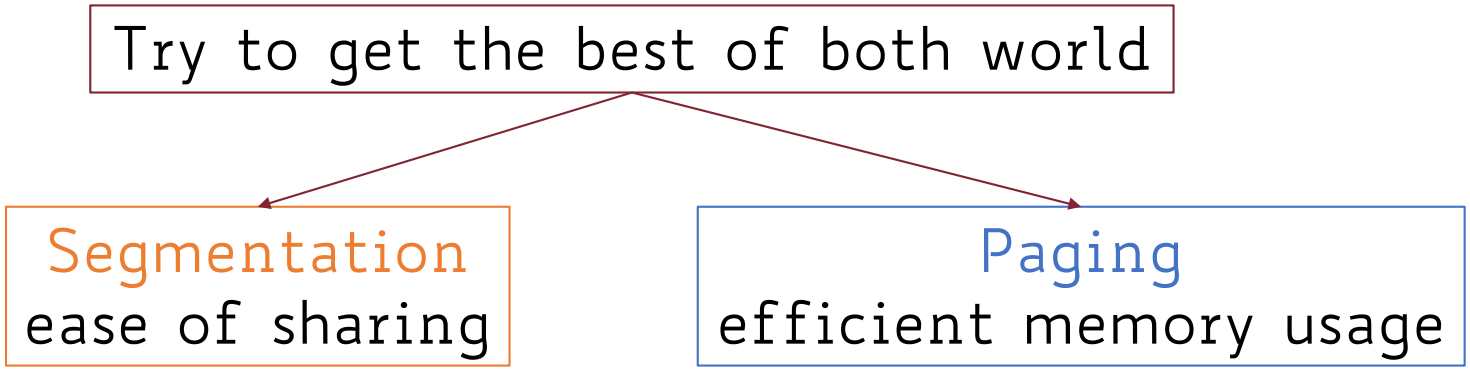

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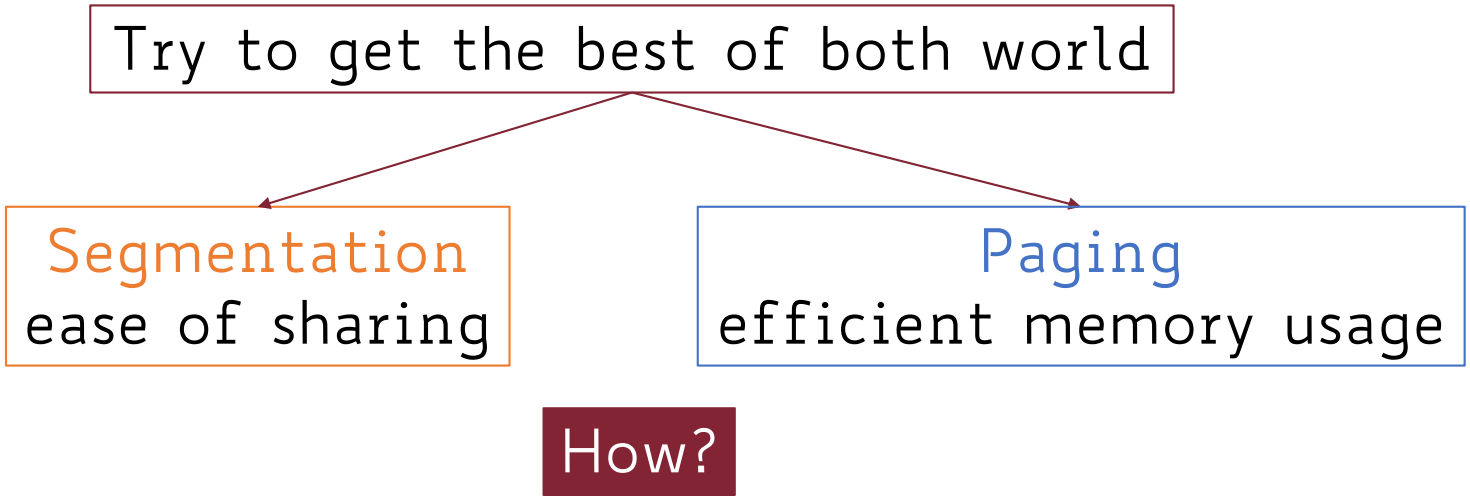

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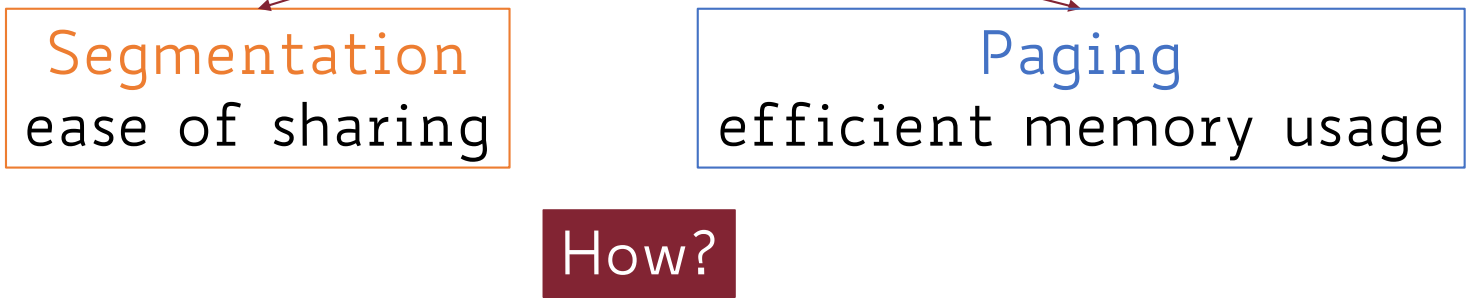

How?

Apply paging to segments!

Combine Segmentation with Paging

- Each process' virtual address space is seen as a collection of segments (i.e., logical units of arbitrary size)

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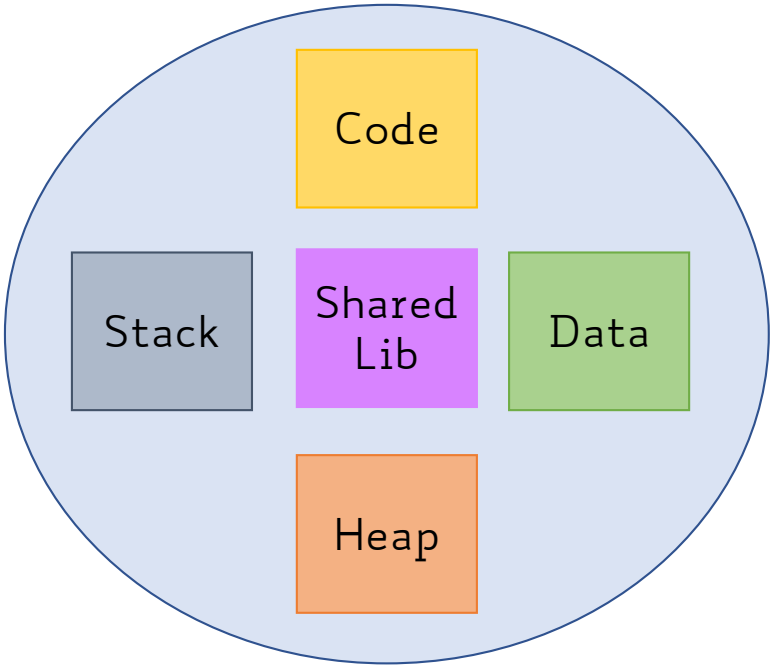
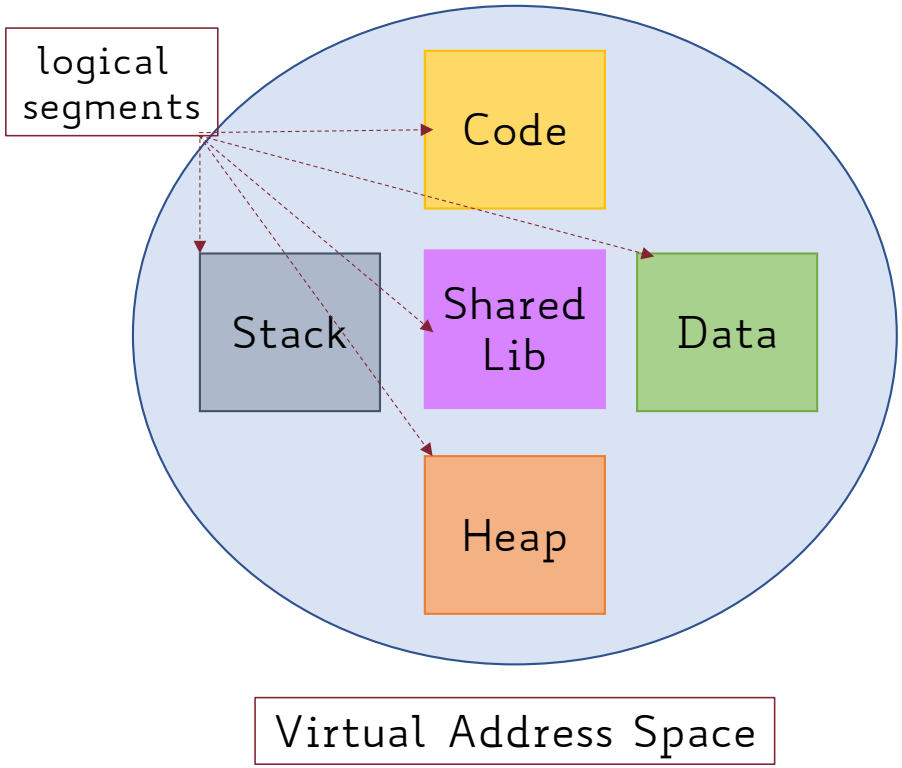
Map a logical segment onto multiple page frames

Paging Logical Segments



Virtual Address Space

Paging Logical Segments



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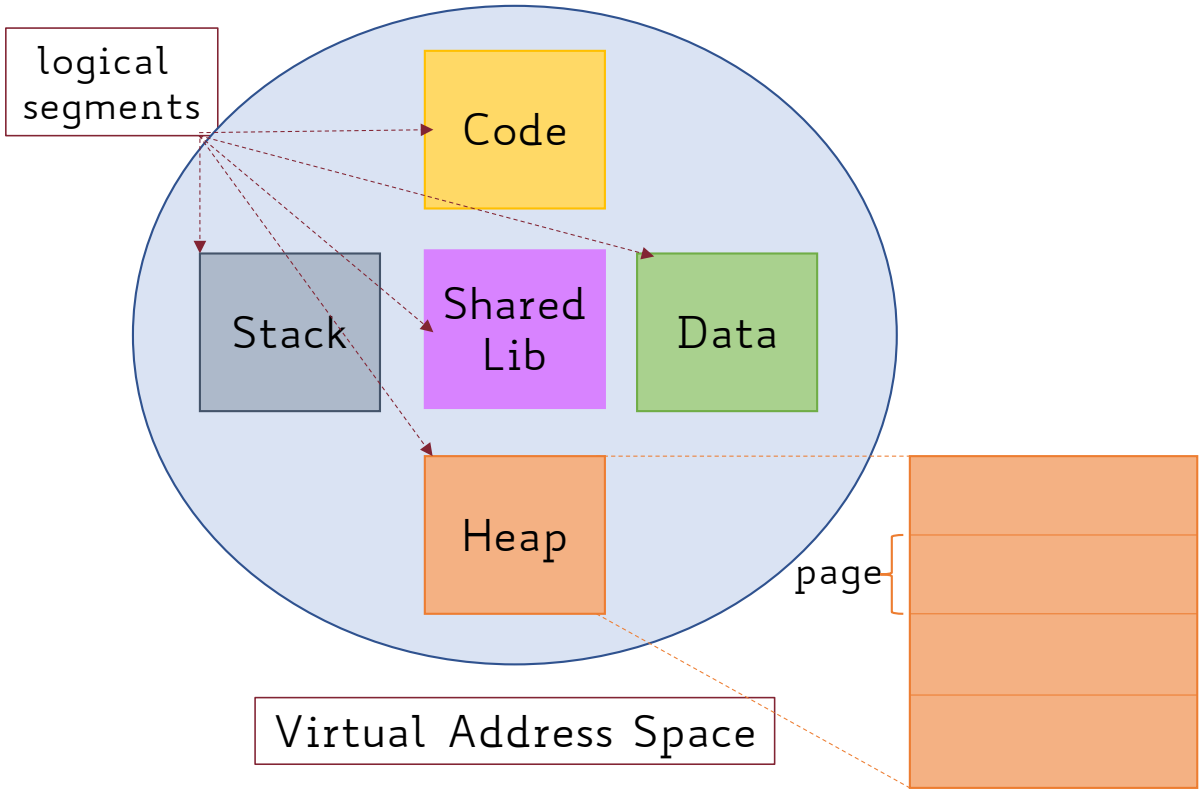

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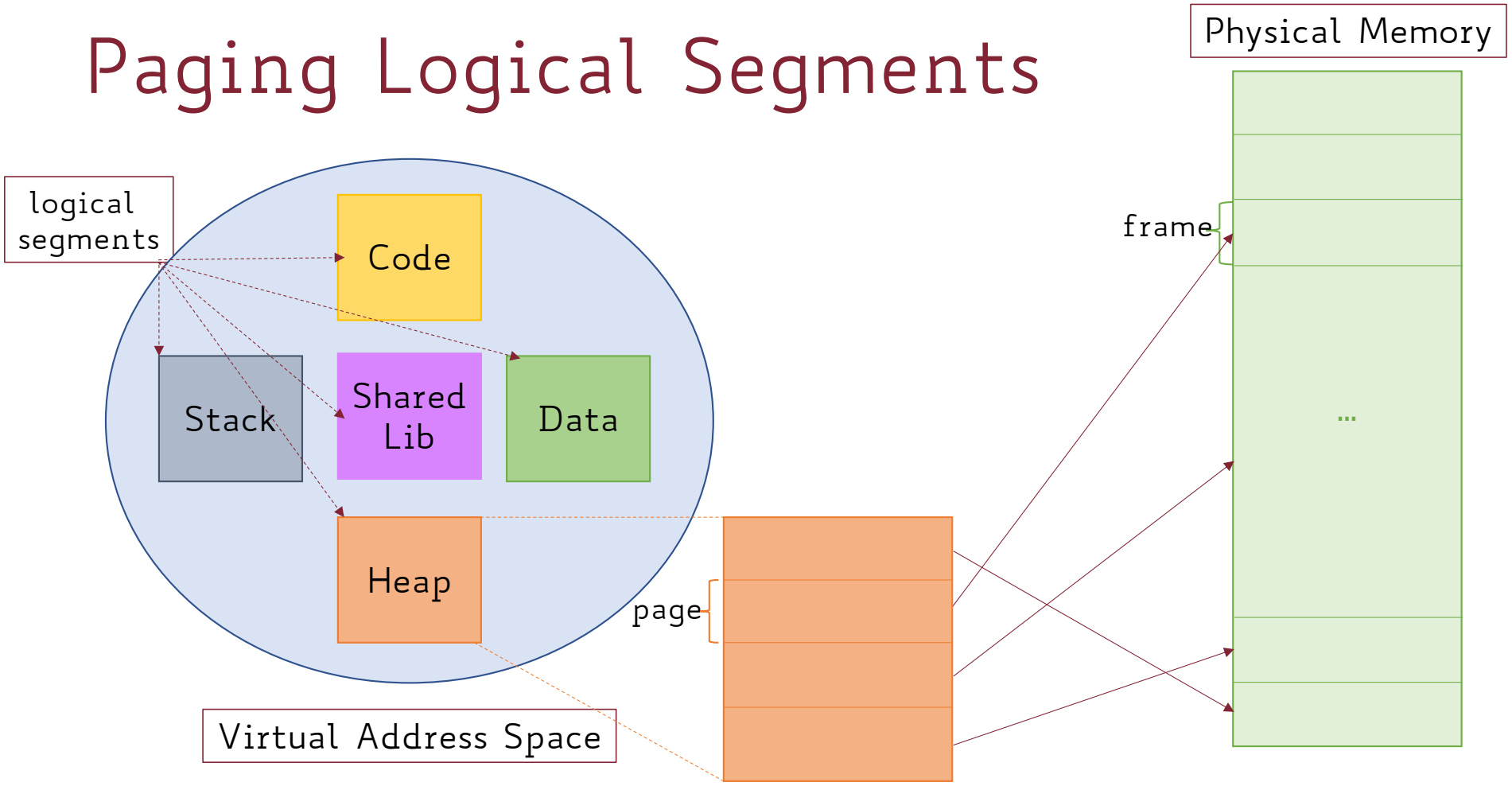
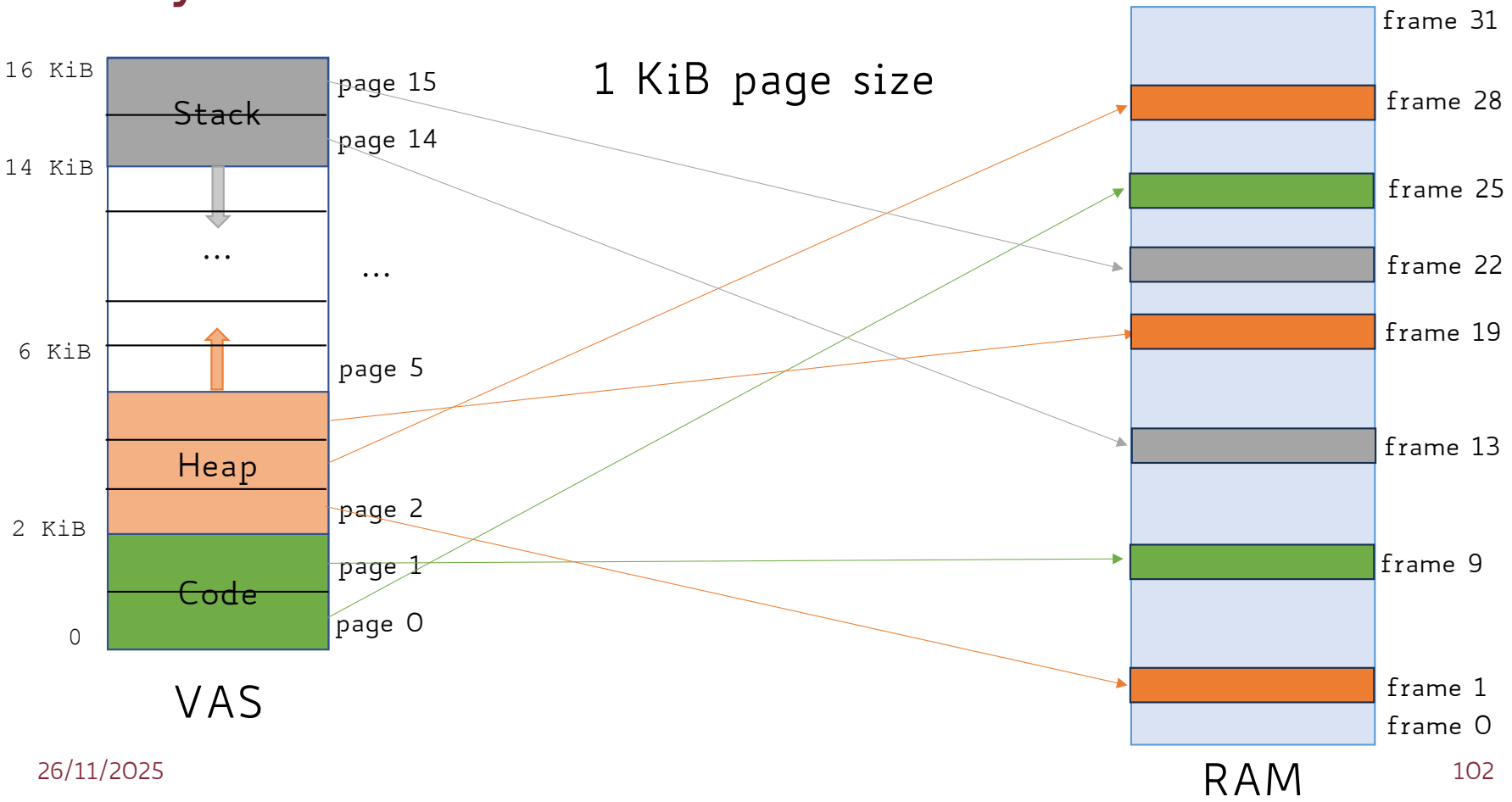


Why Does This Make PT Smaller?



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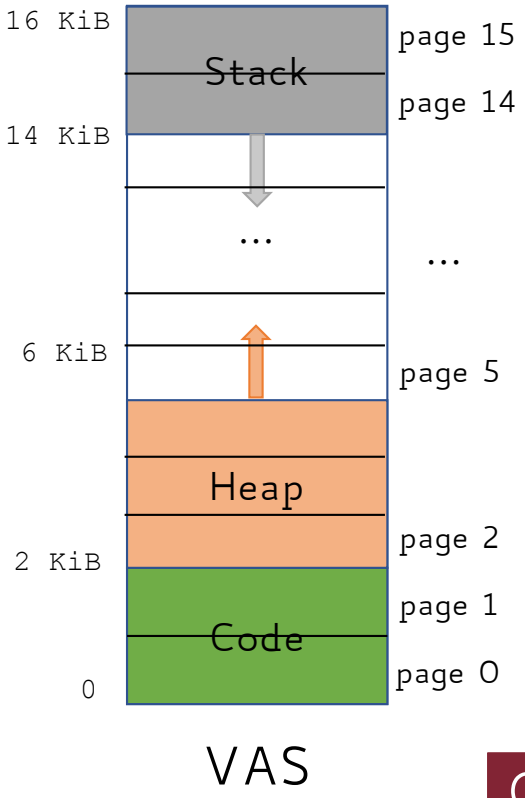
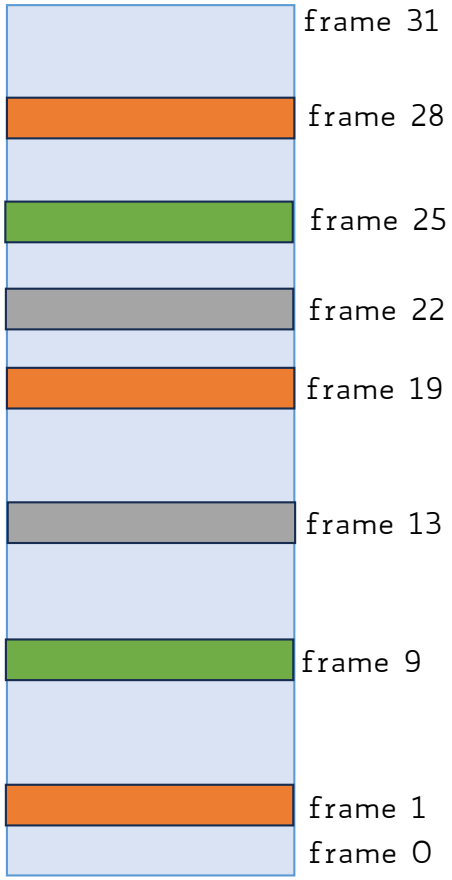


VAS

	PFN	valid	prot.	pres.
0	25	1	r-x	1
1	9	1	r-x	1
2	1	1	rw-	1
3	28	1	rw-	1
4	19	1	rw-	1
5	-	0	-	-
6	-	0	-	-
...				
13	-	0	-	-
14	13	1	rw-	1
15	22	1	rw-	1

One Single Linear Page Table



RAM

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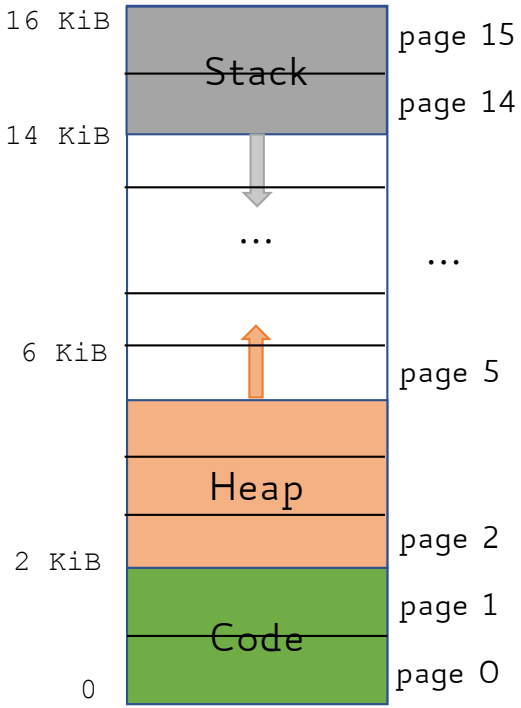

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	...			
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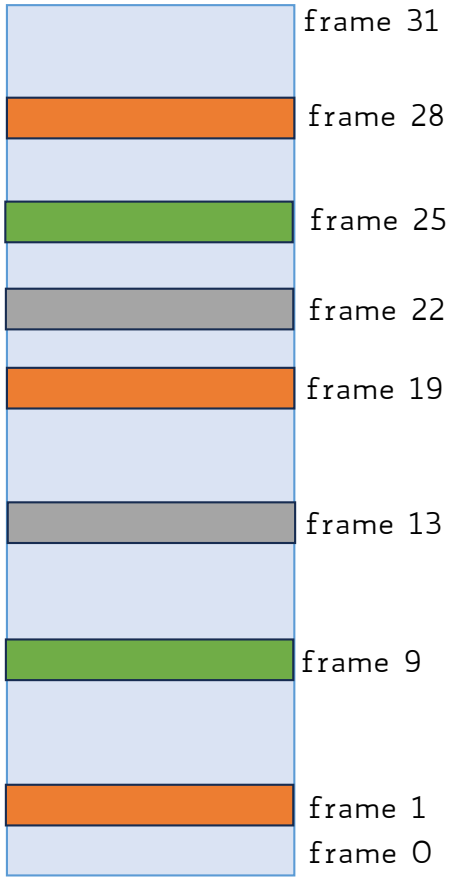
Wasted!



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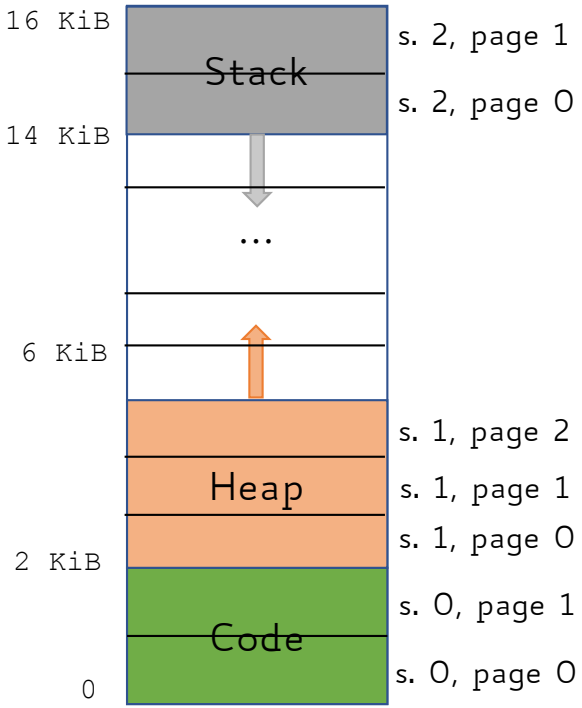

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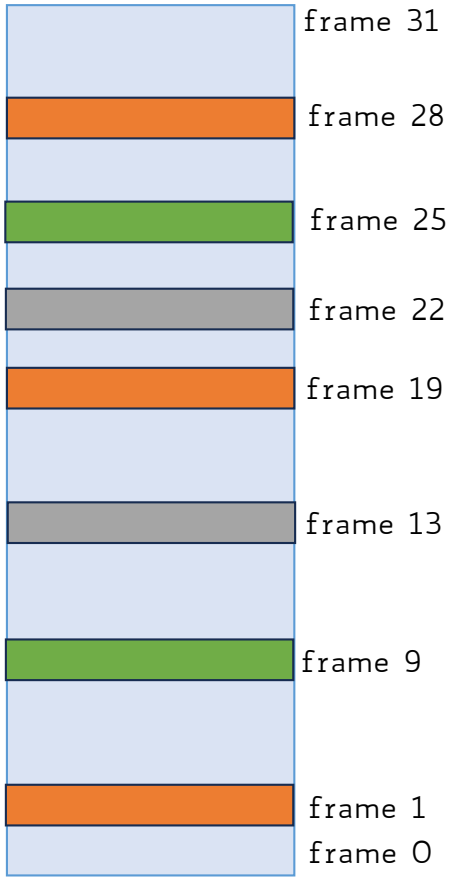
3 Linear Page Tables (one per segment)



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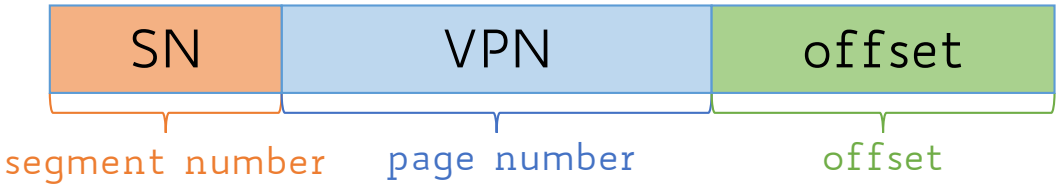
```

  - External fragmentation → page tables may have different sizes

Address Translation with Segmented Paging

A virtual address now becomes:



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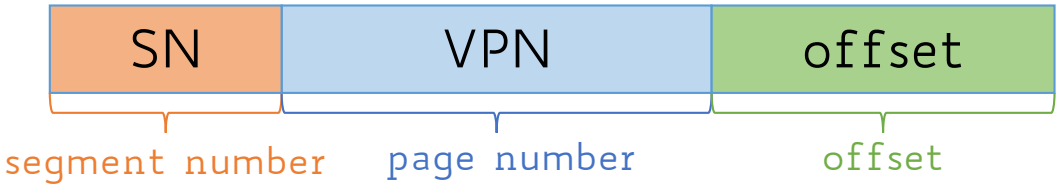

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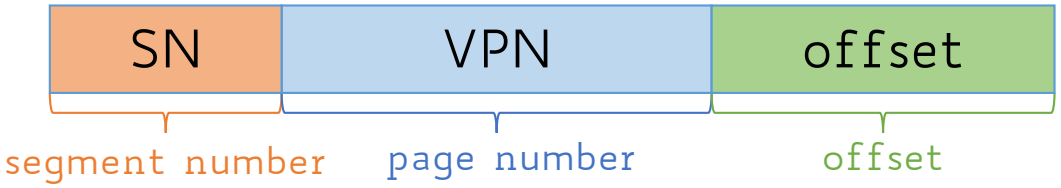

- The segment number (SN) indexes into the **segment table**, which contains the base address of the **page table** for *that* segment
- Check the VPN against the limit of the segment (i.e., the **number of PTEs** in the page table for *that* segment)

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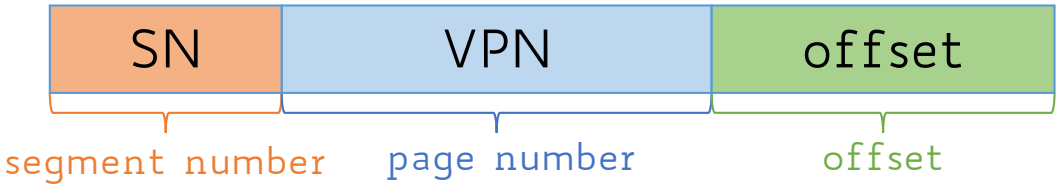

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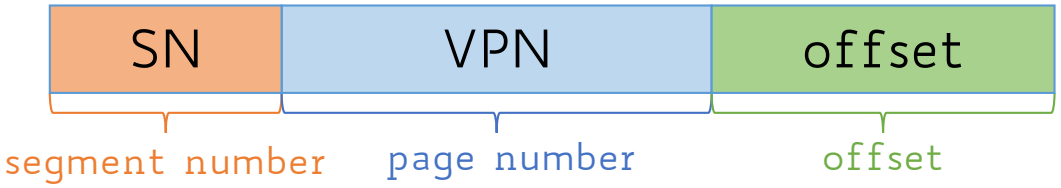
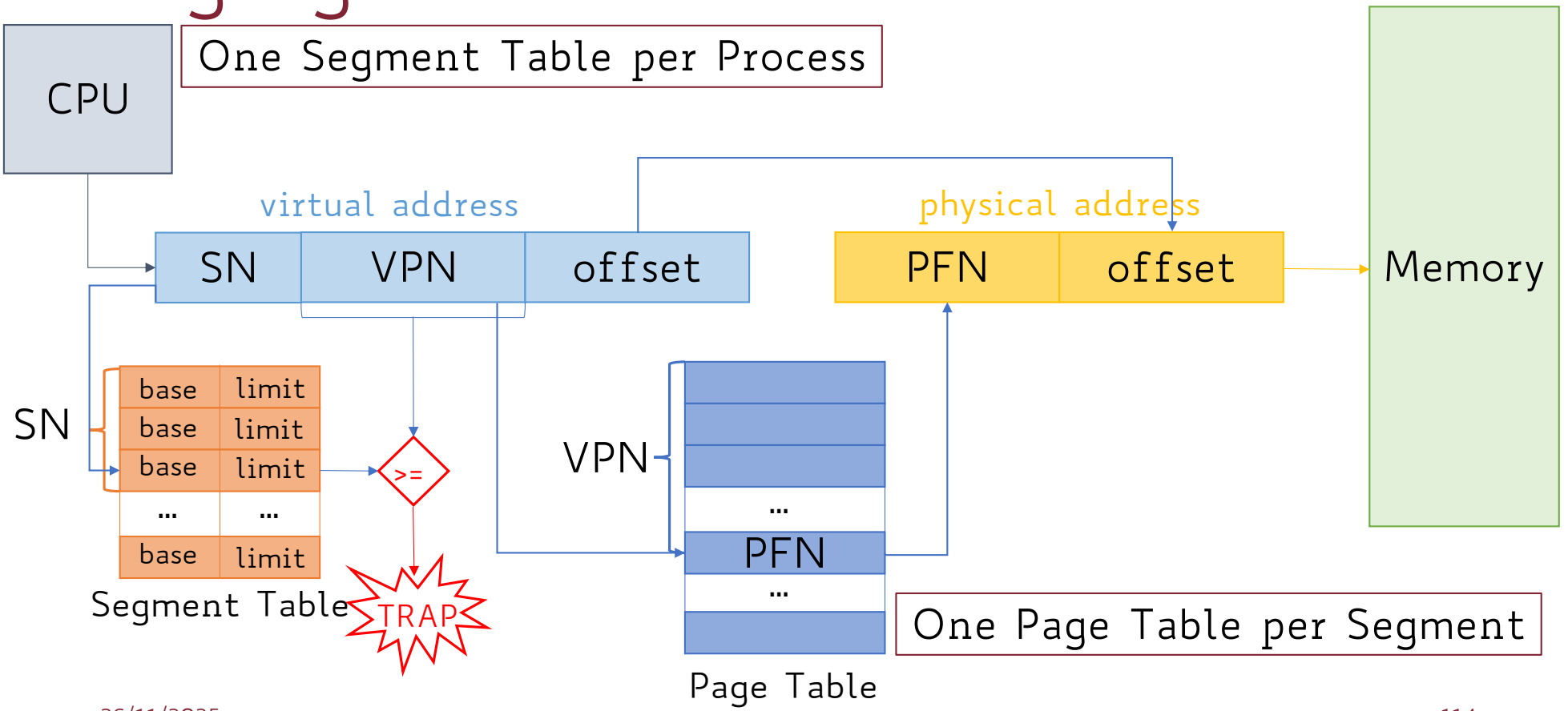


- Use the VPN to index the page table to get the physical frame number (PFN)
- Add the frame number (PFN) to the offset to get the physical address

Address Translation with Segmented Paging



Segmented Paging: Implementation

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Faster but the number of segments is limited

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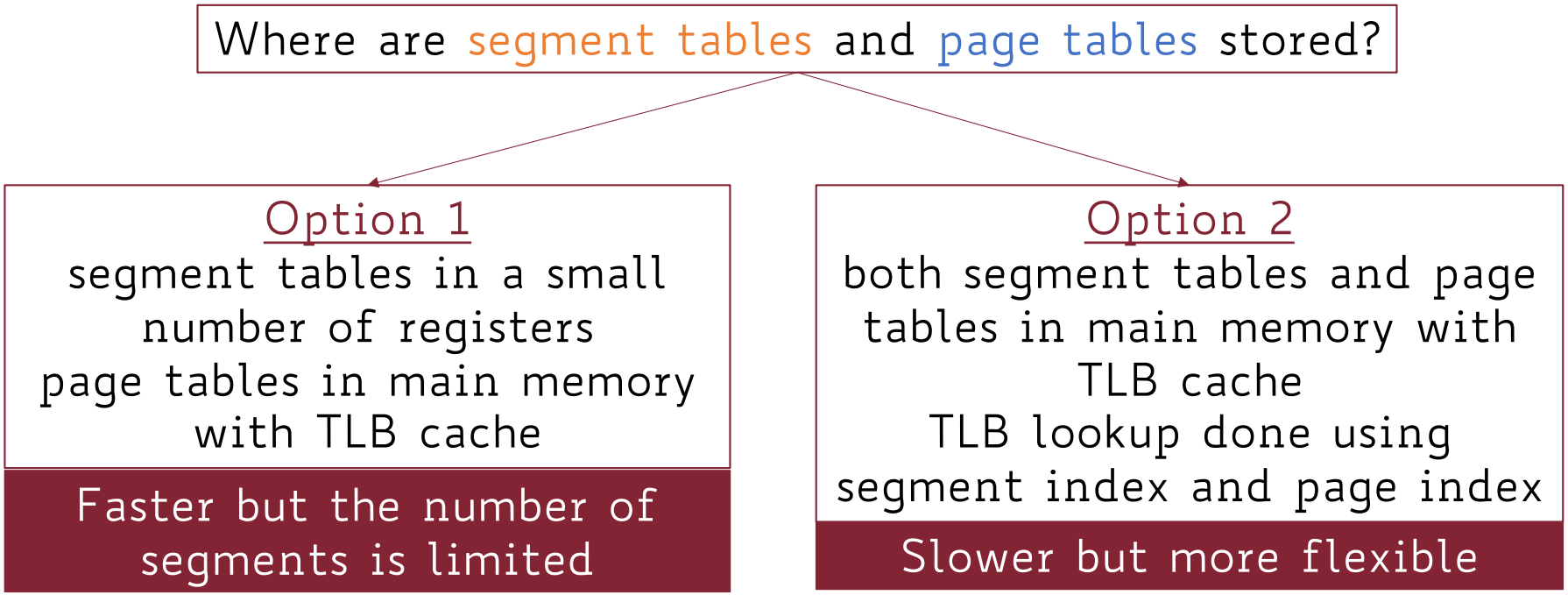

Segmented Paging Hardware: Practical Example 3

Suppose a physical memory of 1024 addressable words (assuming 1 word = 1 byte)
Frame size is 64 words (i.e., 64 bytes)
Page table size (i.e., number of entries) is thus 1024 bytes/64 bytes per frame = 16
8 logical segments

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10 bits to address M = 1024/1 = 1024 1-byte words

Segmented Paging Hardware: Practical Example 3

Q2

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Segmented Paging Hardware: Practical Example 3

Q2

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3 bits to address 8 logical segments (s)

4 bits to address 16 entries of the page table

6 bits to address 64 individual words (i.e., bytes) within each page

Segmented Paging Hardware: Practical Example 3

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13 bits (virtual address) vs. 10 bits (physical address)

Sharing Pages and Segments

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- Even more flexible!

Segmented Paging: Benefits and Costs

- **Benefits:**
  - Merge compiler and OS view of memory
  - Flexibility
  - Less memory waste for sparse VAS w.r.t linear page tables
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  - Sharing memory between processes
- **Costs:**
  - Slower context switches (why?)
  - Slower address translation (why?)

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- On pure paging (no segmented), assuming process' memory footprint is random, internal fragmentation amounts to 0.5 page per process (on average)
- On segmented paging, we can lose 0.5 page per process' segment
- The larger the page size the higher the chance of internal fragmentation

Can We Make Page Tables Smaller?

1. Using segmentation
2. **Using more advanced page table structures beyond simple linear arrays**

Multi-Level Page Tables

- Turns linear page tables into a **tree**
- **Basic Idea:**
  - Divide up the page table into page-sized units (i.e., applying paging to the page table!)
  - If an entire page of PTEs is invalid do not allocate that page at all!
  - Use a new structure (**page directory**) to track if a page of the page table is valid

Multi-Level Page Tables

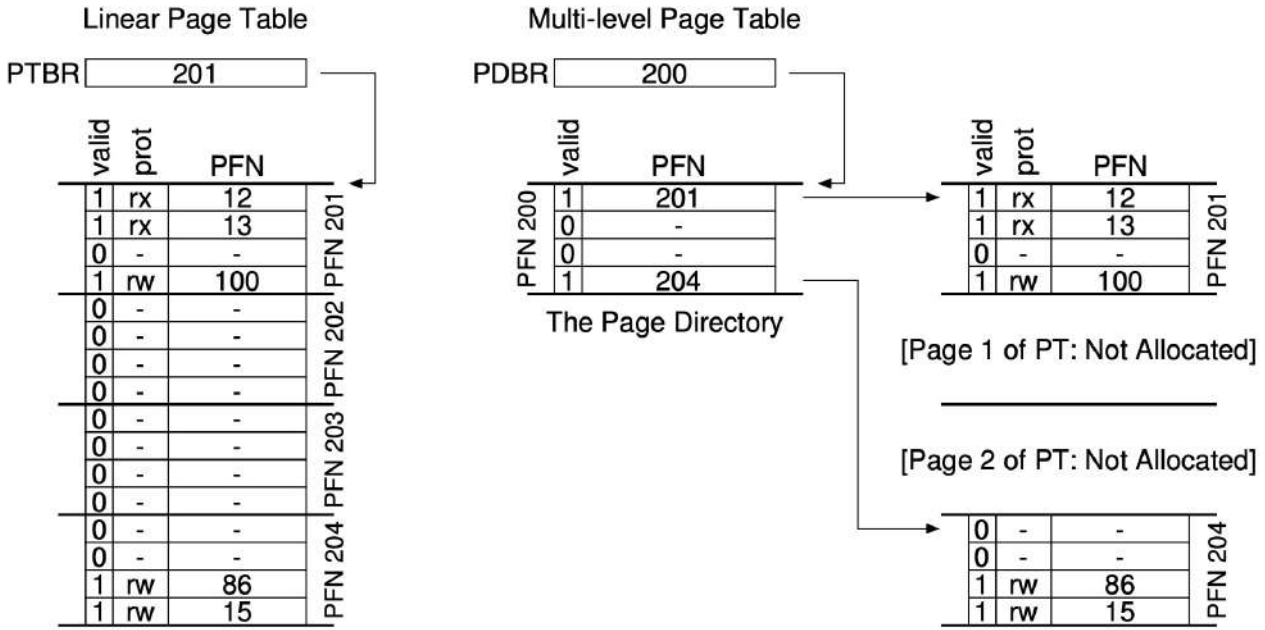


Figure 20.3: **Linear (Left) And Multi-Level (Right) Page Tables**

source: Operating Systems: Three Easy Pieces

Page Directory

- Consists of a number of page directory entries (PDEs)
- In a two-level table: one PDE per page of the page table
- Each PDE at least contains:
  - A valid bit
  - A page frame number (similar to a PTE)
- If the PDE valid bit is set, at least one of the pages that the PDE refers to is valid

Multi-Level Page Tables: PROs

- Allocates only page table space that is proportional to the (sparse) address space used
- If properly designed, each portion of the page table fits the size of a page
- For linear (non-paged) page tables, this array must be allocated contiguously in physical memory
- With multi-level paging, pages of the same page table can be allocated scatteredly in RAM

Multi-Level Page Tables: CONs

- When combined with TLB in case of a cache miss, two extra memory accesses are needed
  - The first one to get to the PDE
  - The second one to get to the PTE
- Page table lookup on TLB miss is typically handled by the OS (rather than just via HW through the MMU)
  - Increased complexity

Beyond Two-Level Page Tables

- Suppose m = 30-bit VAS and page size = 512 B

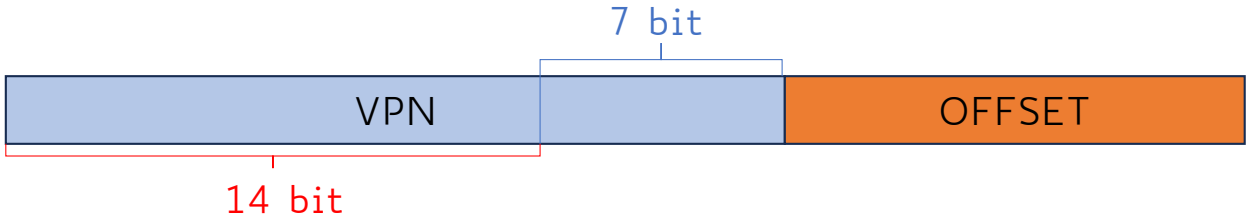
Goal: Divide the entire page table into chunks, so that each chunk fits one page

How many levels do we need?

Beyond Two-Level Page Tables

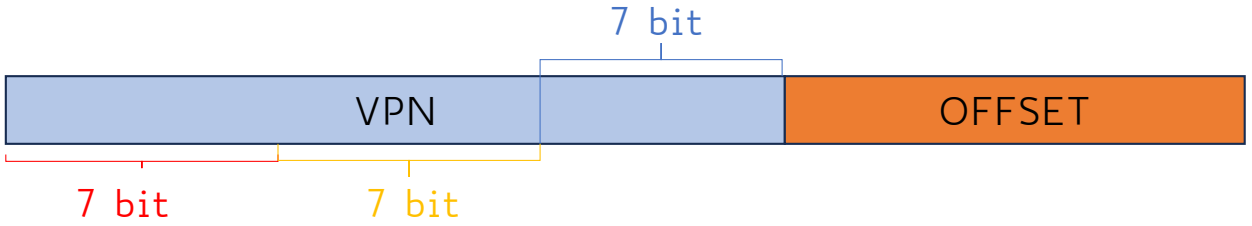
- Let's start by determining how many PTEs fit within a page
  - Given our page size is 512 B and each PTE requires 4 B
  - A single page will contain 512 B/4 B = 128 PTEs
- That means that to index within a single page of the page table we need $\log_2(128)$ bits = 7 bits
  - The least significant 7 bits of the VPN are used as index

Beyond Two-Level Page Tables



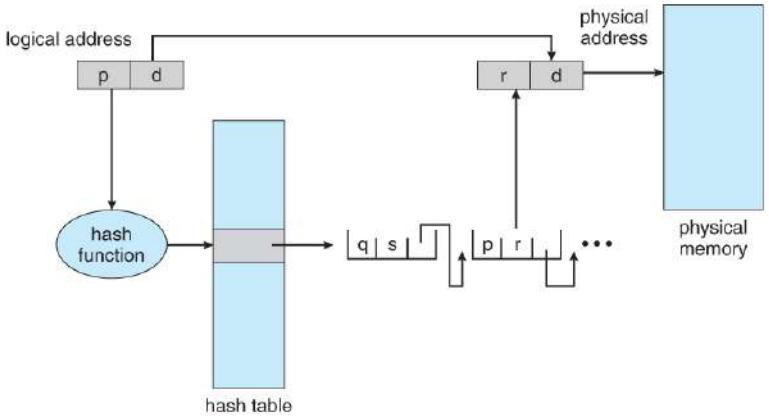
- We are left with 21-7 = 14 bits for the page directory
- 2^{14} page directory entries each of size 4 B would require $2^{14} * 2^2 = 2^{16}$ B
- 2^{16} B is way larger than one page size (2^9 B = 512 B)
- The page directory would require 2^{16} B/2^9 B = 2^7 = 128 pages rather than one as our goal was!

Beyond Two-Level Page Tables



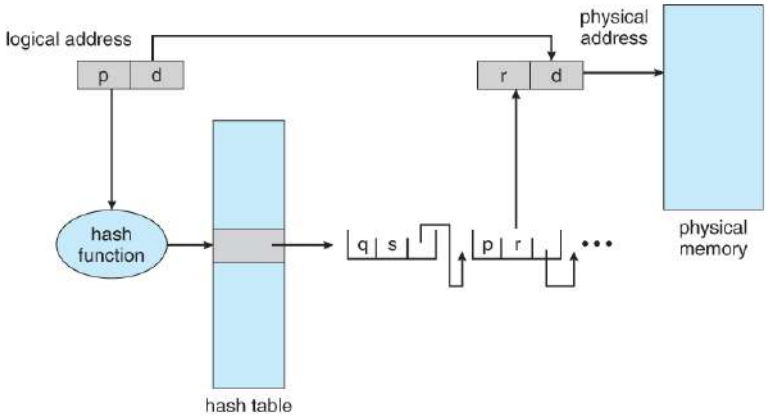
- **Solution:** We add another level to our tree!
- The first 7 bits are used to index the root (level 1) page directory (PD1) and fetch the corresponding PDE
  - This PDE contains the PFN of the base of level-2 page directory (PD2)
- The second 7 bits are used to index in PD2 and fetch the PDE
  - This PDE contains the PFN of the base of level-3 page table (PT)
- The third 7 bits are used to index in PT and fetch the final PTE

Advanced Paging: Hashed Page Table



Use hash tables to store highly sparse page tables

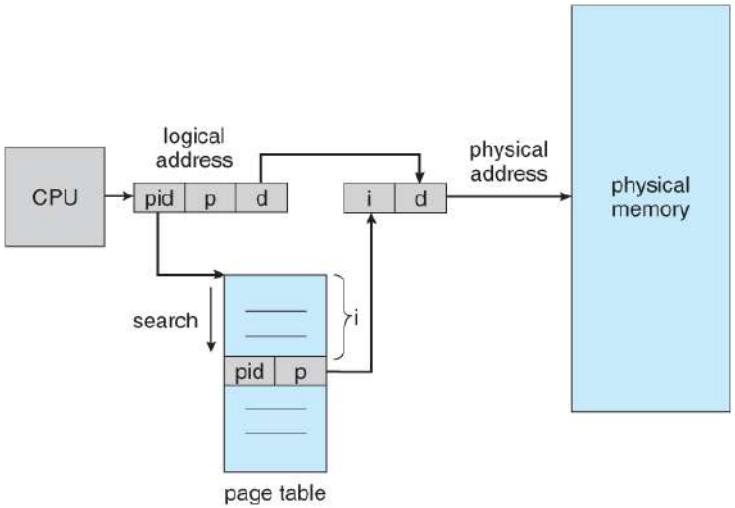
Advanced Paging: Hashed Page Table



Use hash tables to store highly sparse page tables

Indexing via hash function rather than integers

Advanced Paging: Inverted Page Table



An inverted page table lists all of the frames currently loaded in memory, for all processes

Instead of a table listing all of the pages for a particular process

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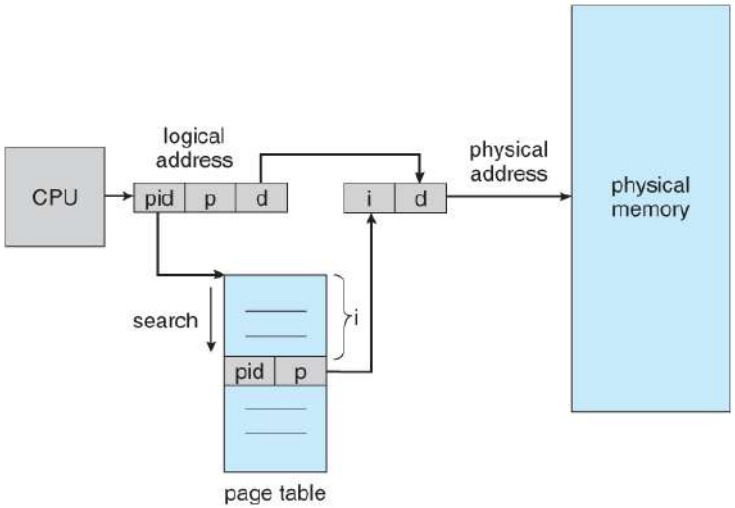

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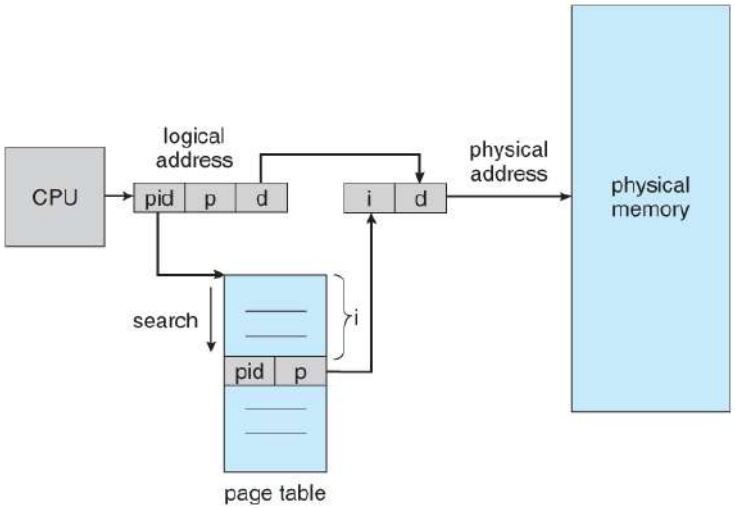
Access to an inverted page table can be slow (linear search)

Hashing the table speeds up the search process

Advanced Paging: Inverted Page Table



An inverted page table lists all of the frames currently loaded in memory, for all processes

Instead of a table listing all of the pages for a particular process

Access to an inverted page table can be slow (linear search)

Hashing the table speeds up the search process

Inverted page tables do not easily allow mapping multiple logical pages to a common physical frame (page sharing)

Each frame is mapped to exactly one process

Summary

- **Relocation** using base and limit registers
  - Simple yet inflexible

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  - Simple yet inflexible
- **Segmentation**
  - Compiler's logical view of memory presented to the OS
  - Segment tables tend to be small enough to be stored in registers
  - Contiguous memory allocation is expensive and complicated (first-fit, best-fit, or worst-fit)
  - Compaction is needed to solve external fragmentation

Summary

- **Paging**
  - Simplifies memory allocation by relaxing contiguous assumption
  - Each logical page can be allocated to any physical frame
  - Page tables can be extremely large

Summary

- **Segmentation + Paging**
  - One page table per segment vs. of one page table per VAS
  - Segments can still be sparse (e.g., heap)
  - Sharing either at the segment or at the page level
  - Might increase internal fragmentation over pure paging
  - 2 lookups per memory reference are needed

Summary

- **Multi-Level Paging**
  - Paging applied to the page table!
  - From linear page table (array) to a tree
  - Goal: Create as many levels as needed to fit each page table chunk into a page
  - Minimize memory waste (only touched pages are materialized)
  - On a TLB miss, as many memory accesses as the number of levels