

Sistemi Operativi I

Corso di Laurea in Informatica
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SAPIENZA
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Problems Seen So Far

- Contiguous allocation
 - Hard to grow or shrink process memory
- Fragmentation
 - Frequent compaction needed
- Process entirely loaded
 - Swapping helps but it may be too inefficient

Paging

- A memory management scheme that addresses the problems above

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90/10 Rule

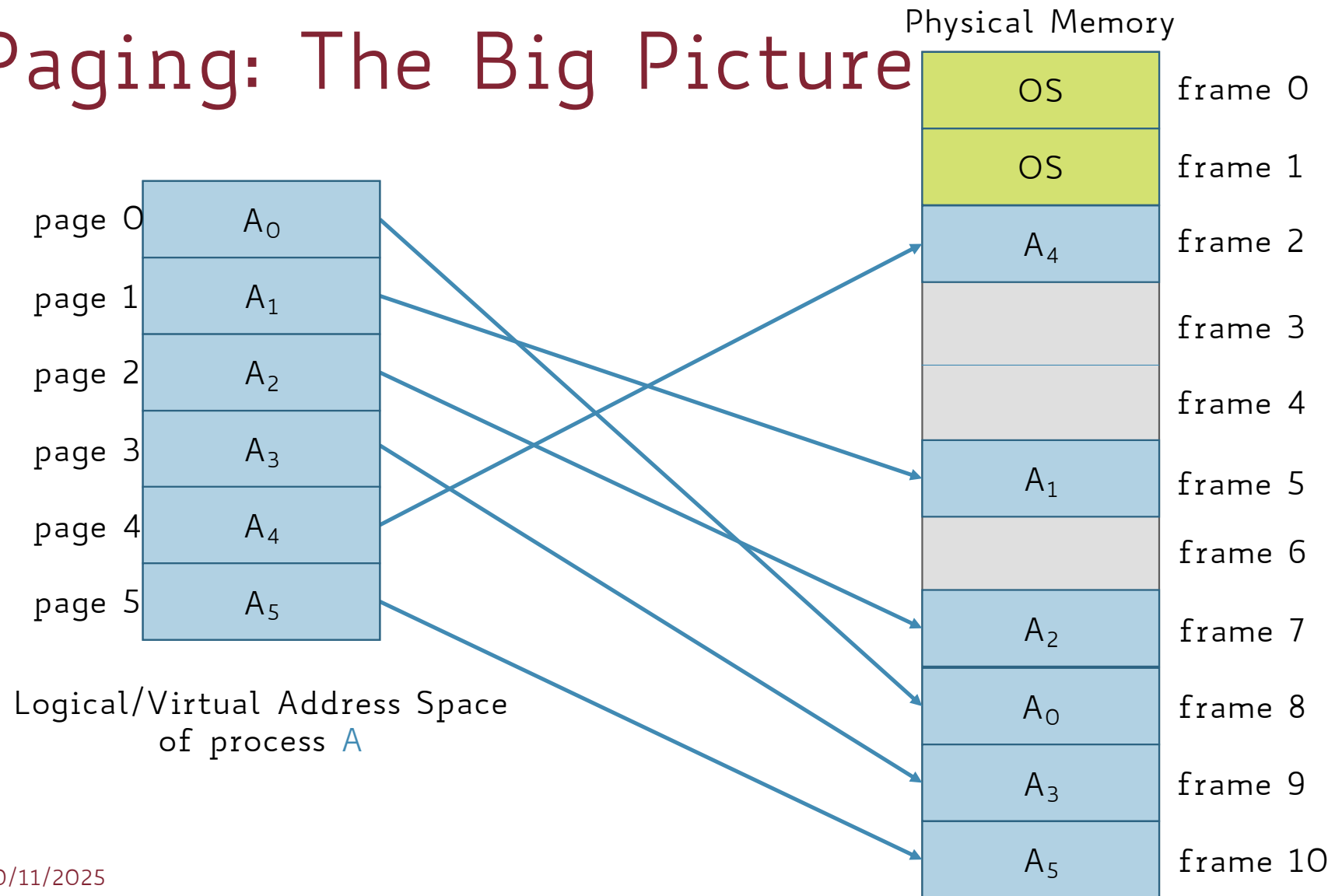
Processes spend **90%** of their time accessing only **10%** of their allocated memory space

Paging: The Big Picture

page 0	A_0
page 1	A_1
page 2	A_2
page 3	A_3
page 4	A_4
page 5	A_5

Logical/Virtual Address Space
of process A

Paging: The Big Picture



Basic OS Responsibilities for Paging

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 - mapping between logical pages and physical frames
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- All of this must be done efficiently!
 - Remember, memory addresses are referenced all the time
- OS needs dedicated support for doing it → **Page Table**

Page Table: Mapping Pages to Frames

0	A_0
1	A_1
2	A_2
3	A_3
4	A_4
5	A_5

OS	0
OS	1
A_4	2
	3
	4
A_1	5
	6
A_2	7
A_0	8
A_3	9
A_5	10

Page Table: Mapping Pages to Frames

Lookup table to retrieve what frame a page is stored in

0	A ₀
1	A ₁
2	A ₂
3	A ₃
4	A ₄
5	A ₅

Page	Frame
0	8
1	5
2	7
3	9
4	2
5	10

OS	0
OS	1
A ₄	2
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	4
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	4
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A ₂	7
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We have assumed **all** pages of a process are mapped to physical frames, but this is not always the case

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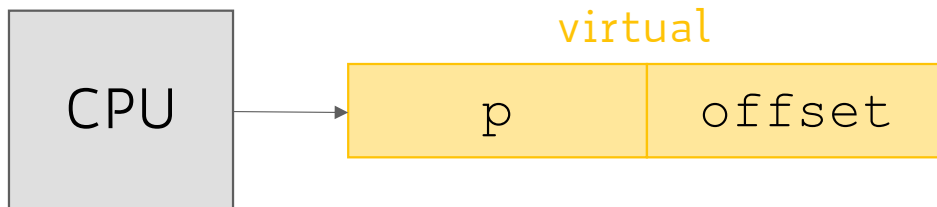
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- Processes use virtual (logical) addresses to refer to memory (not page number!)
- Virtual (logical) address space is still contiguous starting from 0
- Page table must ultimately translate virtual address to physical address

Page Table: Virtual to Physical Address

virtual address consists of 2 parts:

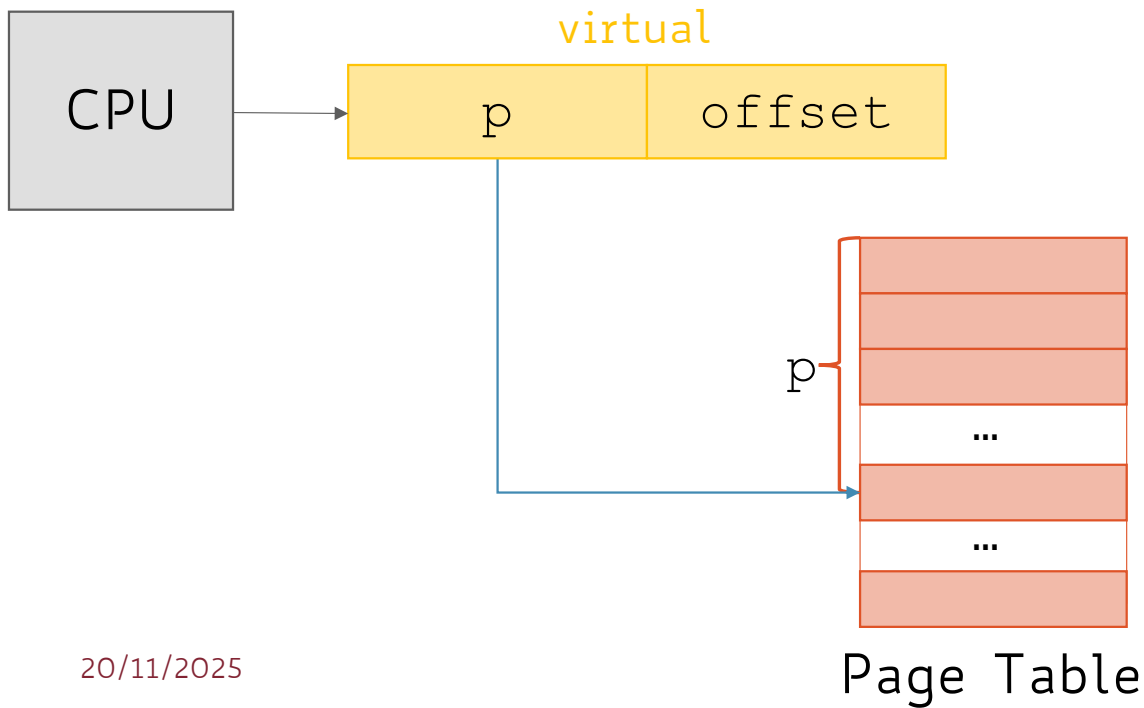
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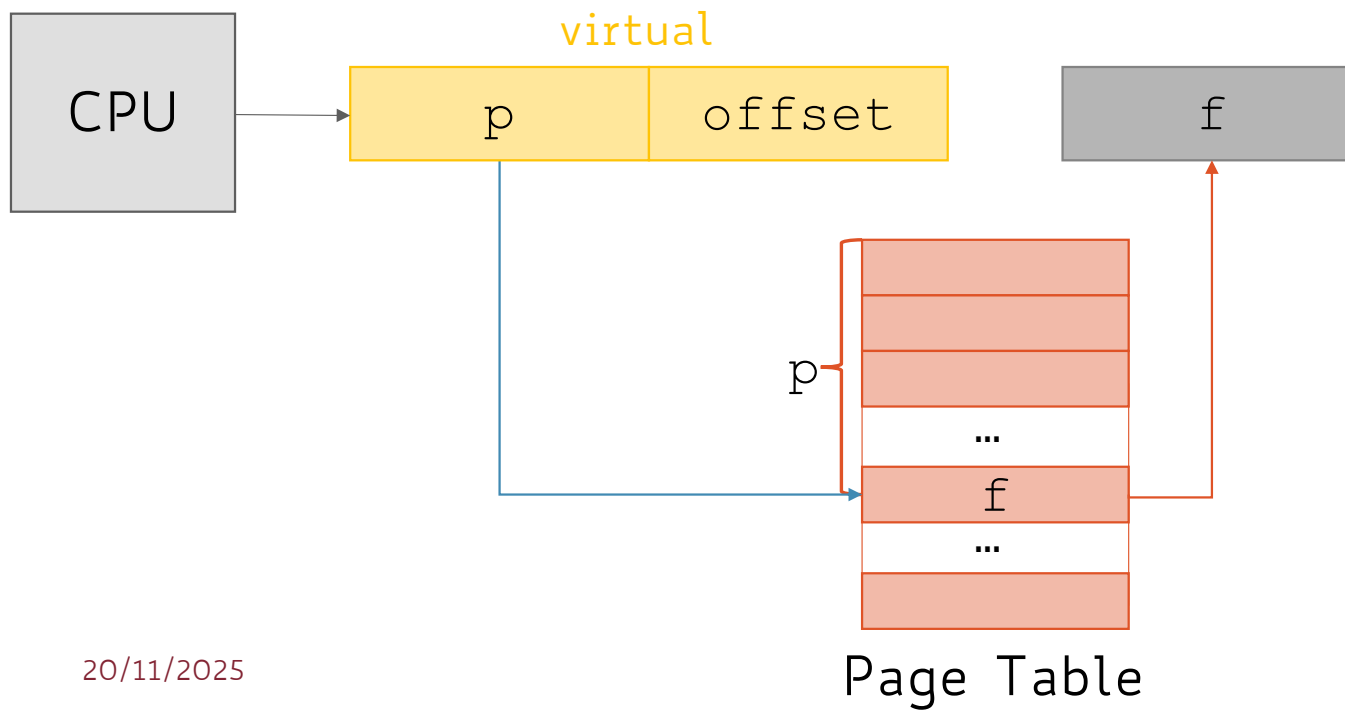
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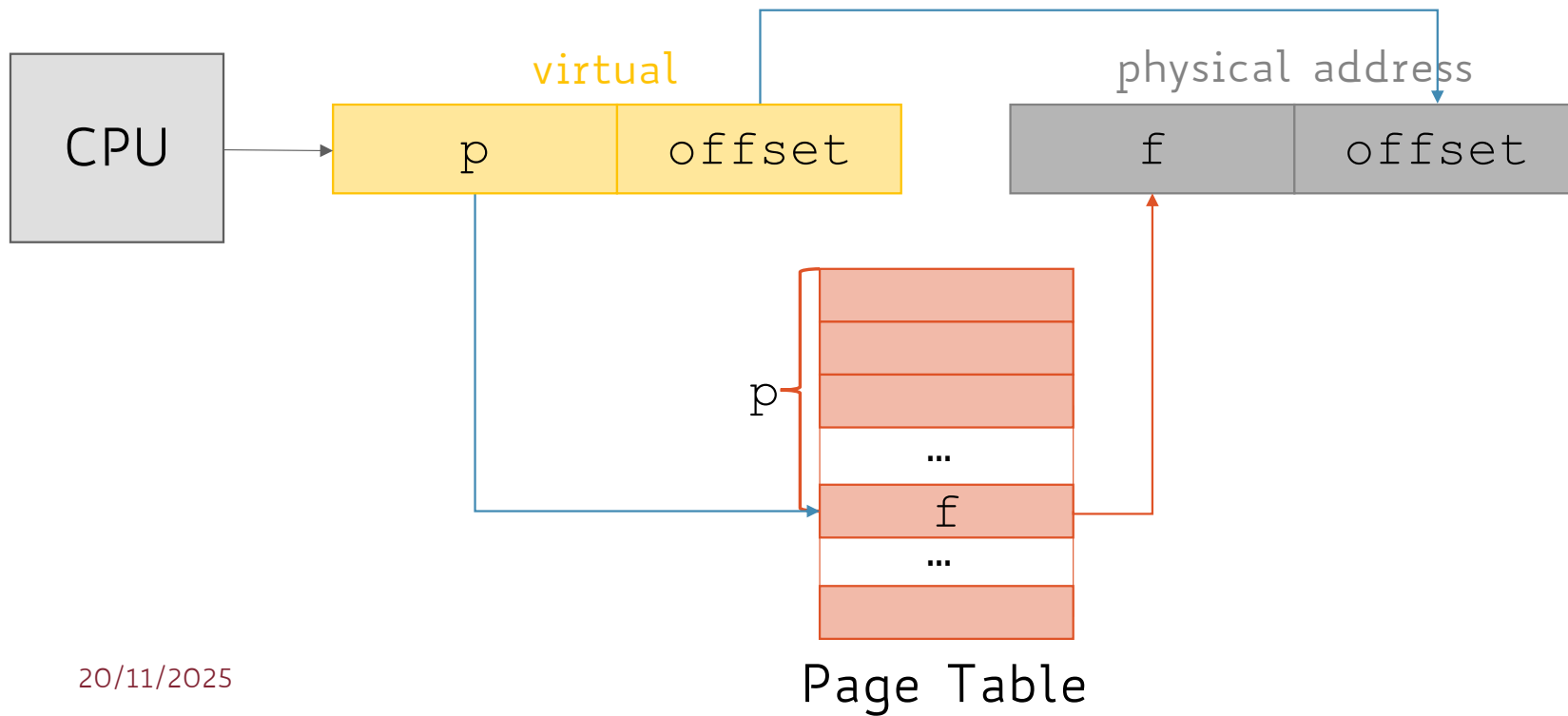
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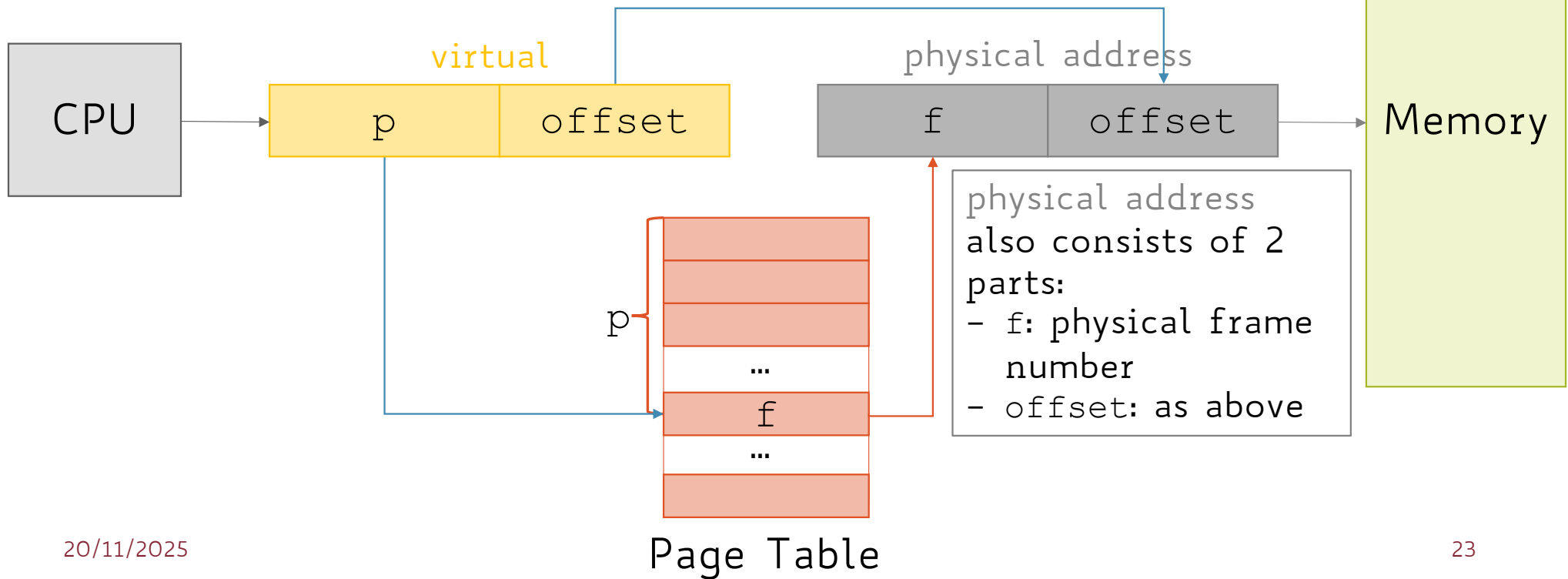
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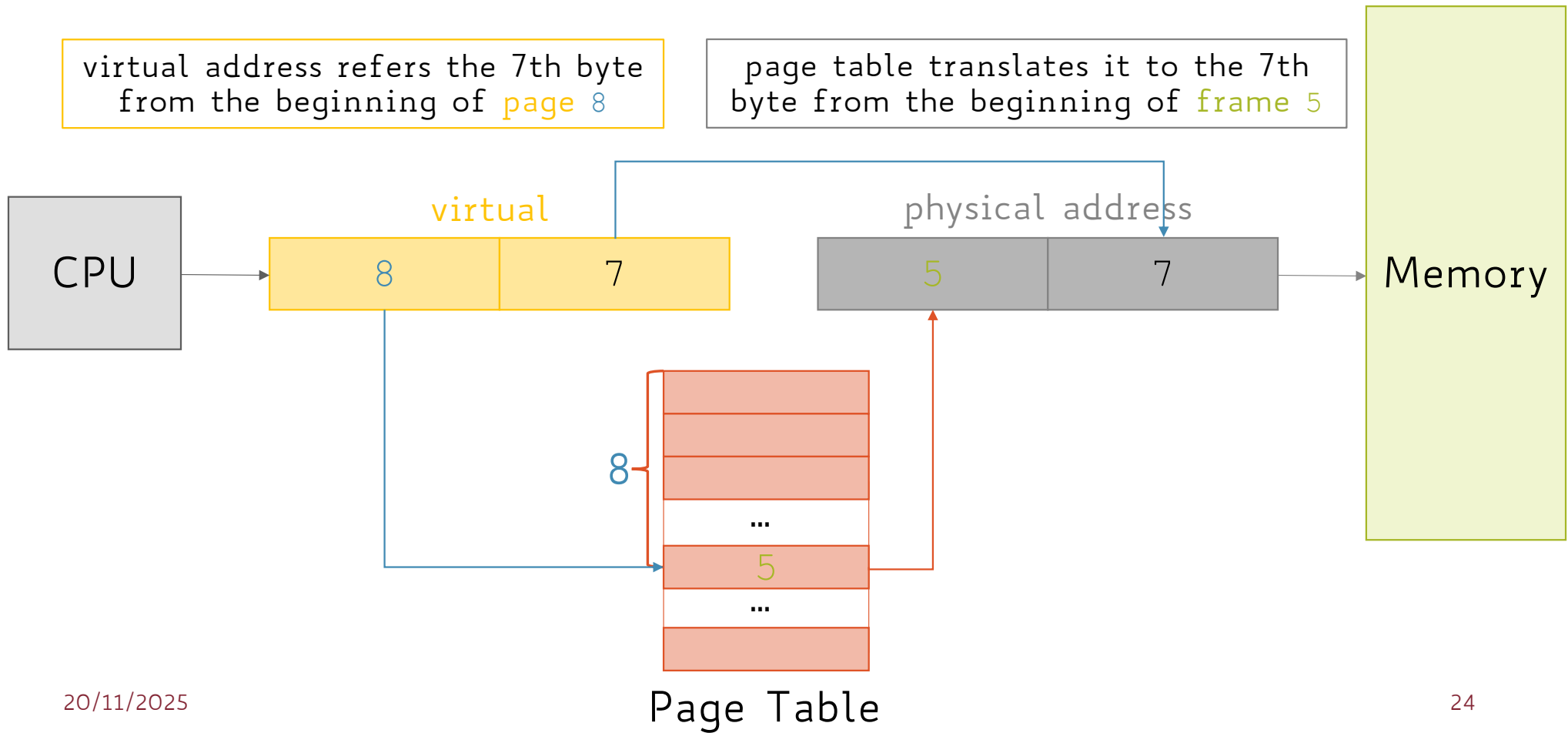
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Page Table: Example of Address Translation

virtual address refers the 7th byte from the beginning of **page 8**

page table translates it to the 7th byte from the beginning of **frame 5**



Paging as Dynamic Relocation

- Paging is an advanced form of dynamic relocation
- Each virtual address is bound by the page table to a physical address
- Page table can be seen just as a set of base (relocation) registers, one for each frame
- Mapping is invisible to the user process: the OS maintains the page table and translation happens in hardware (via the MMU)
- Protection is provided similarly to dynamic relocation (limit register)

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1. Get the page number (**p**) and the **offset** where the virtual address **x** resides
2. Use **p** to index into the page table to retrieve the frame number **f**
3. Combine **f** with **offset** to obtain the physical address **y**

Paging: Get **p** and **offset** from **x**

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$$\mathbf{p} = \mathbf{x} \mathbf{div} \mathbf{S}$$

page number

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Address translation requires a **div** and a **mod** operation

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Why?

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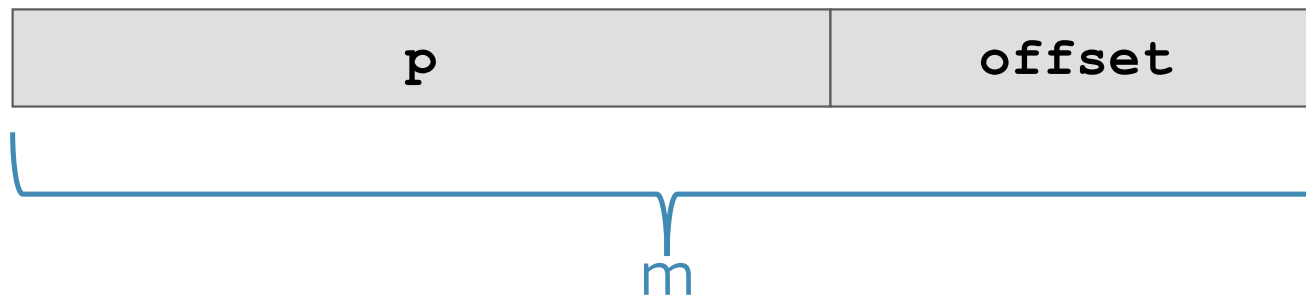
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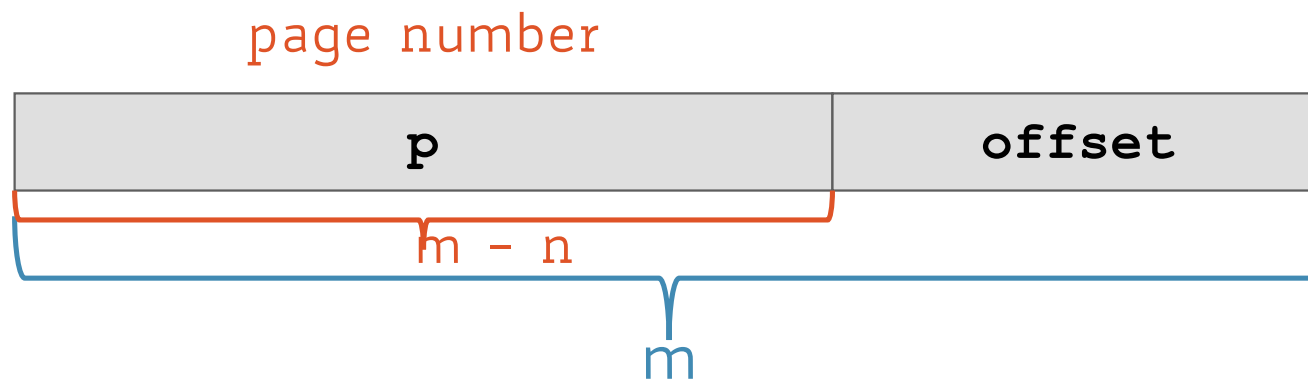
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- The low order n bits represent the **offset**

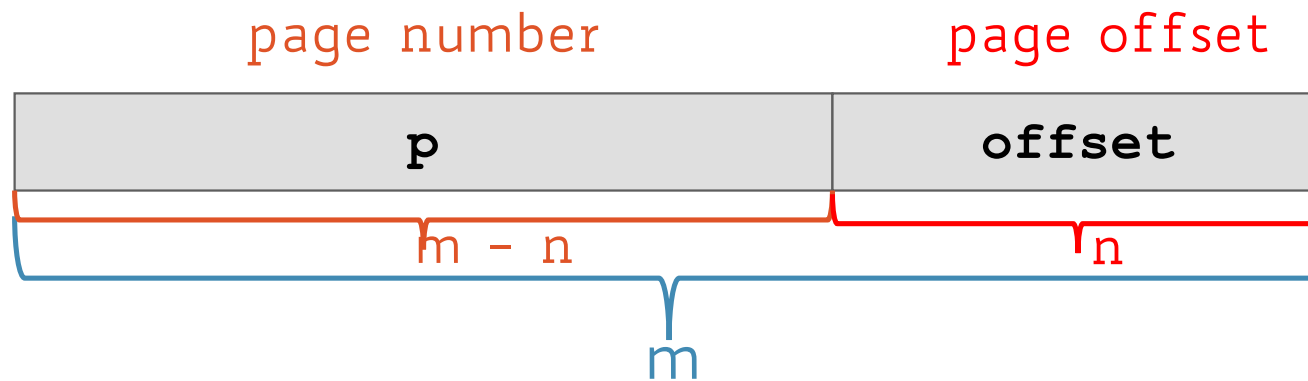
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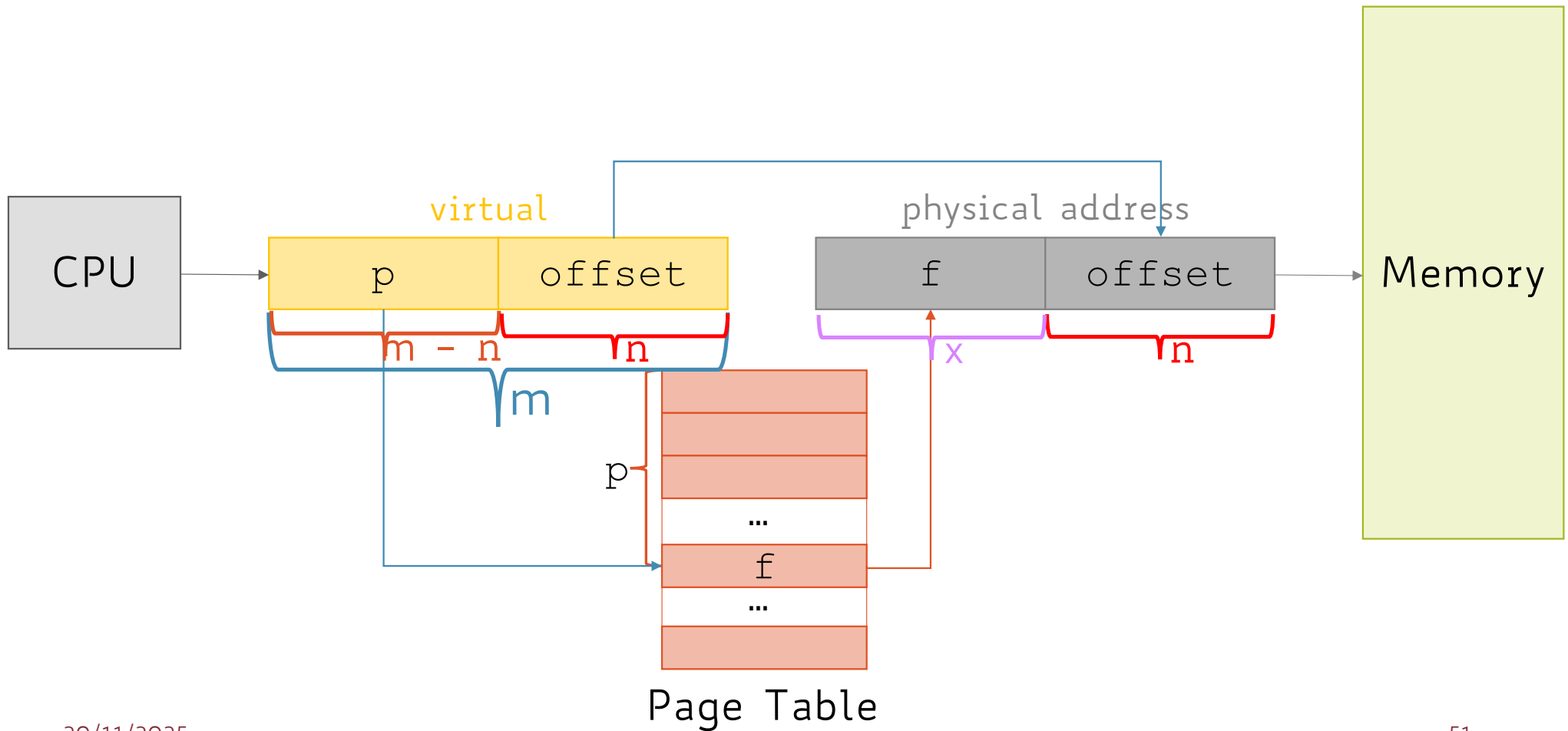
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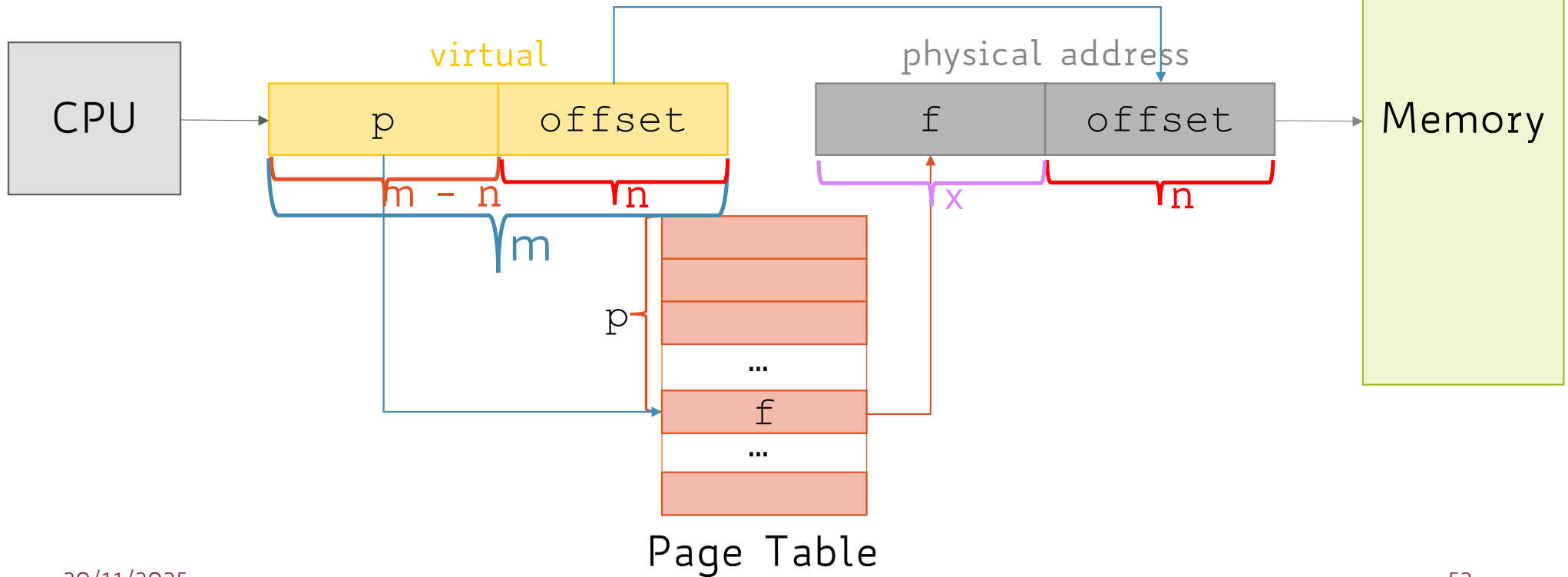
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NOTE

$m-n$ doesn't necessarily have to be equal to x



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- Typical values of page/frame sizes is $n = 12$ bits
 - Each page/frame is $2^{12} = 4\text{KiB}$
- Assuming $m = 32$ bits, there are $2^{m-n} = 2^{20} = \sim 1\text{M}$ pages/frames
 - The page table has 2^{20} entries (i.e., one for each page/frame)

Paging: Practical Example

Suppose we have a virtual memory and a physical memory, both of size $M = 1024\text{B}$ (1KiB)

Q1

How many bits are needed for a virtual/physical address (assuming single-byte addressing)

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R1

10 bits to address $M = 1024$ bytes (both for virtual and physical address)

Paging: Practical Example

Now, assume we use paging with page/frame size $S = 16B$

Q2

How big is the page table? (i.e., how many pages/entries does it have to index?)

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R2

$T = M / S = 1024 \text{ memory bytes} / 16 \text{ bytes per page} = 64 \text{ pages}$

Paging: Practical Example

Q3

What is p and $offset$ (i.e., how many bits for p and $offset$?)

Paging: Practical Example

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R3

Our logical address is made of $m = 10$ bits
 $n = 4$ bits are used to represent the $offset$, as each page/frame is $S = 16$ bytes
 $m - n = 6$ bits are used to represent page number p , as there are $T = 64$ pages

Paging: Practical Example

Q4

Translate the virtual address $x = 42$, assuming the following page table

page	frame
0	12
1	5
2	37
3	0
...	..
63	29

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Translate the virtual address $x = 42$, assuming the following page table

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R4

$$p = x \text{ div } S = 42 \text{ div } 16 = 2$$

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R4

$$p = x \text{ div } S = 42 \text{ div } 16 = 2$$

$$\text{offset} = x \text{ mod } S = 42 \text{ mod } 16 = 10$$

10th byte from the beginning of frame 37

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Modern computers however operate natively on multiple of bytes (i.e., words) rather than single-byte. Typical values of word length is: 16, 32 or 64 bits.

If we assume 32-bit architecture (i.e., word = 32 bits = 4 bytes), virtual addresses refer to words instead of bytes

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How many bits are therefore needed to address the number of words available on M ?

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Q1

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R1

8 bits to address $M = 1024/4 = 256$ 4-byte words

Paging: Practical Example 2

Now, assume we still use paging with page/frame size $S = 16\text{B}$

Q2

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R3

Our logical address is now made of $m = 8$ bits
 $n = 2$ bits are used to represent the $offset$, as each page/frame is:
 $S = 16$ bytes = $4 * 4$ -byte words
 $m - n = 6$ bits are used to represent page number p , as there are still
 $T = 64$ pages

Paging: Practical Example 2

Q4

Translate the virtual address $x = 7$, assuming the following page table

page	frame
0	12
1	5
2	37
3	0
...	..
63	29

Paging: Practical Example 2

Q4

Translate the virtual address $x = 7$, assuming the following page table

page	frame
0	12
1	5
2	37
3	0
...	..
63	29

Remember: now virtual address refers to a 4-byte word!

Paging: Practical Example 2

Q4

Translate the virtual address $x = 7$, assuming the following page table

page	frame
0	12
1	5
2	37
3	0
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63	29

$S = 16 \text{ bytes} = 4 * 4\text{-byte}$
words
Must be expressed in terms
of number of words

R4

$$p = x \text{ div } S = 7 \text{ div } 4 = 1$$

Paging: Practical Example 2

Q4

Translate the virtual address $x = 7$, assuming the following page table

page	frame
0	12
1	5
2	37
3	0
...	..
63	29

R4

$$p = x \text{ div } S = 7 \text{ div } 4 = 1$$

$$\text{offset} = x \text{ mod } S = 7 \text{ mod } 4 = 3$$

3rd word from the beginning of frame 5

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- It decouples logical from physical memory layout
- An advanced form of dynamic relocation that requires OS intervention (**Page Tables**)
- Standard paging alone can be inefficient...