Systems and Networking I

Applied Computer Science and Artificial Intelligence

2025-2026

SAPIENZA
UNIVERSITÀ DI ROMA

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Useful Information

Class schedule

- **Tuesday:** 4 PM - 7 PM
- **Thursday:** 3 PM - 5 PM

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Contacts

- email: tolomei@di.uniroma1.it
- website: https://github.com/gtolomei/systems-and-networking
- moodle: https://elearning.uniroma1.it/course/view.php?id=20053

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Office hours

- Arranged via email
- in-person or remotely
- Room 106, 1st floor Building E (map)

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Class Material

- Released on the class website
- Suggested books (though not mandatory!):
  - "*Operating System Concepts*" Ninth Edition – Silberschatz, Galvin, Gagne
  - "*Modern Operating Systems*" Fourth Edition – Tanenbaum, Bos
  - "*Operating Systems: Three Easy Pieces*" – Remzi and Andrea Arpaci-Dusseau [available online]
- Any additional resource available on the Web!

Moodle

- Provides native support for:
  - Sharing news and messages (forum)
  - Additional class material (e.g., exercises)
  - Exam simulations (e.g., quizzes)
  - …

Remember to enroll in the course from the moodle web page!

Exam

- **Moodle Quiz:**
  - **20** multiple-answer questions (max. **45** minutes)
  - Marks: **+3** (correct answer), **0** (no answer), **-1** (wrong answer)
    - score <= **14**/30 → **FAIL**
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- Oral Session:
  - Questions and exercises on the subjects covered during the whole semester

Outline of the Course

- Part I: Introduction

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- Part II: Process Management

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- Part VI: File System
- Part VII: Advanced Topics(?)

Part I: Introduction

Language and Naming Conventions

- OS → Operating System
- HW → Hardware
- SW → Software
- VM → Virtual Machine
- …
- Other shortcuts/acronyms may appear here and there without notice!

  Please, ask if anything is not clear!

What is an Operating System?

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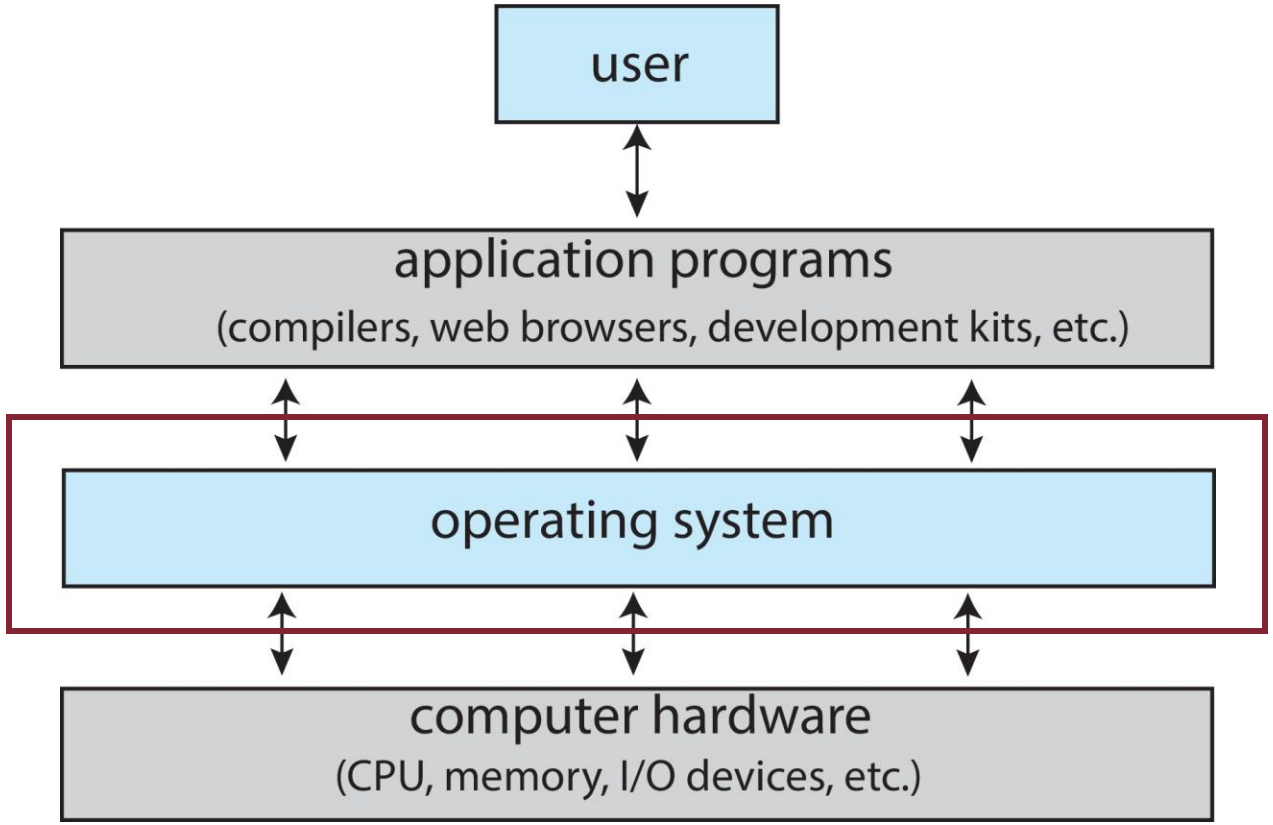
- However, the definition below is quite appropriate:

> Implementation of a virtual machine that is (hopefully) easier to program than bare hardware

Computer System Overview



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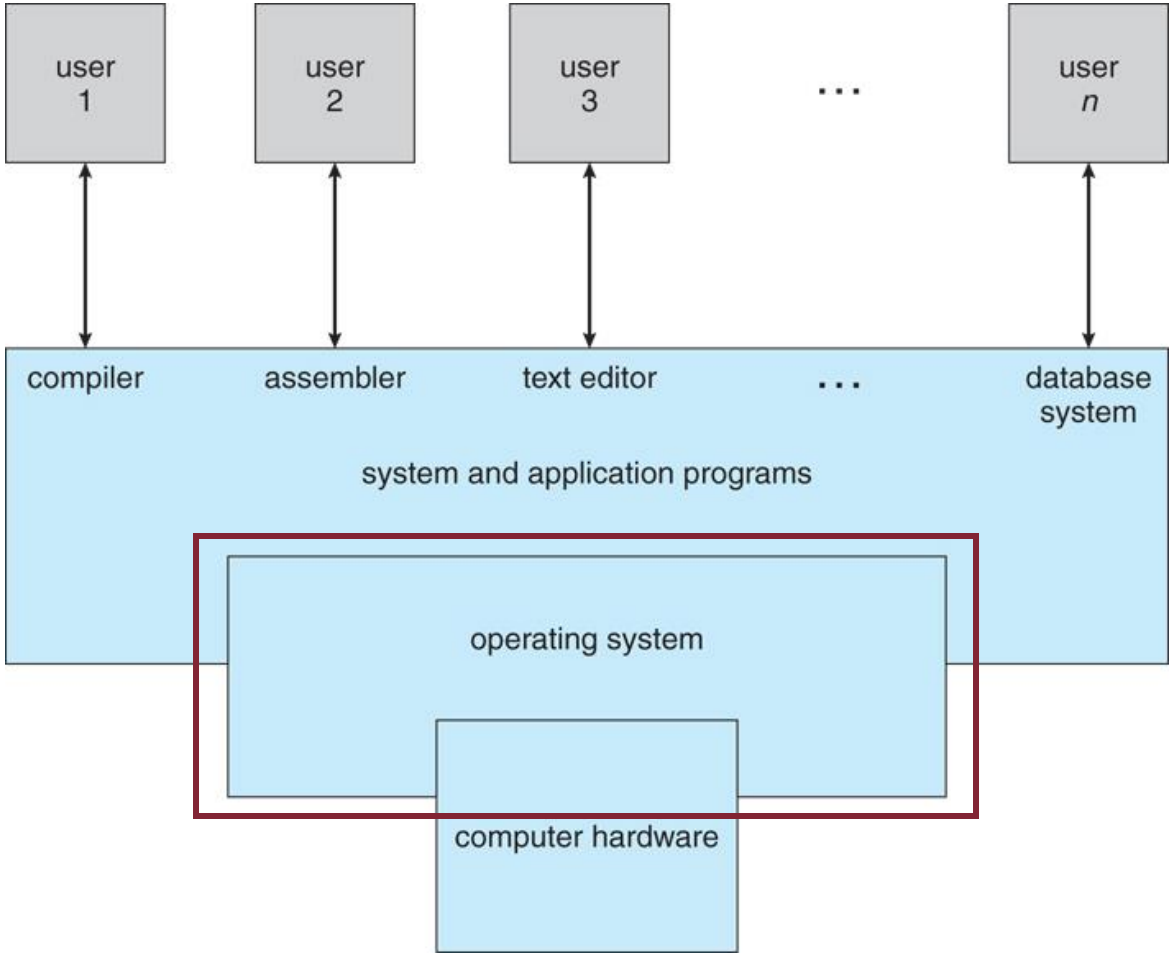

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- Typically, we distinguish between:
  - **kernel** → the "core" of the OS (always up and running)
  - **system programs** → everything else which is still part of the OS

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- **Referee (Resource Manager)**
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  - To achieve **fairness** and **efficiency**

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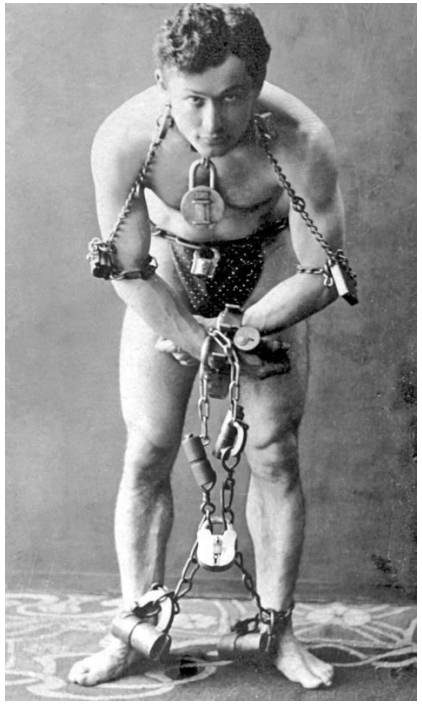
  - Virtualize any physical resource



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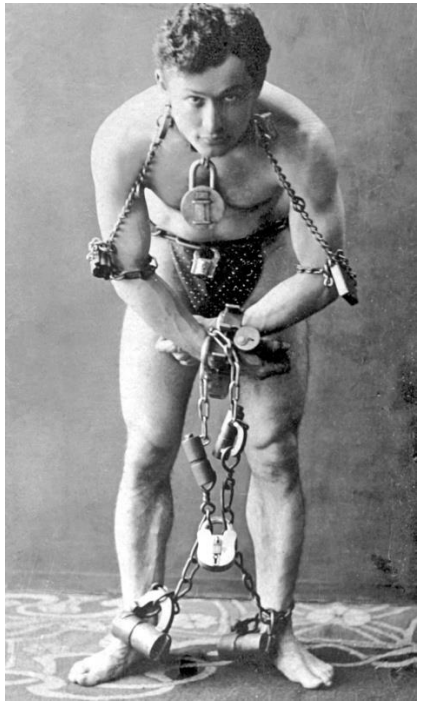
- **Illusionist (Virtual Machine)**
  - Virtualize any physical resource
  - To give applications/users the **illusion of infinite resources** available



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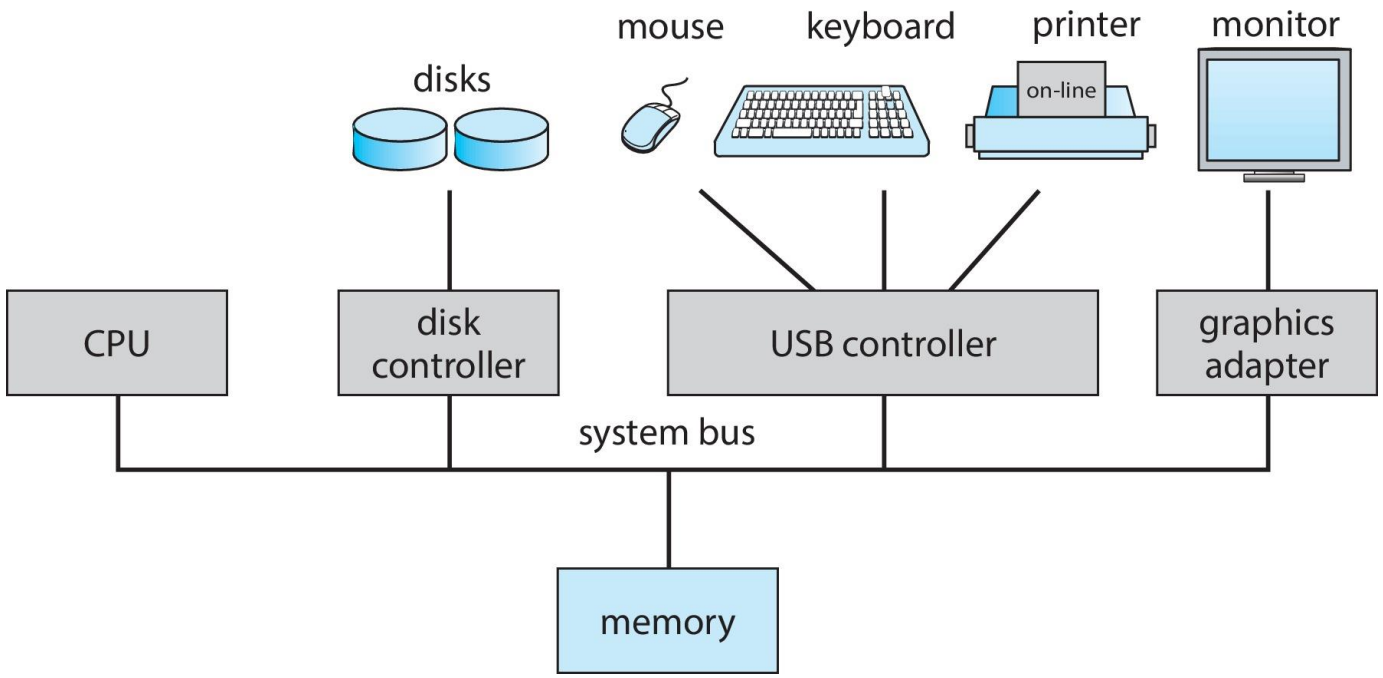
  - To allow applications/users to interact with the system **without talking directly to the HW**

Computer System Organization

High-Level View of a Computer



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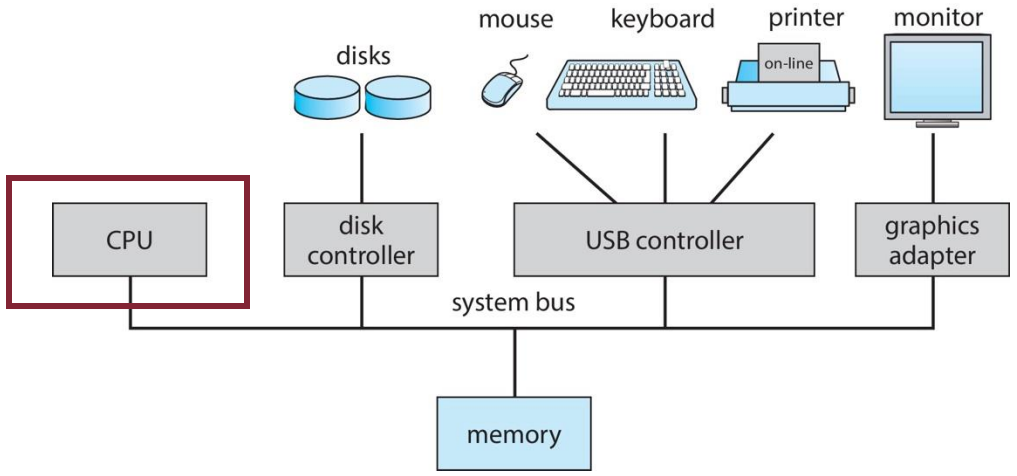

CPU

- The processor that performs the actual computation
- Multiple cores are now common in modern architectures

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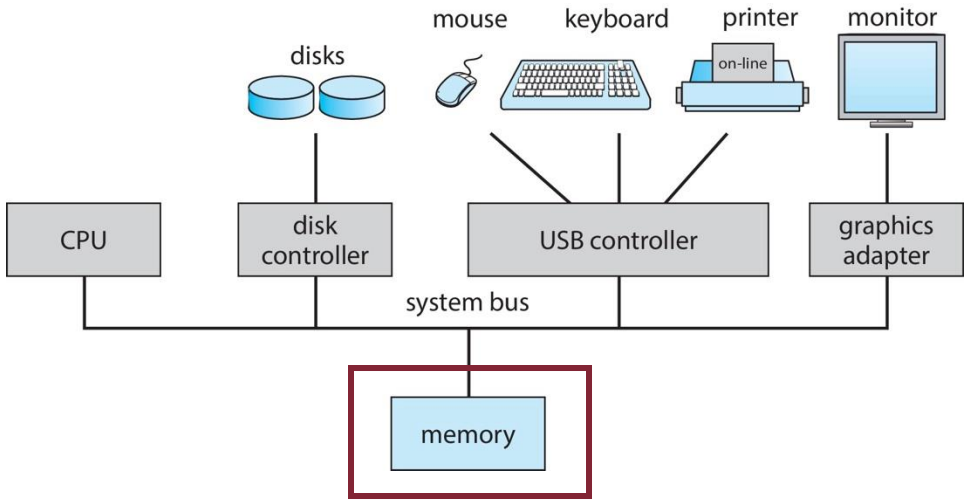
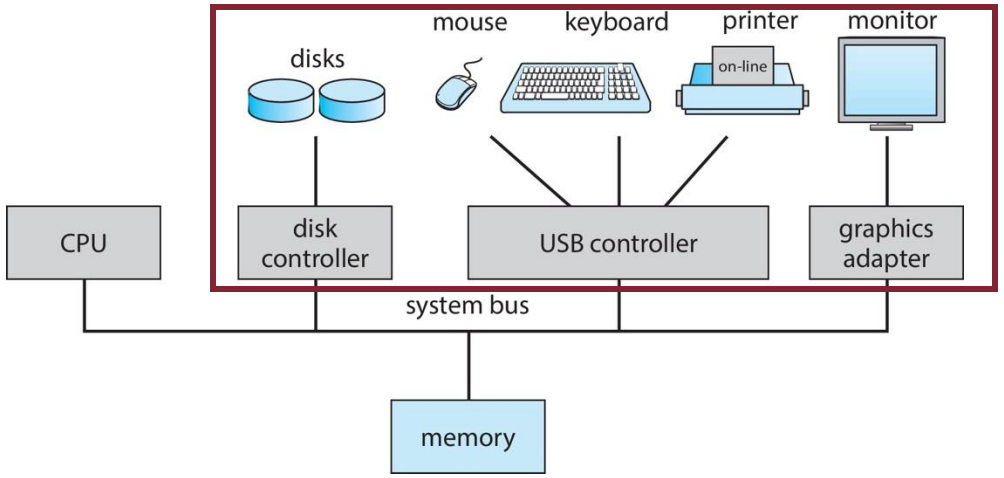


Main Memory

- Stores data and instructions used by the CPU
- Shared between CPU and I/O

High-Level View of a Computer



I/O devices

- terminal, keyboard, disks, etc.
- Associated with specific device controllers

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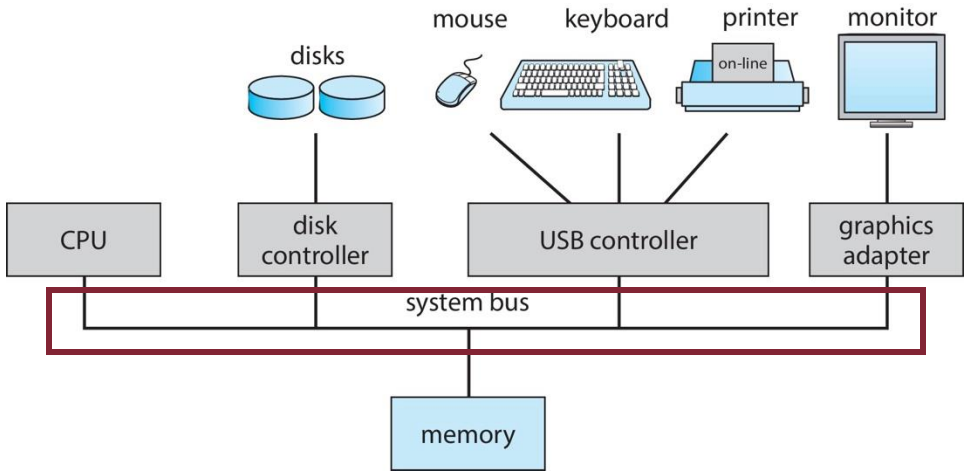

System Bus

- Communication medium between CPU, memory, and peripherals

Computer Architecture Model

- Conceptually, the same architectural model for many computing devices:
  - PCs/laptops
  - High-end servers
  - Smartphones/Tablets
  - etc.

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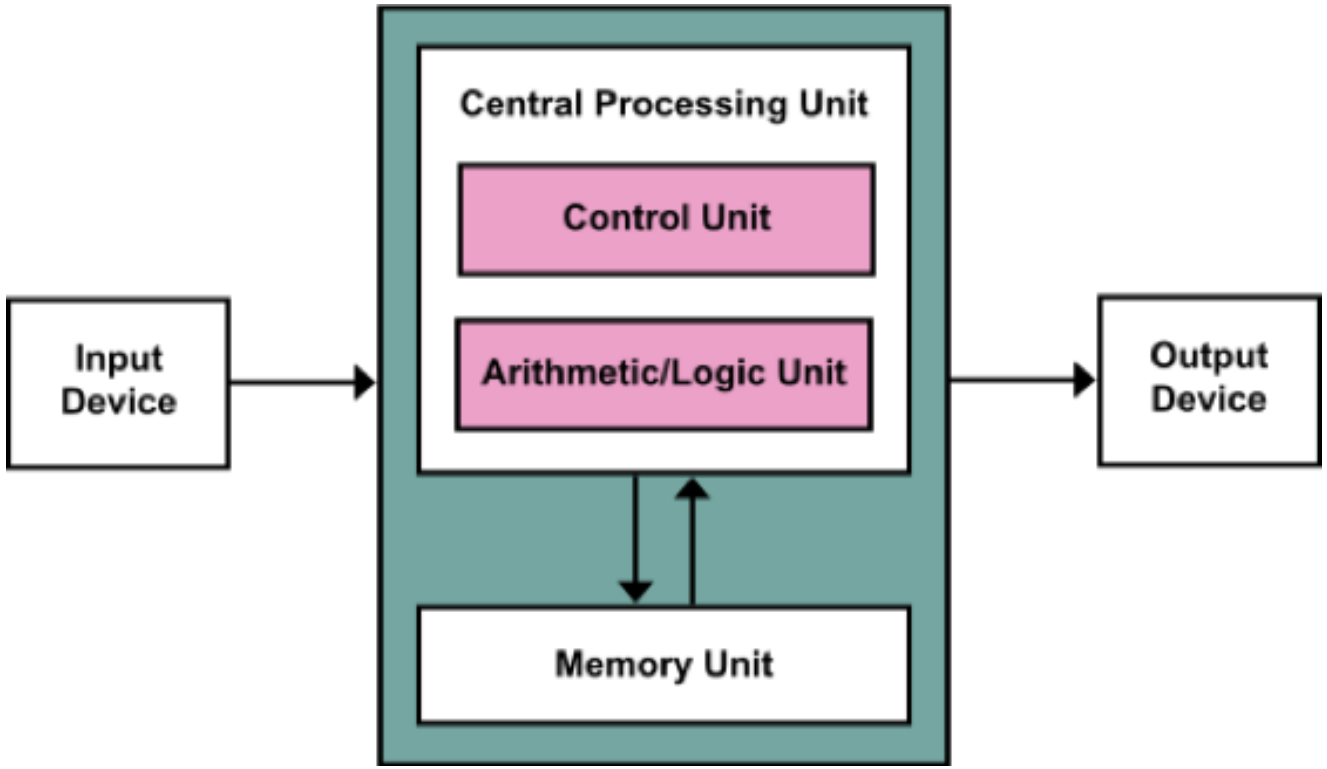
- Based on **stored-program** concept (as opposed to fixed-program)

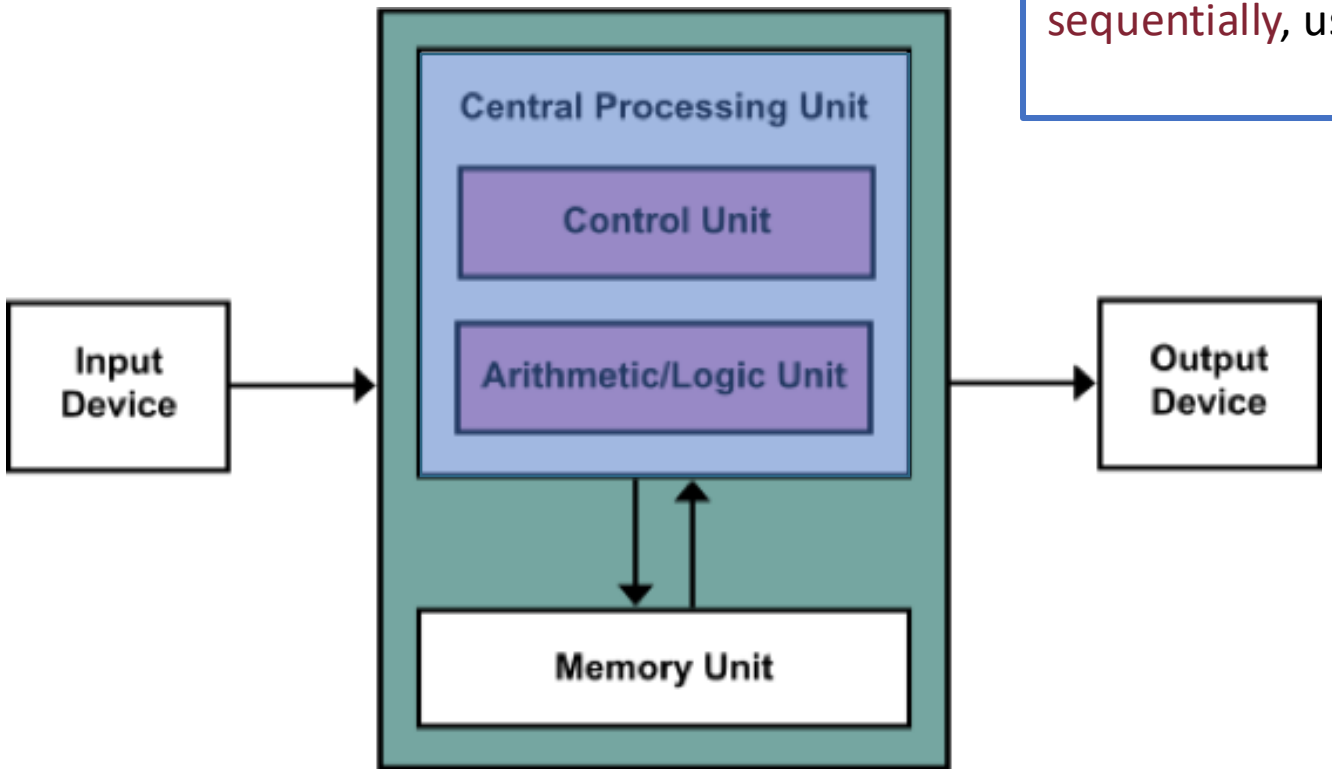
John von Neumann

von Neumann Architecture



von Neumann Architecture

Executes instructions (i.e., basic arithmetical/logical computations) sequentially, using internal registers



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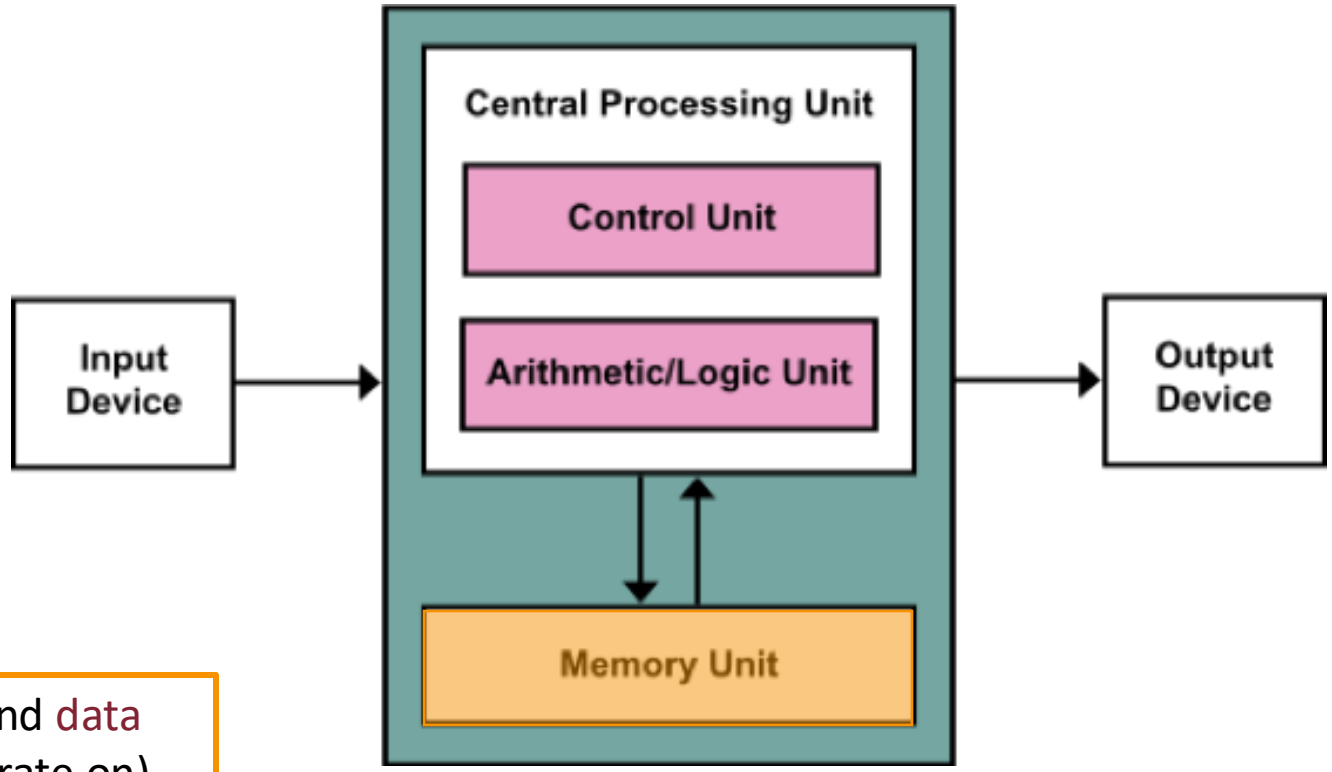

Contains instructions and data
(which instructions operate on)

Central Processing Unit

(CPU)

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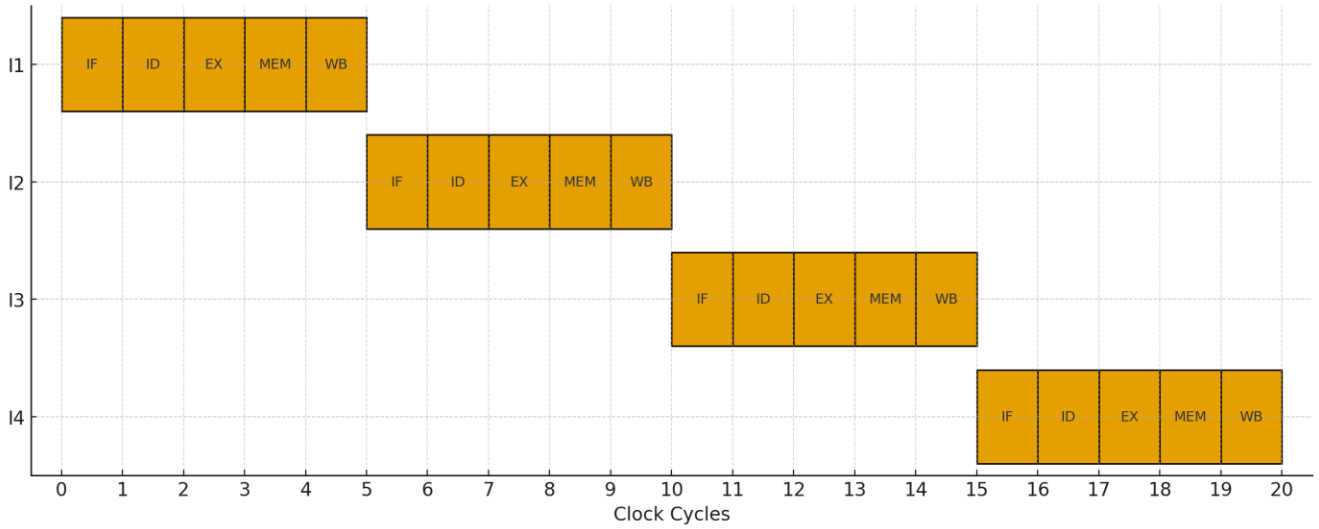

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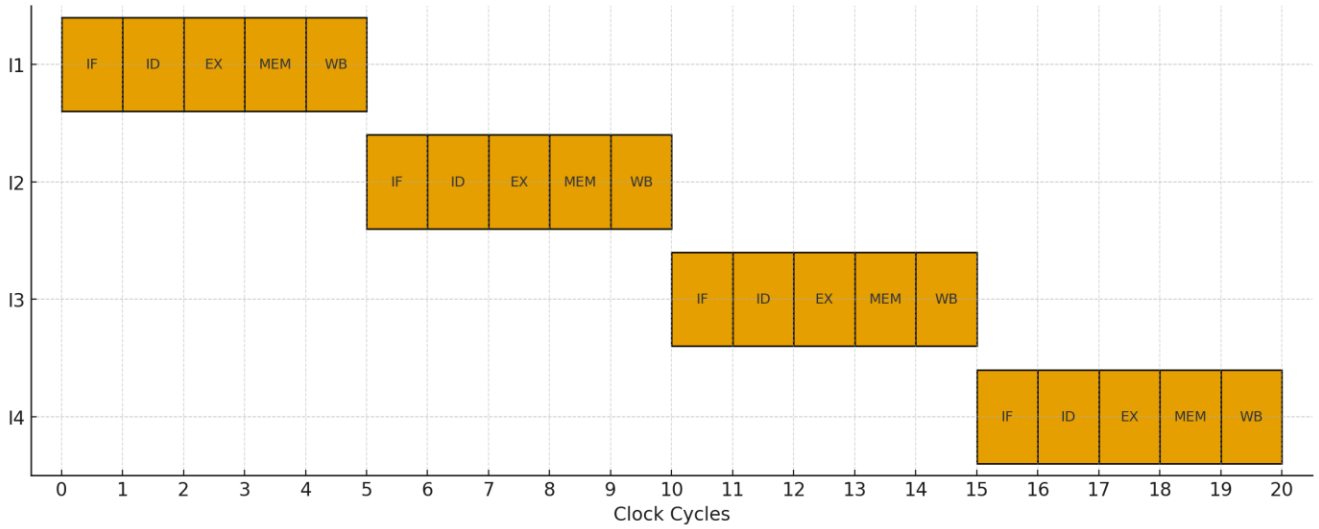

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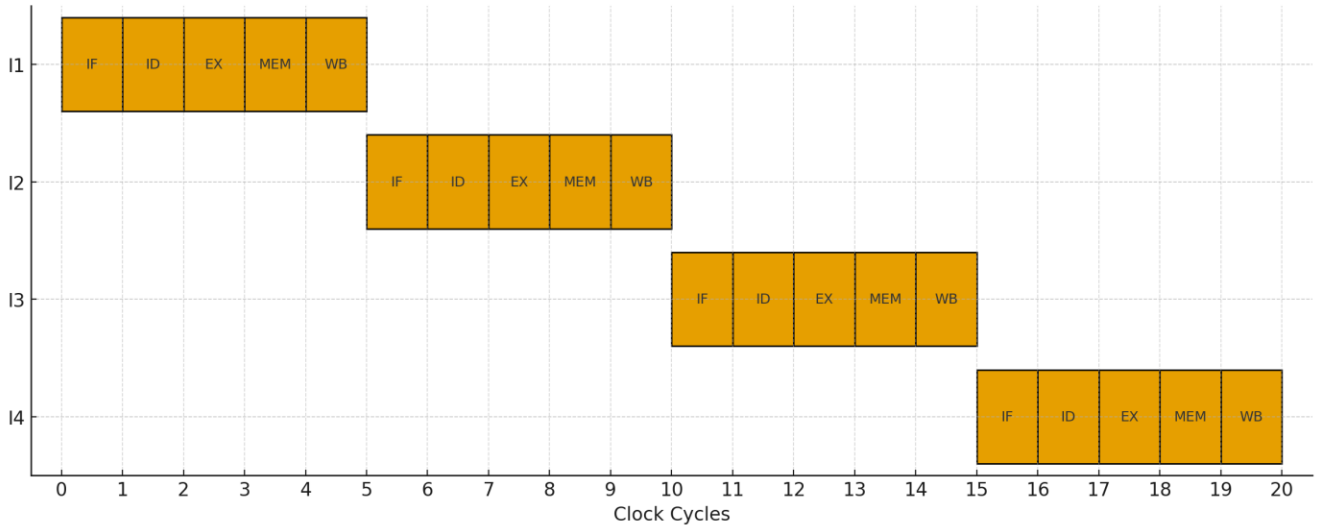

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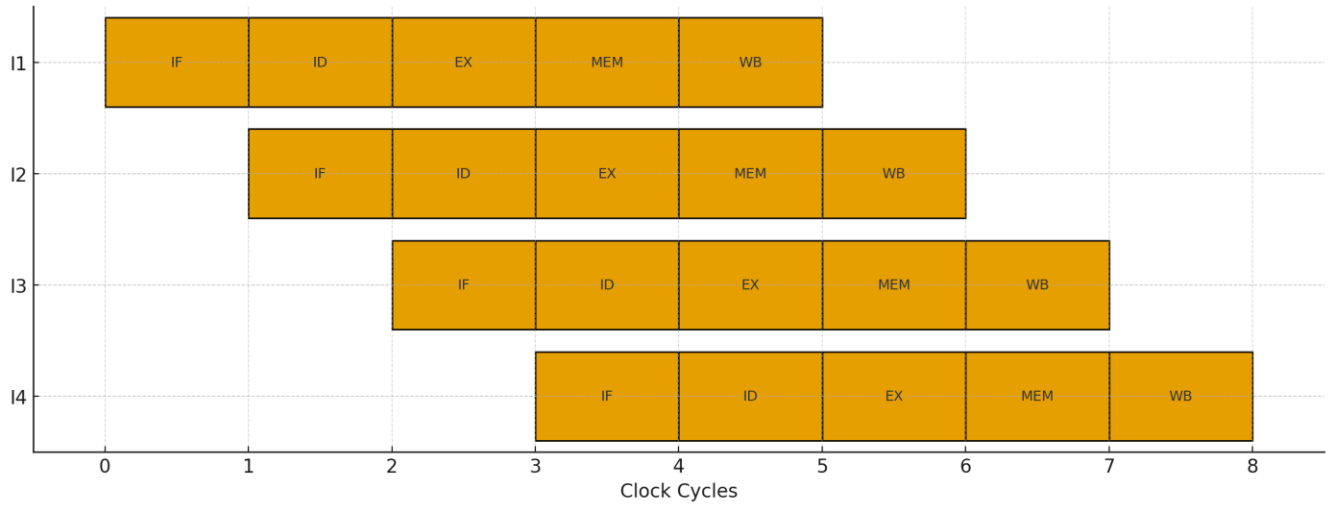
5 Cycles per Instruction (CPI)

Instruction Cycle: Pipelined



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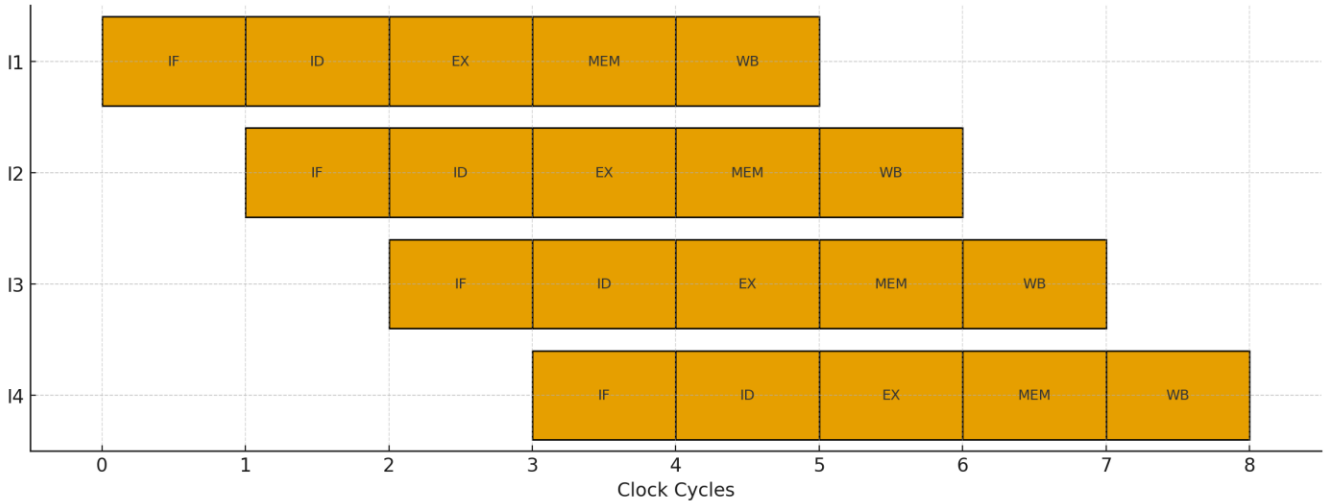

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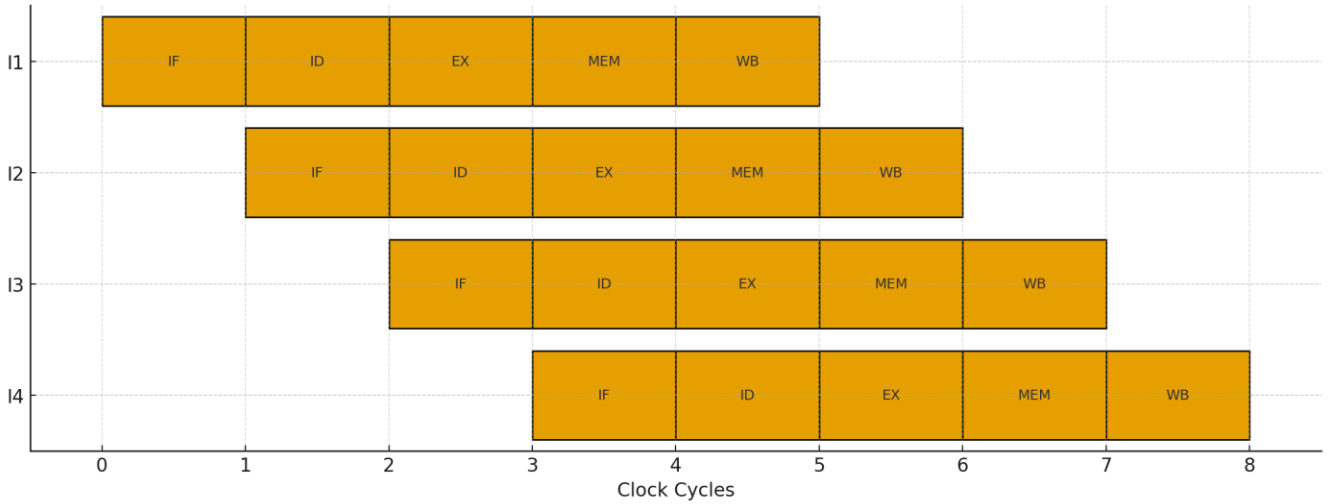

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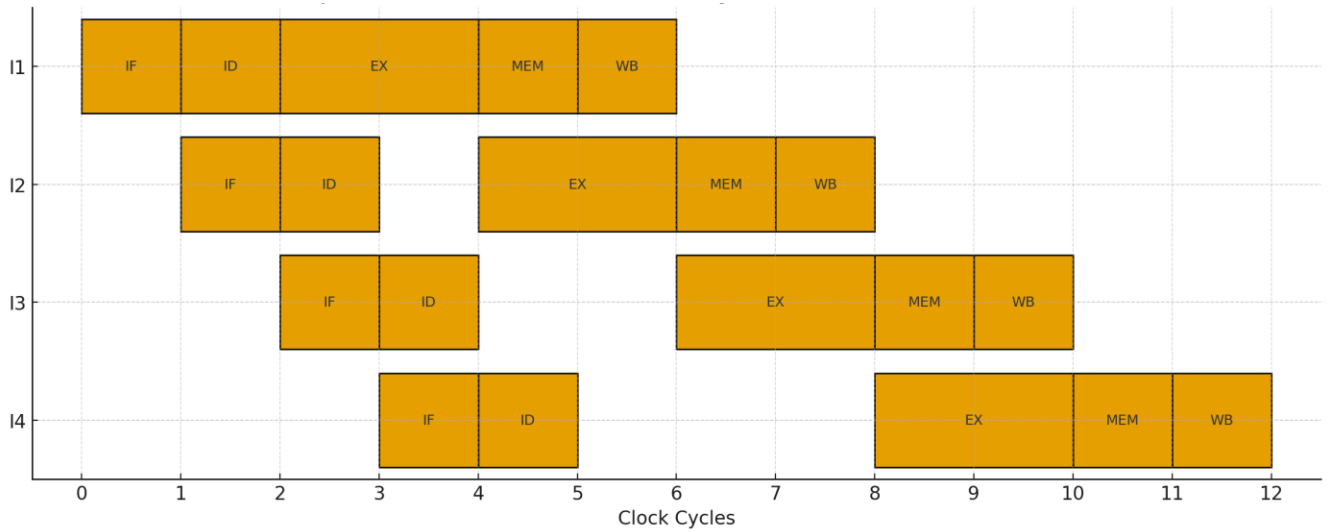
1 Cycle per Instruction (CPI) on average

Instruction Cycle: Pipelined (v.2)



4 instructions: I1,… I4

Each stage runs **in parallel** whenever possible or **wait**

Each stage may take more than one clock cycle (e.g., EX takes two!)

2 Cycles per Instruction (CPI) on average

Machine Language

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- Each instruction is encoded as a **sequence of bits**
  - A single bit is the smallest unit of (digital) information
  - It takes on two possible values: 0 or 1
- A **word** is the unit of data the CPU can directly operate on
  - today ranging from 32 to 64 bits

A Side Note on Units

Prefixes for multiples of bits (bit) or bytes (B)

Decimal				Binary				
Value		SI		Value		IEC		JEDEC
1000	10^3	k	kilo	1024	2^{10}	Ki	kibi	K kilo
1000^2	10^6	M	mega	1024^2	2^{20}	Mi	mebi	M mega
1000^3	10^9	G	giga	1024^3	2^{30}	Gi	gibi	G giga
1000^4	10^{12}	T	tera	1024^4	2^{40}	Ti	tebi	–
1000^5	10^{15}	P	peta	1024^5	2^{50}	Pi	pebi	–
1000^6	10^{18}	E	exa	1024^6	2^{60}	Ei	exbi	–
1000^7	10^{21}	Z	zetta	1024^7	2^{70}	Zi	zebi	–
1000^8	10^{24}	Y	yotta	1024^8	2^{80}	Yi	yobi	–

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- Machine language instructions are made of **2 parts**:
  - An **operator** (op code)
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- An **abstraction** of the underlying physical (hardware) architecture (e.g., x86, ARM, SPARC, MIPS, etc.)

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  - `eax`, `ebx`, `ecx`, etc.
- Special-purpose (x86):
  - `esp` → Stack pointer for top address of the stack
  - `ebp` → Stack base pointer for the address of the current stack frame
  - `eip` → Instruction pointer, holds the program counter (i.e., the address of next instruction)

Single- vs. Multi-Processor

Single-Processor Systems

- One main CPU for executing programs
- Other dedicated processors that do not run programs (e.g., disk controllers, GPUs, etc.)

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- Higher resiliency to failures

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Our main focus!

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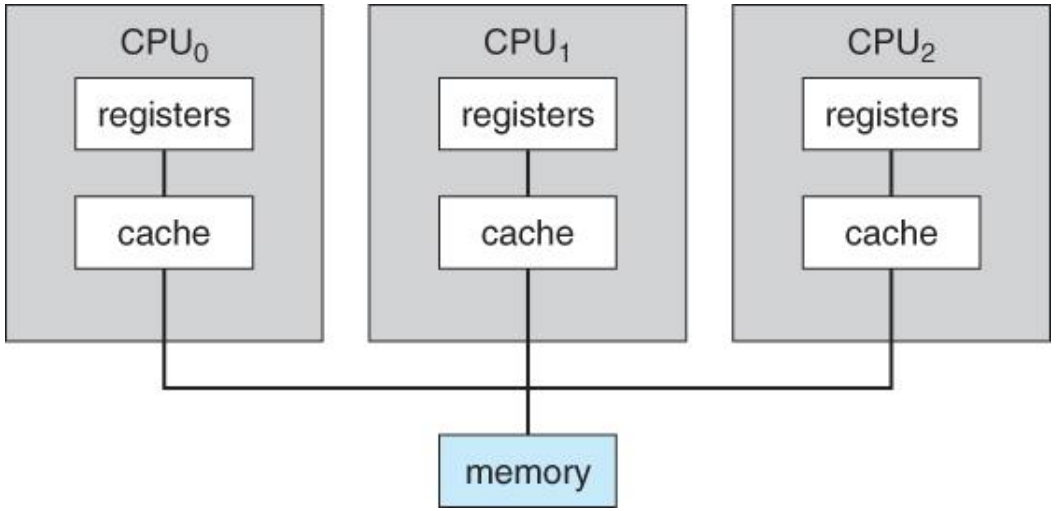
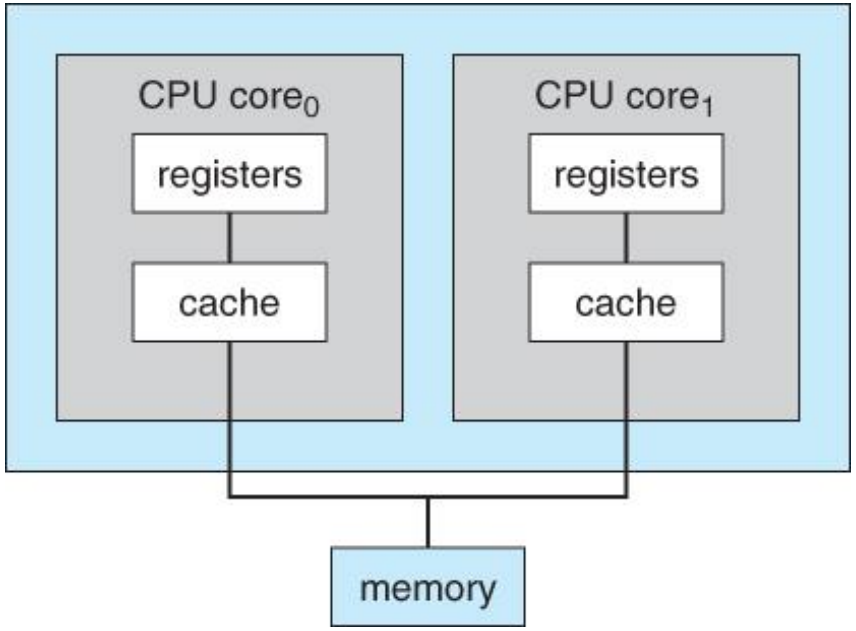
Multi-Processor Systems: Examples

Symmetric Multiprocessing Architecture

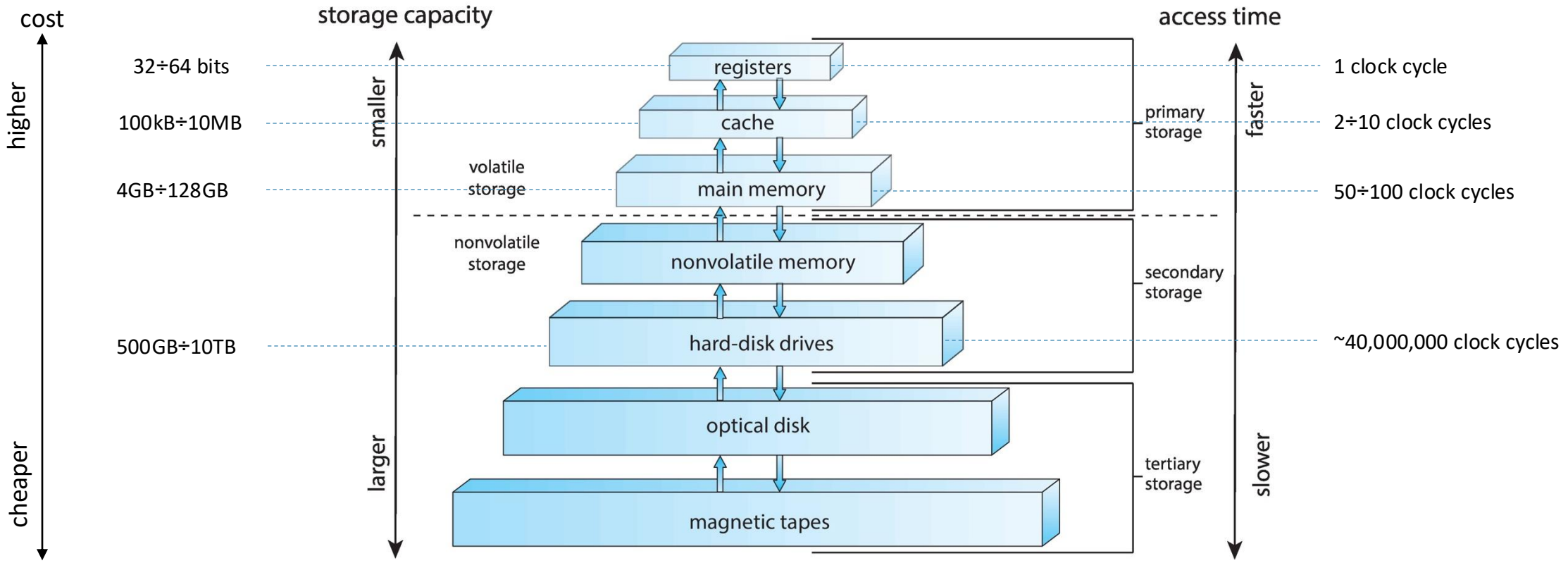


Multicore Architecture



Memory

Memory Hierarchy



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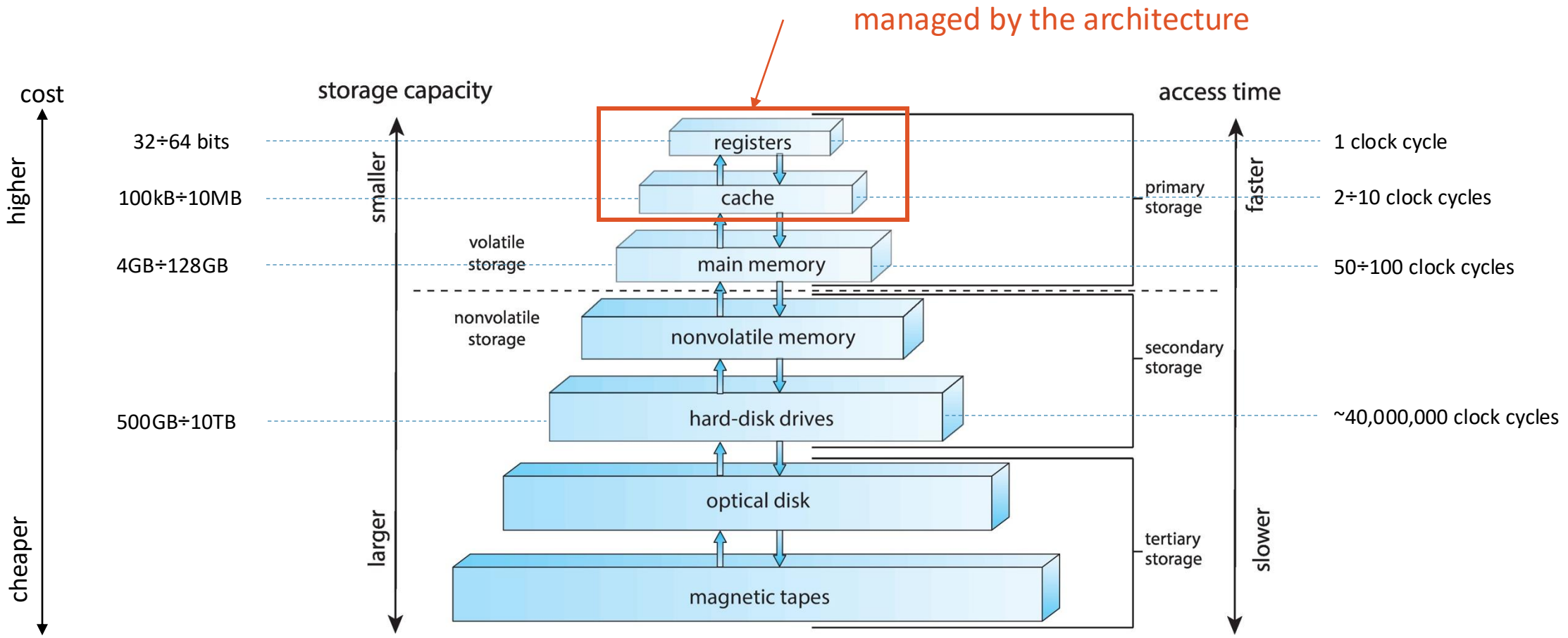

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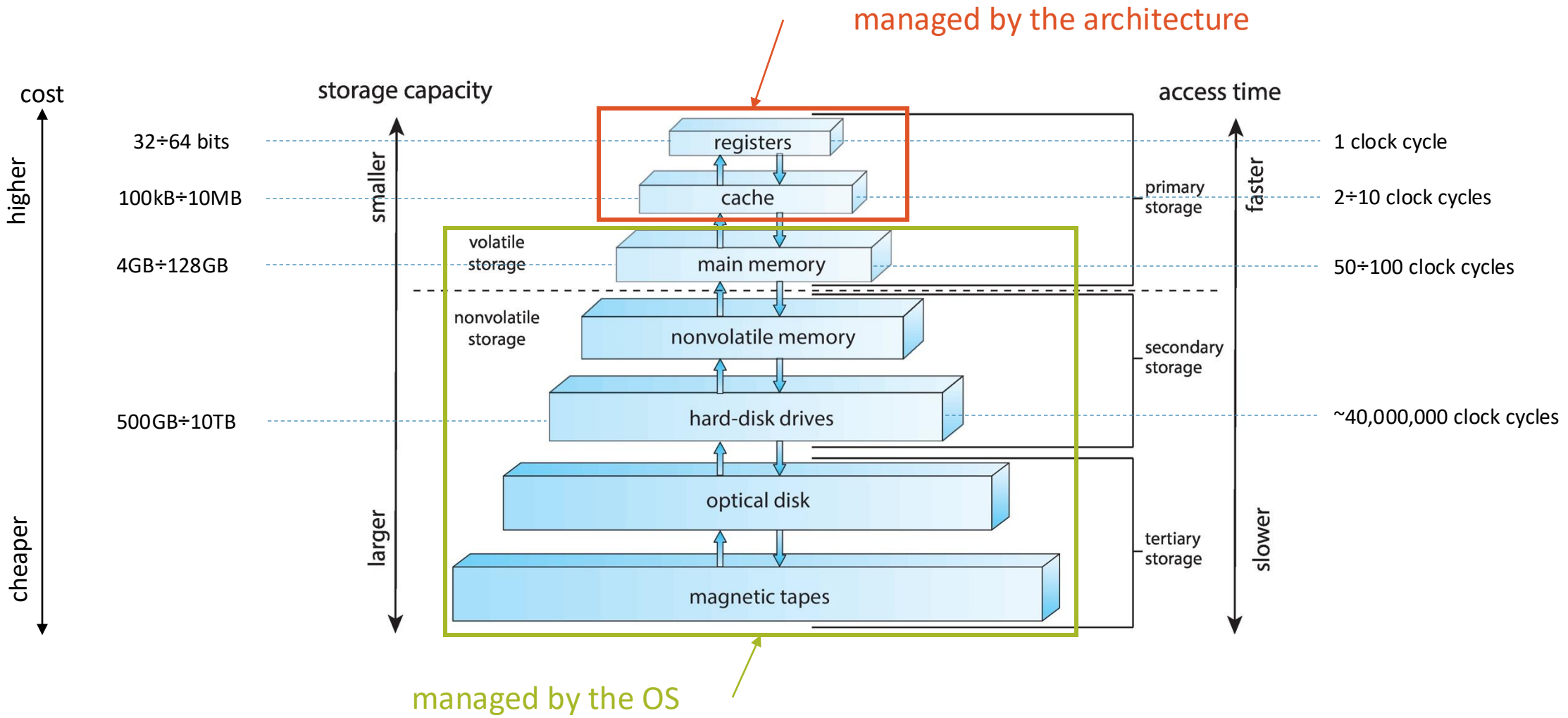

Main Memory Representation

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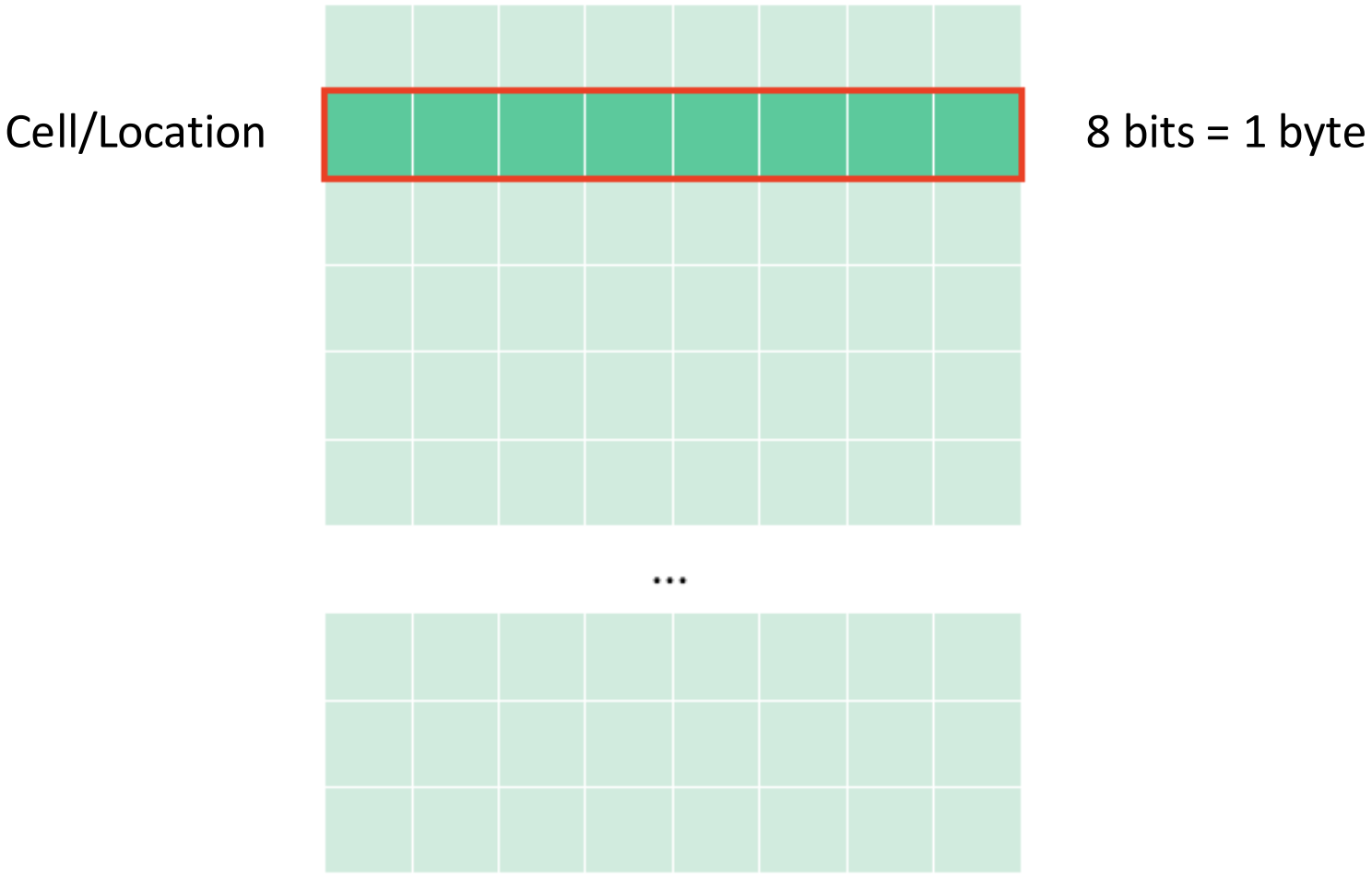
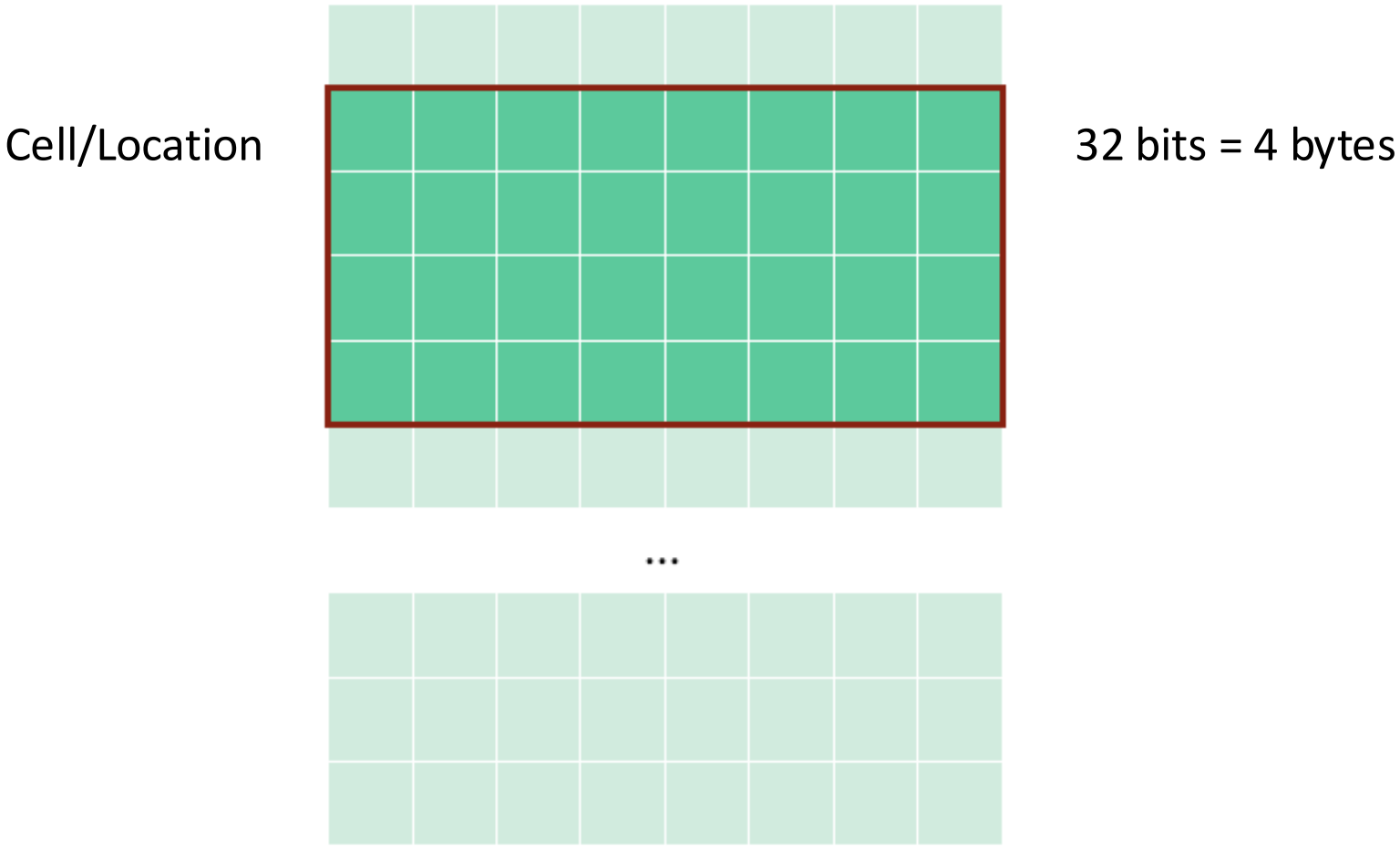
- The smallest addressable unit is usually 1 byte

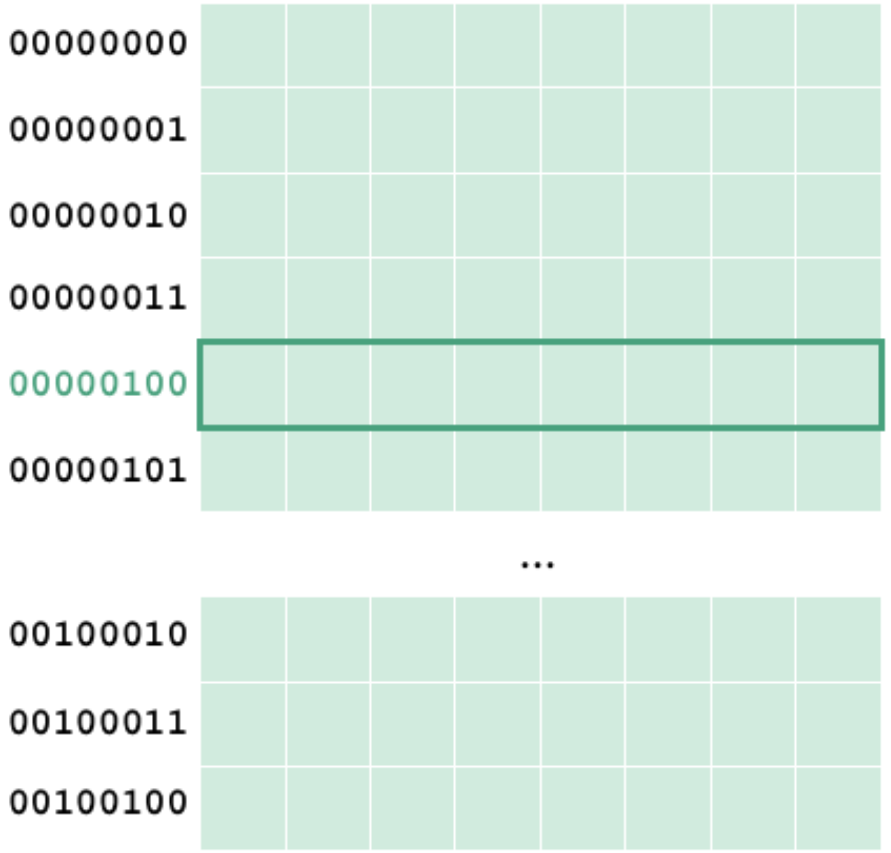
Memory Cell (1)



Memory Cell (2)



Memory Address (Single Byte)



Computer Buses

System Bus

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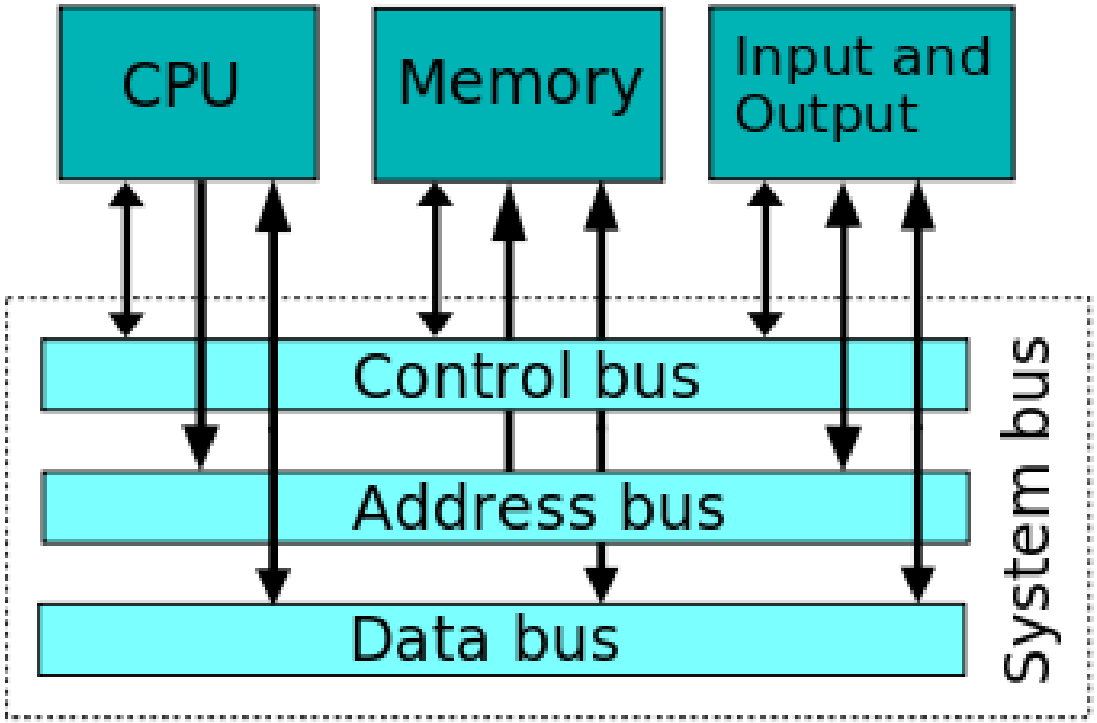
- More dedicated buses have been added to manage CPU-to-memory and I/O traffic
  - PCI, SATA, USB, etc.

System Bus


CPU
Memory
Input and Output
Control bus
Address bus
Data bus
System bus

I/O Devices

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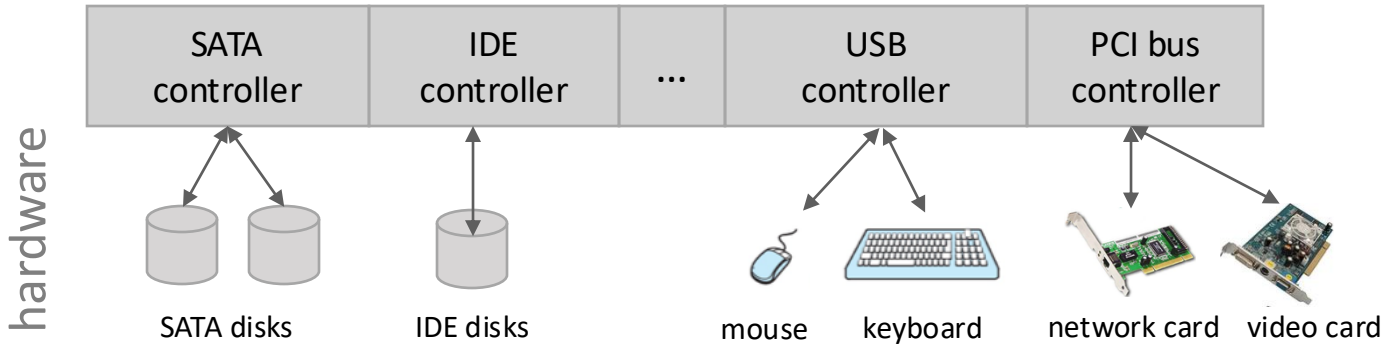
- OS talks to a device controller using a specific **device driver**

Device Drivers: OS Abstraction



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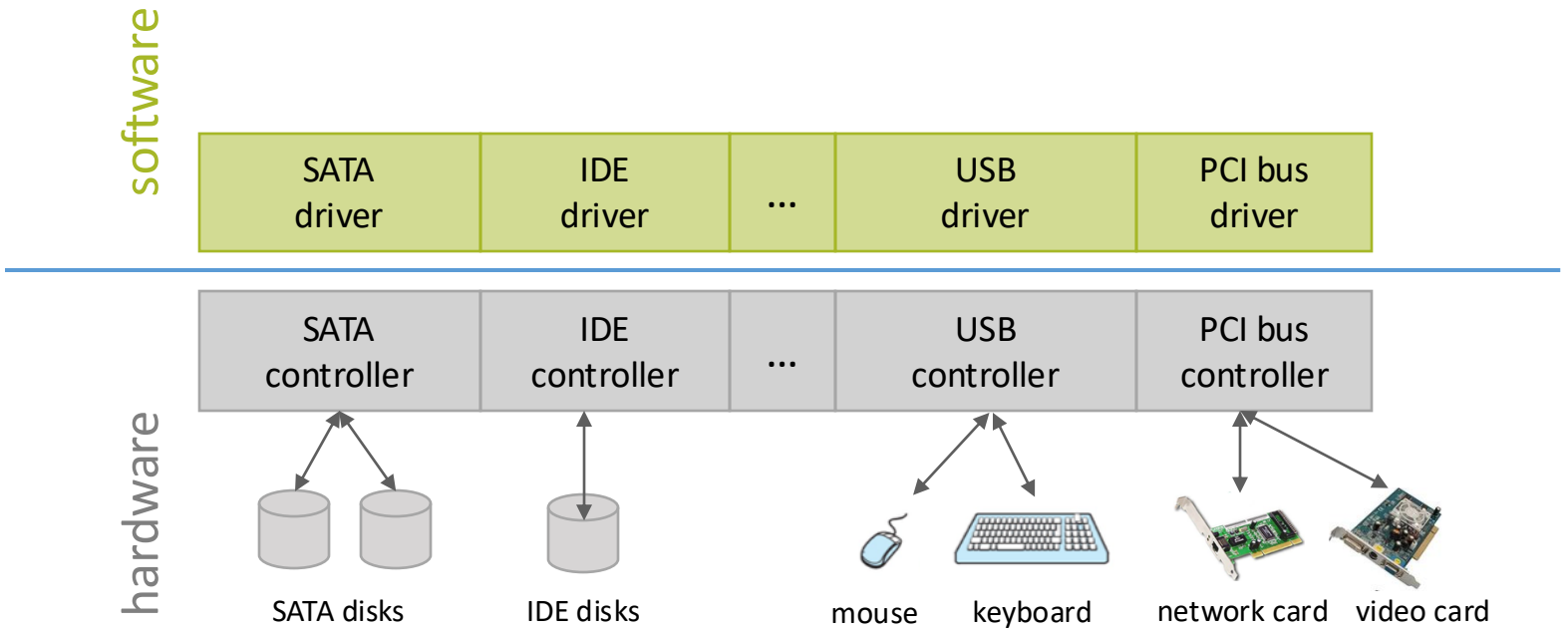

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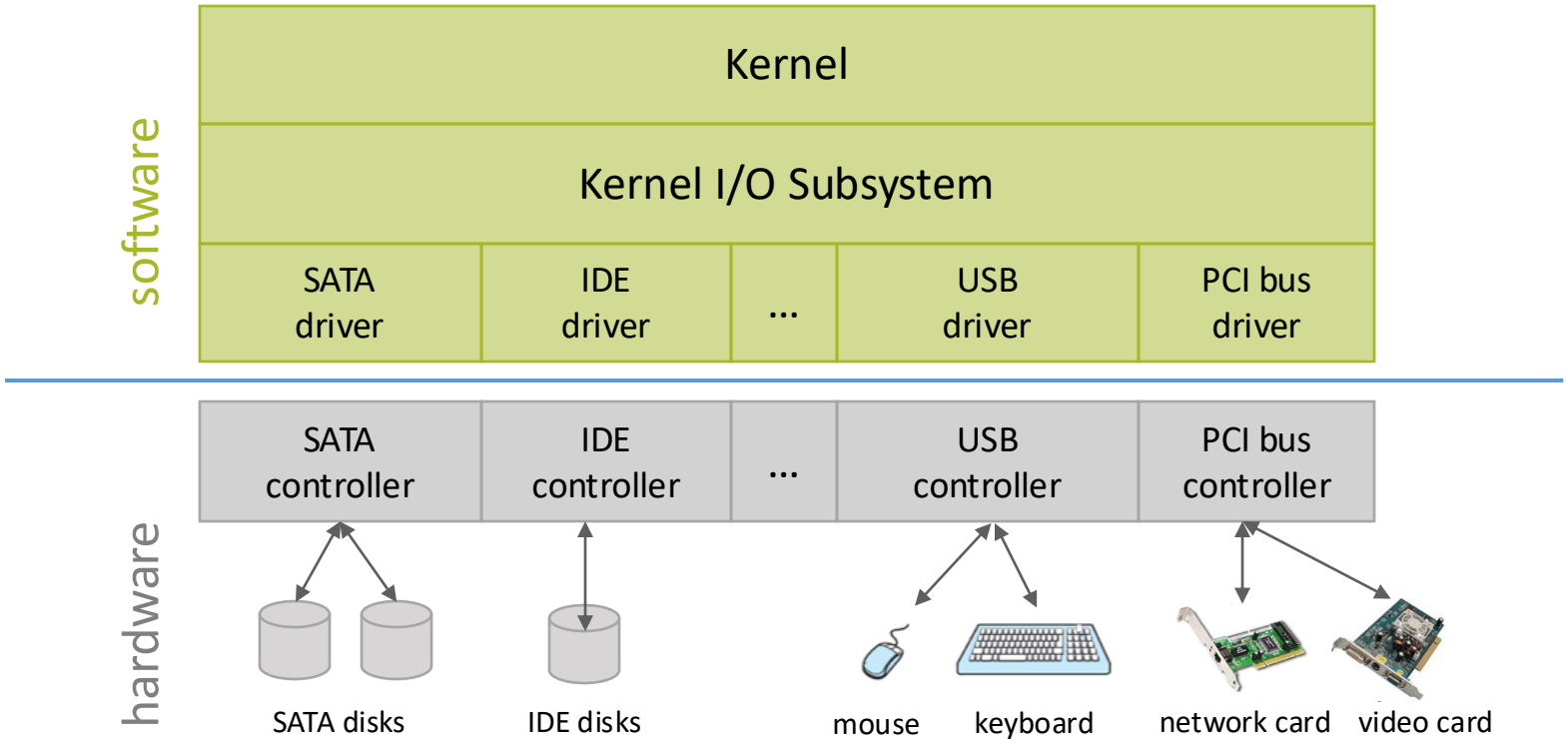

Device Controllers

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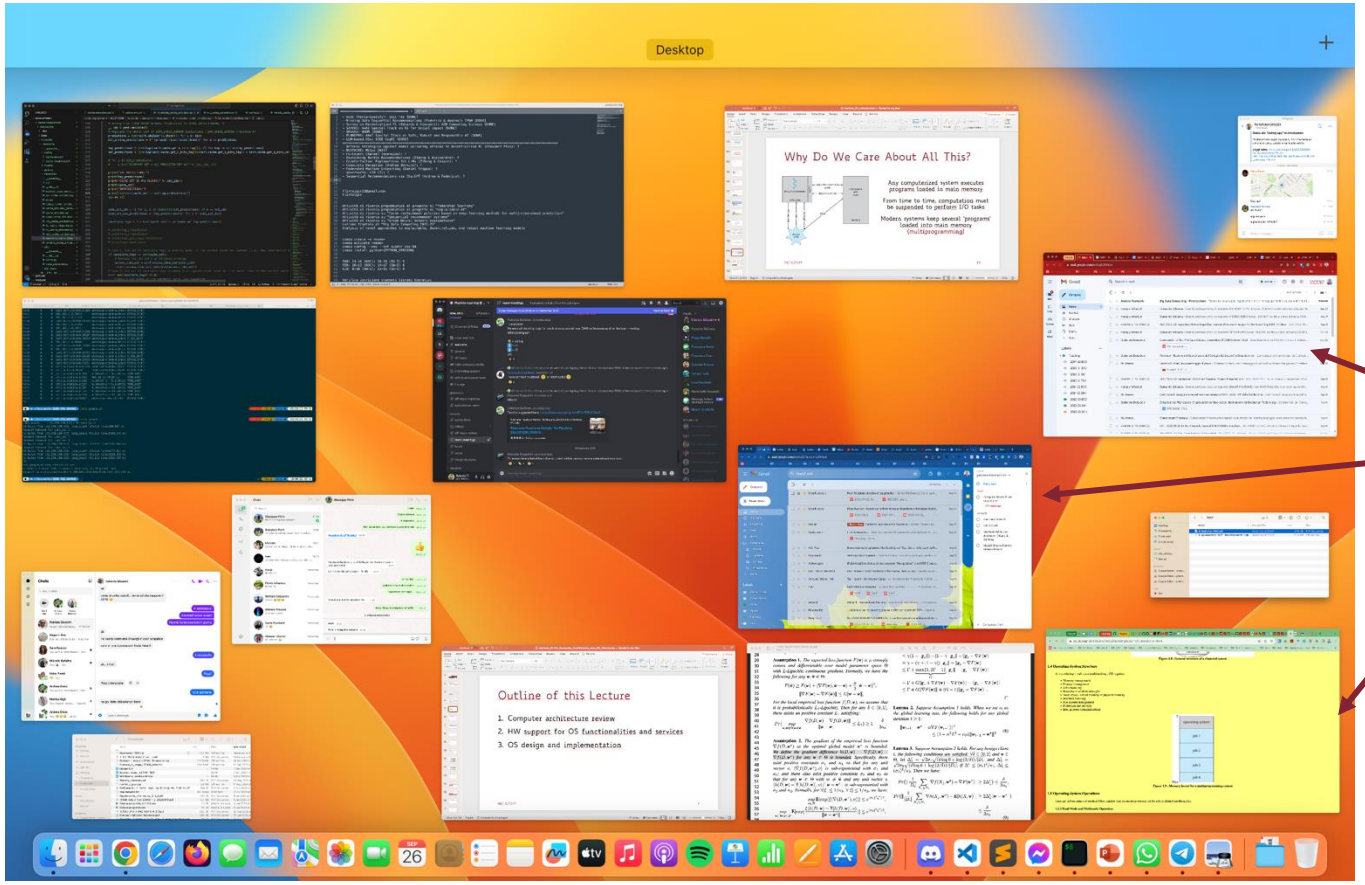
  - **Data registers** → used to read data from or send data to the I/O device

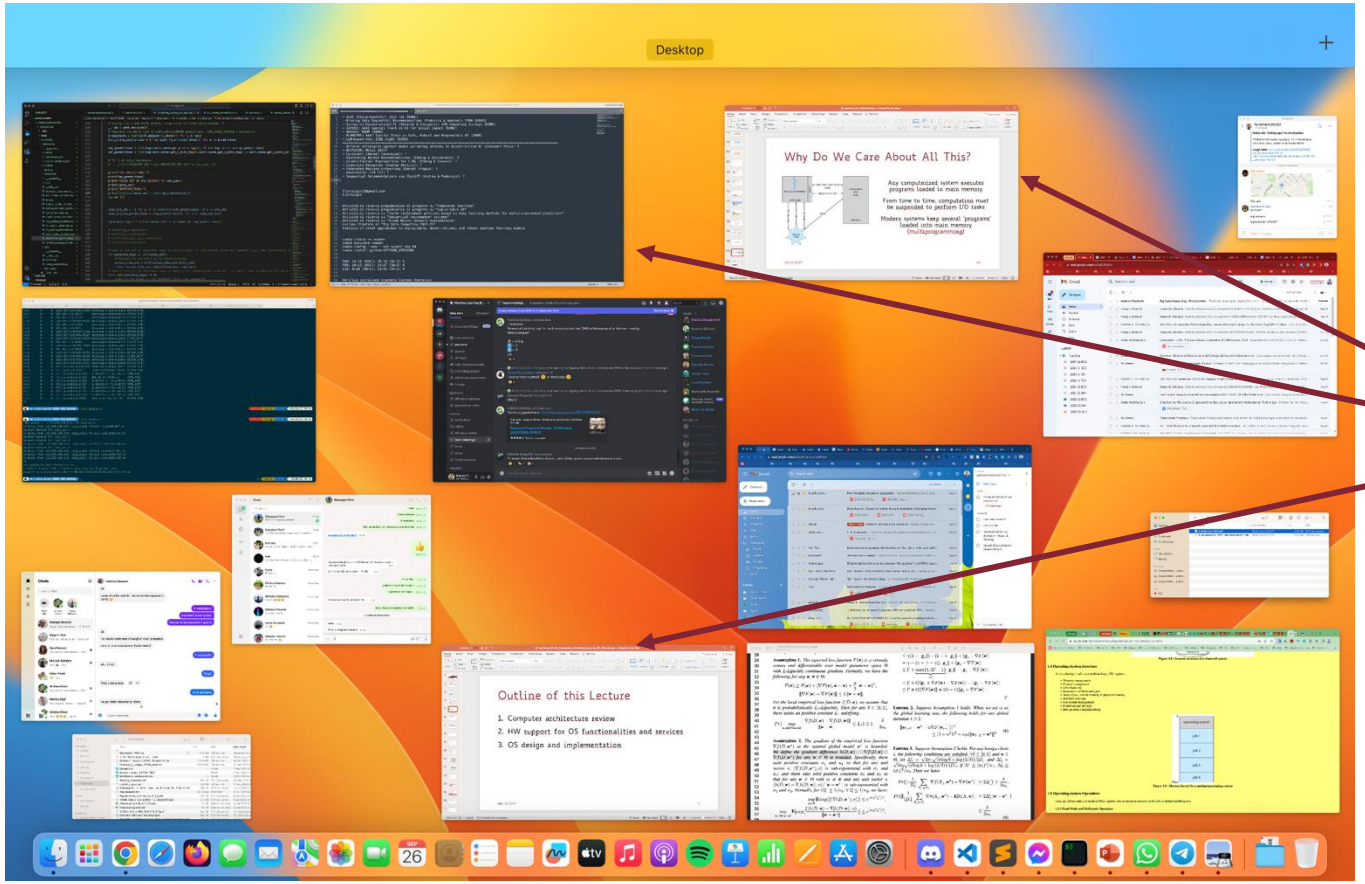
Modern Computer Systems

Many User Applications Running



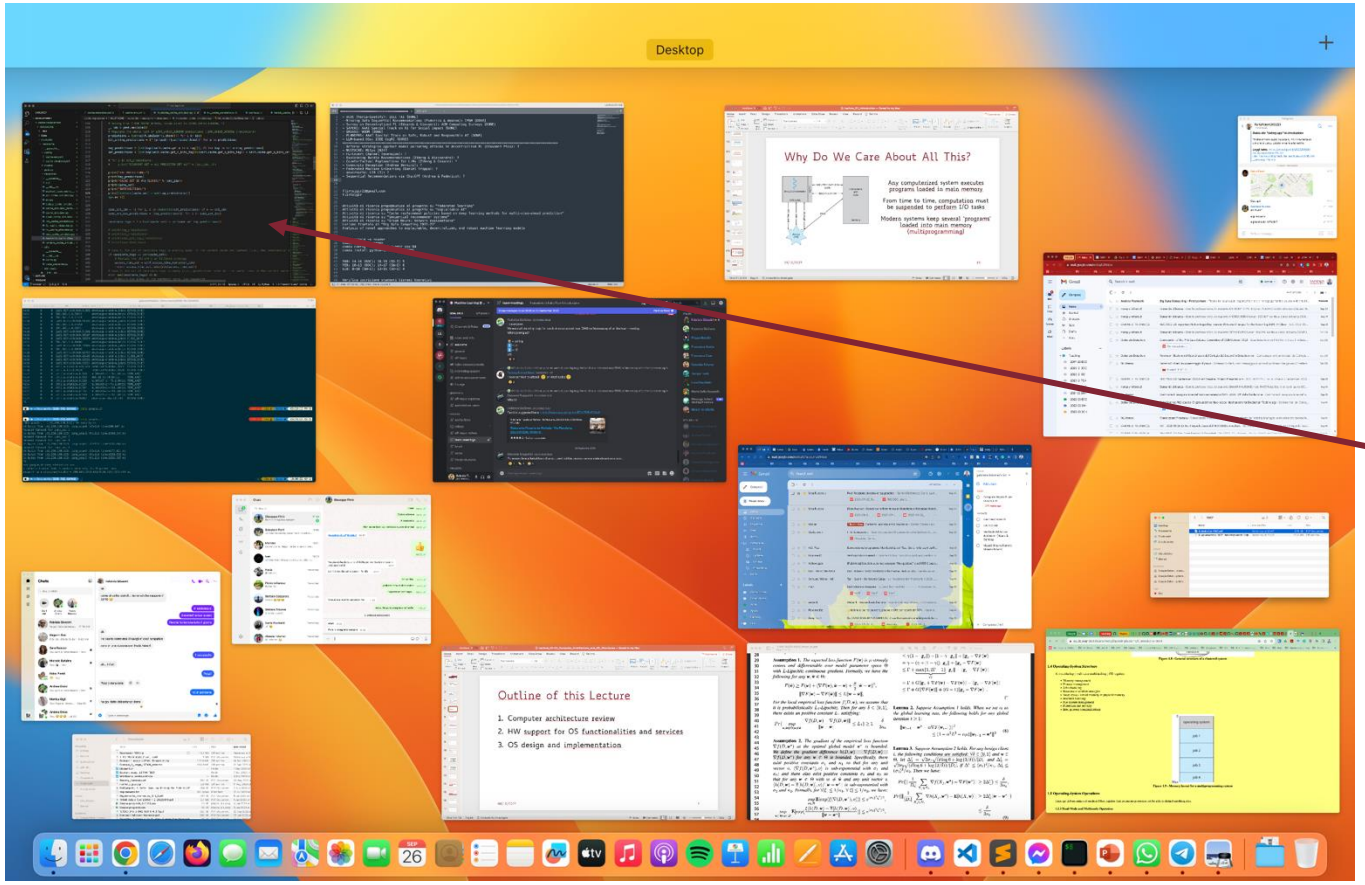
Web Browsers

Many User Applications Running



Text Editors

Many User Applications Running



IDE
(code development)

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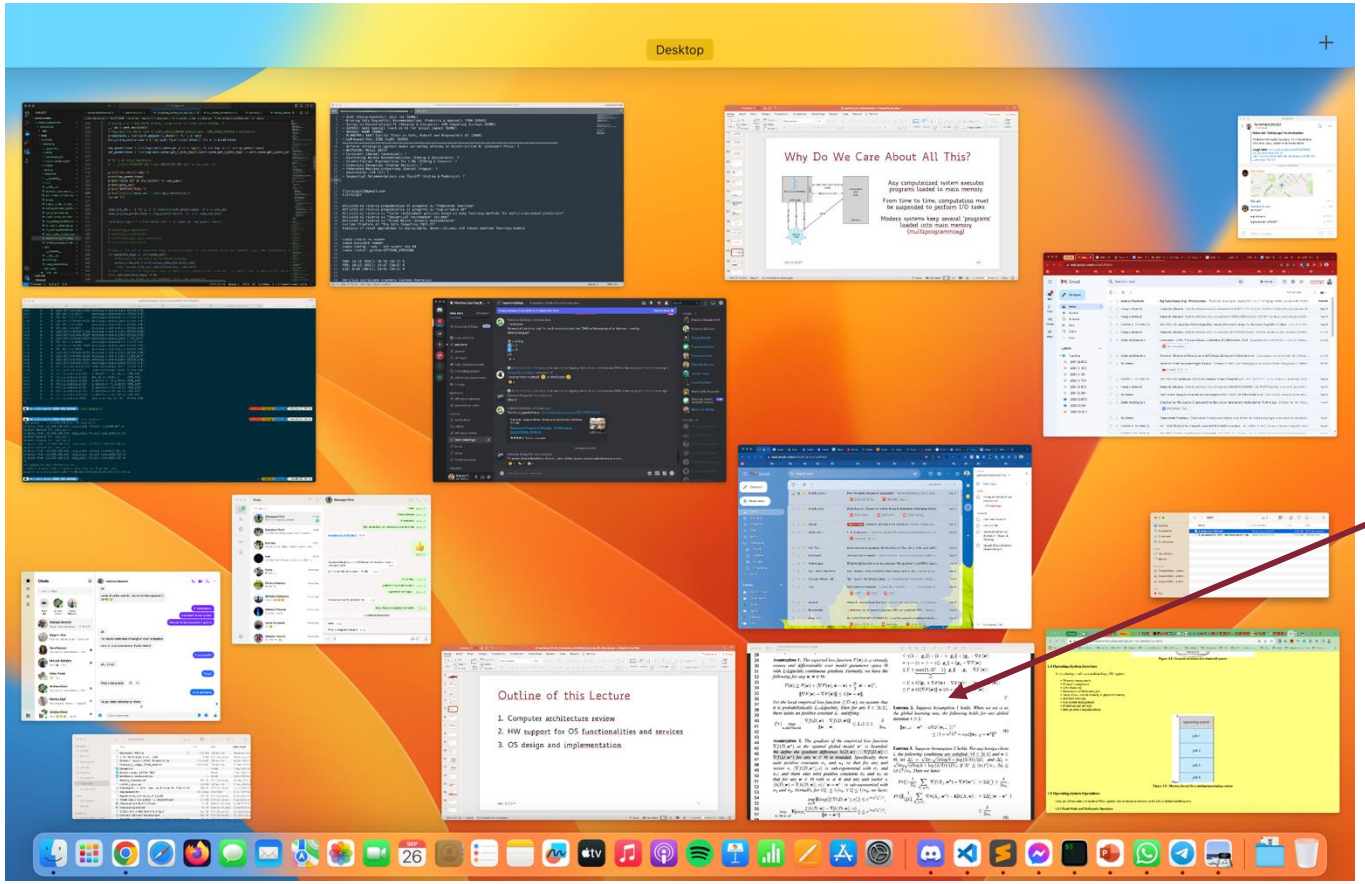
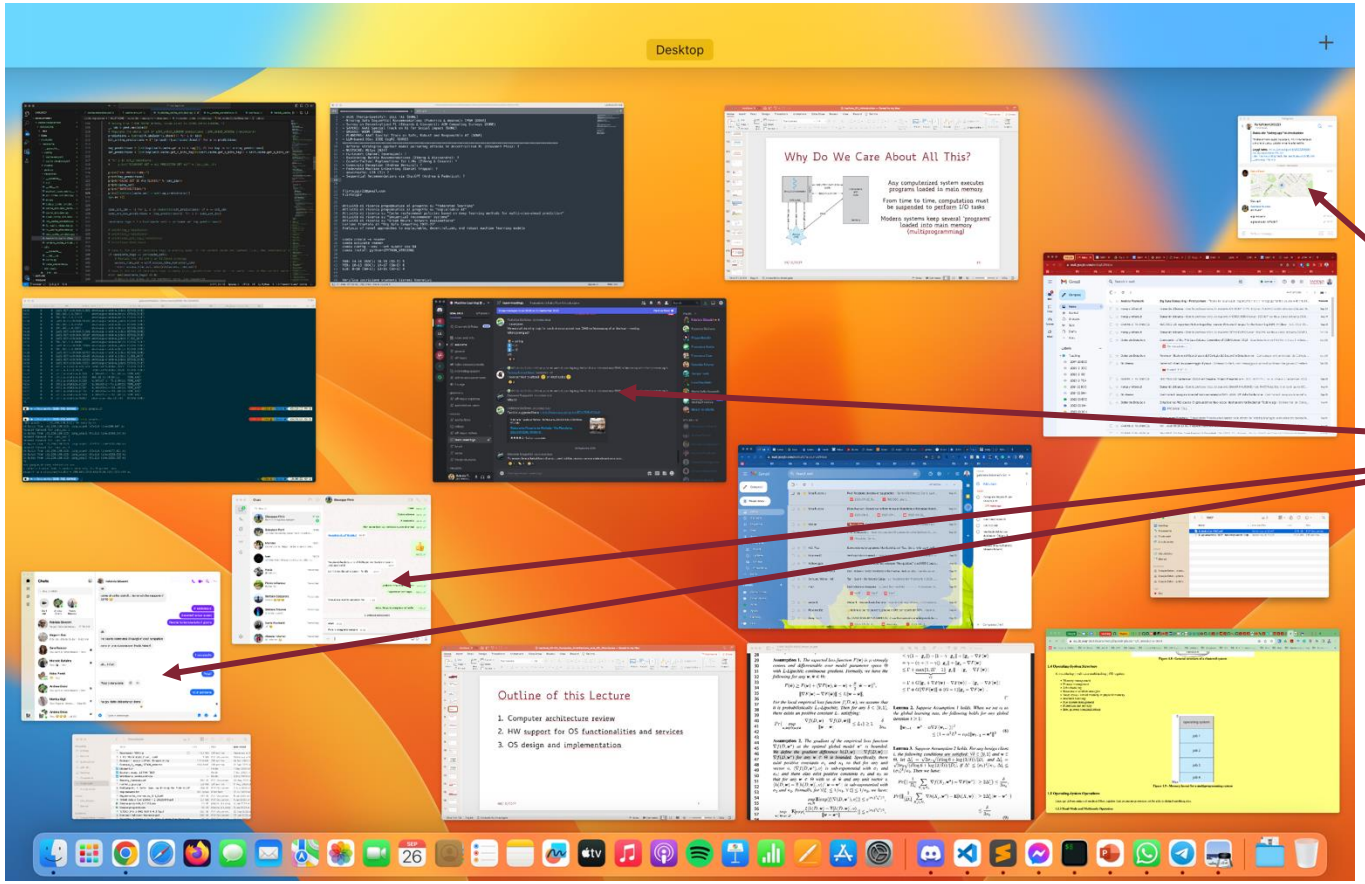


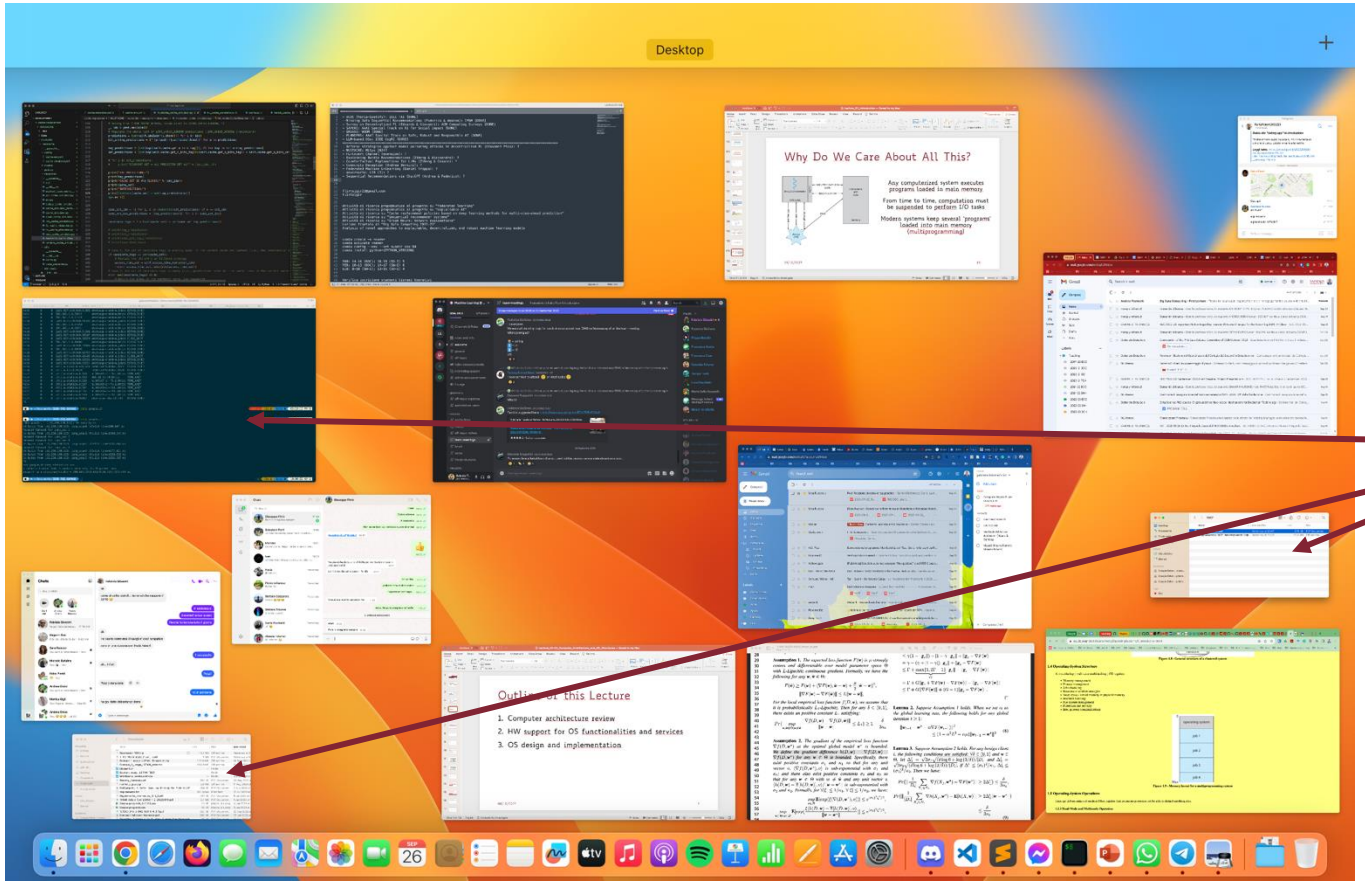
PDF Viewer

Many User Applications Running



Messaging

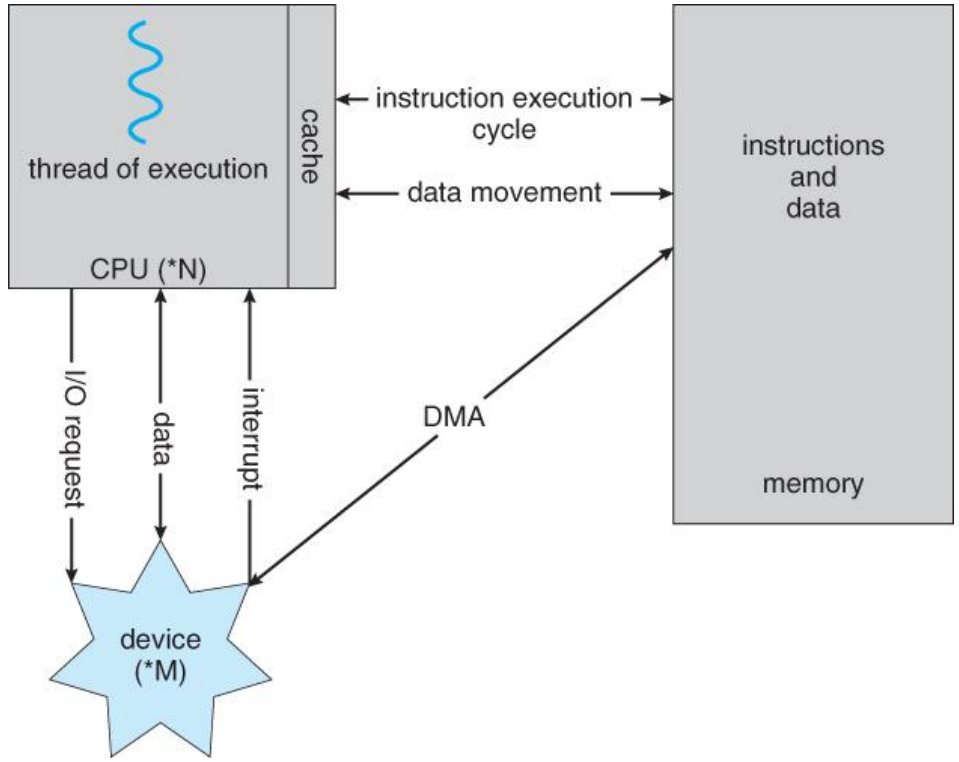
Many System Programs Running



Finder/Shell

Not Just Laptops/PCs…

Why Do We Care About All This?

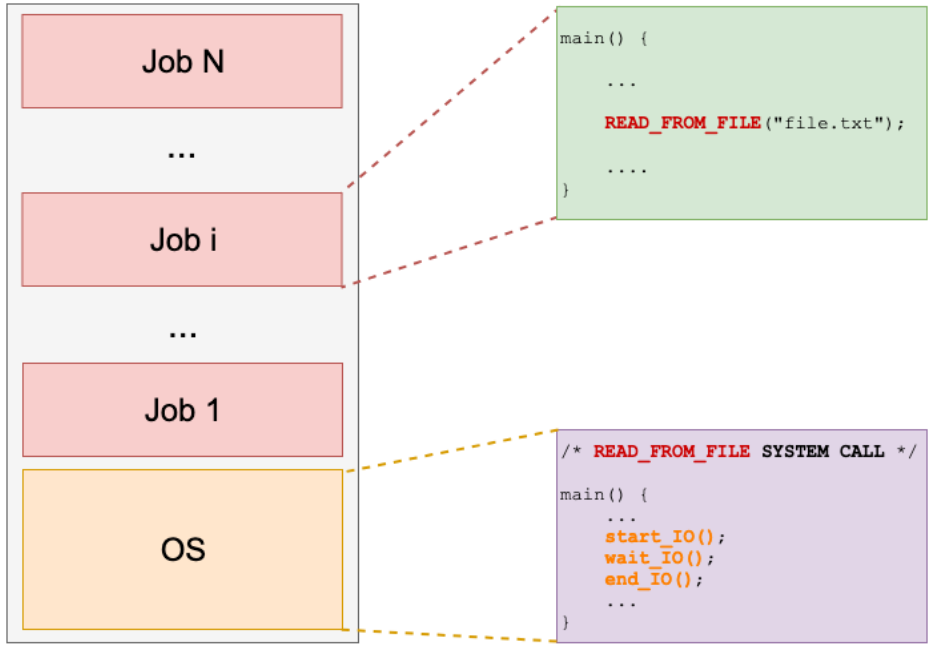


Any computerized system executes programs loaded in main memory

From time to time, computation must be suspended to perform I/O tasks

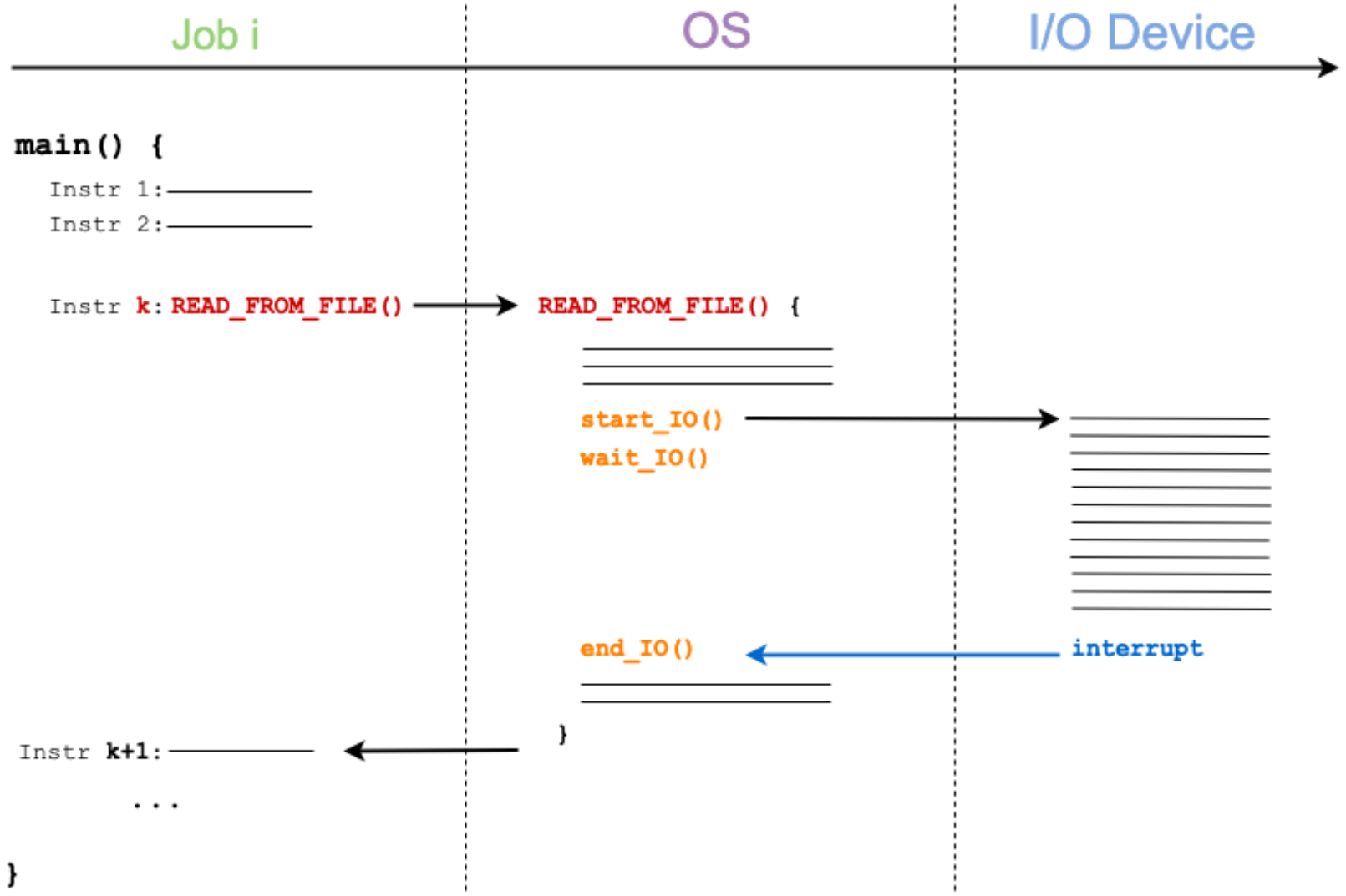
Modern systems keep several "programs" loaded into main memory (**multiprogramming**)

Multiprogramming Systems (1960s)

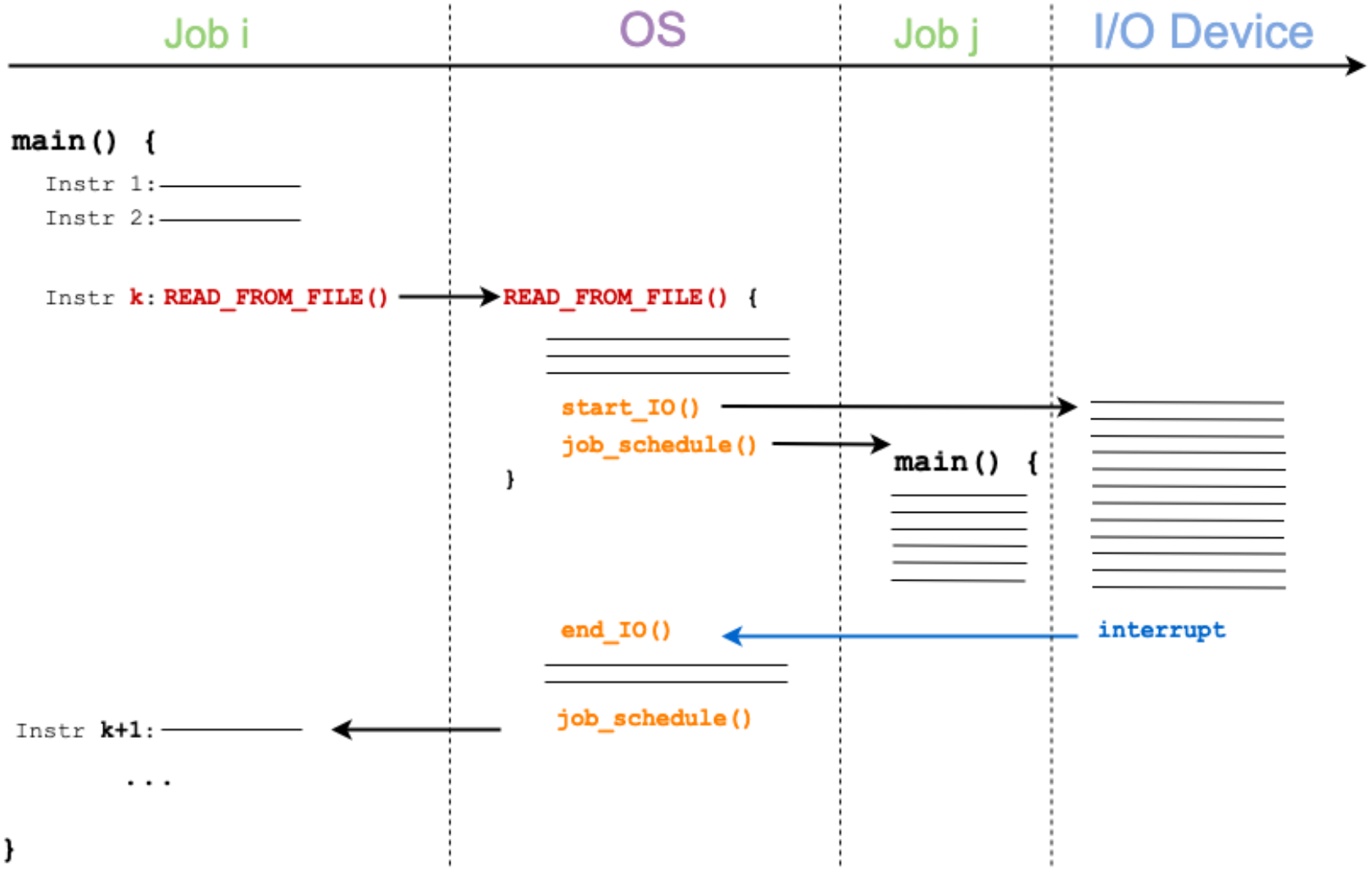


- Keep several jobs loaded in memory
- Multiplex CPU between jobs
- OS responsibilities:
  - job scheduling
  - memory protection
  - I/O operations
- **Problem:** CPU is left idle while blocking I/O operations take place

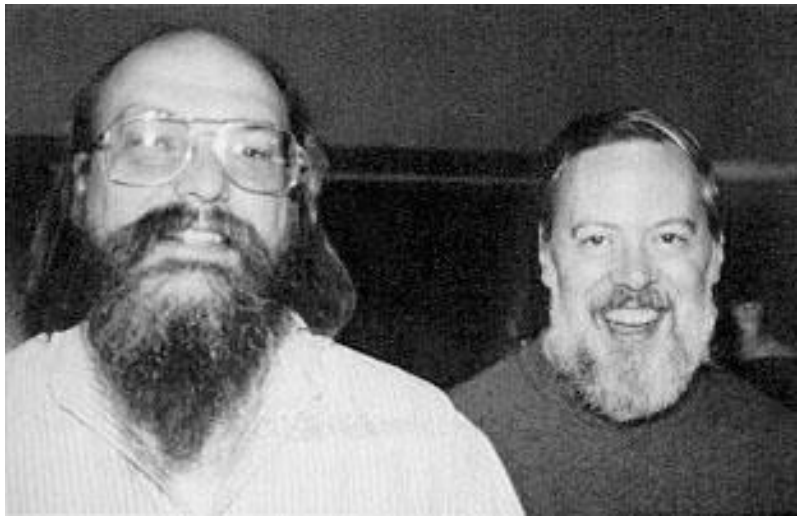
Blocking System I/O



Non-Blocking System I/O

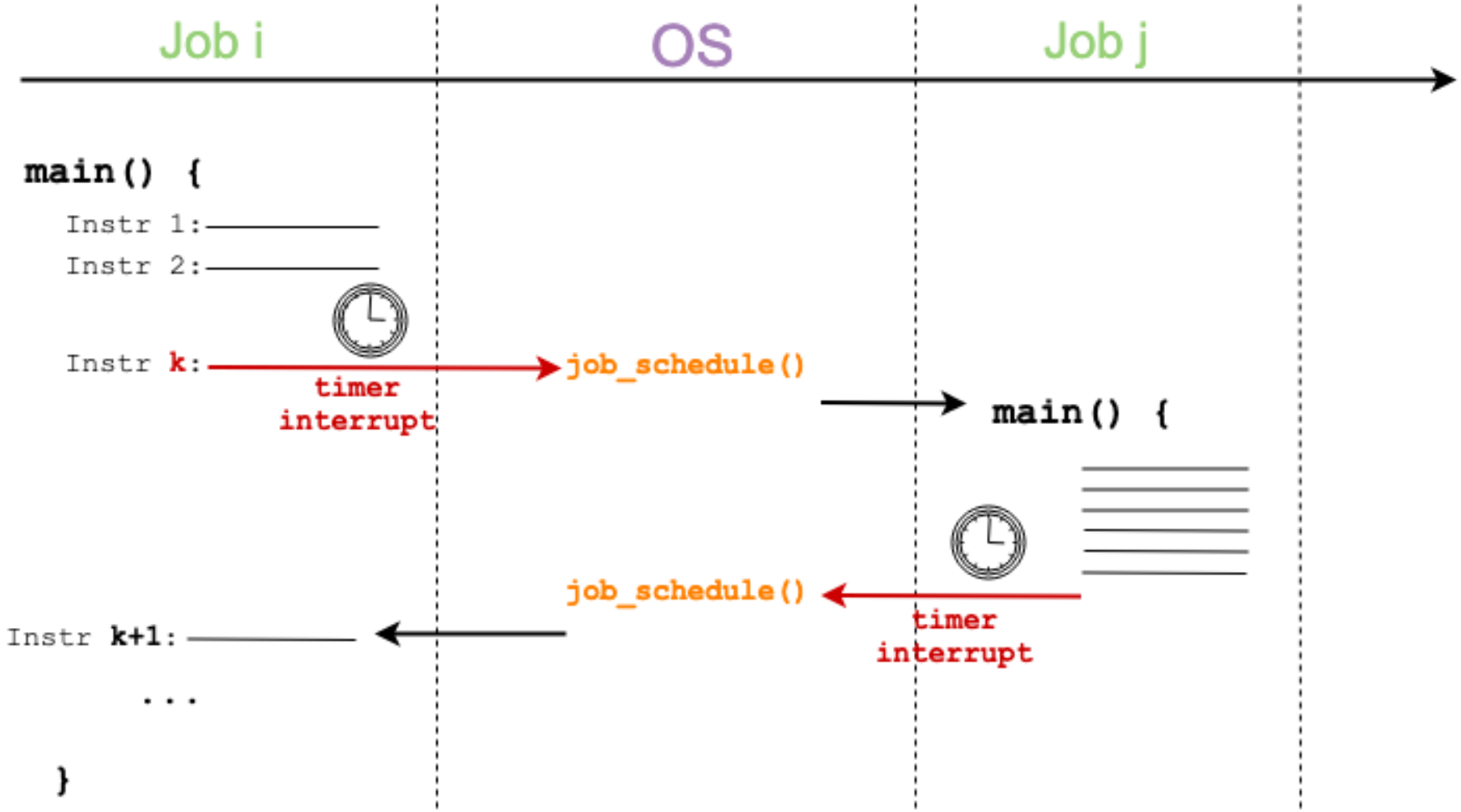


Time-sharing Systems (1970s)



- Many users connected to the same CPU via cheap consoles
- Timer interrupt used to multiplex CPU between jobs
- Illusion of parallelism (pseudo-parallelism)
- Ken Thompson&Dennis Ritchie → **UNIX OS**

Pseudo-parallelism



New Trends in OS Design

- Active field of research
  - OS demand is growing (many computing devices are available)
  - New application settings (Web, Cloud, mobile, cars, etc.)
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  - New application settings (Web, Cloud, mobile, cars, etc.)
  - Hardware is rapidly changing (new CPUs coming out)
- Open-source OS (Linux)
  - Allows developers to contribute to OS development
  - Excellent research platform to experiment with

Why Study OSs?

- To learn important concepts of computer science
  - **Abstraction**
    - Virtualize any physical resource (CPUs, memory, I/O, etc.)

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  - **How computers work**

Large Computer Systems

- The world is increasingly dependent on computer systems
  - Large, complex, interconnected, distributed, etc.

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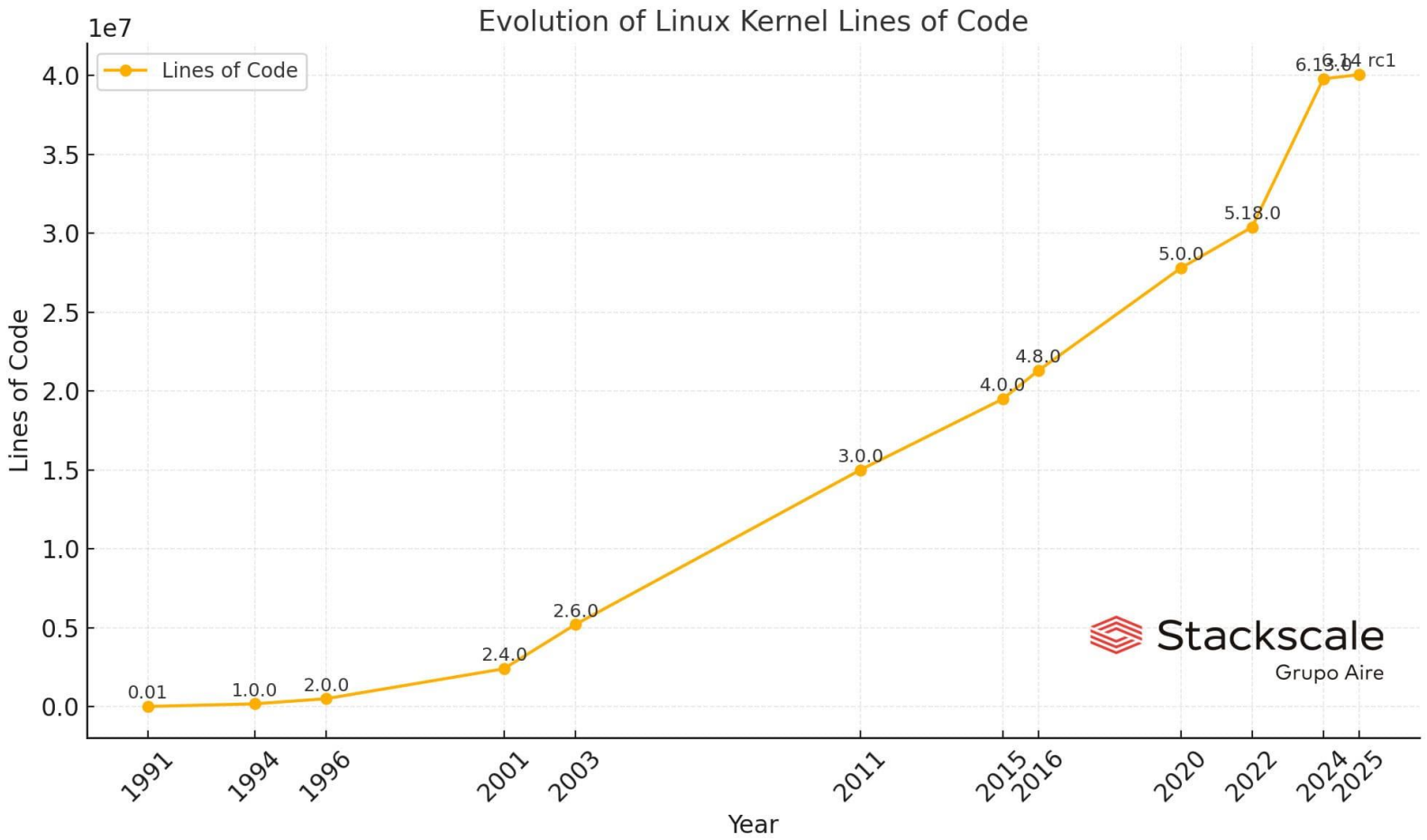
OS is a great example of a large computer system

Linux Kernel Size (Lines of Code)



~40M LoC
as of 2025!

source: https://www.stackscale.com/blog/linux-kernel-surpasses-40-million-lines-code/

OS as Large Computer System

- Designing large computer systems requires you to know
  - **Each computer:**
    - Architectural details
    - High-level programming language (mostly, C/C++)
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  - **Across clusters of computers:**
    - Server architectures
    - Distributed file systems and computing frameworks

OS Design Issues (1)

- **Structure** → How the whole system is organized
- **Concurrency** → How parallel tasks are managed
- **Sharing** → How resources are shared
- **Naming** → How resources are identified by users
- **Protection** → How critical tasks are protected from each other
- **Security** → How to authenticate, authorize, and ensure privacy
- **Performance** → How to make it more efficient (quick, compact)

OS Design Issues (2)

- **Reliability** → How to deal with failures
- **Portability** → How to write once and run anywhere
- **Extensibility** → How to add new features/capabilities
- **Communication** → How to exchange information
- **Scalability** → How to scale up as demand increases
- **Persistency** → How to save task's status
- **Accounting** → How to claim on control resource usage

Architectural Trends: CPU

*Million Instructions Per Second

**1 MHz = 1,000,000 clock cycles per second

	1971 (Intel 4004)	Today (Intel Core i9)	Δ (orders of magnitude)
MIPS*	~0.09	~400,000+	+7
Instructions per clock cycle (1/CPI)	~0.12	~100+	+3
Clock frequency (MHz)**	0.74	~5,000	+4
Cheap size (µm)	10	0.014	-3

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Moore's law: the number of transistors in a dense integrated circuit doubles about every two years

Architectural Trends: Main Memory

	1973 (DEC PDP-8)	Today (Samsung DDR4)	Δ (orders of magnitude)
Capacity (kB)	12	128,000,000	+7
Cost ($/MB)	~400,000	~0.005	-8

Architectural Trends: Disk

	1956 (IBM RAMAC 305)	Today (Western Digital)	Δ (orders of magnitude)
Capacity (MB)	5	15,000,000	+7
Size (inch)	24 (x50)	3.5	-3
Cost ($/MB)	640 (per month)	~0.000018	-9

What's Next?

- Moore's law has hit its limit(?)
  - chip size has physical constraints
  - power vs. heat tradeoff
  - alternatives have already pushed forward the end of it:
    - multicore-manycore processors
  - other approaches are subject of research:
    - molecular/DNA transistors
    - quantum computing

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