Systems and Networking I

Applied Computer Science and Artificial Intelligence

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SAPIENZA
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Problems Seen So Far

- Contiguous allocation
  - Hard to grow or shrink process memory
- Fragmentation
  - Frequent compaction needed
- Process entirely loaded
  - Swapping helps but it may be too inefficient

Paging

- A memory management scheme that addresses the problems above

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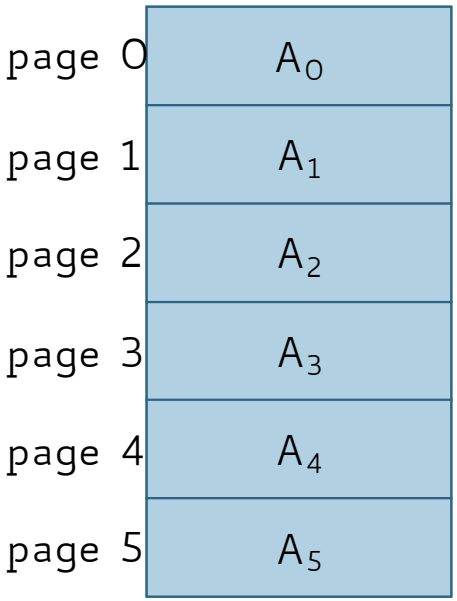
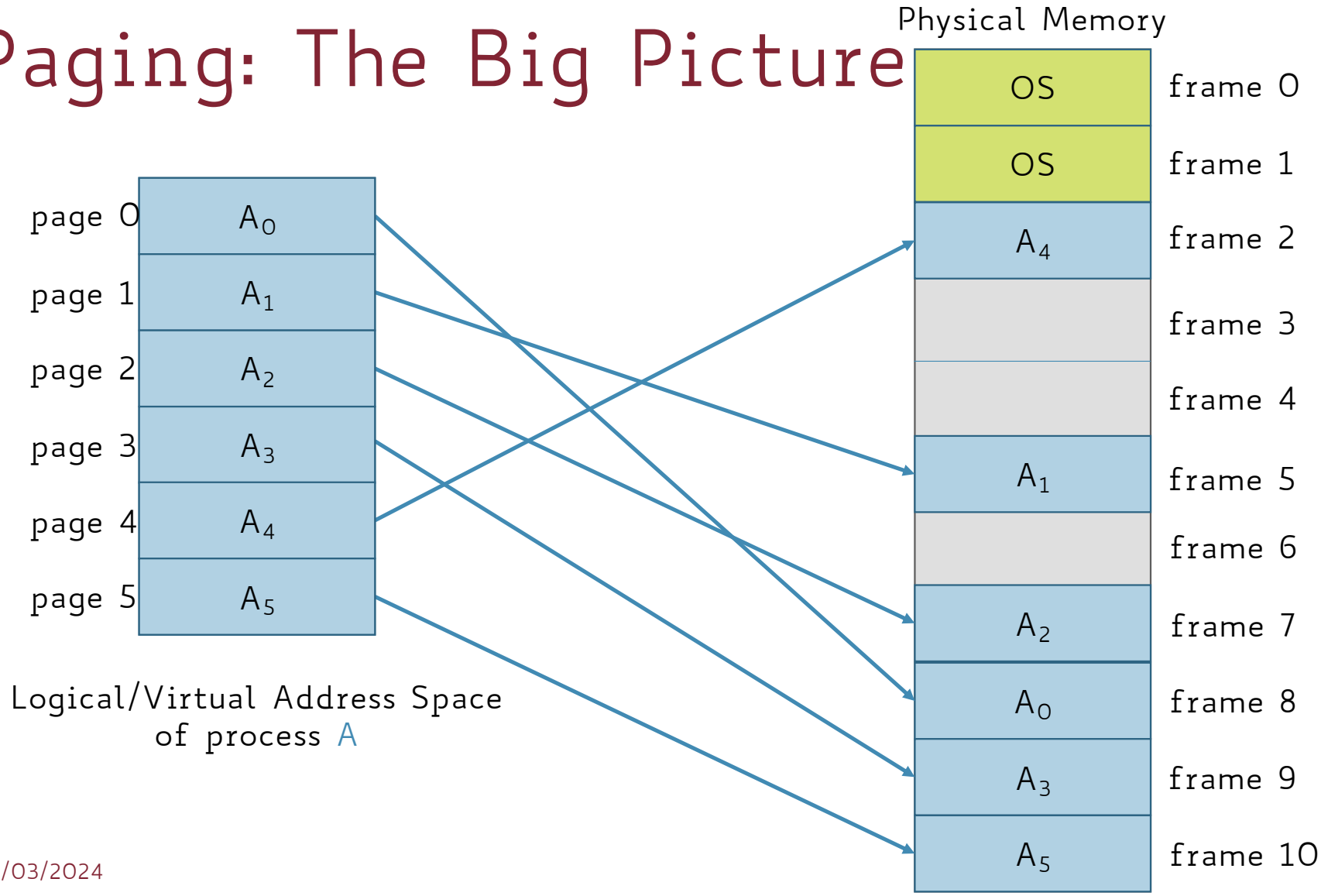
90/10 Rule
Processes spend 90% of their time accessing only 10% of their allocated memory space

Paging: The Big Picture



Logical/Virtual Address Space
of process A

Paging: The Big Picture



Basic OS Responsibilities for Paging

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  - mapping between logical pages and physical frames
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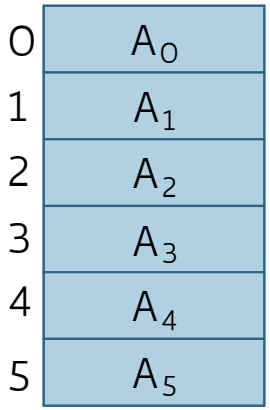
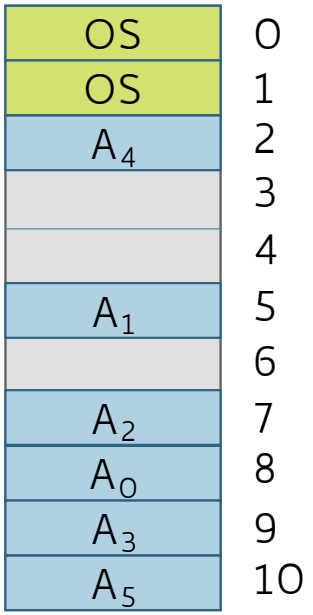
- All of this must be done efficiently!
  - Remember, memory addresses are referenced all the time
- OS needs dedicated support for doing it → Page Table

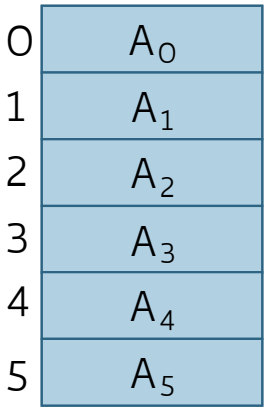
Page Table: Mapping Pages to Frames



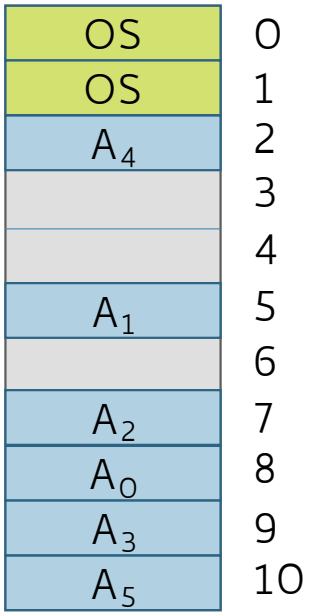


Page Table: Mapping Pages to Frames

Lookup table to retrieve what frame a page is stored in



Page	Frame
0	8
1	5
2	7
3	9
4	2
5	10



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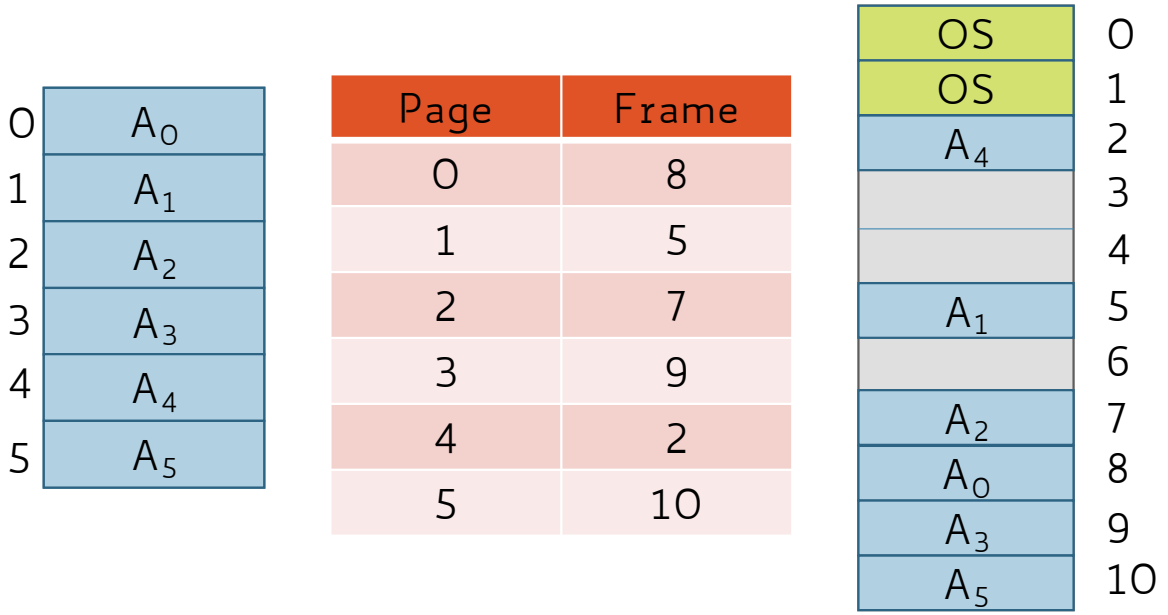

We have assumed all pages of a process are mapped to physical frames, but this is not always the case

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- Virtual (logical) address space is still contiguous starting from 0
- Page table must ultimately translate virtual address to physical address

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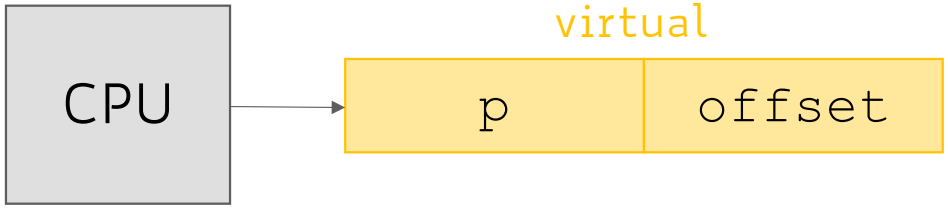
virtual address consists of 2 parts:
- p: page number where the address resides
- offset: relative from the beginning of the page



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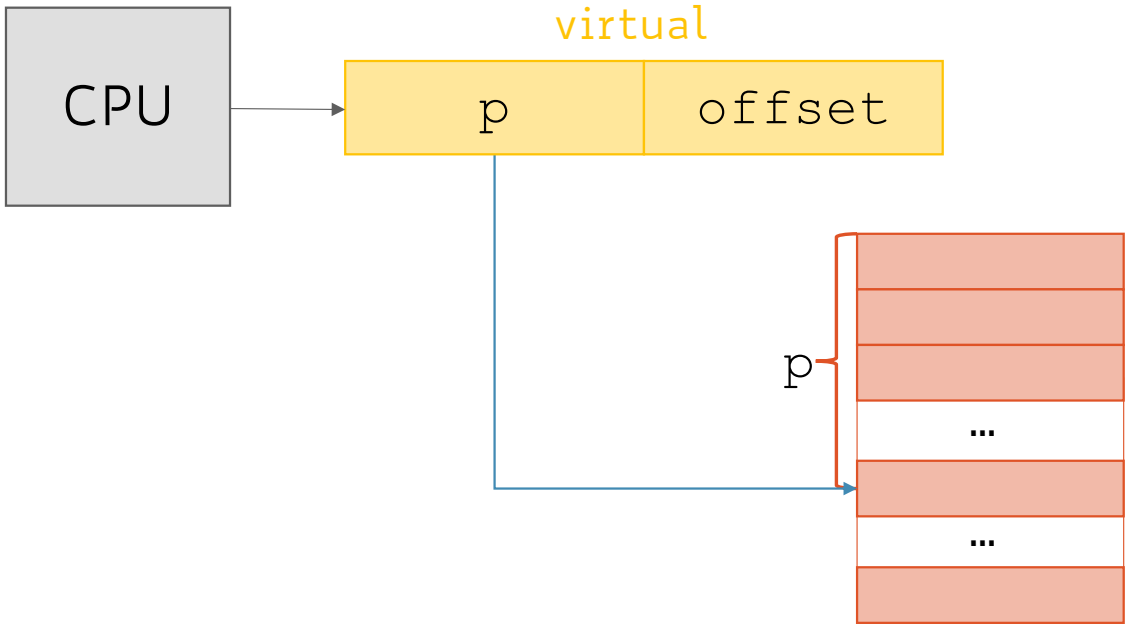

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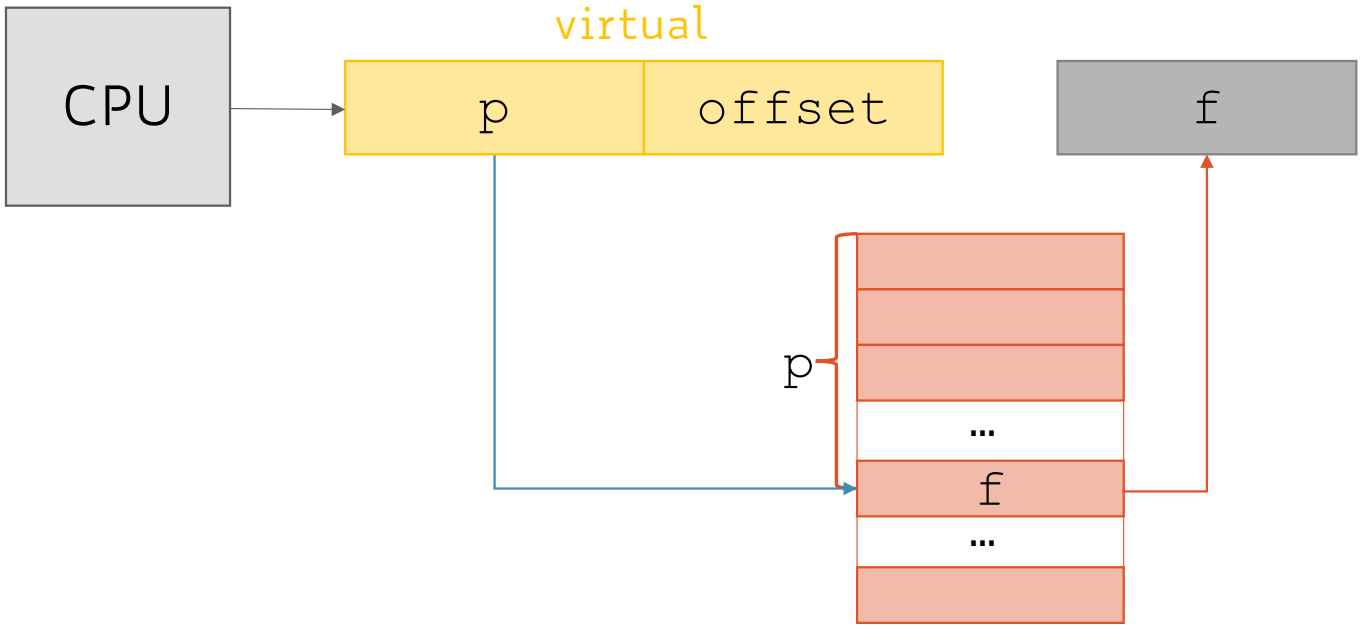

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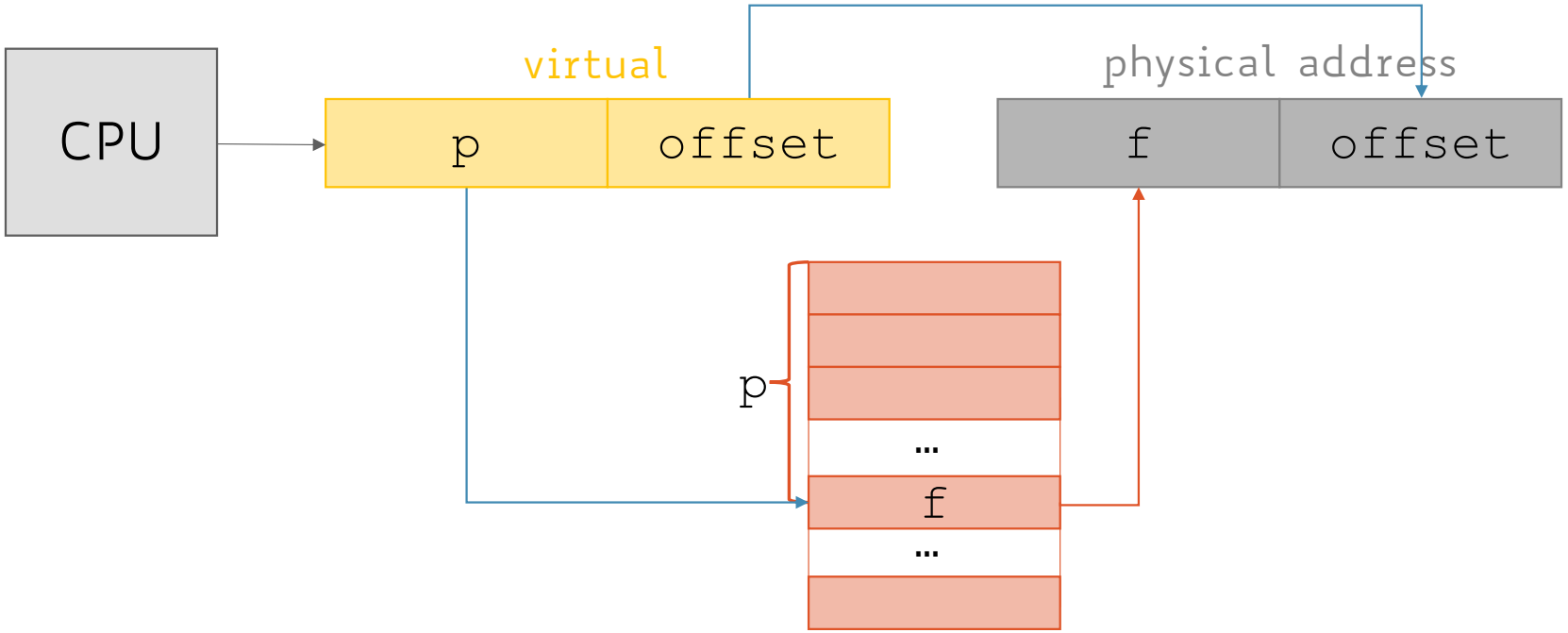

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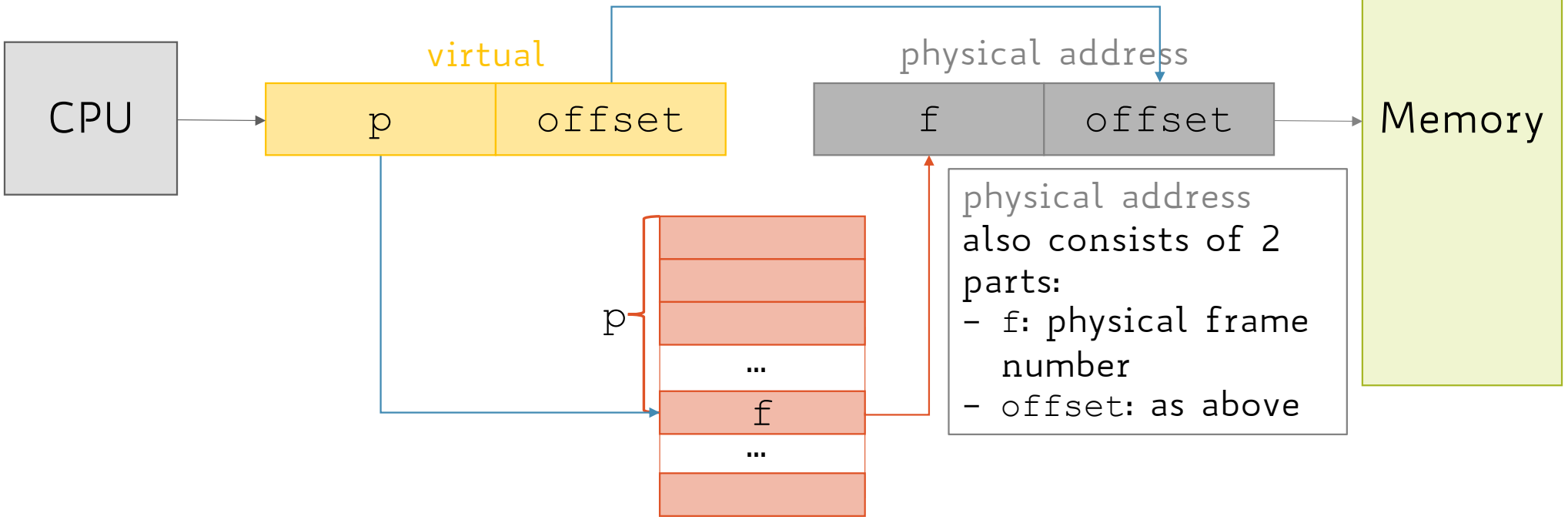
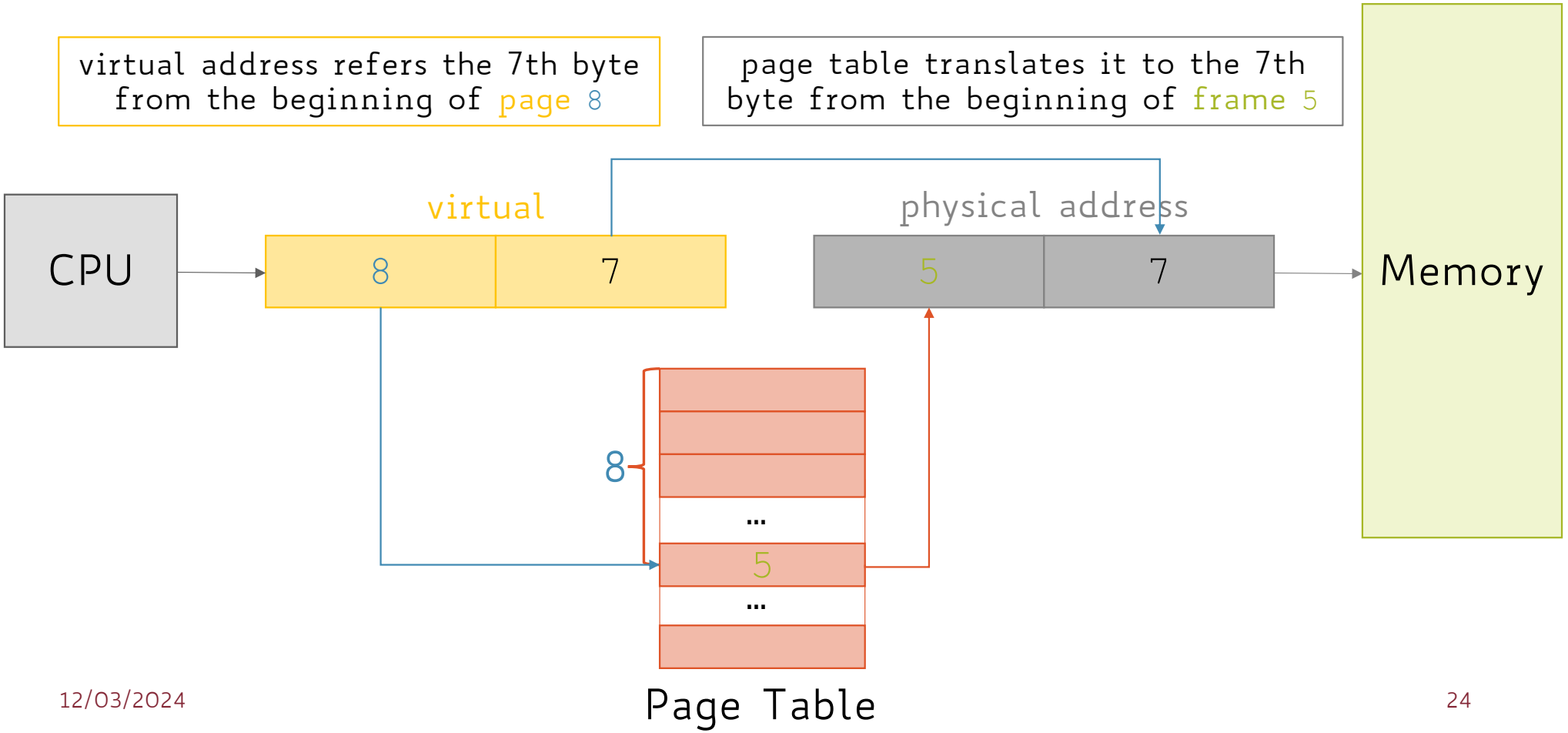


Page Table: Example of Address Translation



Paging as Dynamic Relocation

- Paging is an advanced form of dynamic relocation
- Each virtual address is bound by the page table to a physical address
- Page table can be seen just as a set of base (relocation) registers, one for each frame
- Mapping is invisible to the user process: the OS maintains the page table and translation happens in hardware (via the MMU)
- Protection is provided similarly to dynamic relocation (limit register)

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How does MMU use page table to translate a virtual address **x** into a physical address **y**?

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1. Get the page number (`p`) and the **`offset`** where the virtual address `x` resides

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3. Combine `f` with **`offset`** to obtain the physical address `y`

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Address translation requires a **div** and a **mod** operation

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Why?

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- The higher **m-n** bits of the virtual address indicates the **page number**
- The low order **n** bits represent the **offset**

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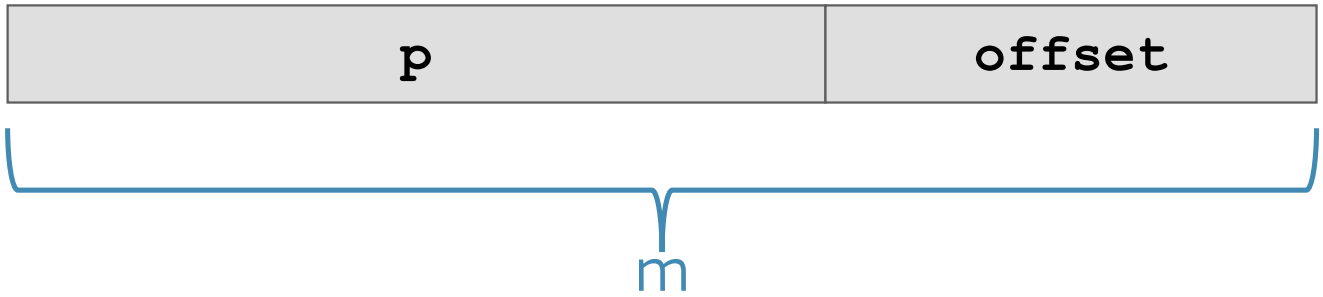

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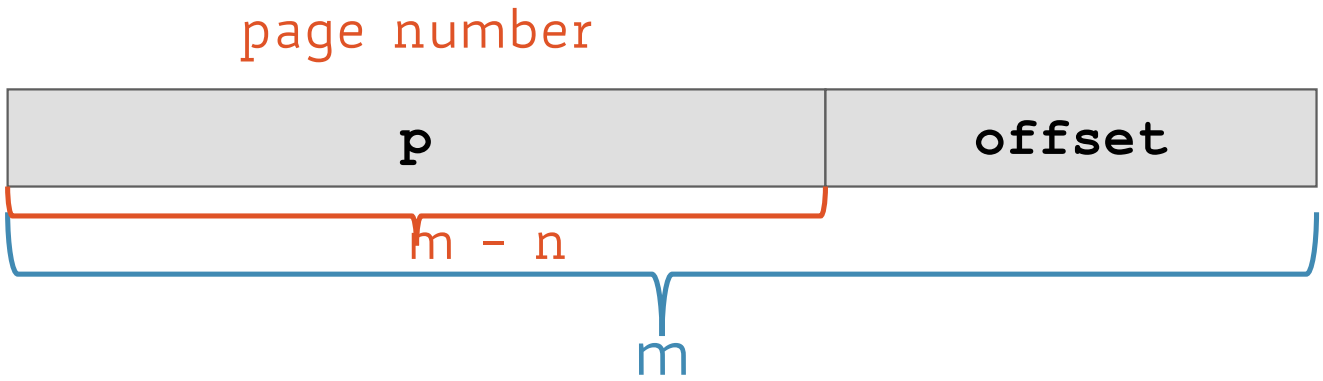

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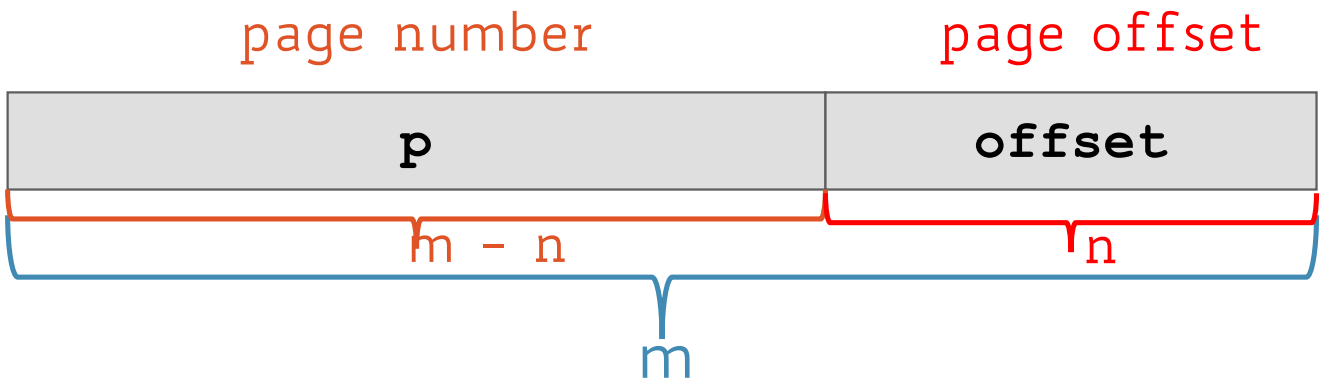
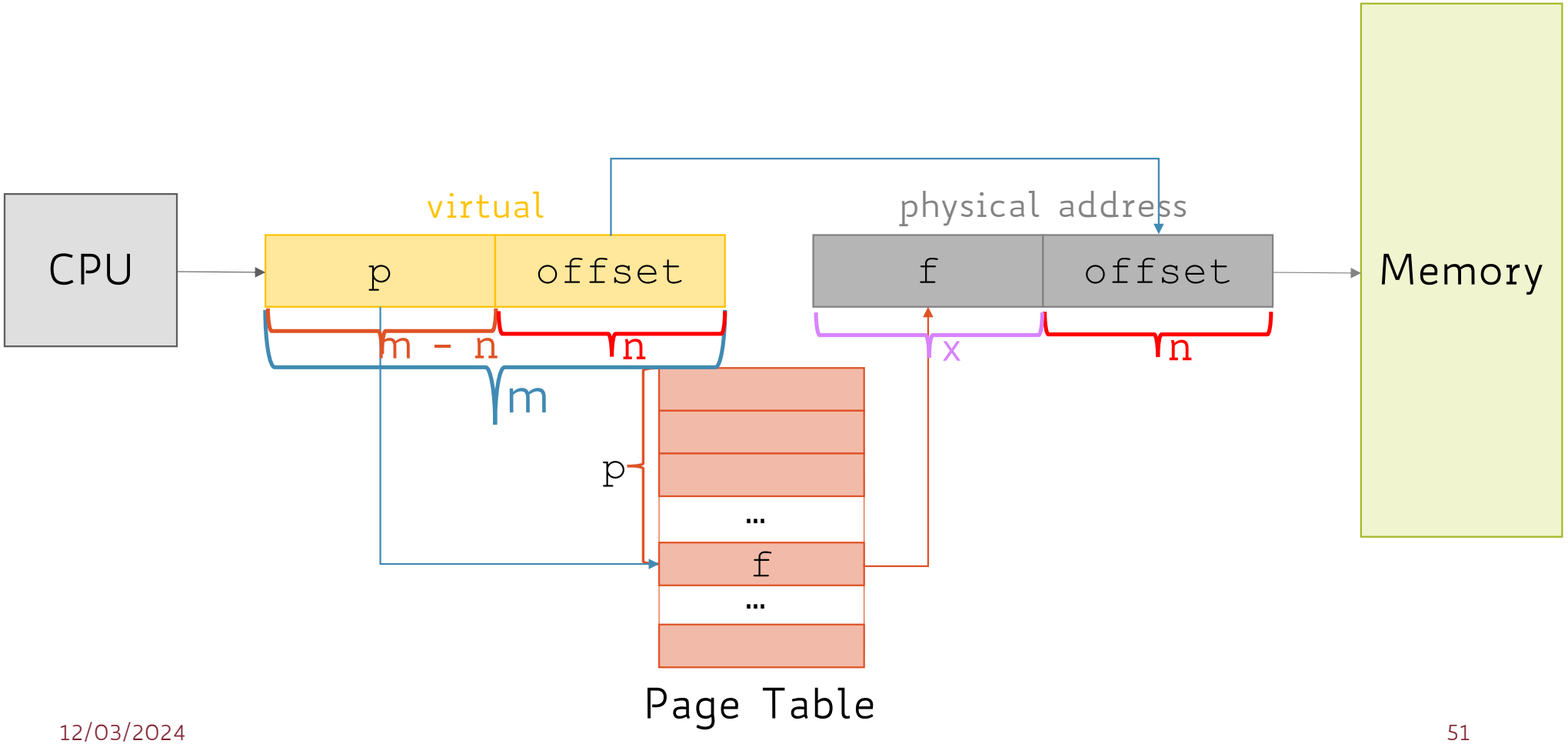


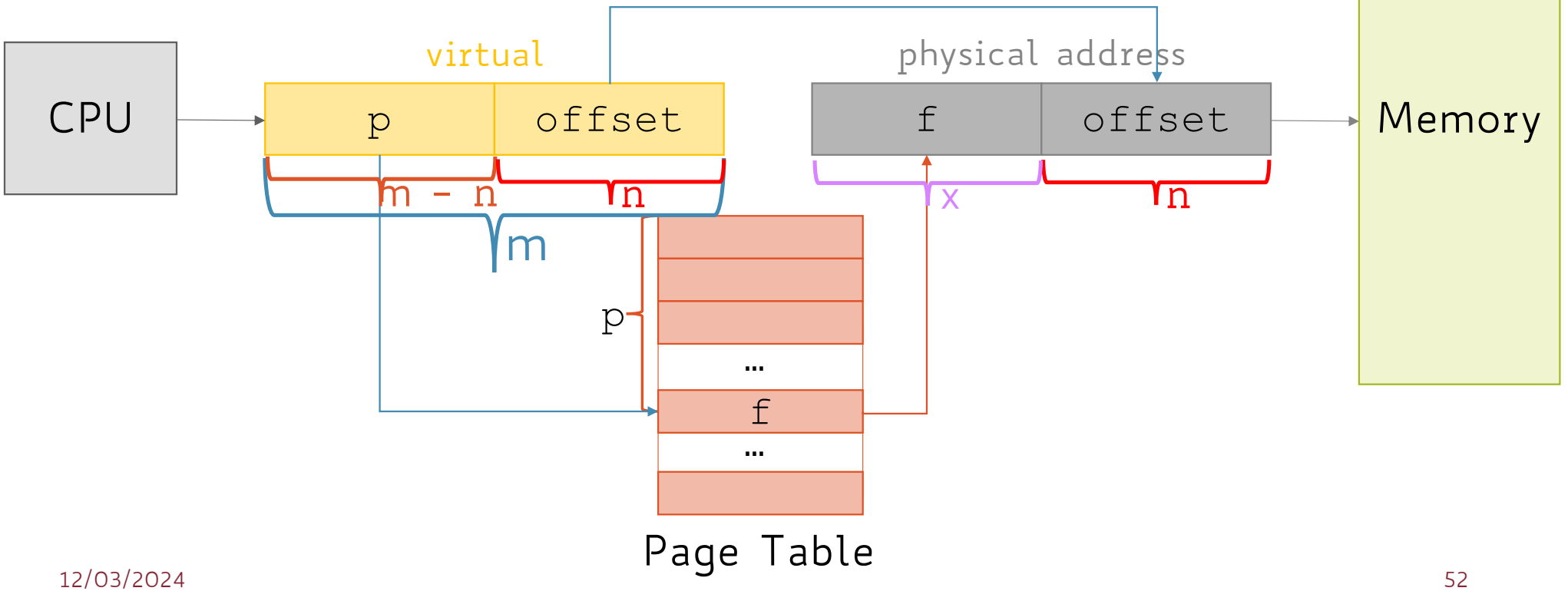
Paging: Practical Details



Paging: Practical Details

NOTE

m-n doesn't necessarily have to be equal to x



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- Typical values of page/frame sizes is n = 12 bits
  - Each page/frame is 2^{12} = 4KiB
- Assuming m = 32 bits, there are 2^{m-n} = 2^{20} = ~1M pages/frames
  - The page table has 2^{20} entries (i.e., one for each page/frame)

Paging: Practical Example

Suppose we have a virtual memory and a physical memory, both of size M = 1024B (1KiB)

Q1

How many bits are needed for a virtual/physical address (assuming single-byte addressing)

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R1

10 bits to address M = 1024 bytes (both for virtual and physical address)

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Now, assume we use paging with page/frame size S = 16B

Q2

How big is the page table? (i.e., how many pages/entries does it have to index?)

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T = M / S = 1024 memory bytes / 16 bytes per page = 64 pages

Paging: Practical Example

Q3

What is `p` and `offset` (i.e., how many bits for `p` and `offset`?)

Paging: Practical Example

Q3

What is `p` and `offset` (i.e., how many bits for `p` and `offset`?)

R3

Our logical address is made of m = 10 bits

n = 4 bits are used to represent the `offset`, as each page/frame is S = 16 bytes

m-n = 6 bits are used to represent page number `p`, as there are T = 64 pages

Paging: Practical Example

Q4

Translate the virtual address `x = 42`, assuming the following page table

page	frame
0	12
1	5
2	37
3	0
…	..
63	29

Paging: Practical Example

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Translate the virtual address `x = 42`, assuming the following page table

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R4

p = x **div** S = 42 **div** 16 = **2**

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R4

p = x **div** S = 42 **div** 16 = **2**

offset = x **mod** S = 42 **mod** 16 = **10**

10th byte from the beginning of frame 37

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Modern computers however operate natively on multiple of bytes (i.e., words) rather than single-byte. Typical values of word length is: 16, 32 or 64 bits.
If we assume 32-bit architecture (i.e., word = 32 bits = 4 bytes), virtual addresses refer to words instead of bytes

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Q1
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R1
8 bits to address M = 1024/4 = 256 4-byte words

Paging: Practical Example 2

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Q2

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R2

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Q3

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R3

Our logical address is now made of m = 8 bits
n = 2 bits are used to represent the `offset`, as each page/frame is:
S = 16 bytes = 4 * 4-byte words
m-n = 6 bits are used to represent page number `p`, as there are still
T = 64 pages

Paging: Practical Example 2

Q4

Translate the virtual address `x = 7`, assuming the following page table

page	frame
0	12
1	5
2	37
3	0
…	..
63	29

Paging: Practical Example 2

Q4

Translate the virtual address `x = 7`, assuming the following page table

page	frame
0	12
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Remember: now virtual address refers to a 4-byte word!

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`S = 16` bytes = 4 * 4-byte words

Must be expressed in terms of number of words

R4

`p = x div S = 7 div 4 = 1`

Paging: Practical Example 2

Q4

Translate the virtual address `x = 7`, assuming the following page table

page	frame
0	12
1	5
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3	0
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R4

p = x **div** S = 7 **div** 4 = **1**

offset = x **mod** S = 7 **mod** 4 = **3**

3rd word from the beginning of frame 5

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- To do so, the MMU must access the page table

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- Trade-off solution: **Translation Look-aside Buffer** (TLB), namely a cache!

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- CPU can only access its registers and main memory (any access to other devices, e.g., hard drive, requires data to be moved into main memory first)

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- Access individual memory locations one at a time from the cache rather than from memory directly

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- Typical TLB sizes range from 8 to 2048 entries

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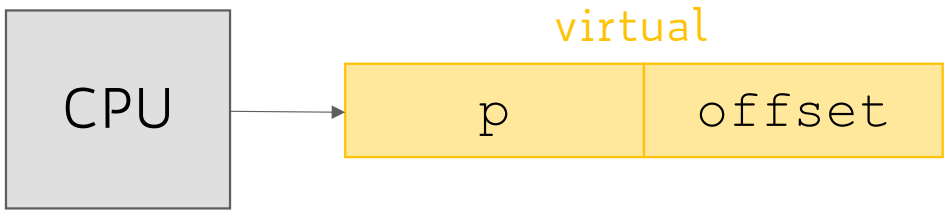

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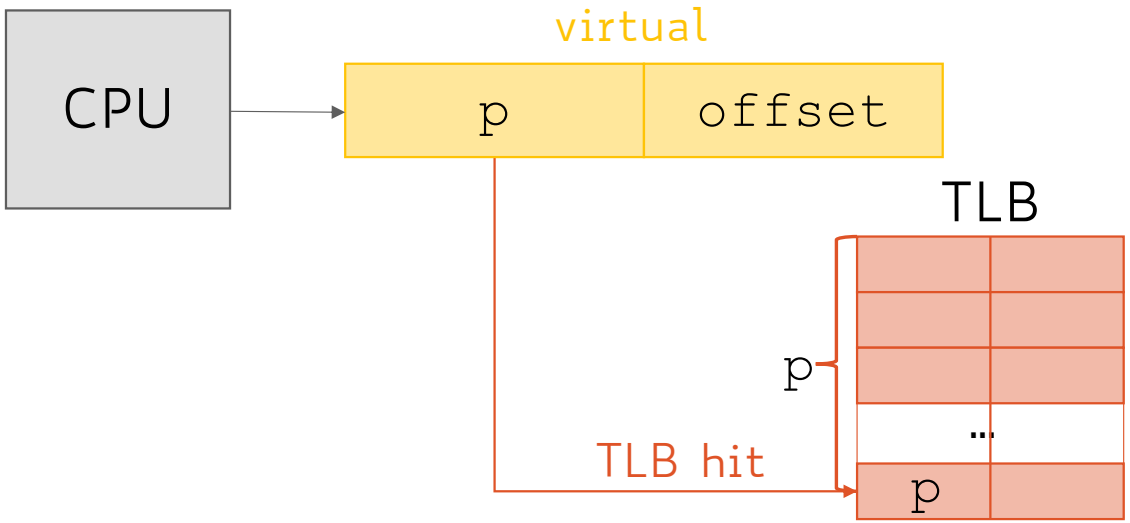

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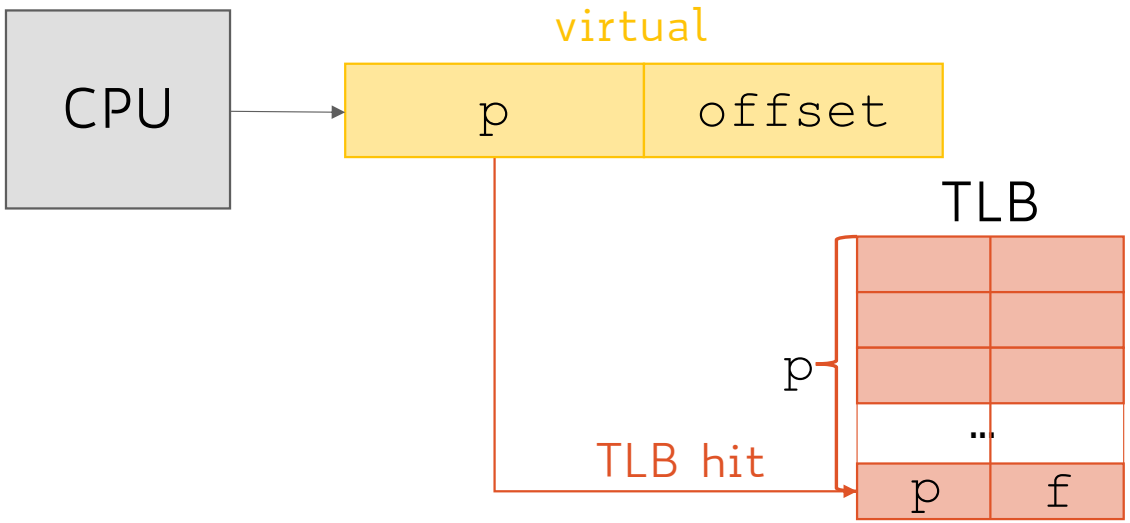

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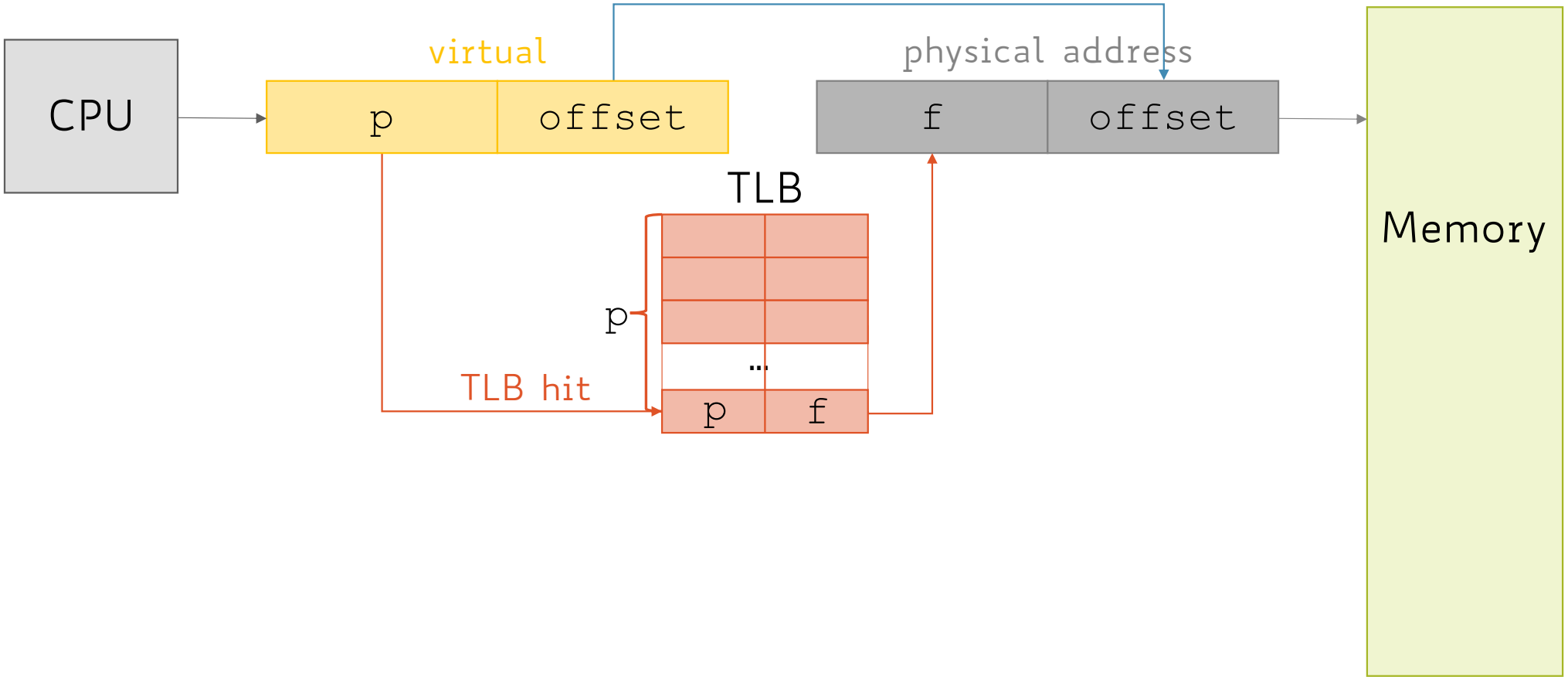

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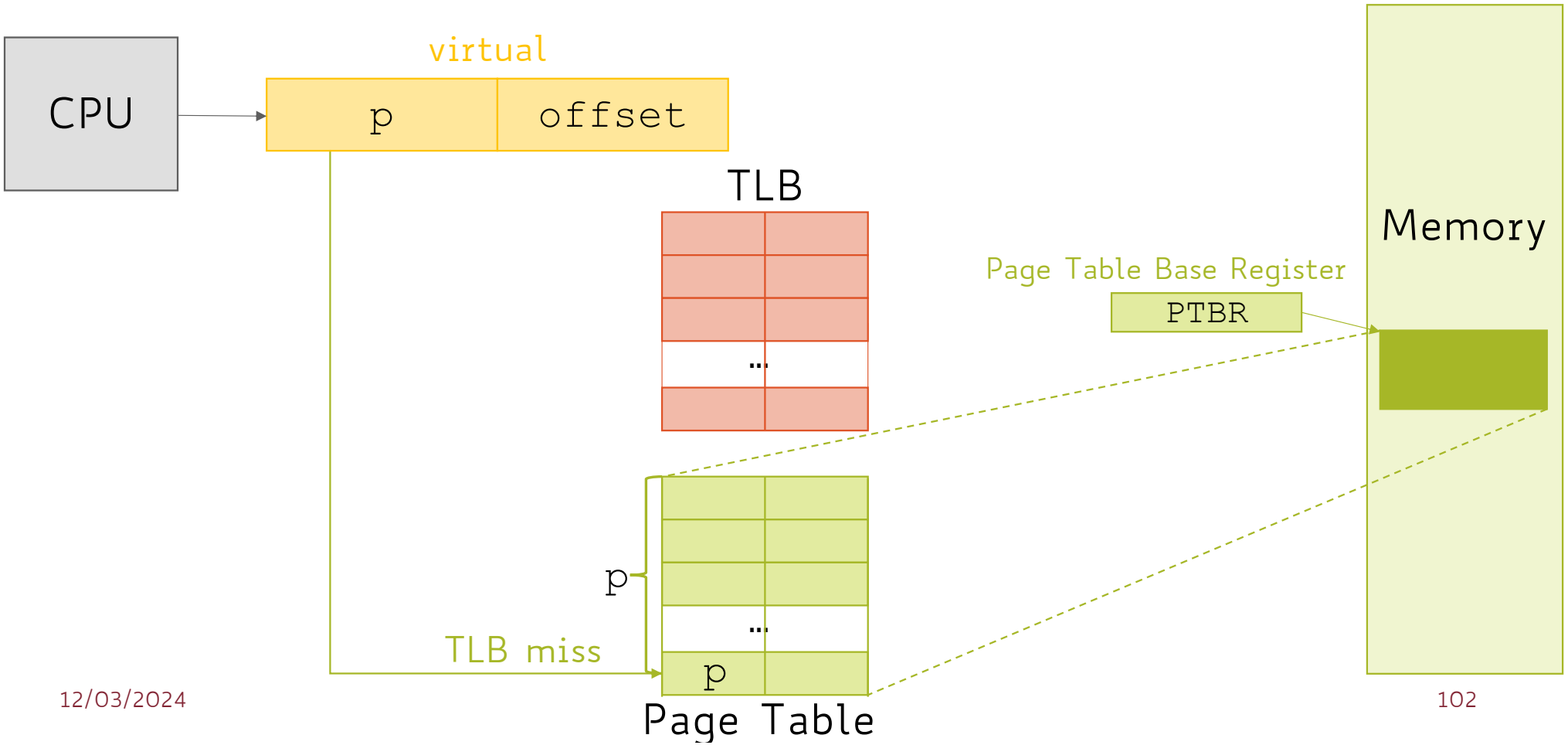

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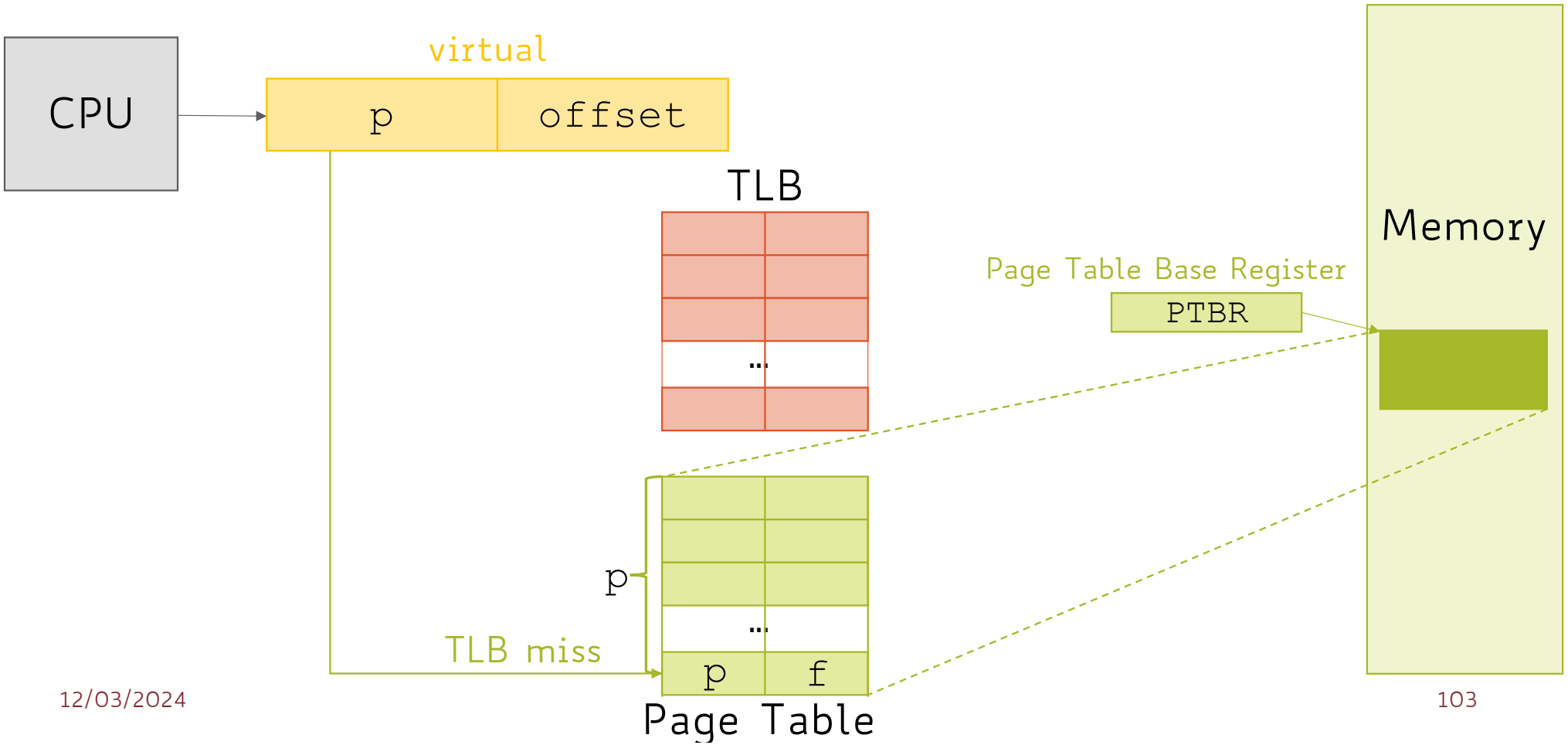

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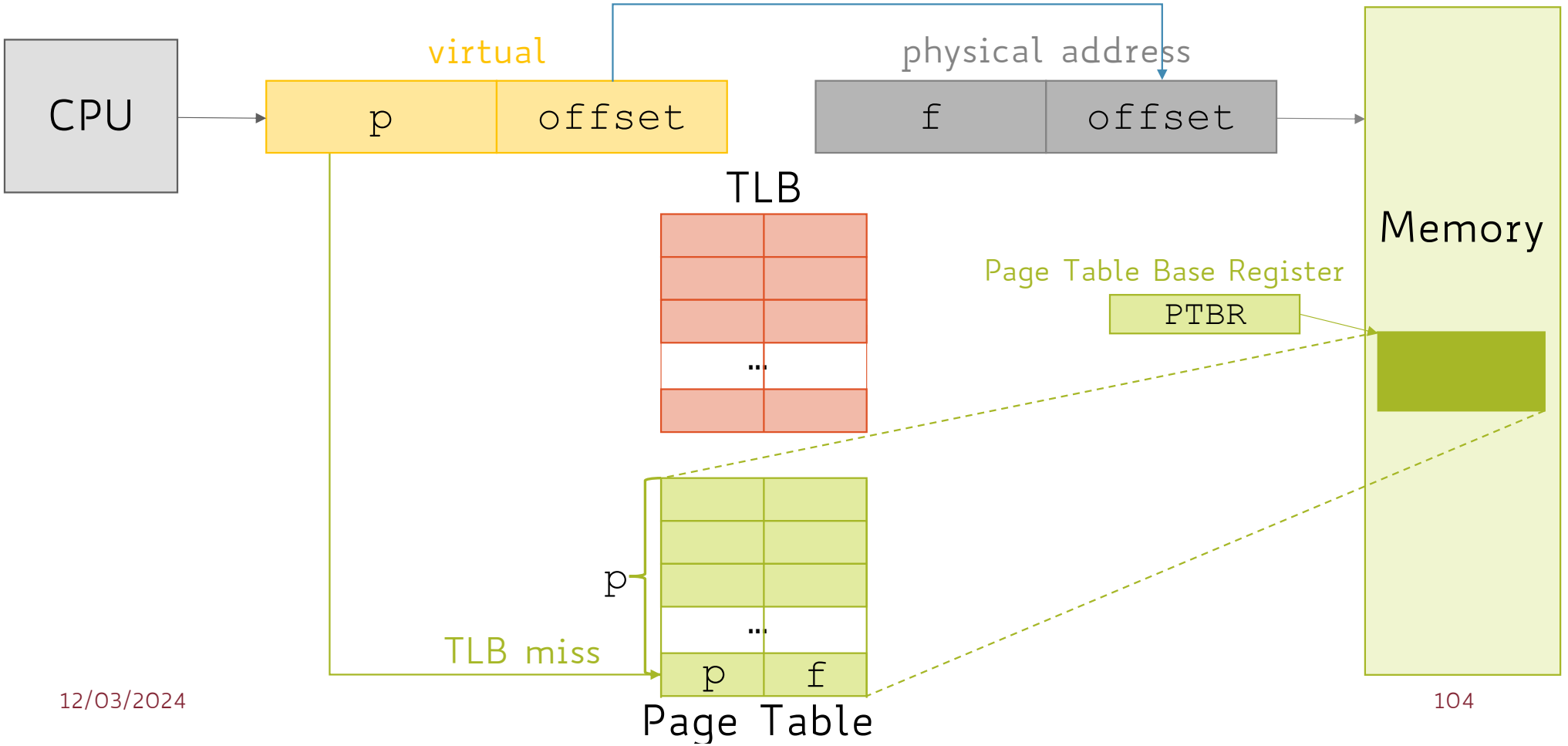

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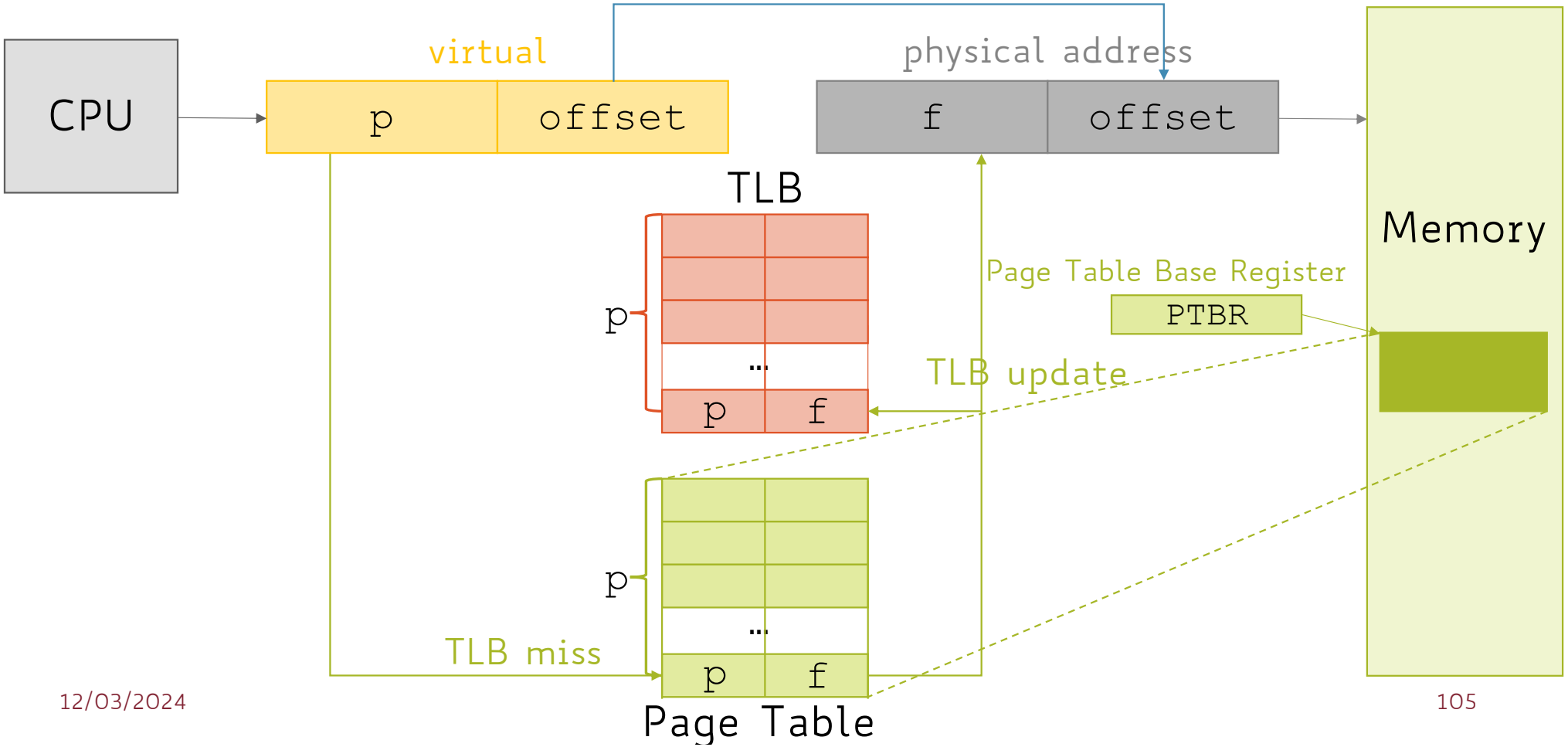

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How to deal with multiple process and a single TLB?

- **2 setups**:
  - **basic**: at each context switch the content of the TLB is fully flushed and cleaned (cold-start → the first accesses will generate all TLB misses)
  - **advanced**: TLB entries dumped and restored within the PCB or adding a so-called process context ID (PCID) to each entry (the CPU will use a TLB entry iff the PCID of that entry corresponds to the ID of the running process)

Memory Access Cost

t_{MA} = physical memory access time
t_{TLB} = lookup time on the TLB cache
(NOTE: $t_{TLB} \ll t_{MA}$)
p = probability of TLB cache hit (i.e., *hit ratio*)
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The larger the TLB the higher the probability p of hit ratio, thereby decreasing the average memory access cost

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- Valid/invalid bits can be added to "mask off" entries in the page table that are not in use by the current process

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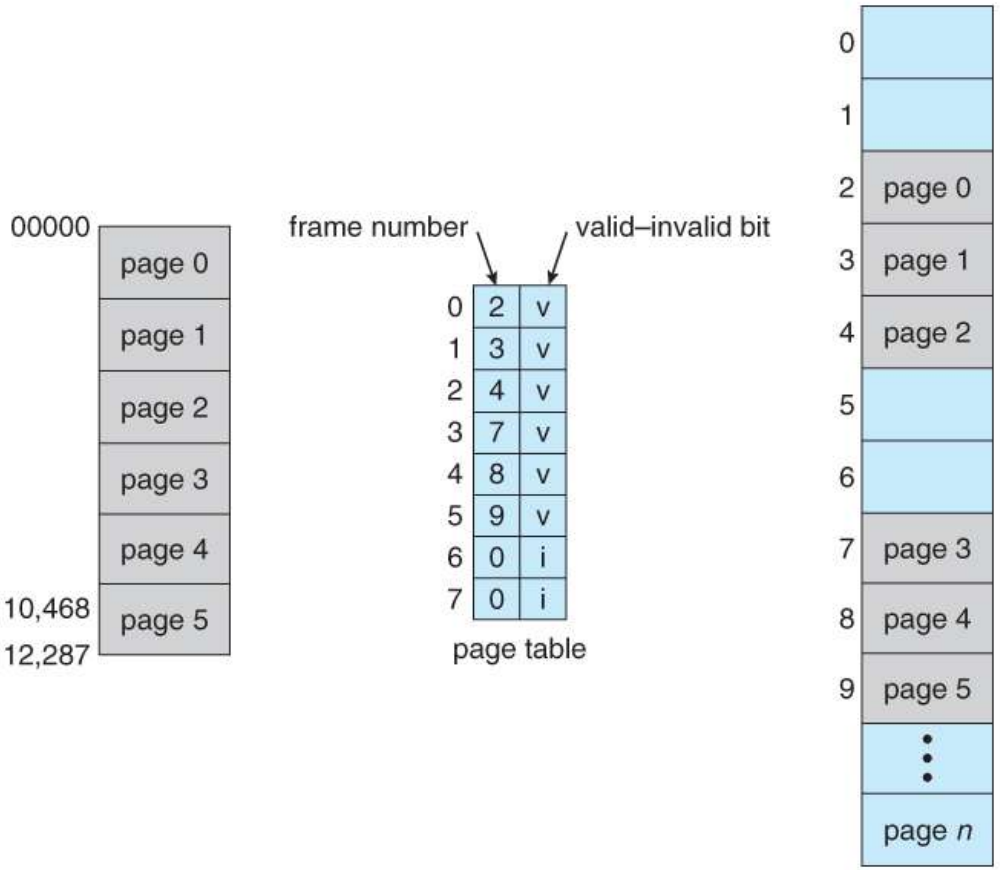

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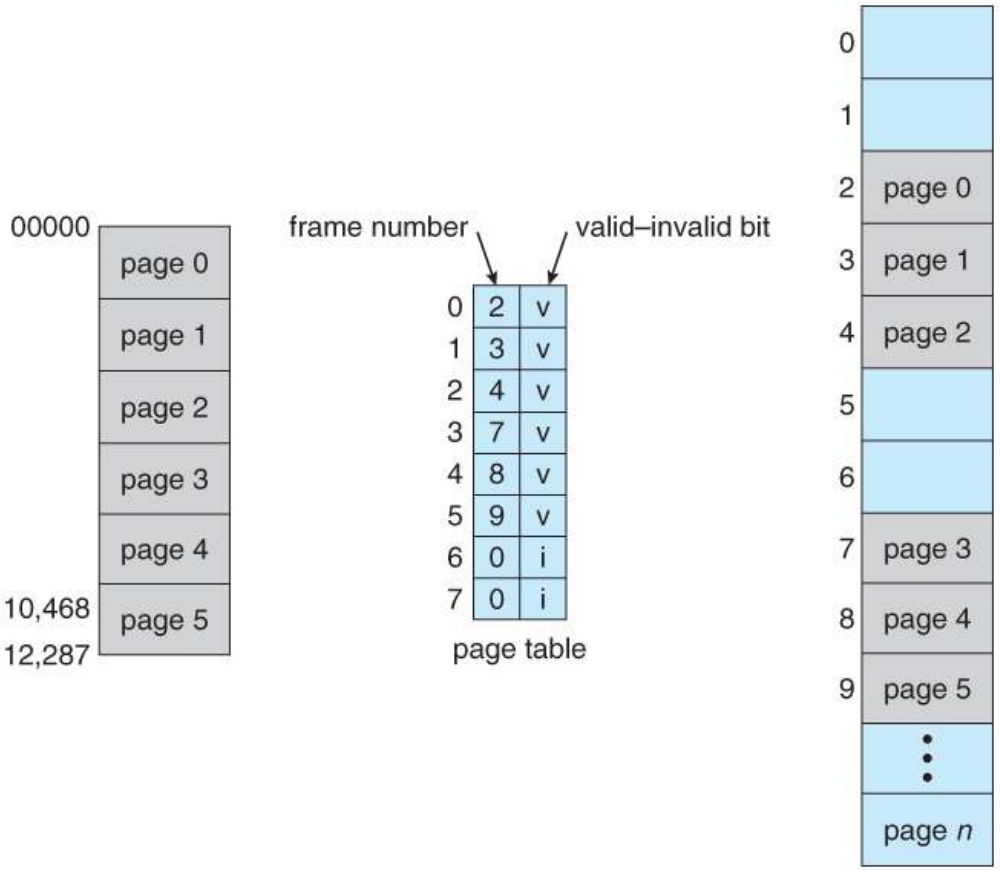

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any entry whose invalid bit is set will be discarded (and updated)

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5. As process runs, OS loads TLB missed entries possibly replacing existing entries if TLB is full

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  - Possibly a copy of the TLB entries
- On a context switch:
  - Copy the `PTBR` value to the PCB
  - Copy the TLB to the PCB (optional)
  - Flush the TLB (if TLB is not saved to/restored from the PCB)
  - Restore the `PTBR` (i.e., with the value of the new running process)
  - Restore the TLB (if it was previously saved)

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- Memory doesn't have to be contiguous anymore!
- Just duplicate page entries of different processes to the same page frames (both for code and data)

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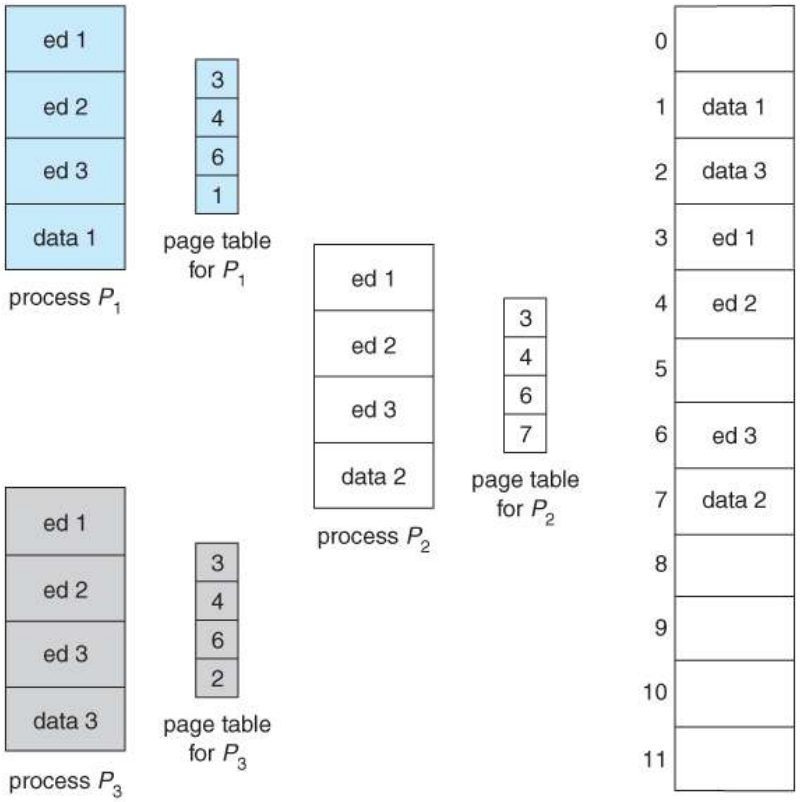
- The code can be shared by multiple processes, as long as each has their own copy of the data and registers, including the instruction register

Sharing Pages: Example



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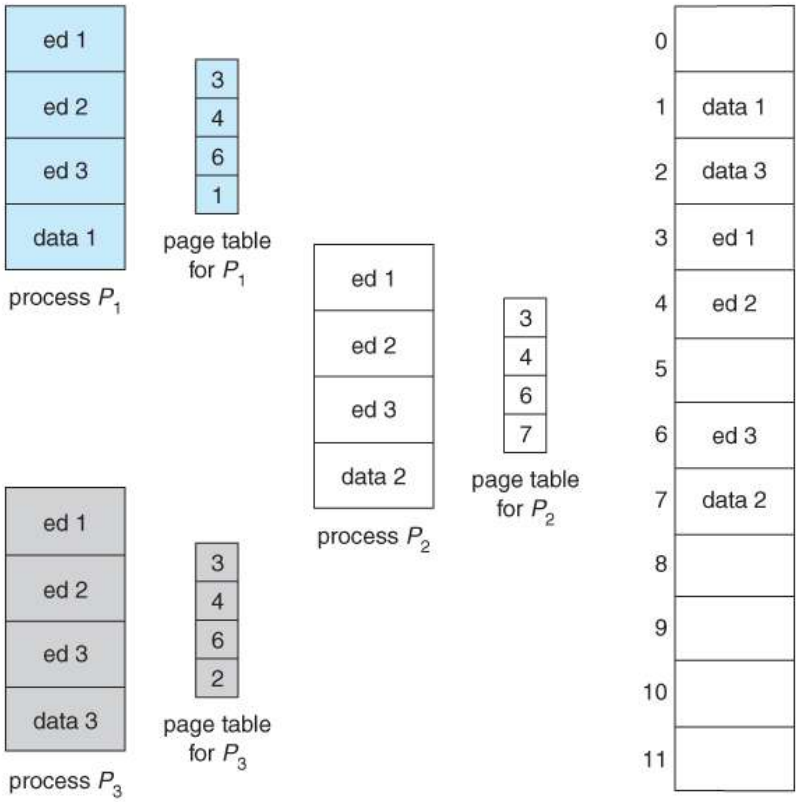

3 user processes are using the editor program `ed`

Only a single copy of the code of `ed` is actually loaded in main memory

Paging: Summary

- A big improvement over **relocation**
- Eliminates the problem of external fragmentation and therefore the need for compaction
- Allows code sharing among processes, reducing memory footprint
- Enables processes to run when they are partially loaded

Paging: Summary

- However, paging comes with its costs…
- Virtual/Physical address translation may be time consuming
- Hardware support like TLB cache is needed to make it efficient enough
- OS has to be inevitably more complex