

Systems and Networking I

Applied Computer Science and Artificial Intelligence
2024-2025



SAPIENZA
UNIVERSITÀ DI ROMA

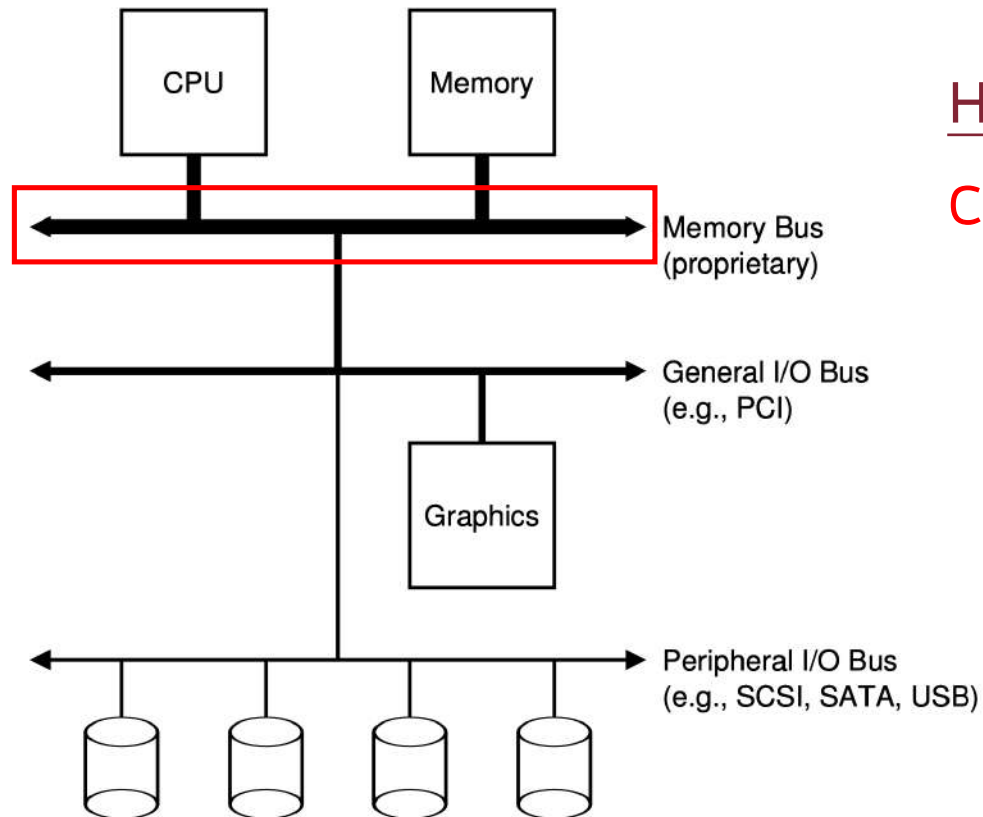
Gabriele Tolomei

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Sapienza Università di Roma

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A Quick Recap on I/O

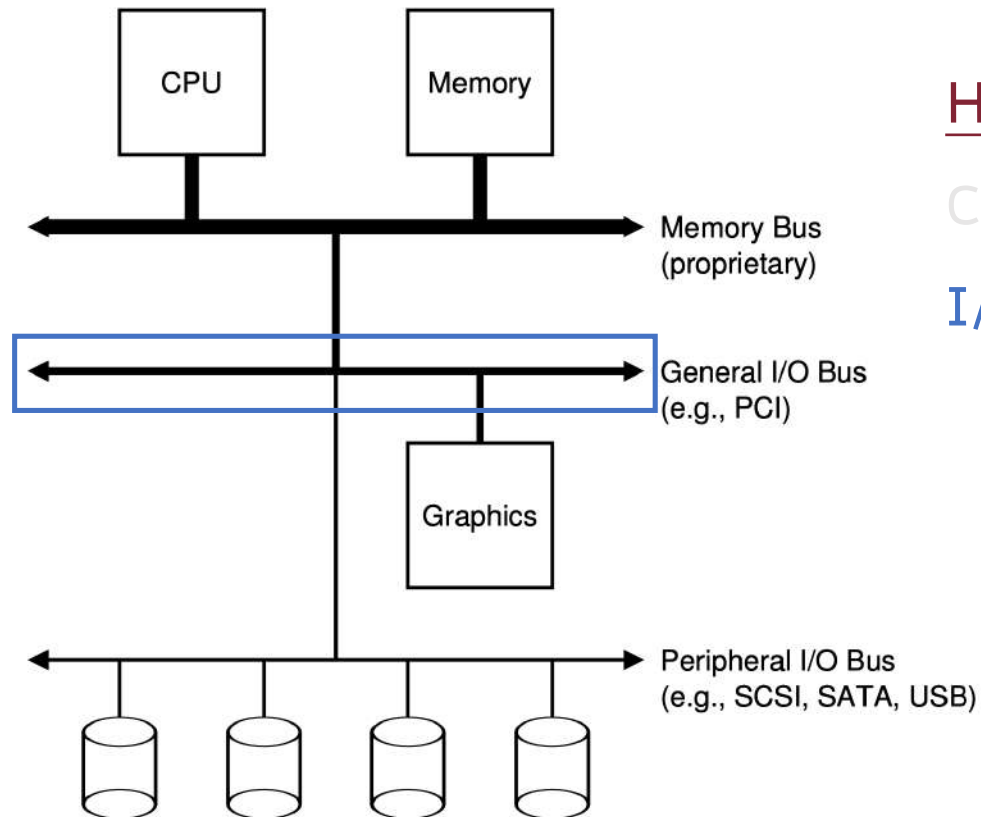
Remember the Basic System Architecture



Hierarchy of Communication Buses

CPU-Memory high-speed bus

Remember the Basic System Architecture

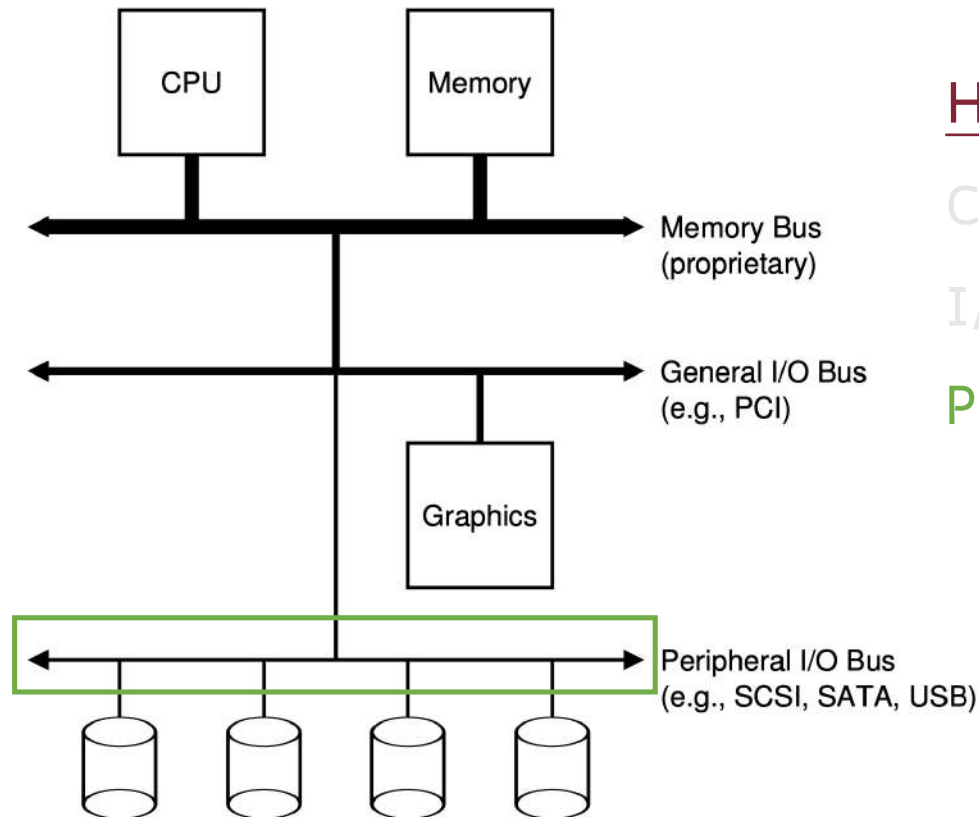


Hierarchy of Communication Buses

CPU-Memory high-speed bus

I/O bus

Remember the Basic System Architecture



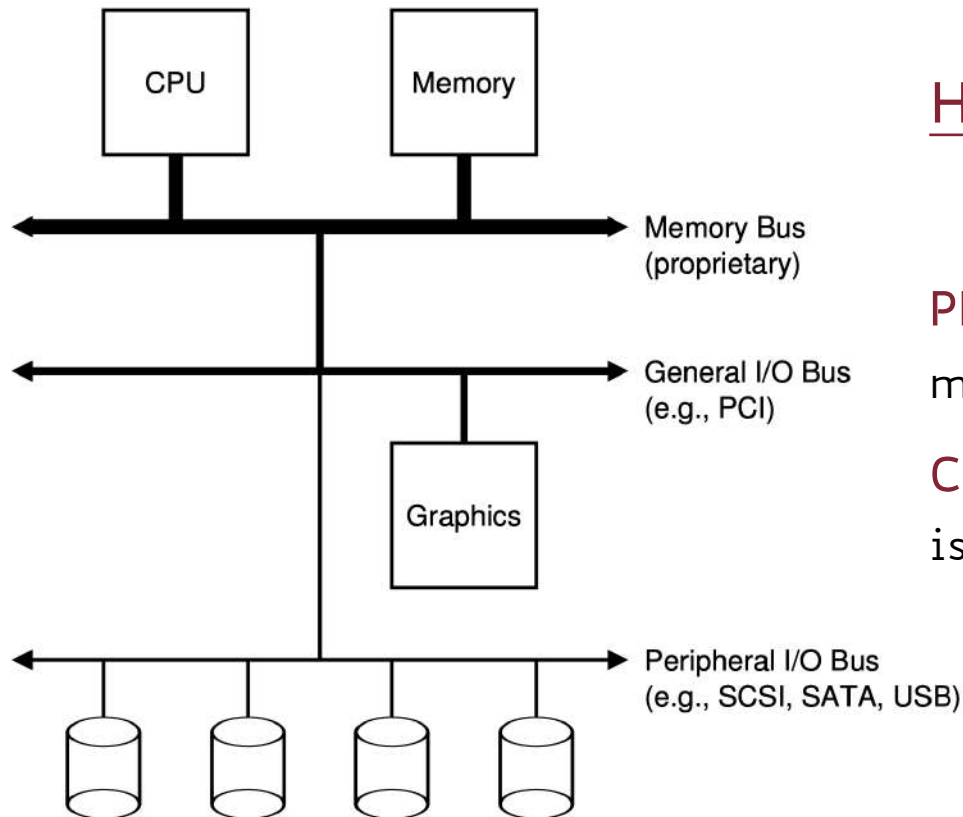
Hierarchy of Communication Buses

CPU-Memory high-speed bus

I/O bus

Peripheral bus

Remember the Basic System Architecture



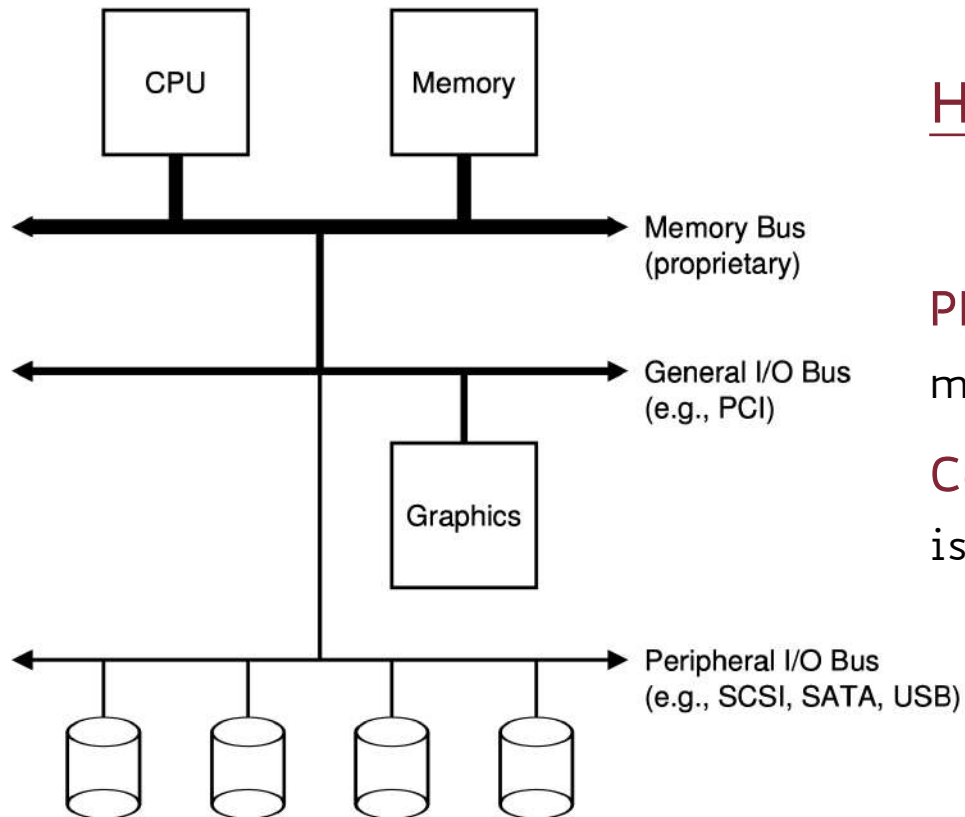
Hierarchy of Communication Buses

Why?

Physics: The faster a bus is, the shorter it must be!

Costs: Engineering a high-performance bus is expensive!

Remember the Basic System Architecture



Hierarchy of Communication Buses

Why?

Physics: The faster a bus is, the shorter it must be!

Costs: Engineering a high-performance bus is expensive!

High-speed I/O devices are closer to the CPU (e.g., graphics card)

Low-speed I/O devices are closer to the CPU (e.g., hard disks)

A Canonical I/O Device: Components

- Each I/O device is made of **2 parts**:
 - the **physical device** itself
 - the **device controller** (chip or set of chips controlling a family of physical devices)

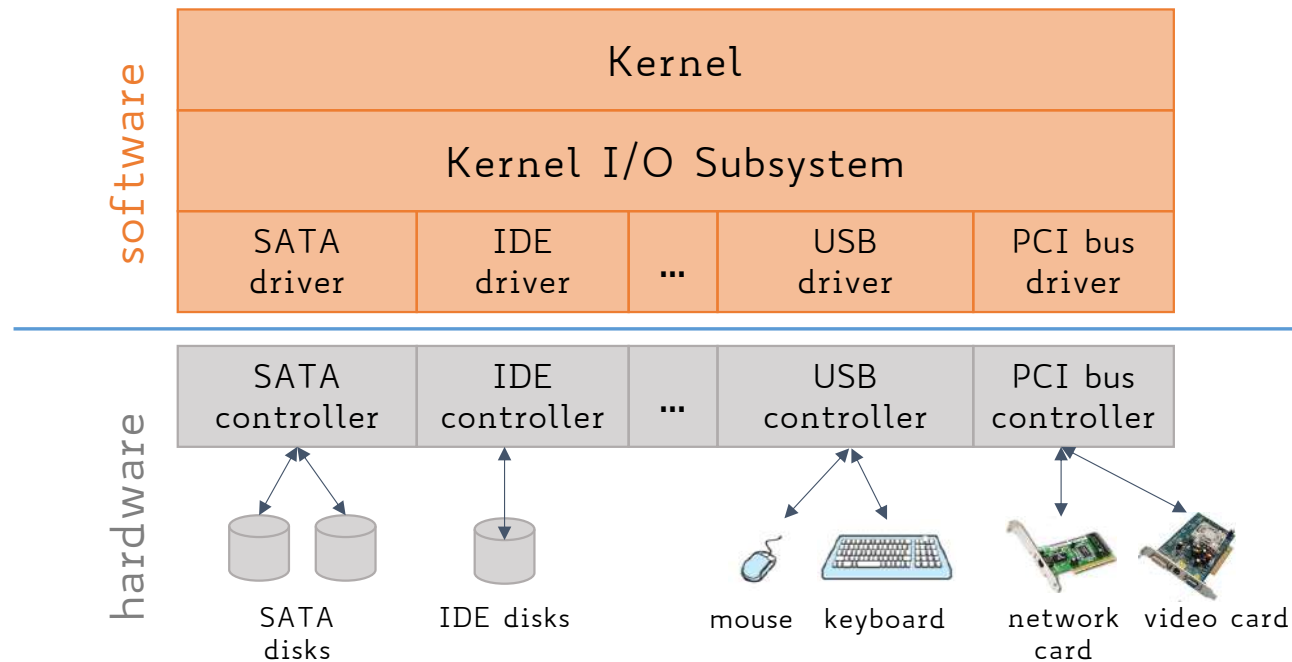
A Canonical I/O Device: Components

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- Can be categorized as:
 - storage, communications, user-interface, etc.

A Canonical I/O Device: Components

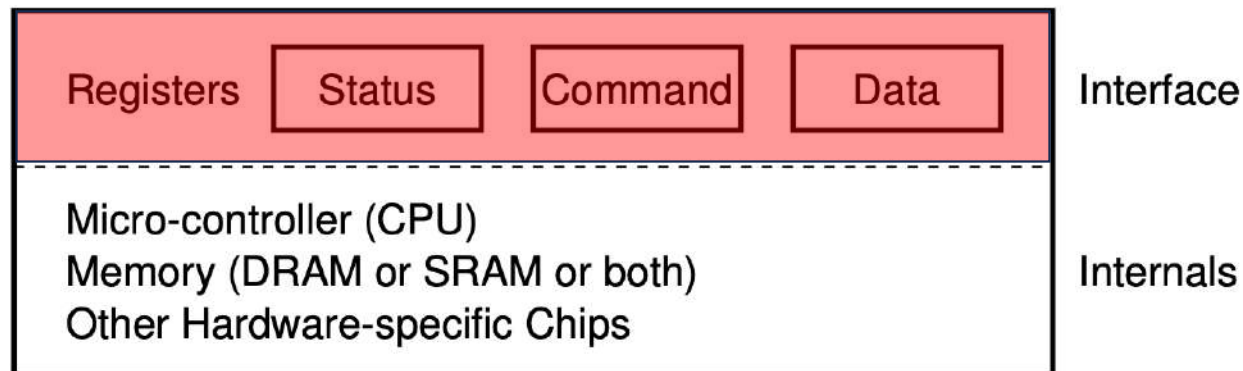
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 - the **physical device** itself
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- Can be categorized as:
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- OS talks to a device controller using a specific **device driver**

Device Drivers: OS Abstraction



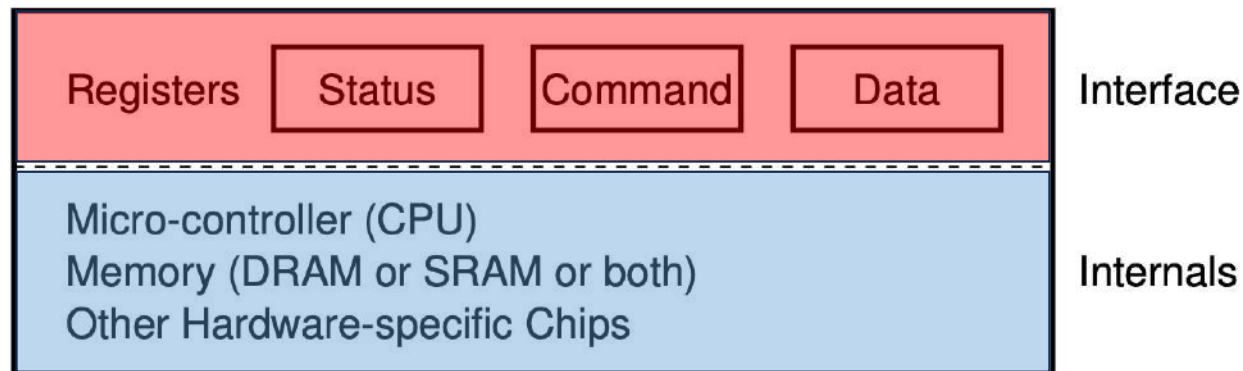
Device Controllers

- Every device controller has:
 - an **interface** → a number of dedicated registers to communicate with it



Device Controllers

- Every device controller has:
 - an **interface** → a number of dedicated registers to communicate with it
 - an **internal structure** → logic circuitry (vendor-specific)



Device Controllers

- **Status registers** → provide status information to the CPU about the I/O device (e.g., idle, ready for input, busy, error, transaction complete)
- **Command/Configuration/Control registers** → used by the CPU to configure and control the device
- **Data registers** → used to read data from or write data to the I/O device

The Basic Protocol: OS-I/O

```
While (STATUS == BUSY)  
    ; // wait until device is not busy
```

The OS waits until the device is ready by repeatedly checking the STATUS register

```
Write data to DATA register
```

```
Write command to COMMAND register
```

```
(starts the device and executes the command)
```

```
While (STATUS == BUSY)
```

```
    ; // wait until device is done with your request
```

polling

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    ; // wait until device is not busy
Write data to DATA register
Write command to COMMAND register
    (starts the device and executes the command)
While (STATUS == BUSY)
    ; // wait until device is done with your request
```

Send some data to the DATA register
(e.g., a 4KiB page to disk)

The Basic Protocol: OS-I/O

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Issue the command

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The OS waits for the device to finish again by polling in a loop

polling

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```

The CPU is responsible for the whole data transfer

Programmed I/O

The Basic Protocol: OS-I/O

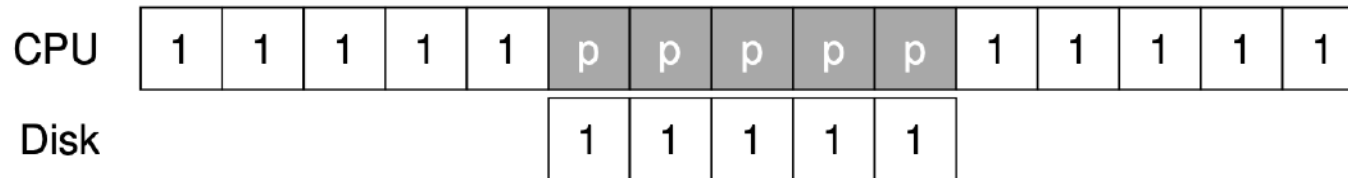
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```

The CPU wastes a lot of time checking a possibly slow I/O device

Programmed I/O + Polling

Lowering CPU Waste: How?

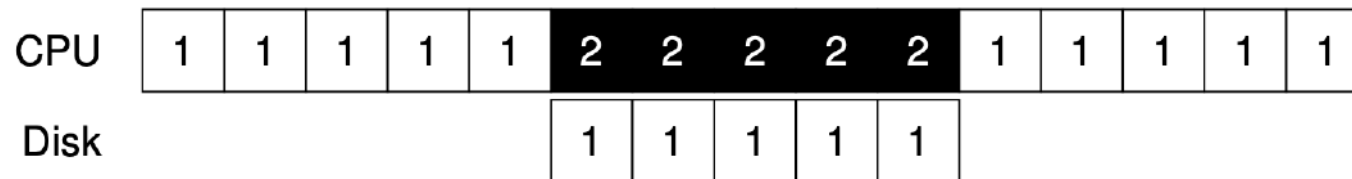
Polling: wastes CPU cycles waiting on a condition



Process 1 runs for some time, issues the I/O request and, while the request is being served, the OS repeatedly checks the status of the device (p)

Lowering CPU Waste: Interrupts!

Interrupt-driven I/O: allows overlap between CPU and I/O

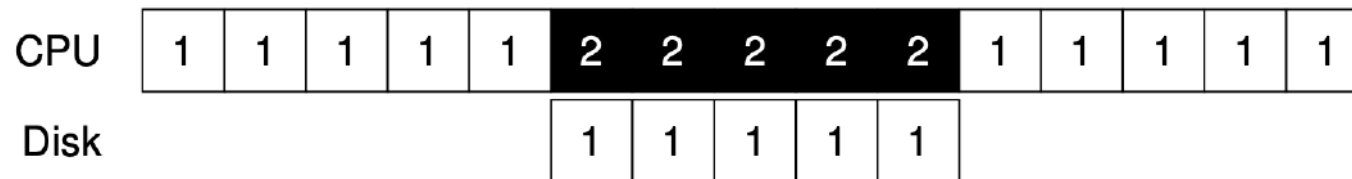


Process 1 runs for some time, issues the I/O request and, while the request is being served, the OS switches to **Process 2**

The I/O device will send an interrupt when done!

Lowering CPU Waste: Interrupts!

Interrupt-driven I/O: allows overlap between CPU and I/O



Process 1 runs for some time, issues the I/O request and, while the request is being served, the OS switches to **Process 2**

Is Interrupt-driven I/O **always** better than
Programmed I/O + Polling?

Lowering CPU Waste: Interrupts!

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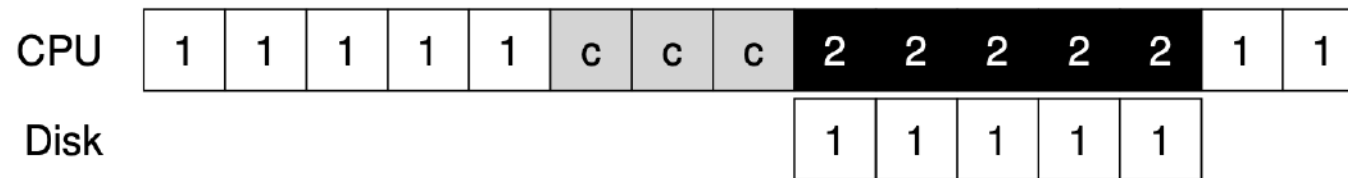
Process 1 runs for some time, issues the I/O request and, while the request is being served, the OS switches to **Process 2**

Is Interrupt-driven I/O **always** better than
Programmed I/O + Polling?

NO! It depends on the speed of the I/O device/task

Beyond Programmed-I/O

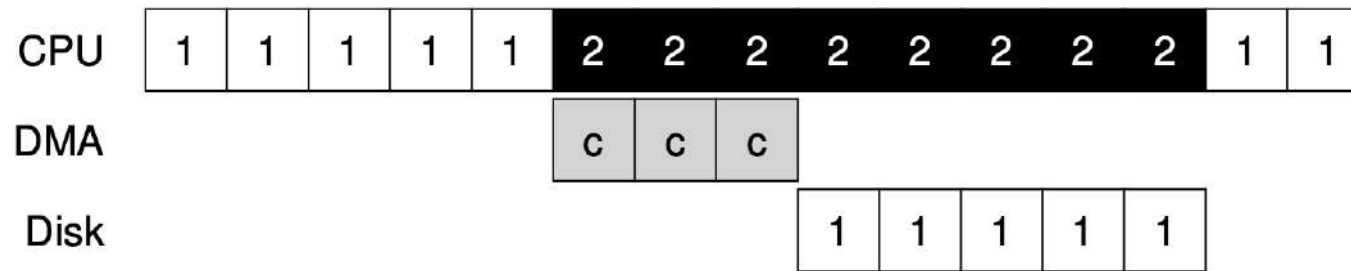
Programmed I/O: the CPU actually transfers data to I/O devices



Process 1 runs for some time, starts the I/O request by copying data from main memory to the I/O device one word at a time (c); when this is done the I/O begins and the OS switches to **Process 2**

Direct Memory Access (DMA)

DMA: a dedicated component to orchestrate memory-I/O transfers



Process 1 runs for some time, the OS starts the I/O by issuing a DMA request, then immediately switches to **Process 2**. Once the whole I/O task is done, the DMA controller sends an interrupt

To Wrap Up: Performing I/O Tasks

- **Polling**

- CPU periodically checks for the I/O task status

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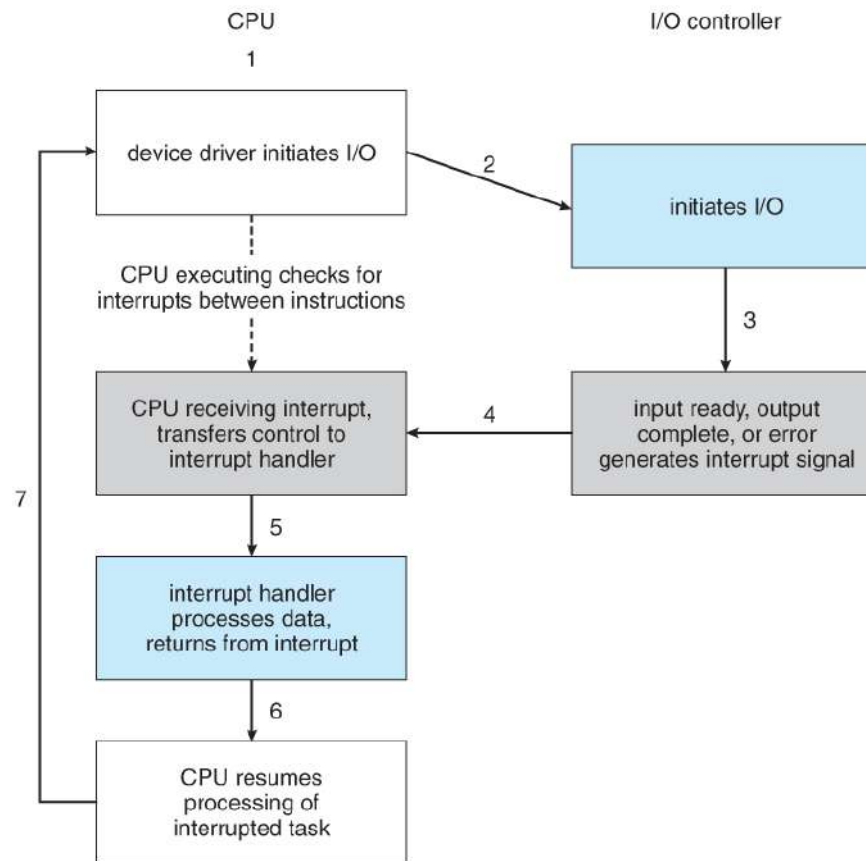
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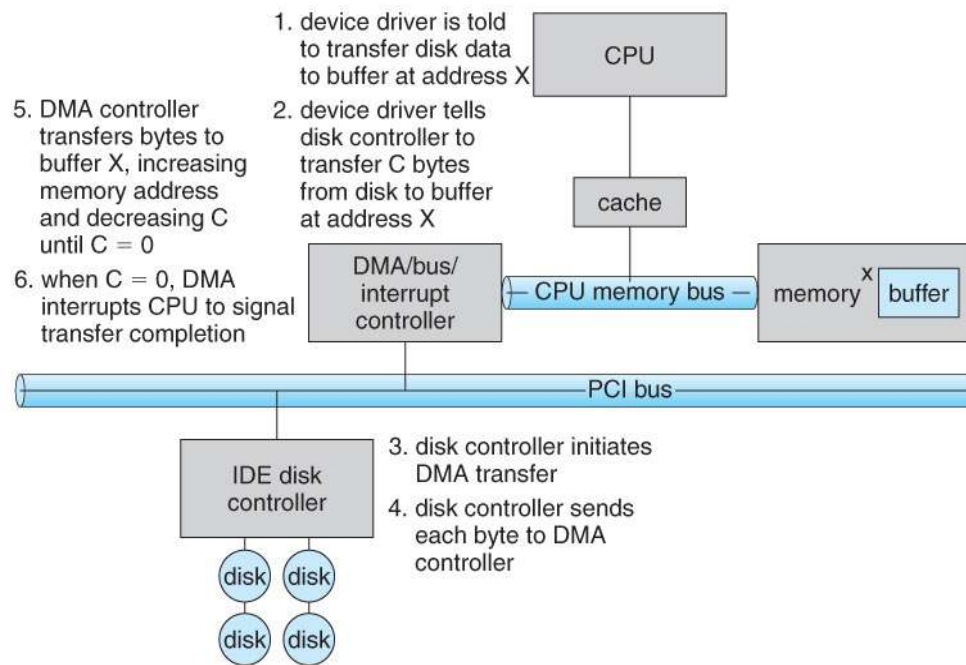
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WHO?

How: Interrupt-driven I/O



Who: Direct Memory Access (DMA)



Overcome the limitation of Programmed I/O

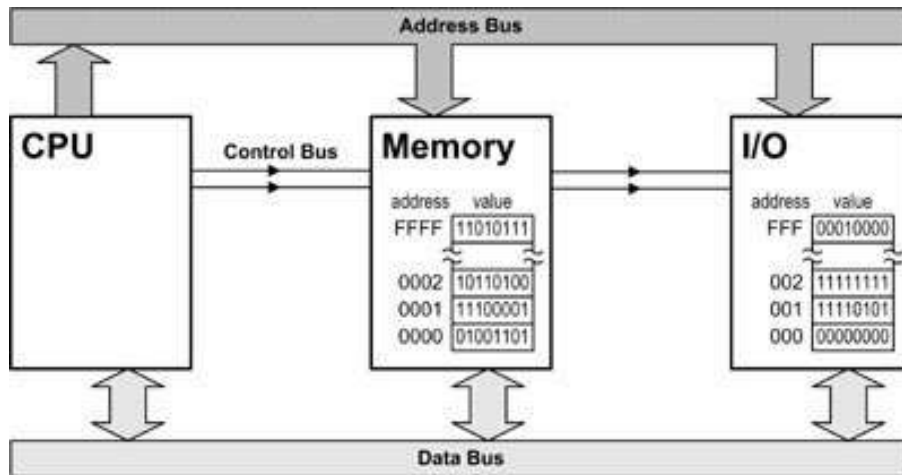
Maybe wasteful to tie up the CPU transferring data in and out of registers **one word at a time**

Useful for devices that transfer large quantities of data (such as disk controllers)

Typically, used in combination with **interrupt-driven I/O**

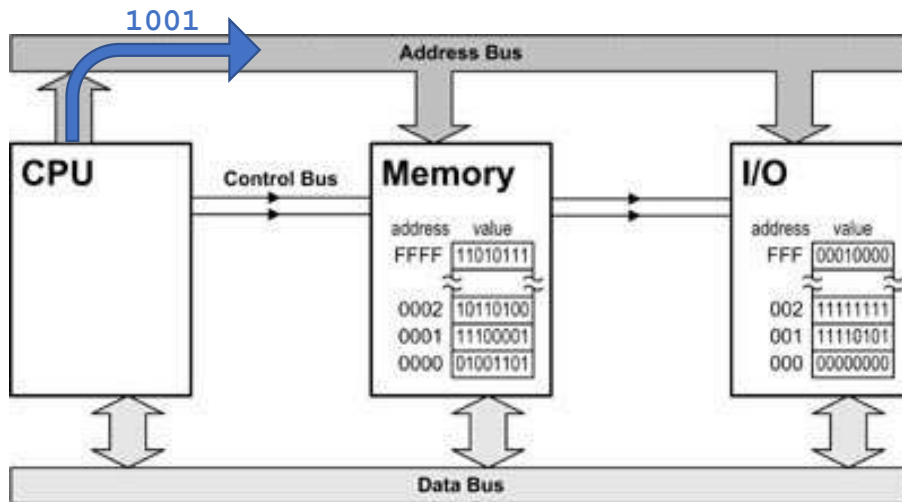
But how does the CPU/OS actually
communicate with I/O devices?

Addressing Using the System Bus



How does CPU reference Memory addresses?

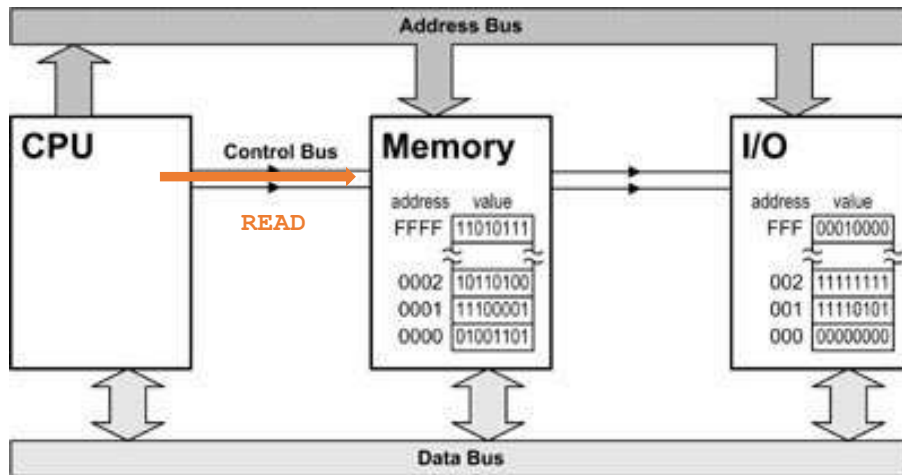
Addressing Using the System Bus



How does CPU reference Memory addresses?

It puts the address of a byte of memory on the address bus

Addressing Using the System Bus

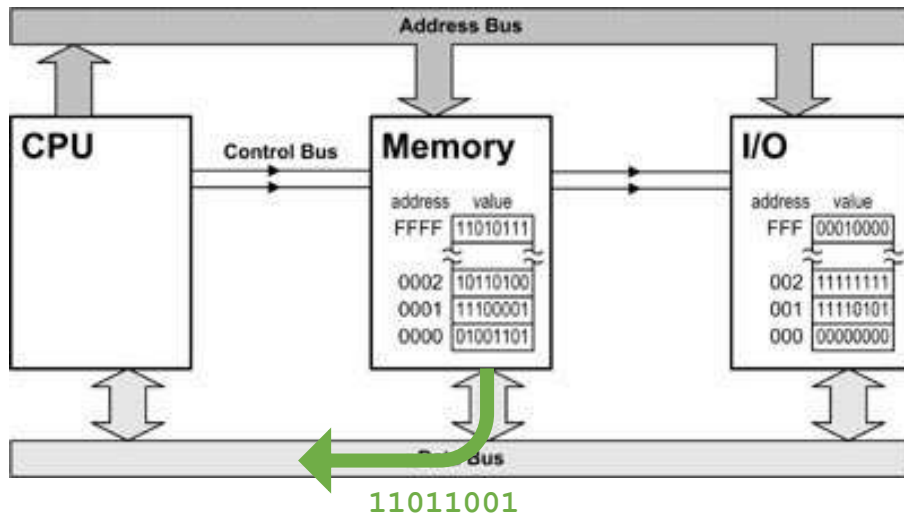


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Addressing Using the System Bus



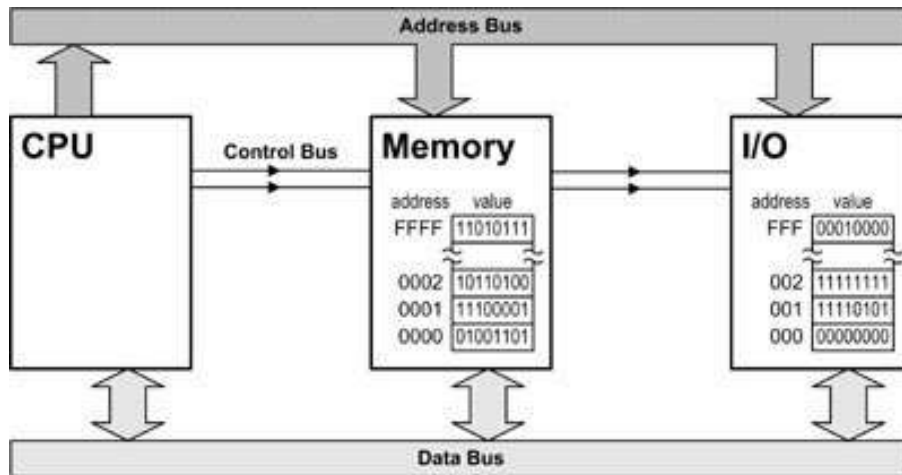
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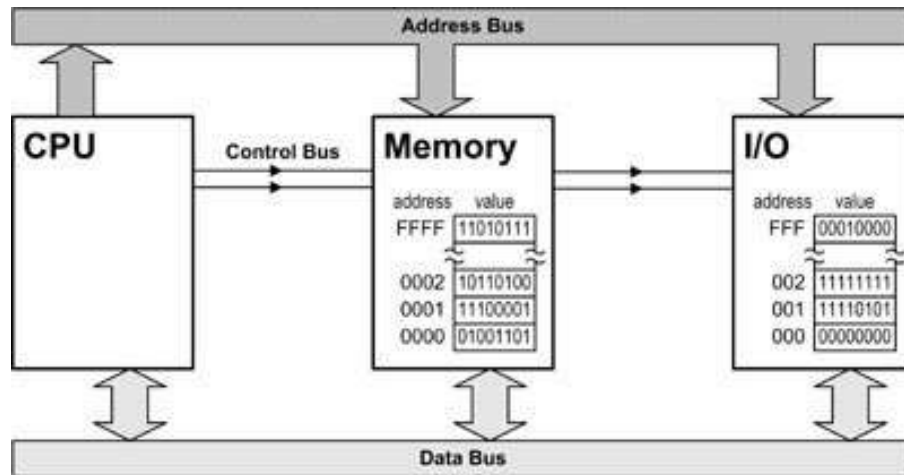
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How about I/O devices? How to distinguish between Memory and I/O devices?

Addressing Using the System Bus



How does CPU reference Memory addresses?

It puts the address of a byte of memory on the address bus

It raises the **READ** signal on the control bus

Eventually, the RAM replies with the memory content on the data bus

If the control bus is shared between memory and I/O there is a special line called "**M/#IO**" that asserts whether the CPU wants to talk to memory or an I/O device

Port- vs. Memory-Mapped I/O

- CPU can talk to a device controller in **2 ways**:

Port- vs. Memory-Mapped I/O

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 - **Port-mapped I/O** → referencing controller's registers using a separate I/O address space

Port- vs. Memory-Mapped I/O

- CPU can talk to a device controller in **2 ways**:
 - **Port-mapped I/O** → referencing controller's registers using a separate I/O address space
 - **Memory-mapped I/O** → mapping controller's registers to the same address space used for main memory

Port-Mapped I/O

- Each I/O device controller's register is mapped to a specific port (address) at boot-up time
- Requires special class of CPU instructions (e.g., **IN**/**OUT**)
 - The **IN** instruction reads from an I/O device, **OUT** writes to it
- With the **IN** or **OUT** instructions, the **M/#IO** is not asserted, so memory does not respond and the I/O chip does

Memory-Mapped I/O

- Memory-mapped I/O "wastes" some address space but doesn't need any special instruction
- To the CPU, I/O device ports are just like normal memory addresses mapped into RAM at boot-up time
- The CPU uses `MOV`-like instructions to access I/O device registers
- The **M/#IO** is always asserted indicating the address requested by the CPU refers to main memory

Port- vs. Memory-Mapped I/O

```
MOV DX,1234h  
MOV AL,[DX]      ;reads memory address 1234h (memory address space)  
IN AL,DX         ;reads I/O port 1234h (I/O address space)
```

Both put the value **1234h** on the CPU address bus,
and both assert a **READ** operation on control bus

Port- vs. Memory-Mapped I/O

```
MOV DX,1234h  
MOV AL,[DX]    ;reads memory address 1234h (memory address space)  
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The first one will assert **M/#IO** to indicate that the address belongs to memory address space

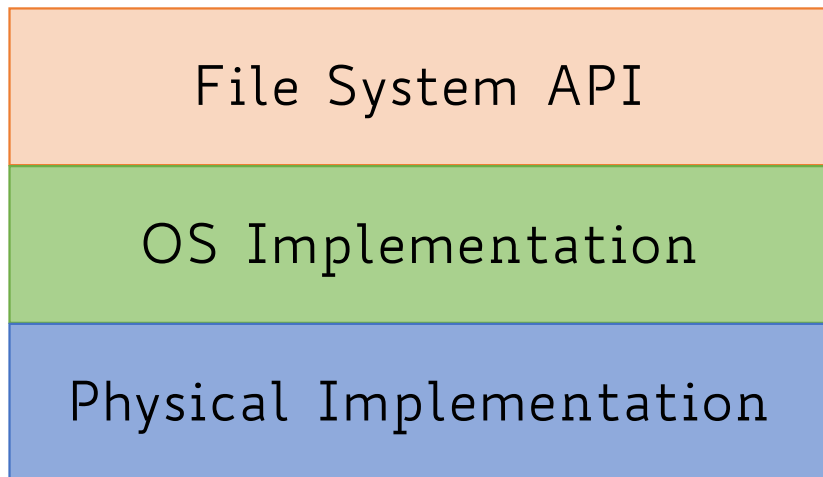
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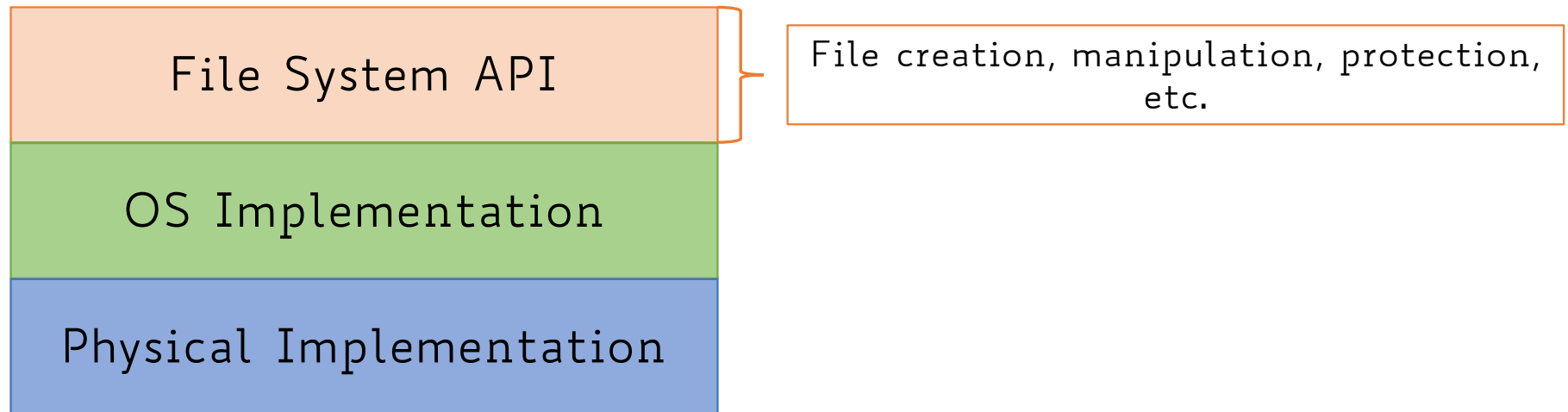
The second one will **not** assert **M/#IO** to indicate that the address belongs to I/O address space

Part V: Storage Management

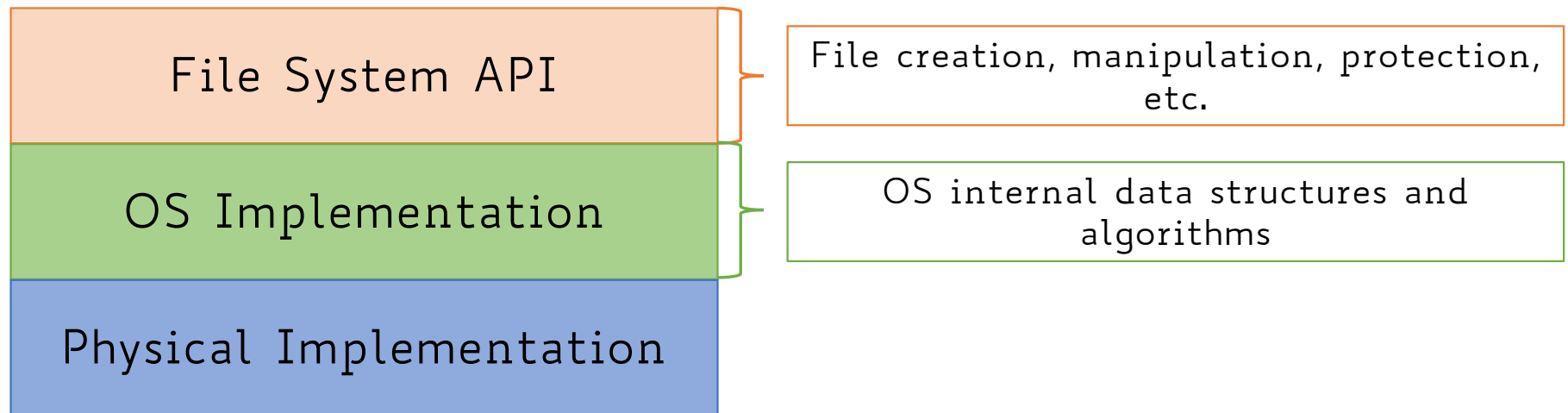
File System's Logical View



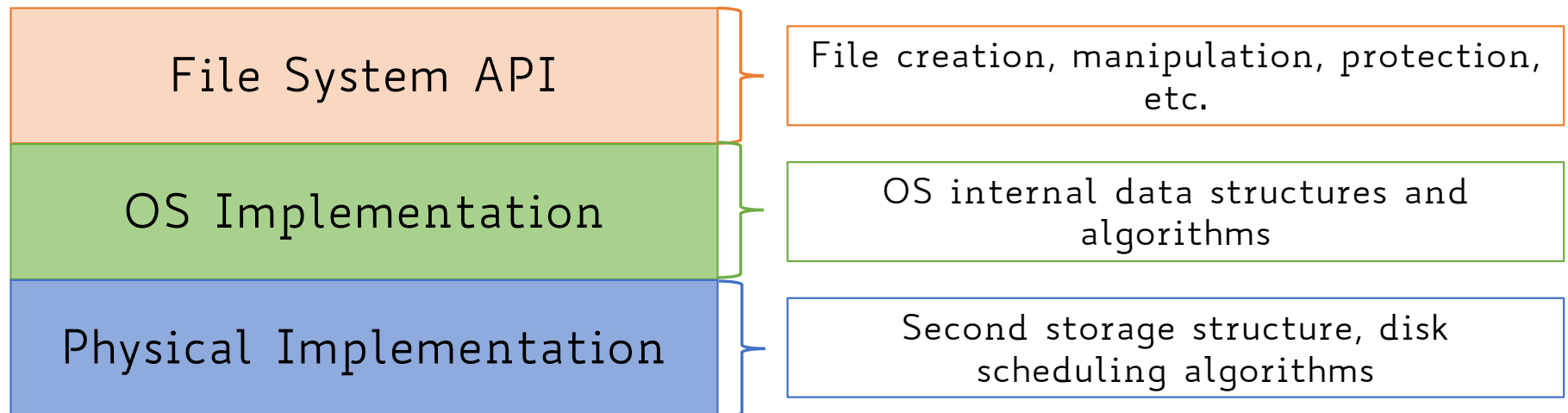
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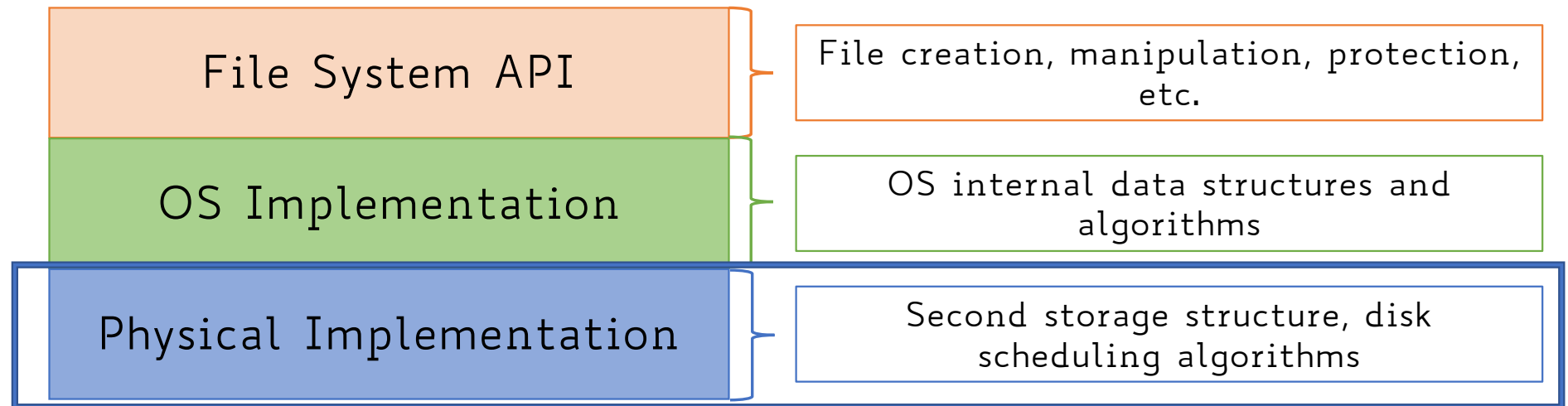
File System's Logical View



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File System's Logical View



Overview of Mass-Storage Structure

3 categories of mass-storage devices

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3 categories of mass-storage devices

Magnetic Disks



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3 categories of mass-storage devices

Magnetic Disks



Solid-State Disks



Overview of Mass-Storage Structure

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Magnetic Disks



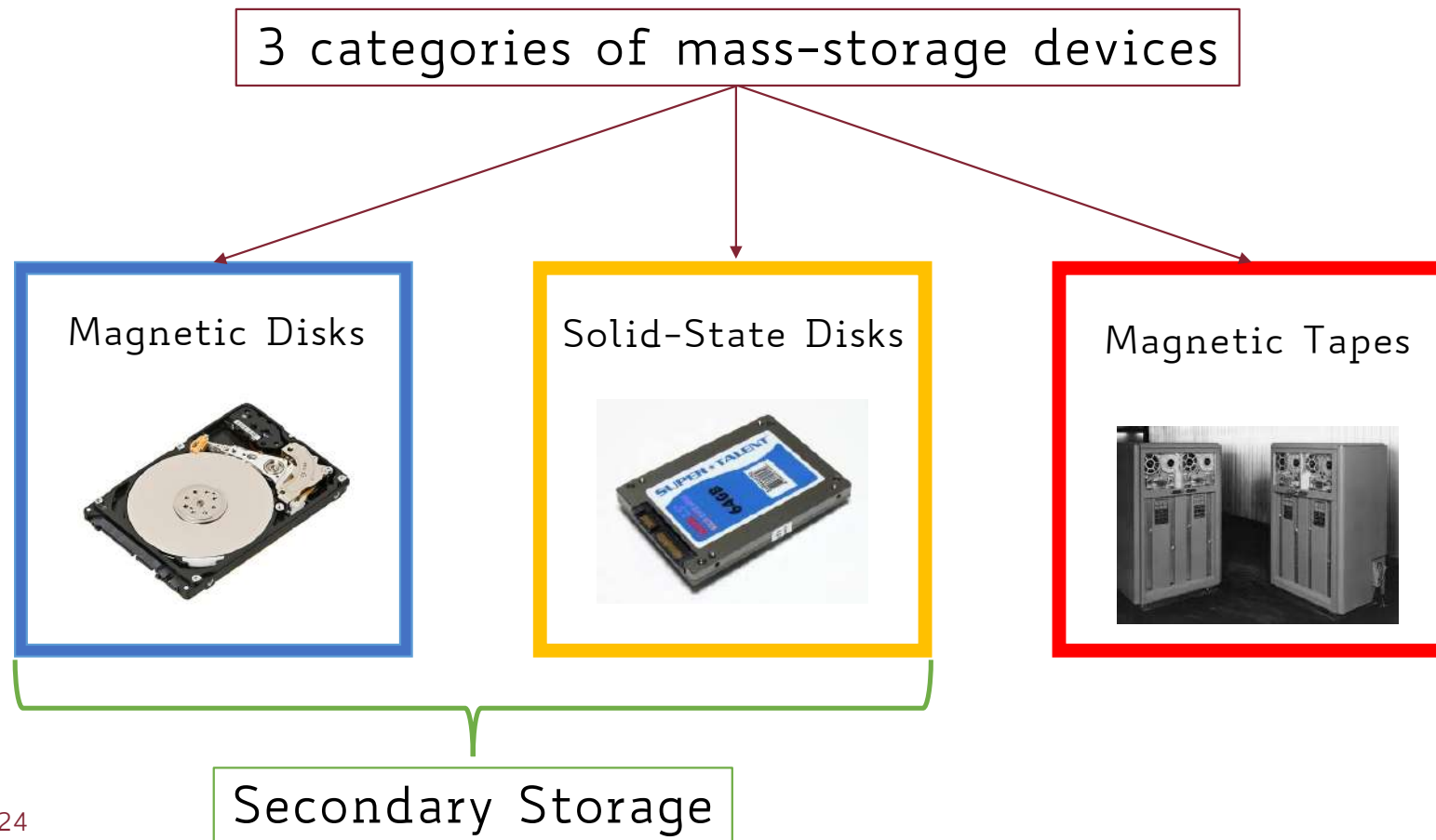
Solid-State Disks



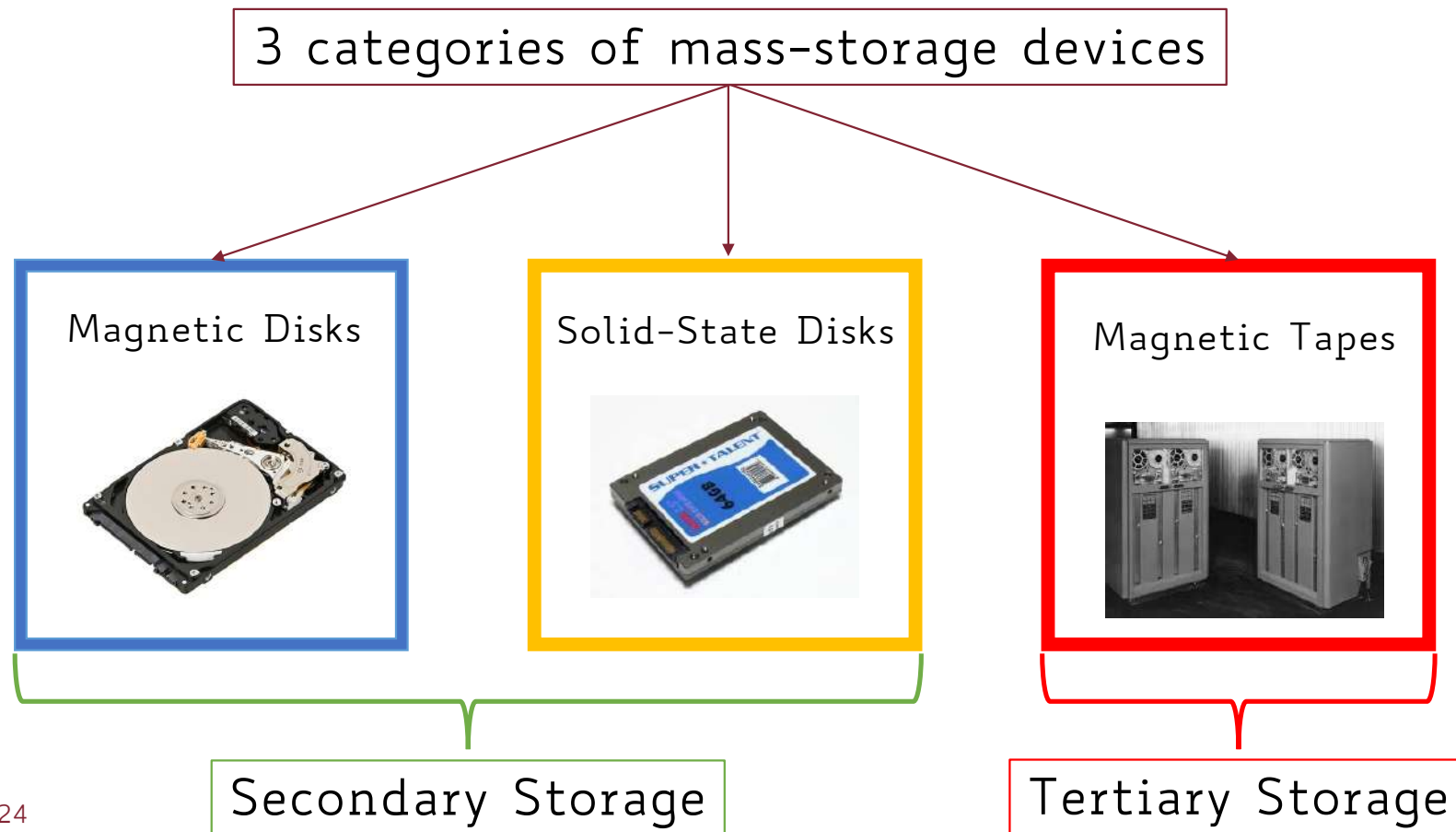
Magnetic Tapes



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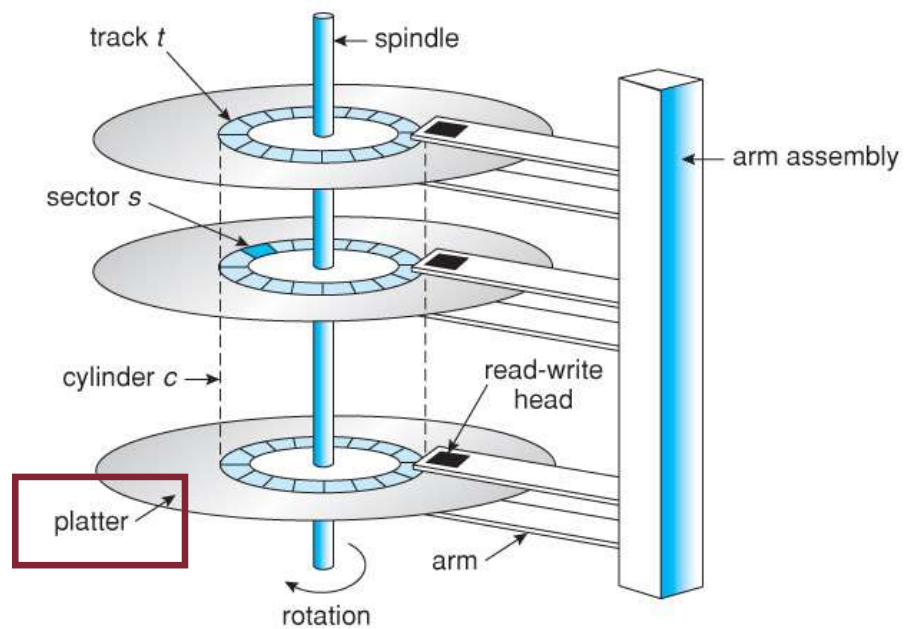
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Magnetic Tapes

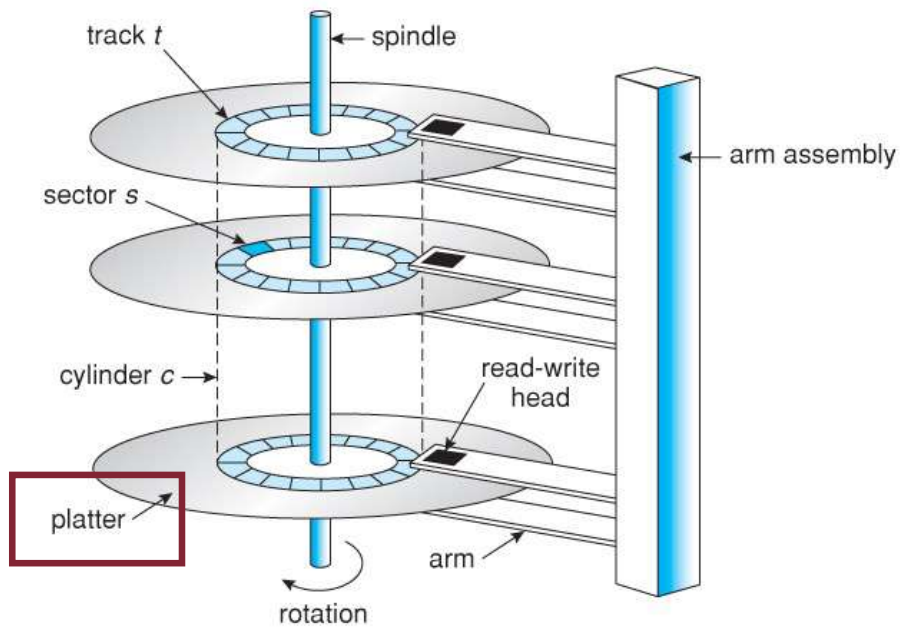


Magnetic Disks: Structure



One or more **platters** covered with **magnetic media**

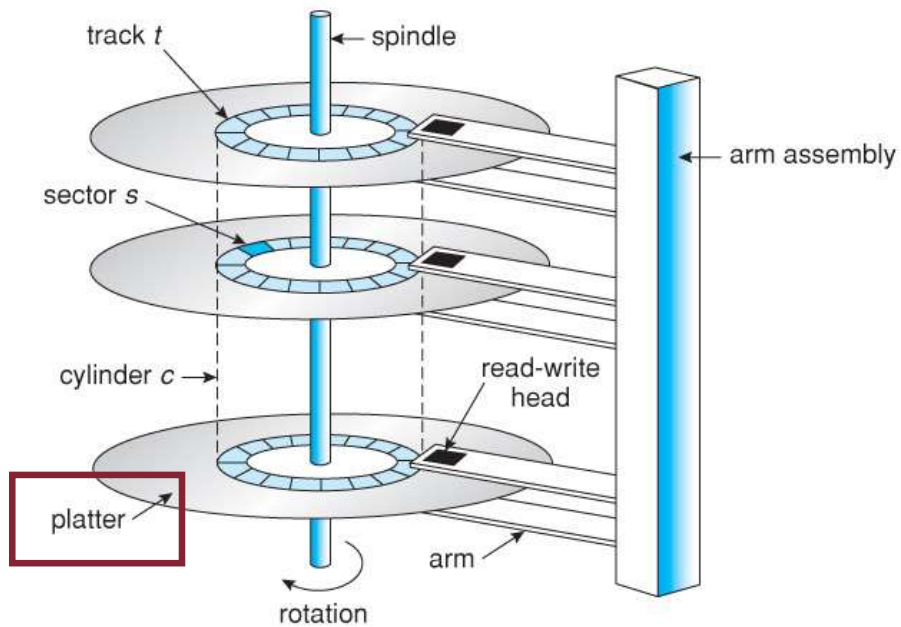
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Hard disk
rigid metal

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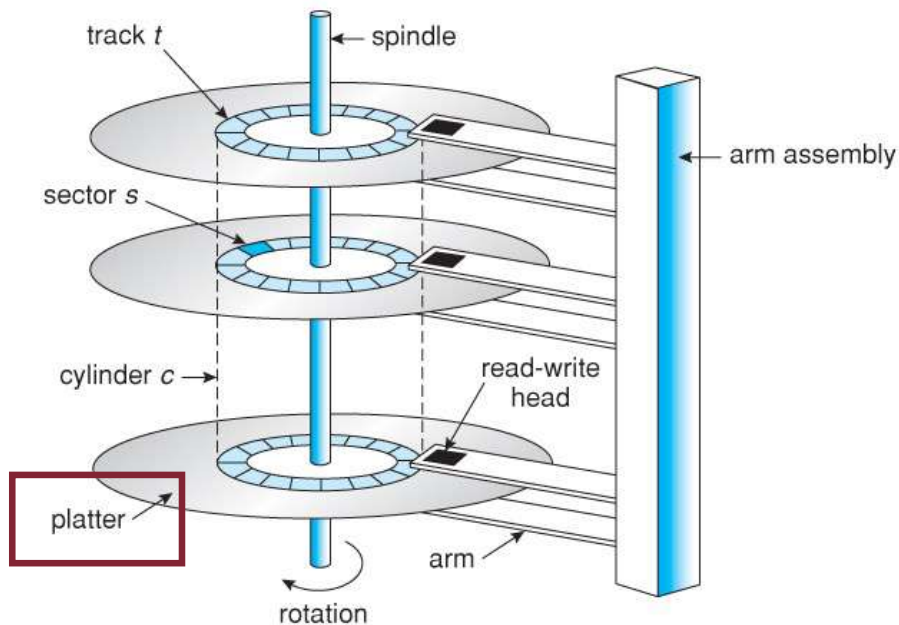


One or more platters covered with magnetic media

Hard disk
rigid metal

Floppy disk
flexible plastic

Magnetic Disks: Structure



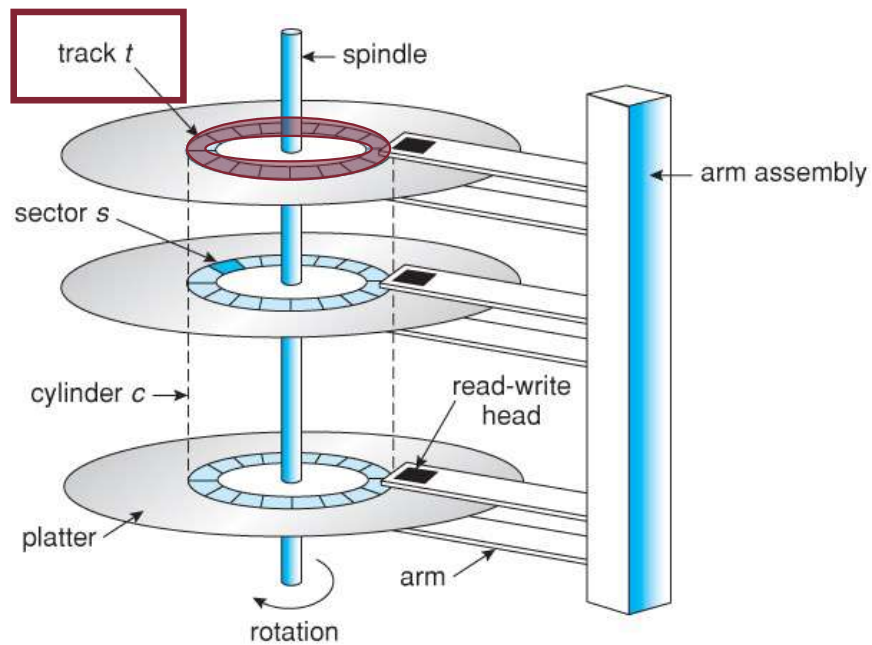
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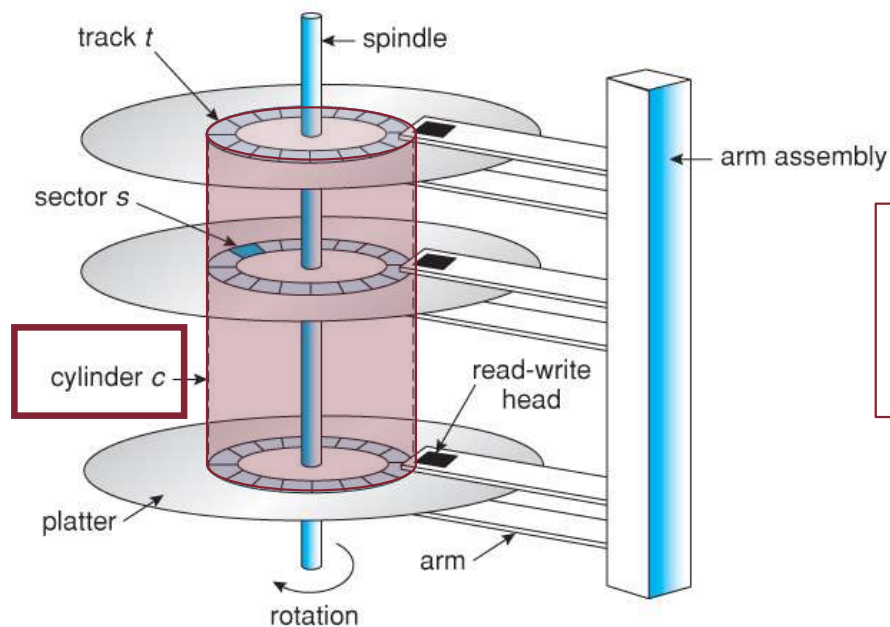
Each platter has **2** working **surfaces**

Magnetic Disks: Tracks and Cylinders



Each surface is divided into a number of concentric rings, called **tracks**

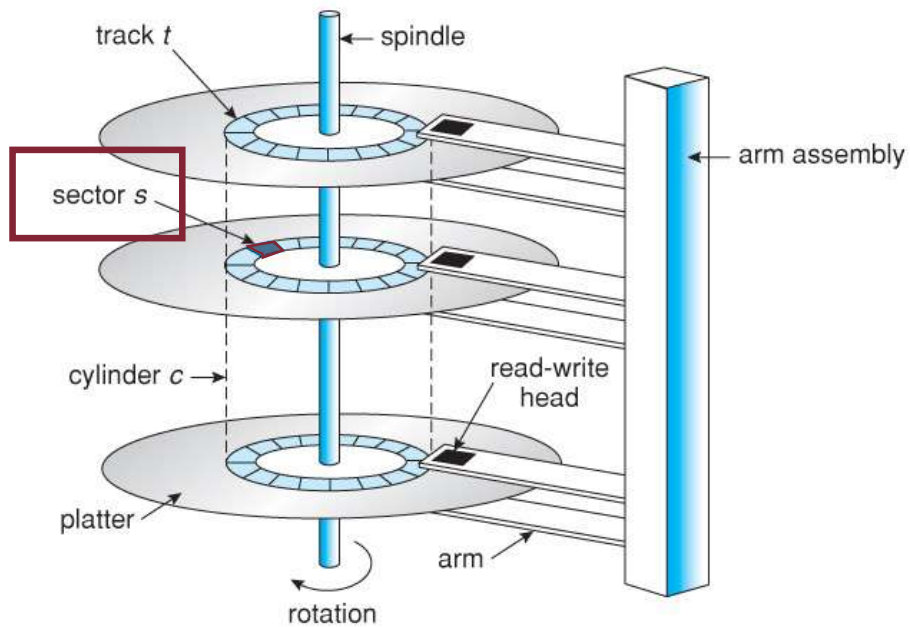
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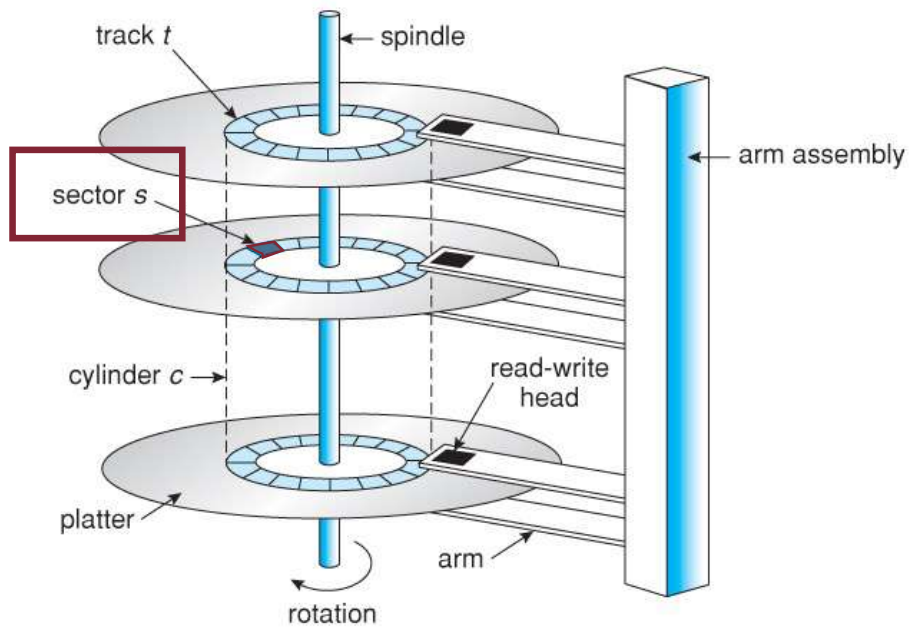
The set of all tracks that are the same distance from the edge of the platter is called a **cylinder**

Magnetic Disks: Sectors



Each track is further divided into sectors

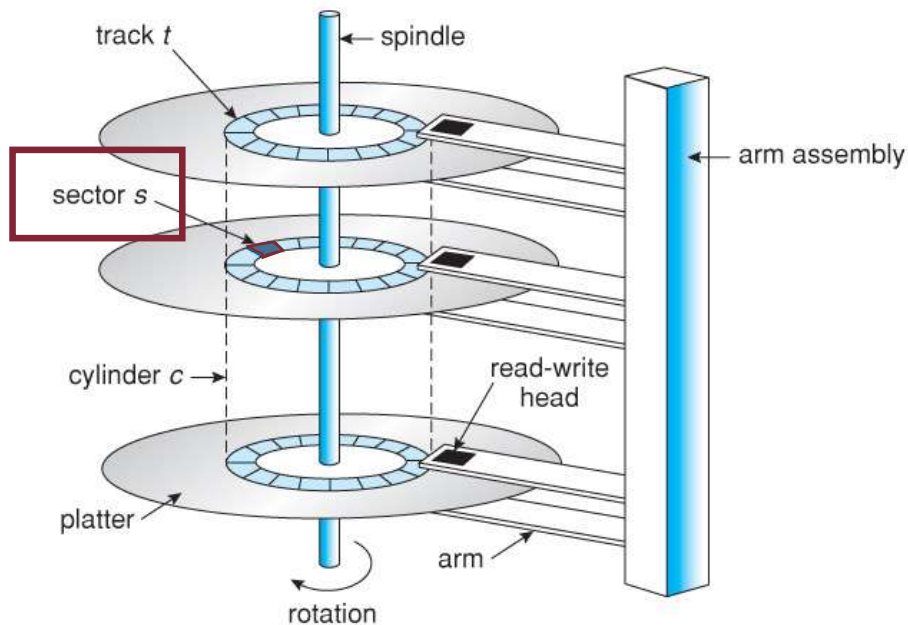
Magnetic Disks: Sectors



Each track is further divided into **sectors**

Each sector usually contains 512 bytes

Magnetic Disks: Sectors

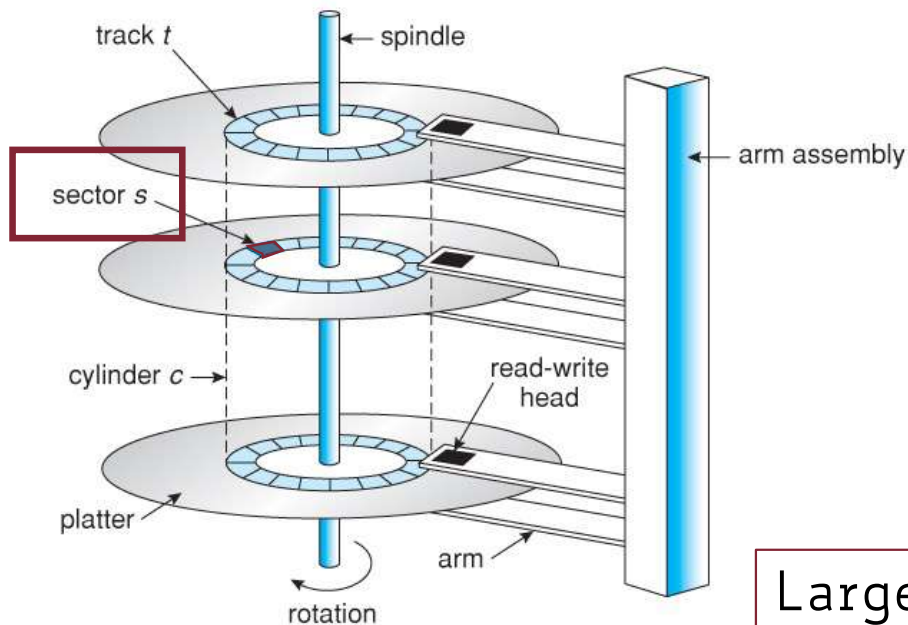


Each track is further divided into **sectors**

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Sectors also include a header and a trailer, and checksum information

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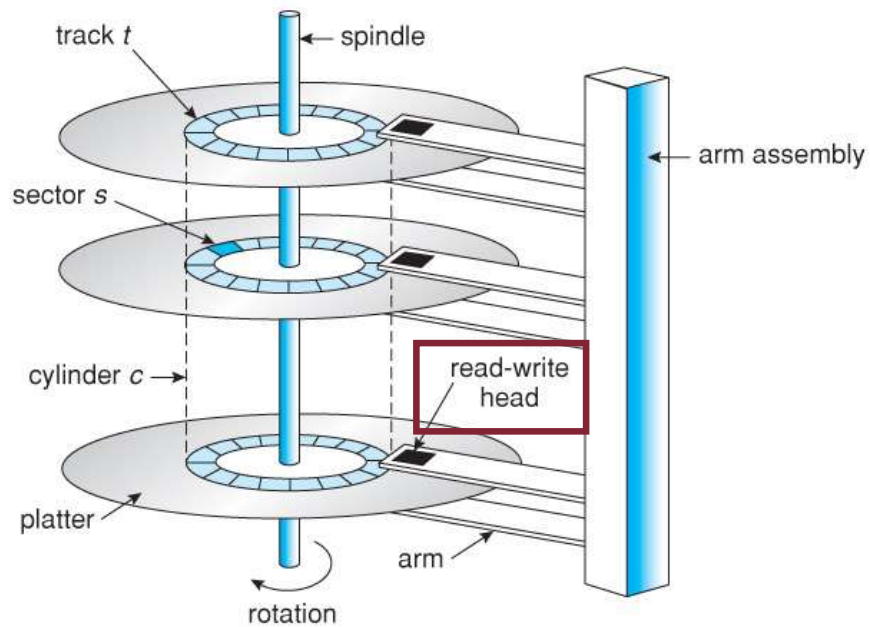
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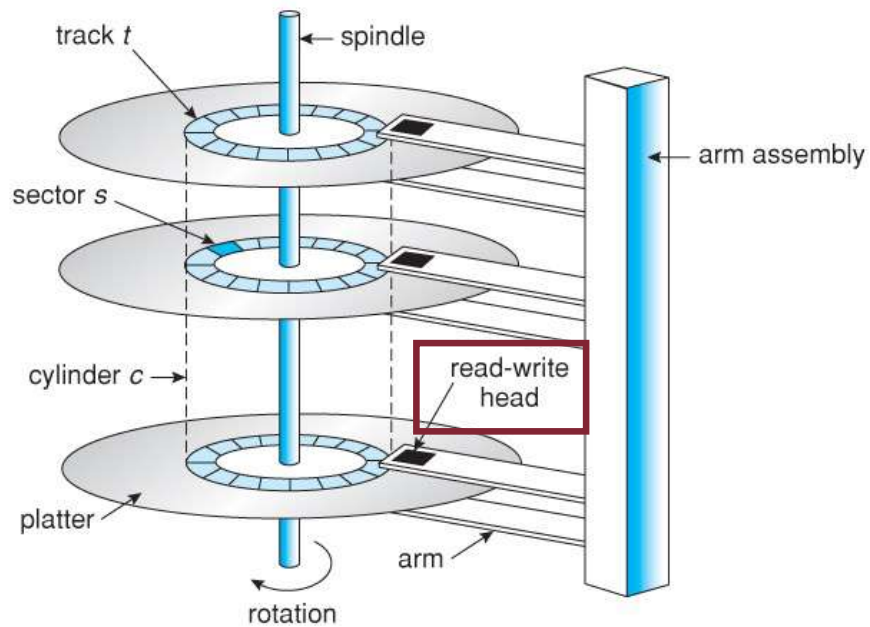
Larger sector sizes reduce the space wasted by headers and trailers, but increase internal fragmentation

Magnetic Disks: Heads

Data on hard drive is read by
read-write heads



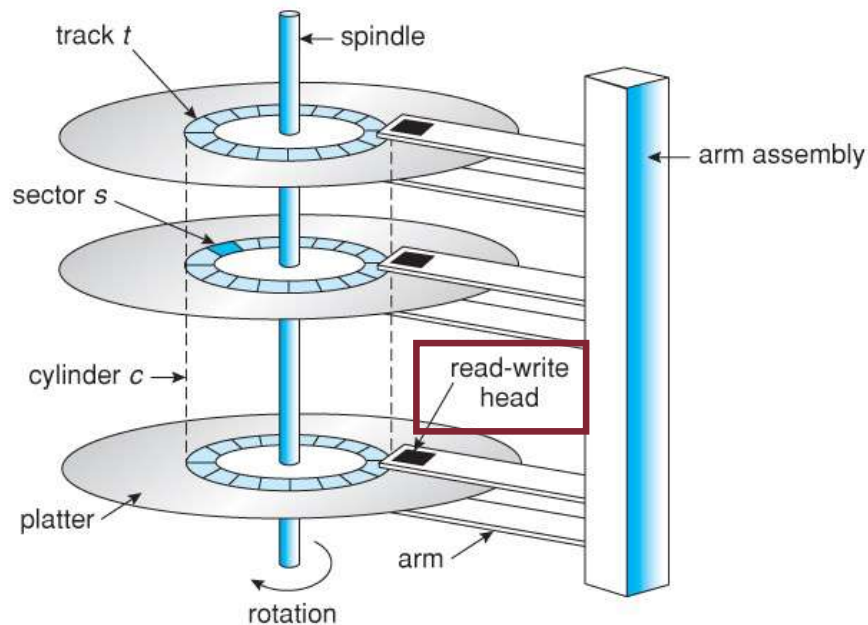
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Standard configuration uses
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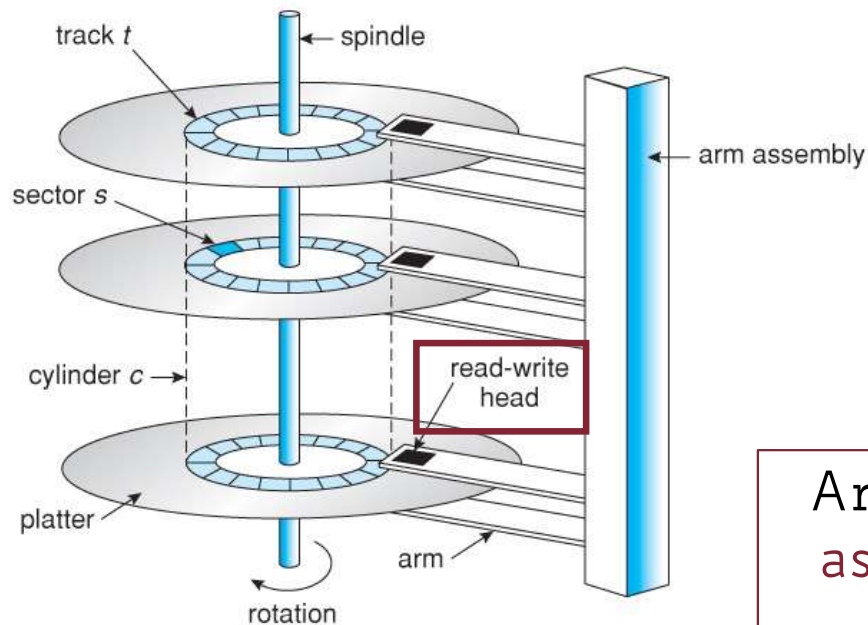


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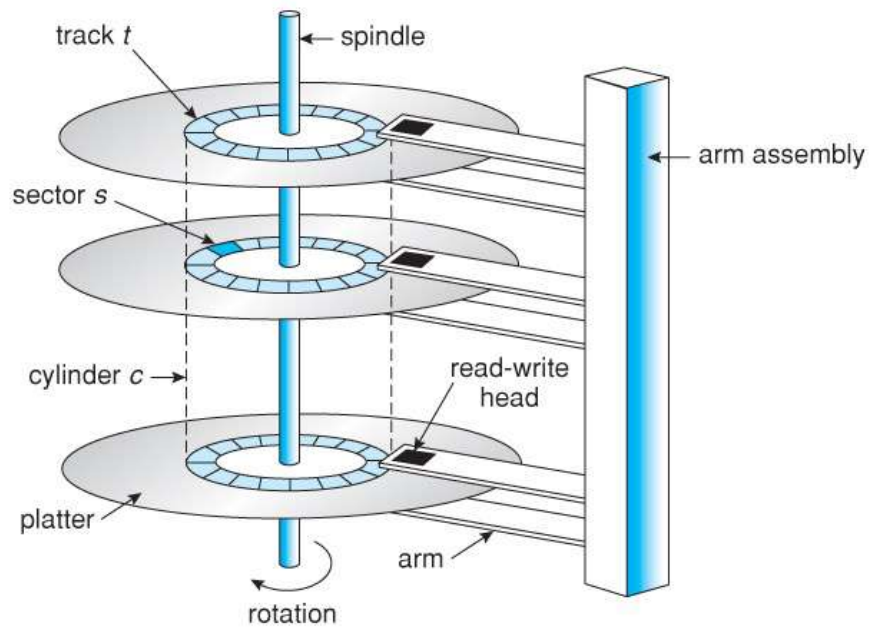
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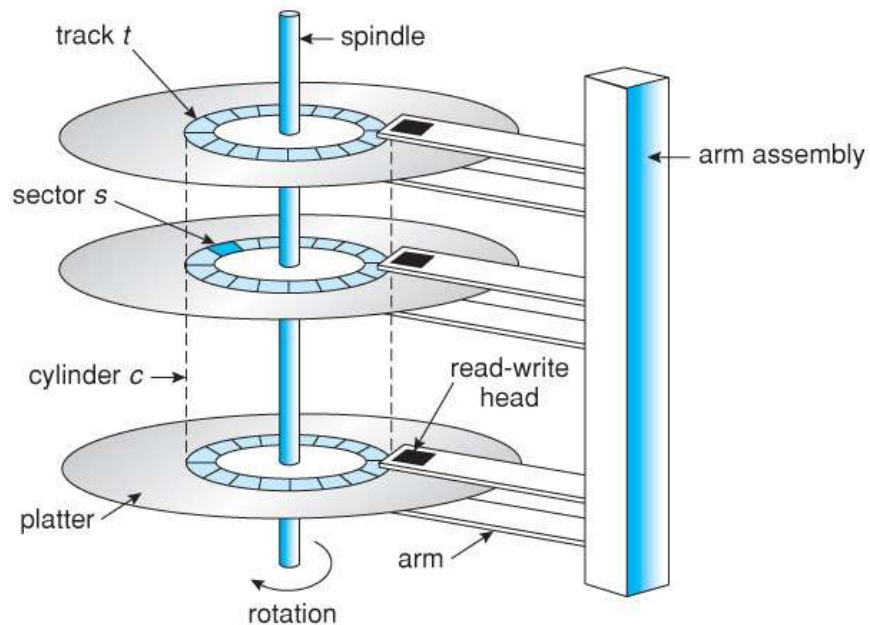
Arms are controlled by a common **arm assembly** moving simultaneously from one cylinder to another

Magnetic Disks: Storage Capacity

H = number of heads (working surfaces)



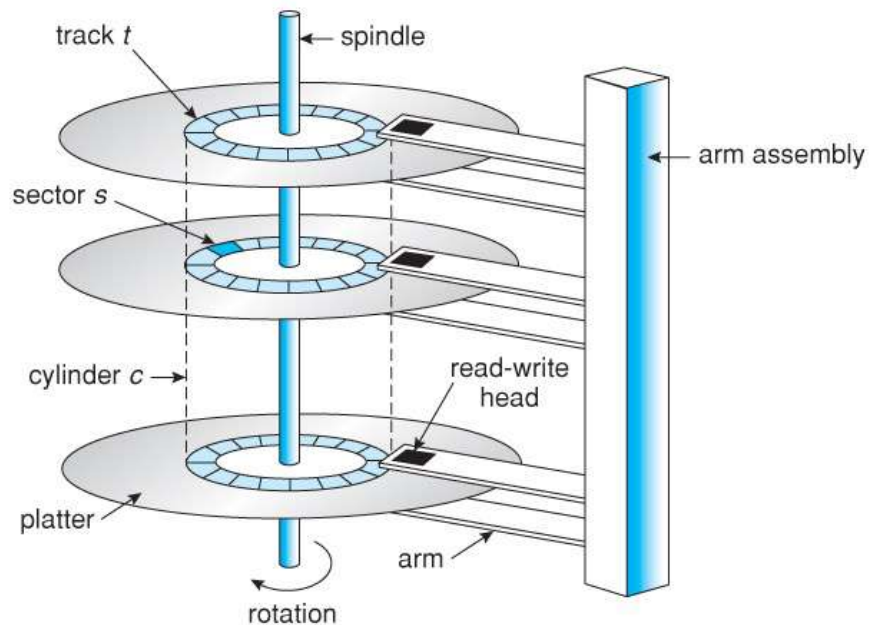
Magnetic Disks: Storage Capacity



H = number of heads (working surfaces)

T = number of tracks per surface

Magnetic Disks: Storage Capacity

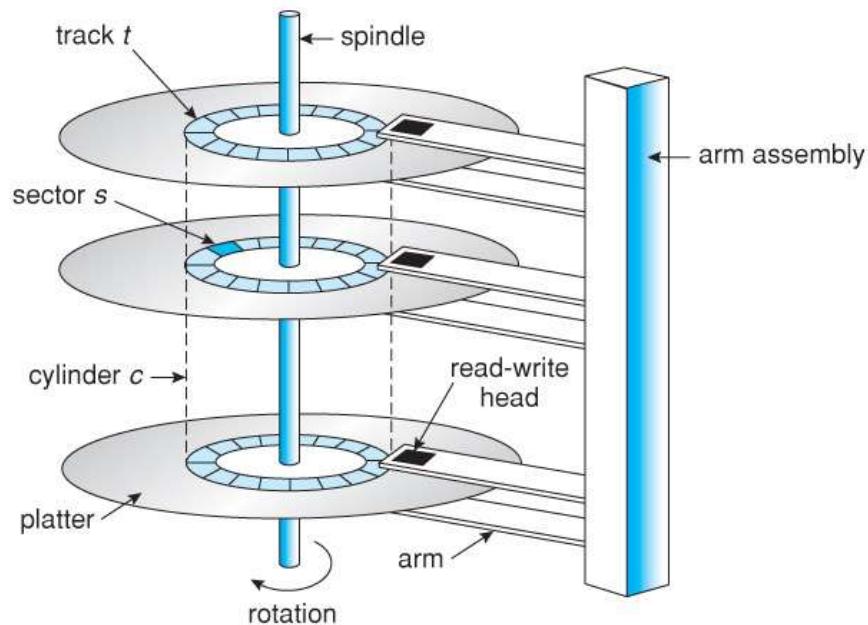


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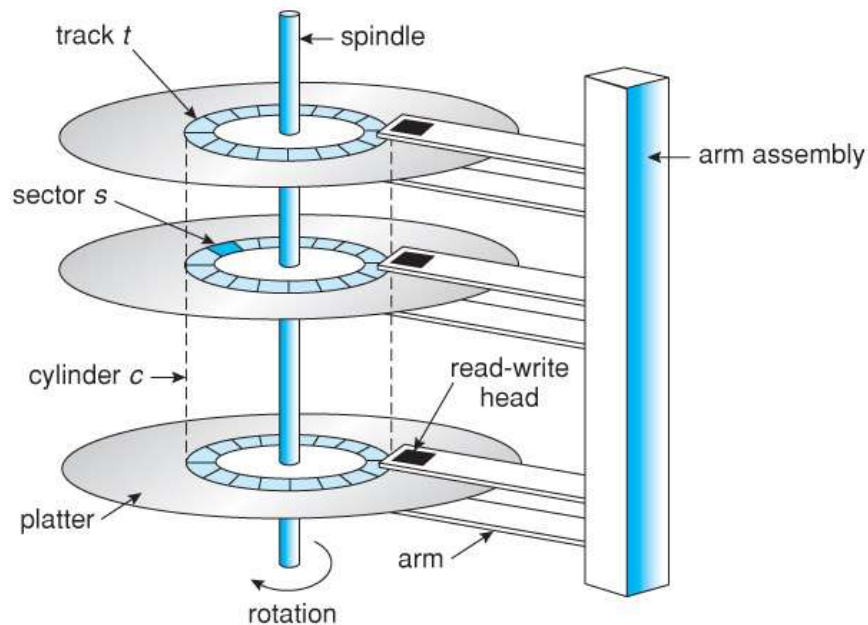
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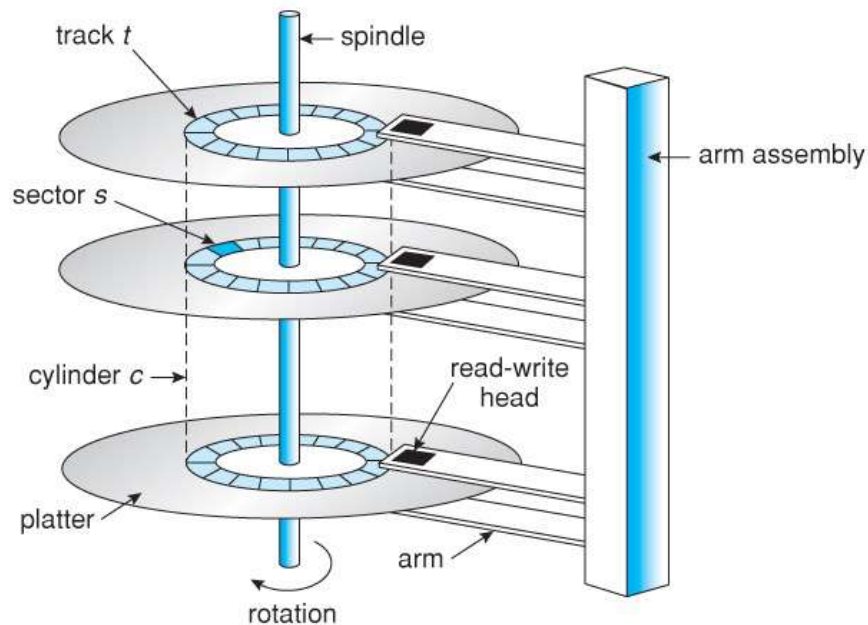
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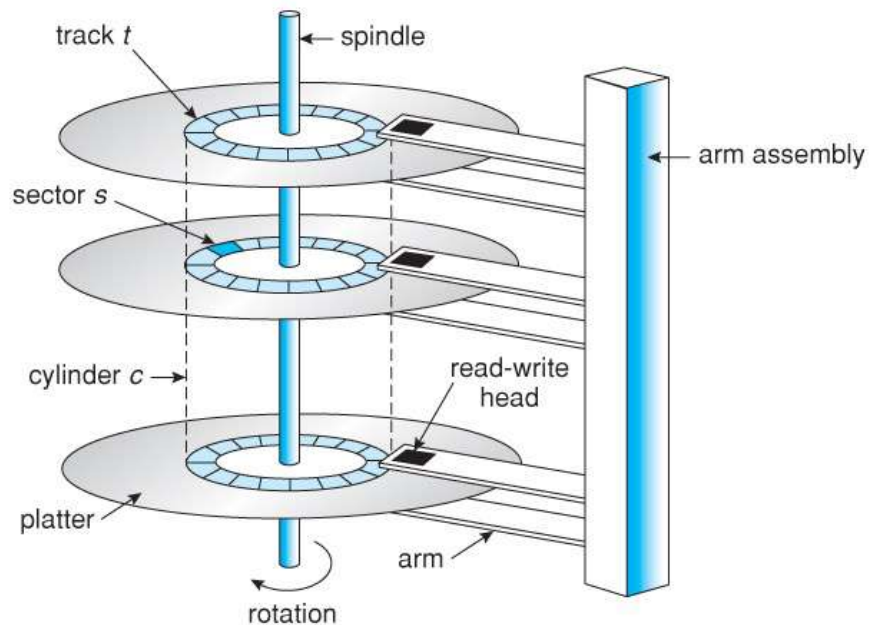
OVERALL CAPACITY

Magnetic Disks: Storage Capacity

Until the end of 1980s, every track had the same number of sectors with the same number of bits



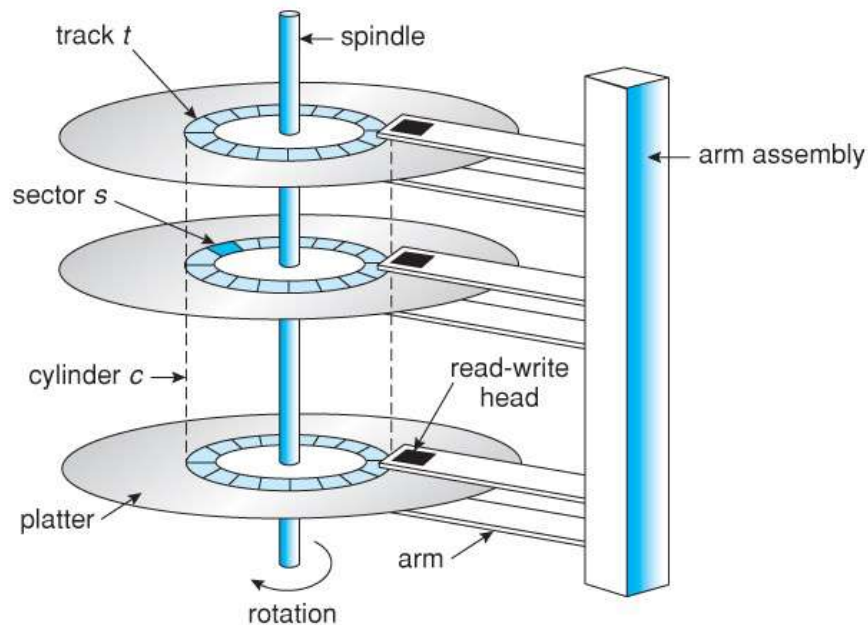
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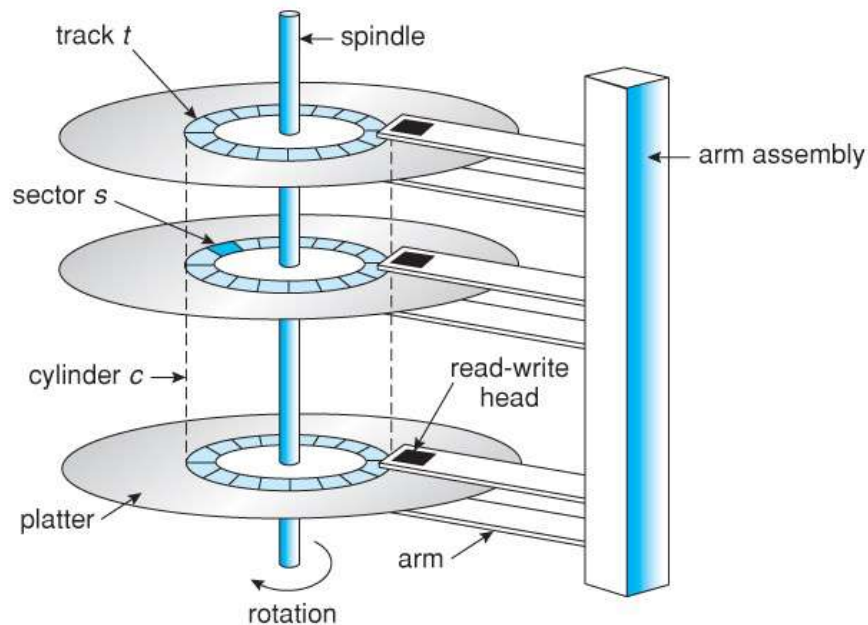


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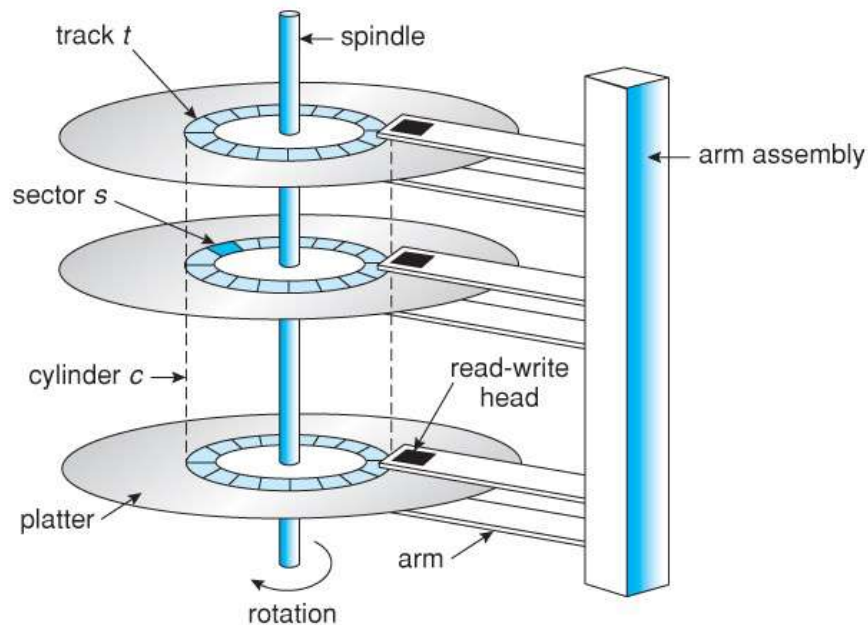
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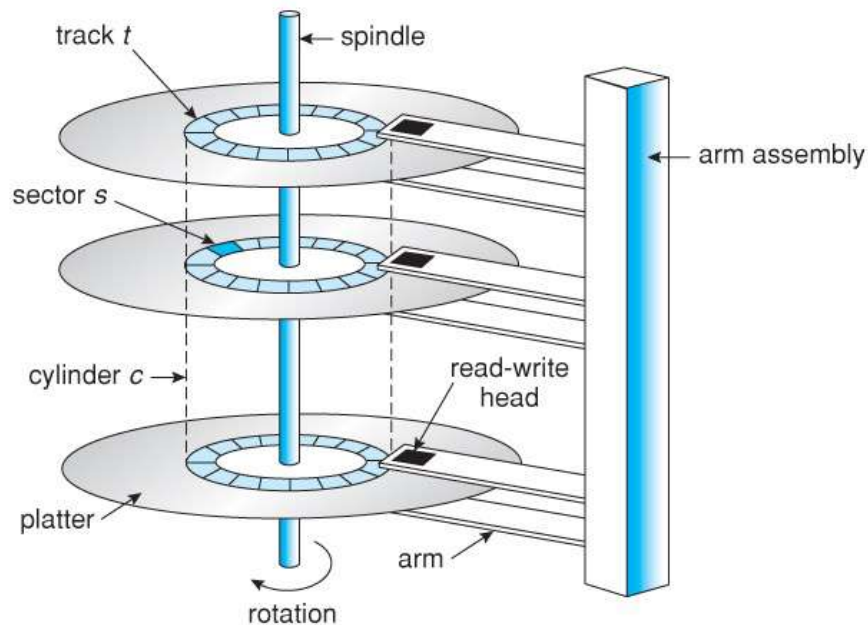
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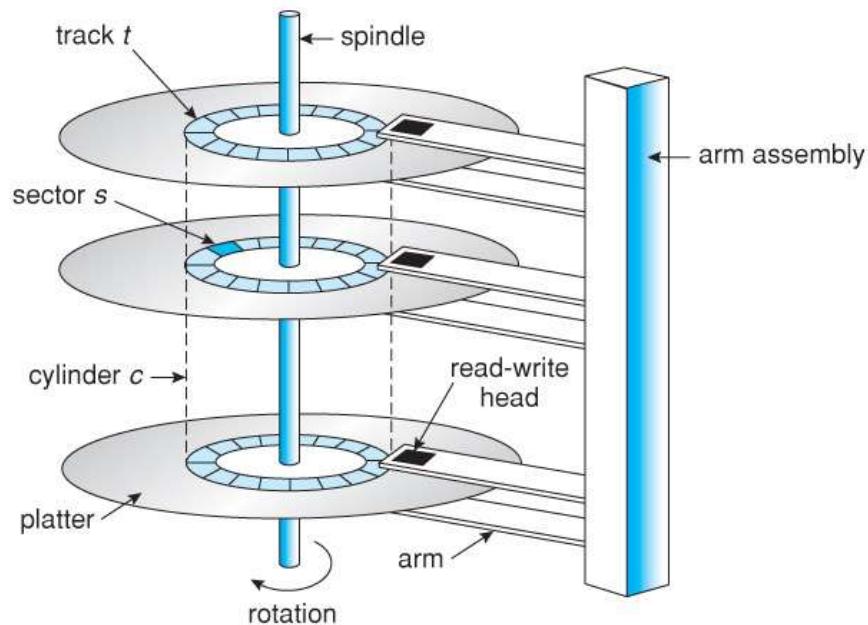
- The capacity of the disk was determined by the maximum bit density a controller could handle
- Different frequencies and timing from innermost to outermost tracks

Magnetic Disks: Storage Capacity



In practice, the number of sectors per track (S) varies with the radius of the track on the platter

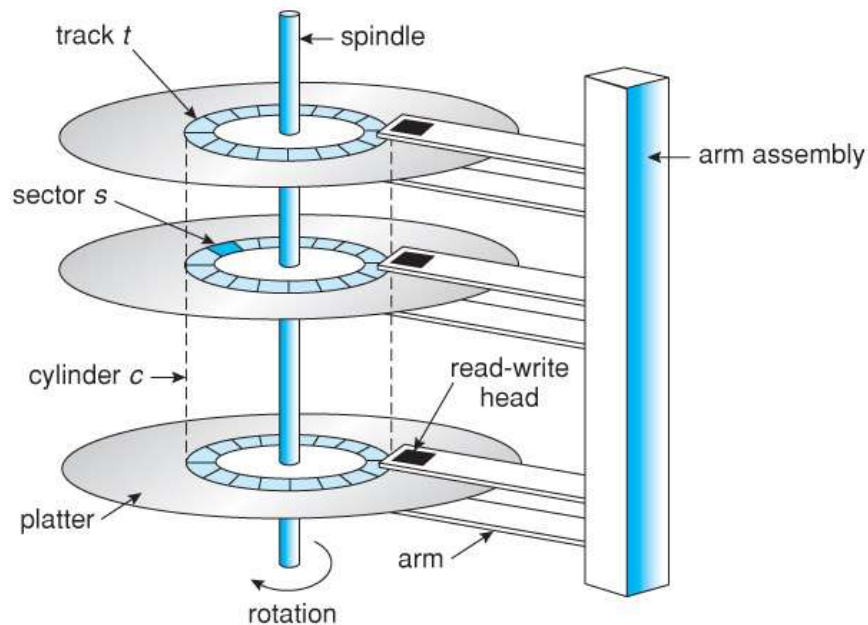
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In practice, the number of sectors per track (S) varies with the **radius** of the track on the platter

The outermost track is larger and can hold more sectors than the inner ones

Magnetic Disks: Storage Capacity

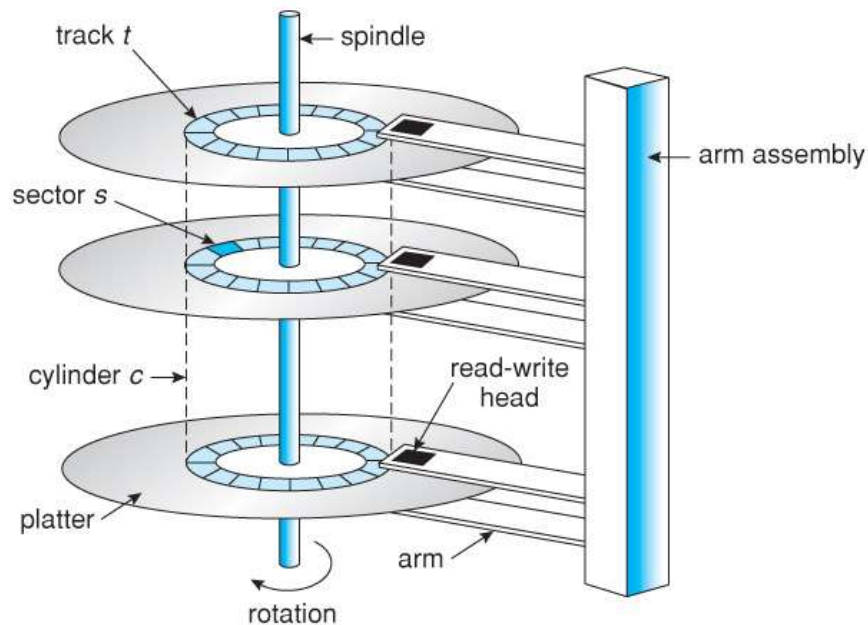


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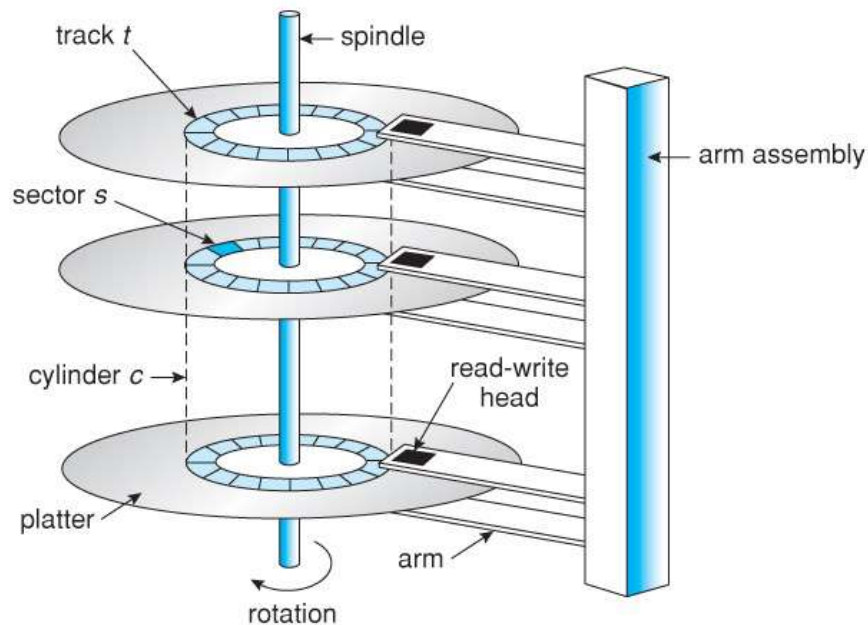
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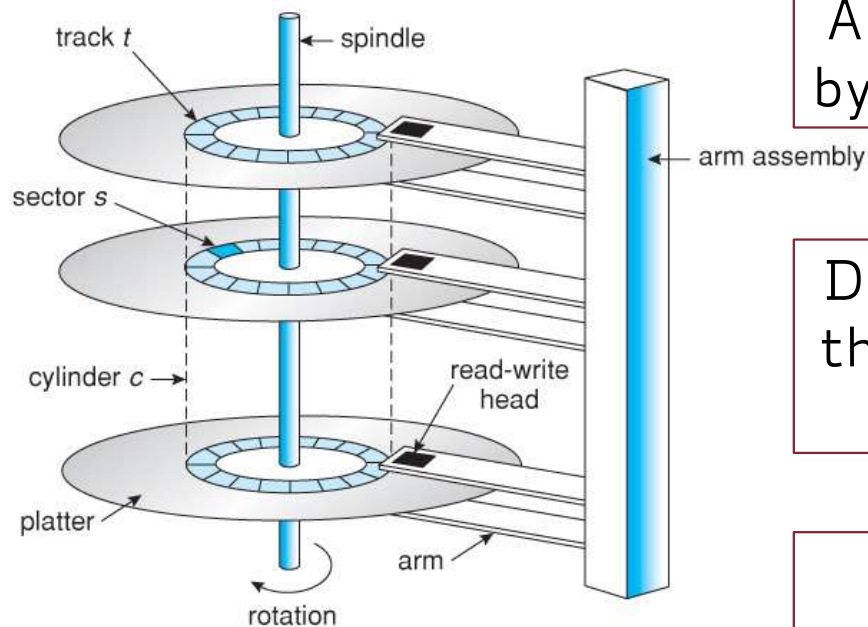
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Zone Bit Recording (ZBR)

Magnetic Disks: (Logical) Referencing



A physical block of data is specified by the (head, cylinder, sector) number

Disk blocks are numbered starting at the outermost cylinder, identified by 0

Note that cylinder coincides with track

Magnetic Disks: Data Transfer

- The disk rotates at **constant angular speed** (e.g., **7200 rpm = 120 rps**)

Magnetic Disks: Data Transfer

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- Outer tracks spin **faster** than inner tracks (more sectors traversed in the same amount of time due to larger radius → more sectors per zone in ZBR)

Magnetic Disks: Data Transfer

- Data transfer from the disk to memory is made of **3 steps**:
 - **positioning time** (seek time or random access time)
 - **rotational delay**
 - **transfer time**

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- Includes the time needed for the heads to settle
- Depends on how fast the hardware moves the arm
- Typically, the slowest step in the entire process

Bottleneck of overall disk data transfer

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 - 0 \rightarrow the sector is already underneath the head
 - full revolution \rightarrow the sector is the one before but in the opposite direction
- On average, **0.5 revolutions** (r)
 - E.g., for a 7200 rpm (120 rps) disk this equals to $0.5 \text{ r} / 120 \text{ rps}$
~4 msec

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Data Transfer Time = **Seek Time** + Rotational Delay + **Transfer Time**

Sometimes the term **transfer rate** is used to refer to the overall data transfer time

Magnetic Disks: Structure

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- The array of blocks is mapped onto disk sectors sequentially

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- Then through the rest of tracks in the same cylinder
- Then through other cylinders (from the outermost to innermost)

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- Head crash may permanently damage the disk or even destroy it
- To avoid such a risk, disk heads are "parked" when the computer is turned off

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- Disk drives are connected to the computer via the I/O bus
- Some of the common interface formats include:
 - Enhanced Integrated Drive Electronics (EIDE);
 - Advanced Technology Attachment (ATA) and Serial ATA (SATA);
 - Universal Serial Bus (USB);
 - Fiber Channel (FC);
 - Small Computer Systems Interface (SCSI)

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- Finally, data is transferred from that cache to the host controller and the motherboard memory at electronic speeds

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 - Seek Time
 - Rotational Delay
- To minimize data transfer time from disk we need to minimize those

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- Smaller disks → lower seek time, since arms have to travel smaller distance
- Fast-spinning disks → lower rotational delay

Hardware Optimization

Minimize Data Transfer Time

- How can the OS help minimize data transfer time?
- Schedule disk operations so as to minimize head movement
- Lay out data on disk so that related data are located on close tracks
- Place commonly-used data on a specific portion of the disk
- Pick carefully the block size contained on each sector:
 - Too small → more seeks are needed to transfer the same amount of data
 - Too large → more internal fragmentation and space wasted

Summary

- Hard disks are slow devices compared to CPUs (and main memory)
- Manage those device efficiently is crucial
- Minimize seek and rotational delay on magnetic disks
- HW optimizations are limited → OS needs to take the lead here!