Systems and Networking I

Applied Computer Science and Artificial Intelligence

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SAPIENZA
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A Quick Step Back: Segmentation

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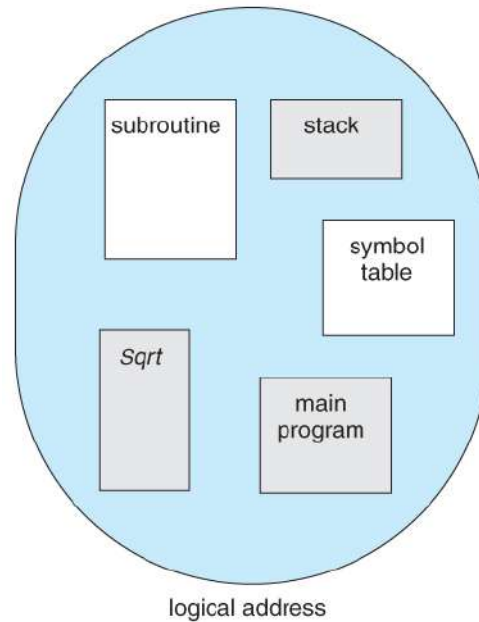
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- Rather they think of memory divided in multiple **segments**, each dedicated to a specific use, such as code, data, stack, heap, etc.

- Memory segmentation supports this view by providing addresses with a **segment number** (mapped to a segment base address) and an **offset**
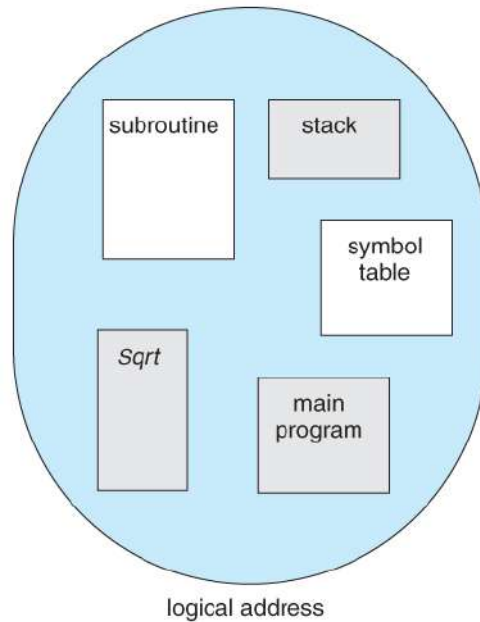
Segmentation: Example

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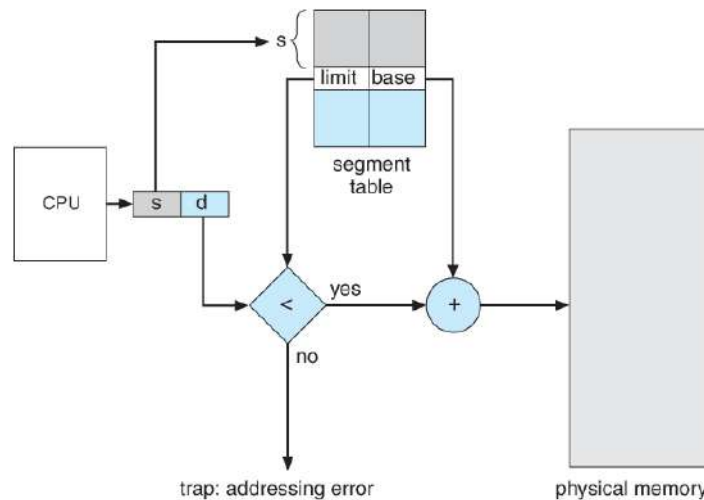The compiler generates addresses identifying segments and offset

Segmentation Hardware

A segment table maps segment-offset addresses to physical addresses, and simultaneously checks for invalid addresses, using a system similar to the page tables and relocation base registers discussed previously
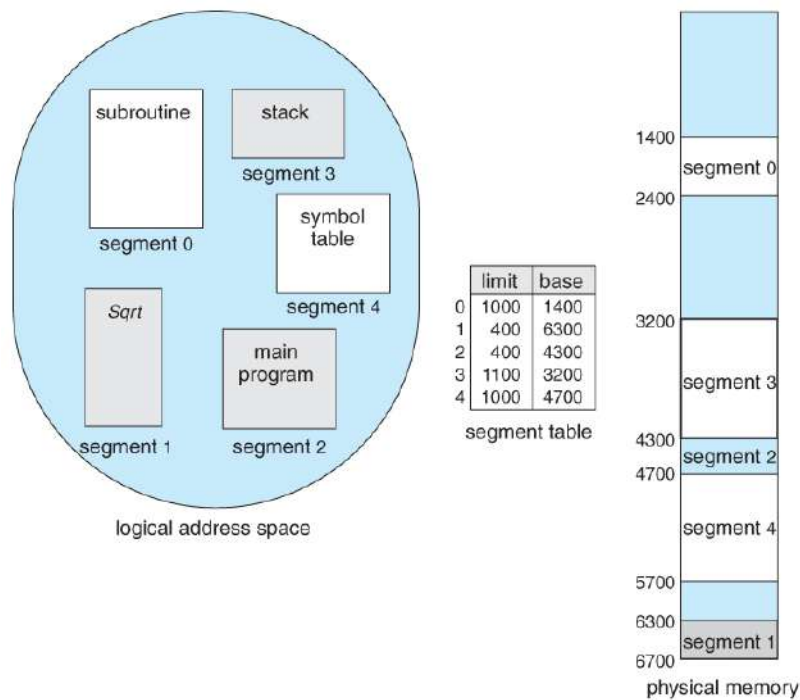
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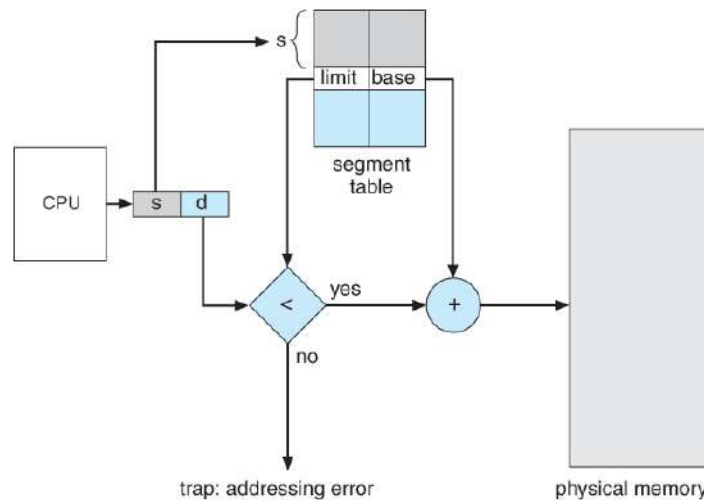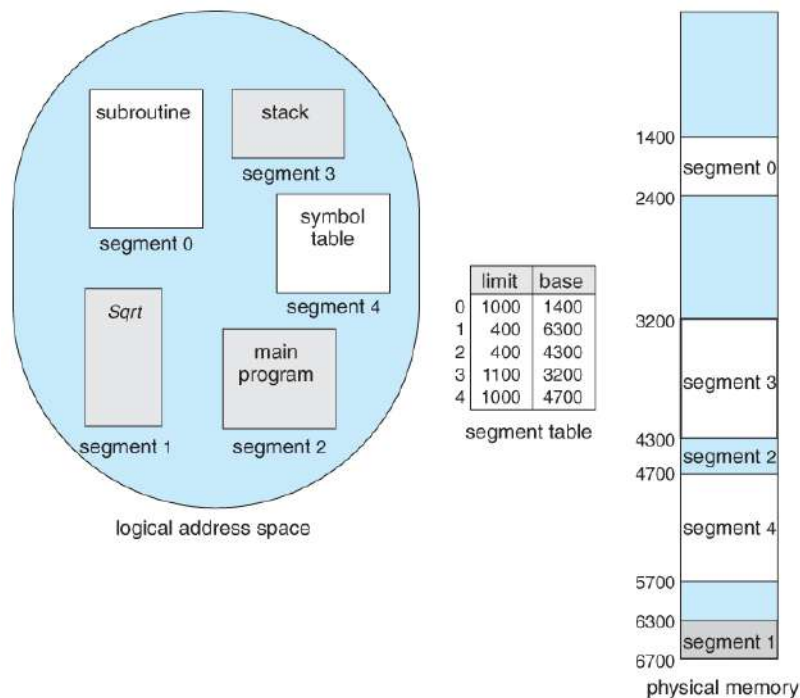

Note that we came back to the assumption that each segment is kept in contiguous memory and may be of different size…

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Each entry contains a base address in memory, the length of the segment, plus additional protection information (e.g., sharing, read/write permissions)

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Segment Table

logical address space

segment table

physical memory

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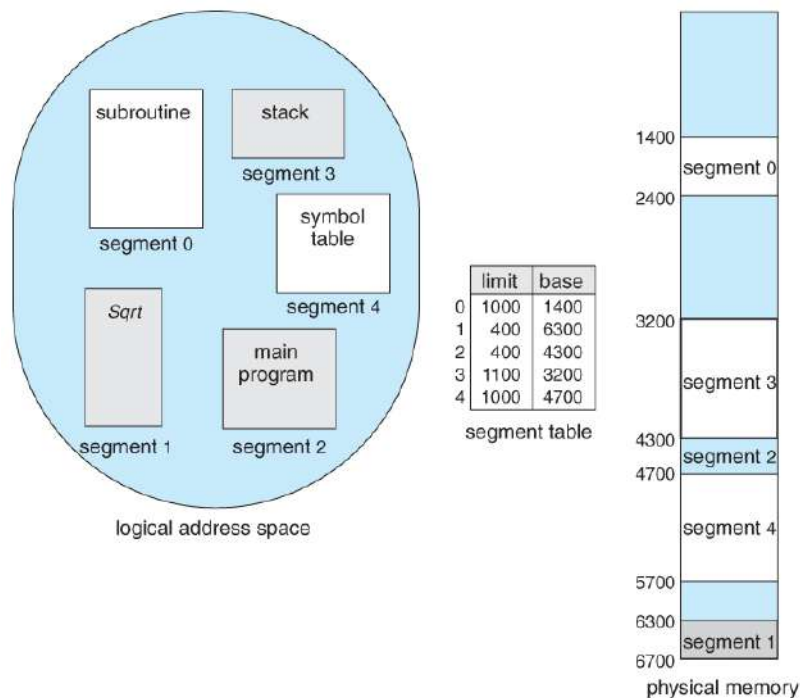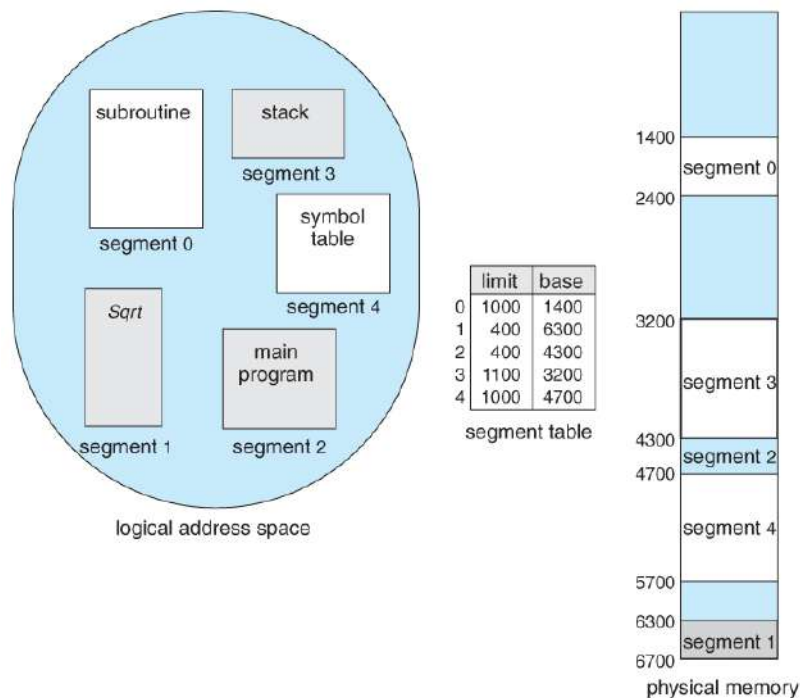
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Segment Table, instead, must store a very limited amount of segments per process (3÷5)

Implementing (Basic) Segmentation

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- Additional HW (like TLB cache) might be needed if programs use many logical segments

Combine Segmentation with Paging

Try to get the best of both world

Combine Segmentation with Paging

Try to get the best of both world

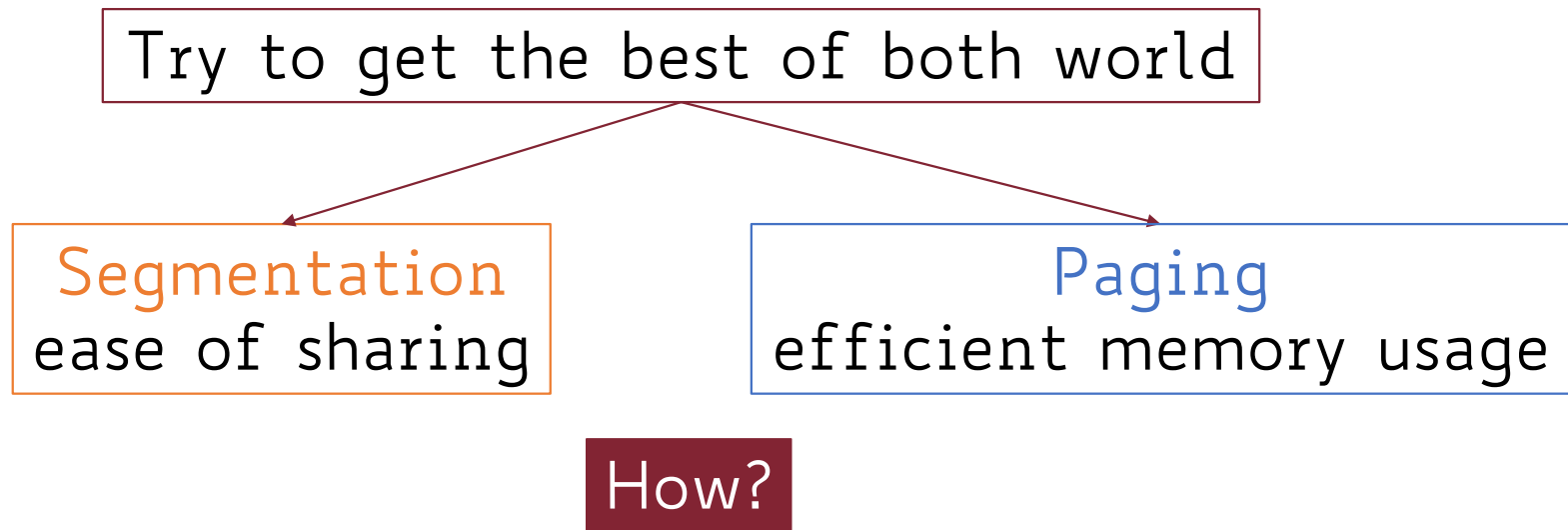Segmentation
ease of sharing

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efficient memory usage

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How?

Combine Segmentation with Paging

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How?

Apply paging to segments!

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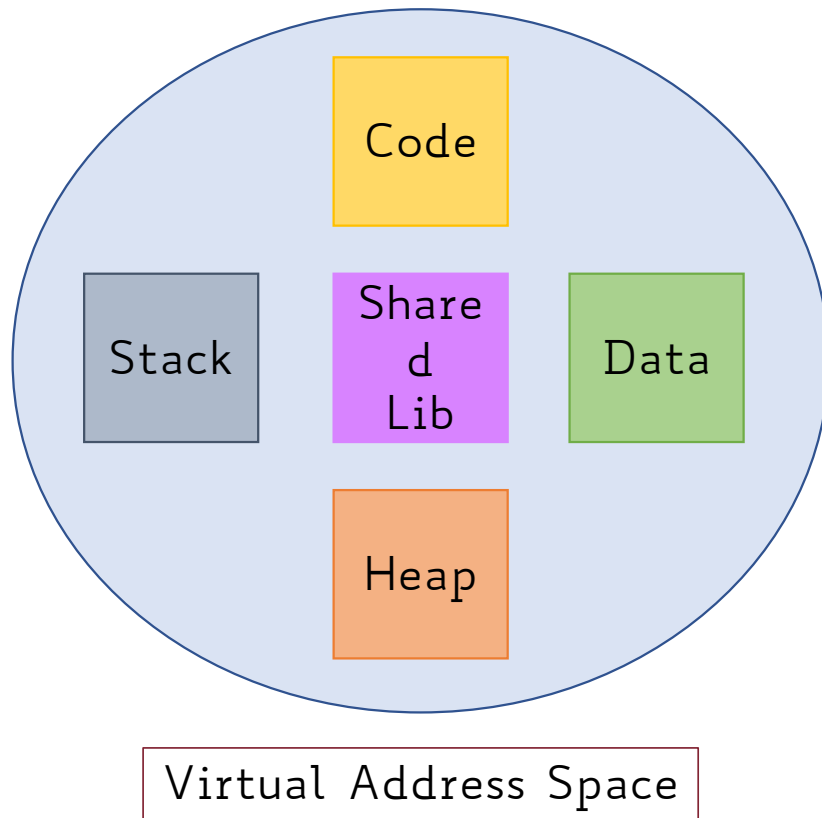- Segments are usually larger than physical page frames

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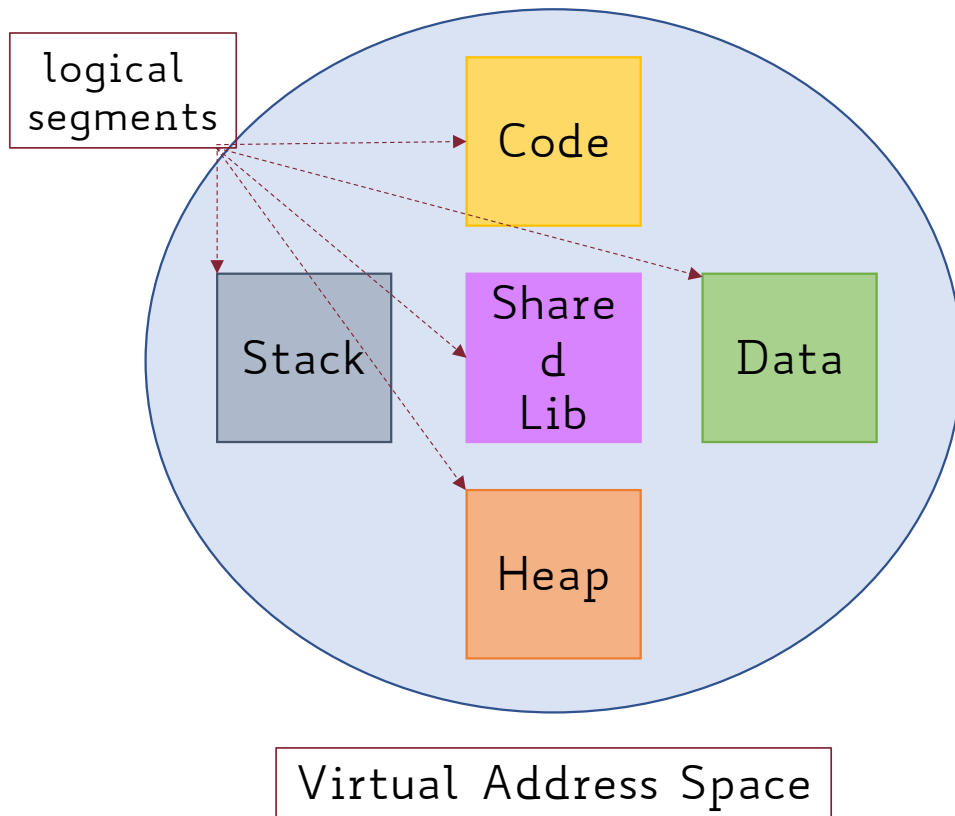
⬇

Map a logical segment onto multiple page frames

Paging Logical Segments

Virtual Address Space

Paging Logical Segments

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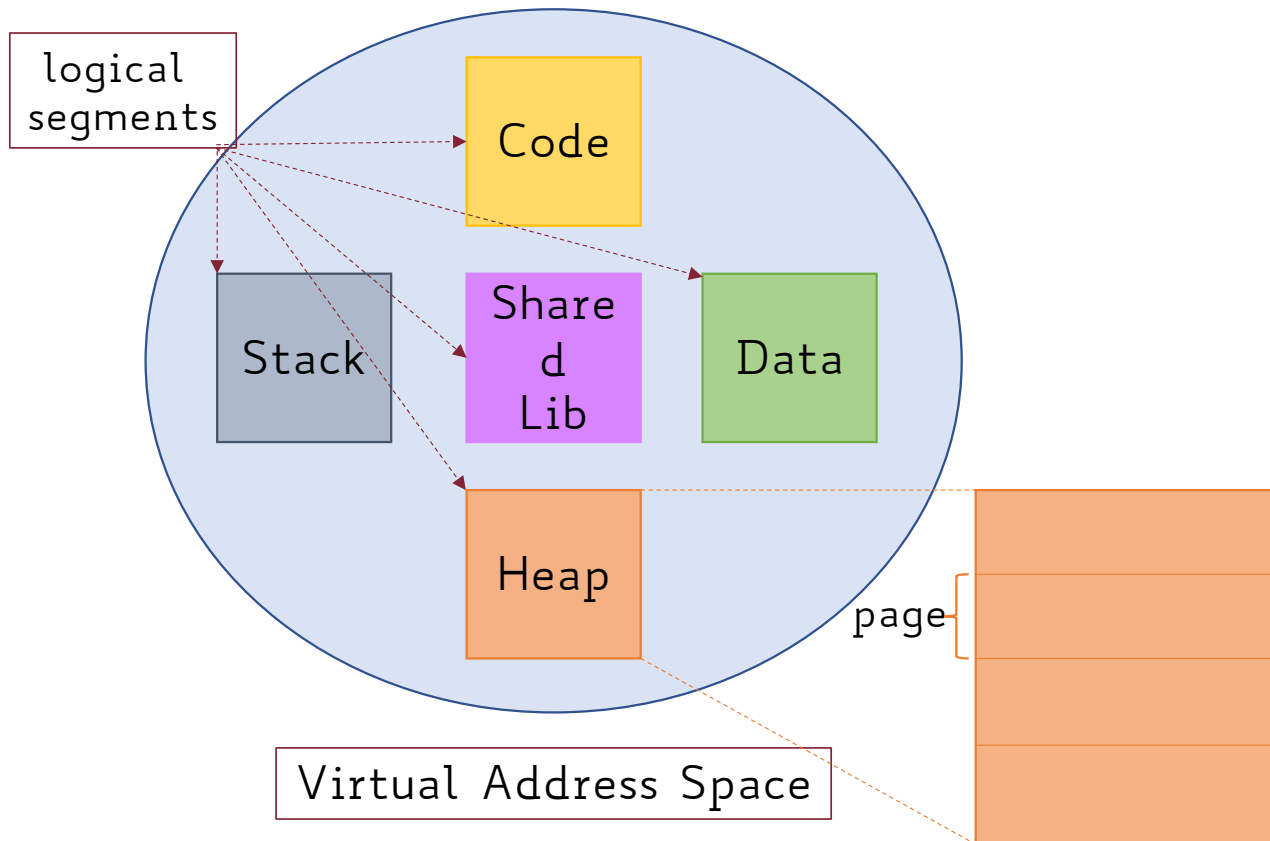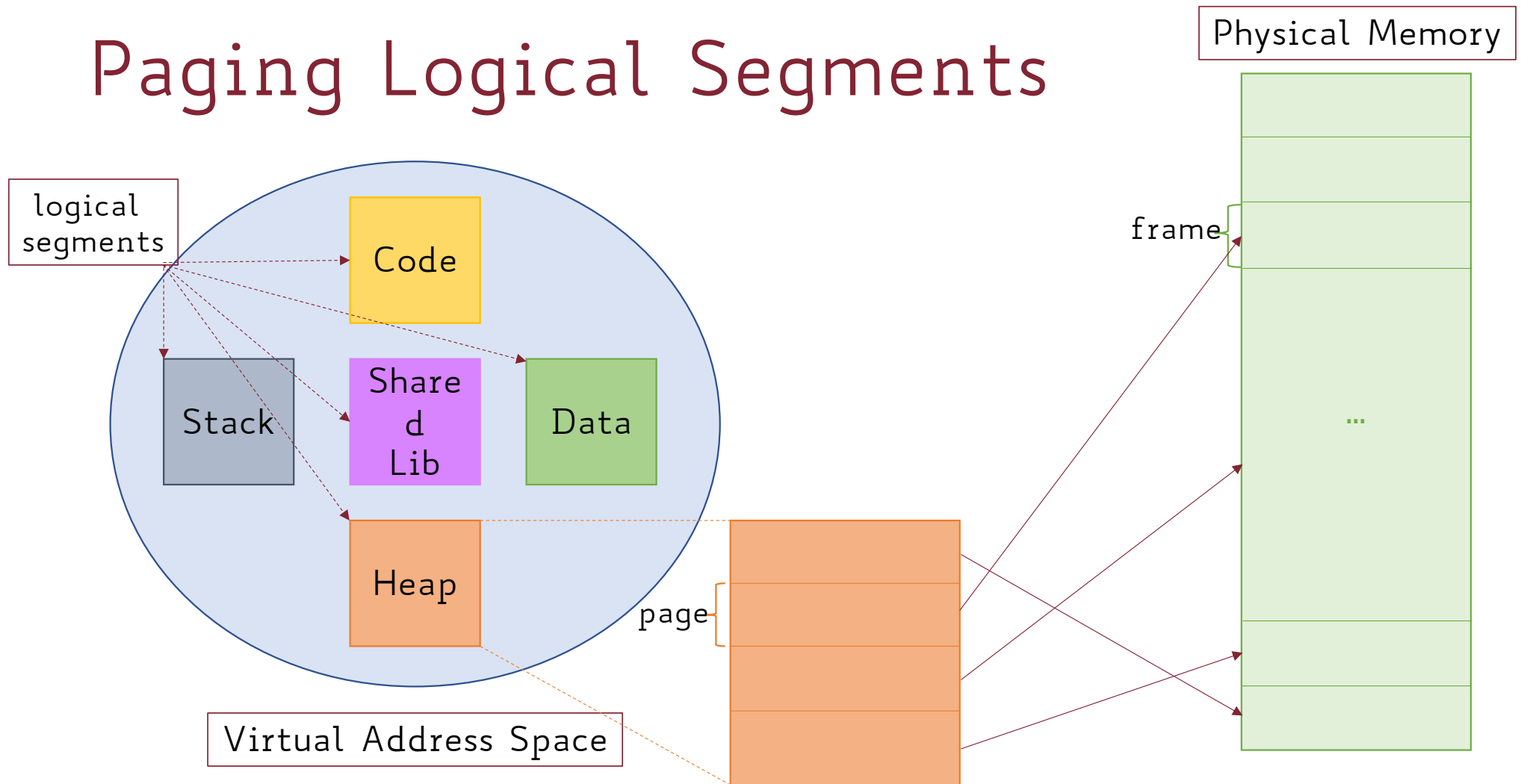
logical segments

Code

Shared Lib

Data

Stack

Heap

page

Virtual Address Space

Paging Logical Segments

logical
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Virtual Address Space

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A virtual address now becomes:

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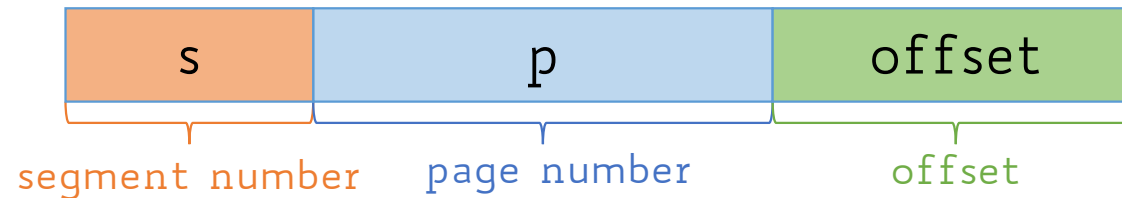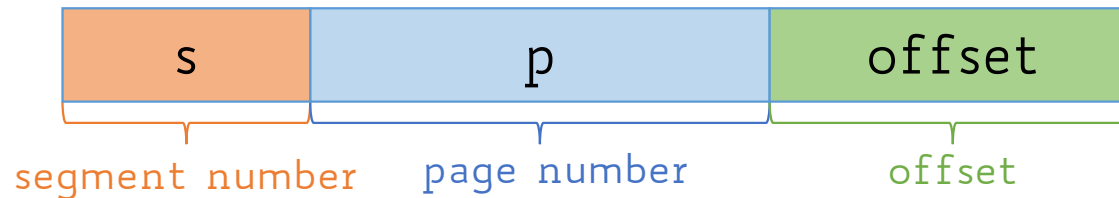
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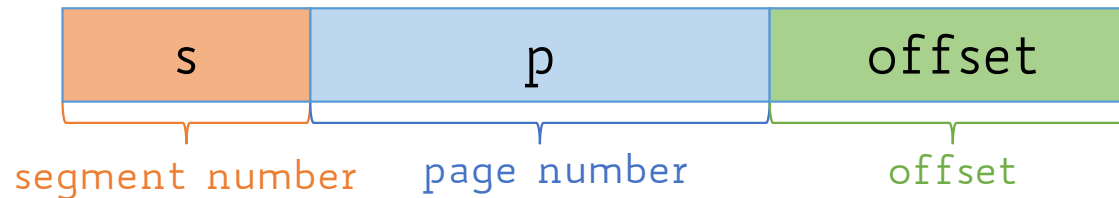
- Check the page number + offset against the limit of the segment

Address Translation with Segmented Paging

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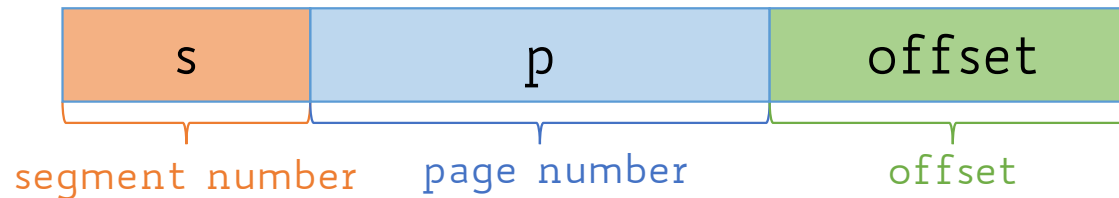| s	p	offset
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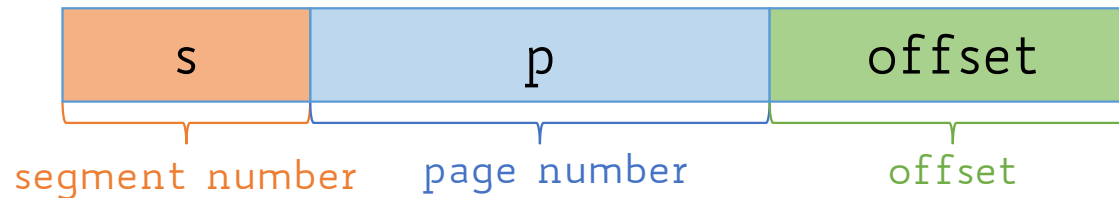
- Use the page number to index the page table to get the physical frame number

Address Translation with Segmented Paging

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s	p	offset

segment number   page number   offset

- Use the page number to index the page table to get the physical frame number

- Add the frame number to the offset to get the physical address

Address Translation with Segmented Paging

CPU

One Segment Table per Process

virtual

| s | p | offset |

physical address

| f | offset |

Memory

s

base	limit
base	limit
base	limit
…	…
base	limit

Segment Table

>=

TRAP

p

| |
| |
| |
| |
| … |
| f |
| … |
| |

Page Table

One Page Table per Segment
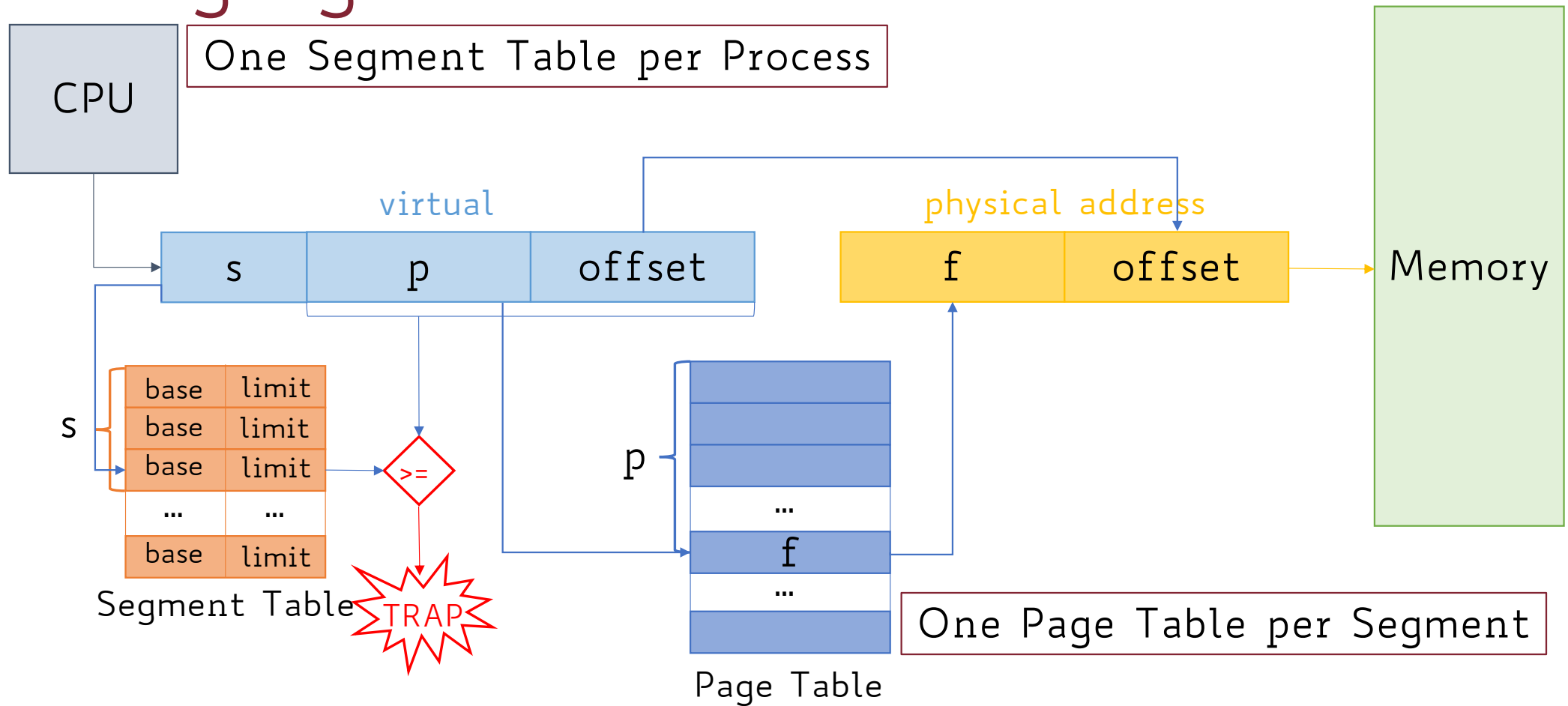
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Slower but more flexible

Segmented Paging Hardware: Practical Example 3

Suppose a physical memory of 1024 addressable words (assuming 1 word = 1 byte)

Frame size is 64 words (i.e., 64 bytes)

Page table size (i.e., number of entries) is thus 1024 bytes/64 bytes per frame = 16

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10 bits to address M = 1024/1 = 1024 1-byte words

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3 bits to address 8 logical segments (s)
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13 bits (virtual address) vs. 10 bits (physical address)

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- Even more flexible!

Segmented Paging: Benefits and Costs

- Benefits:

  - Merge compiler and OS view of memory

  - Flexibility

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- The larger the page size the higher the chance of internal fragmentation

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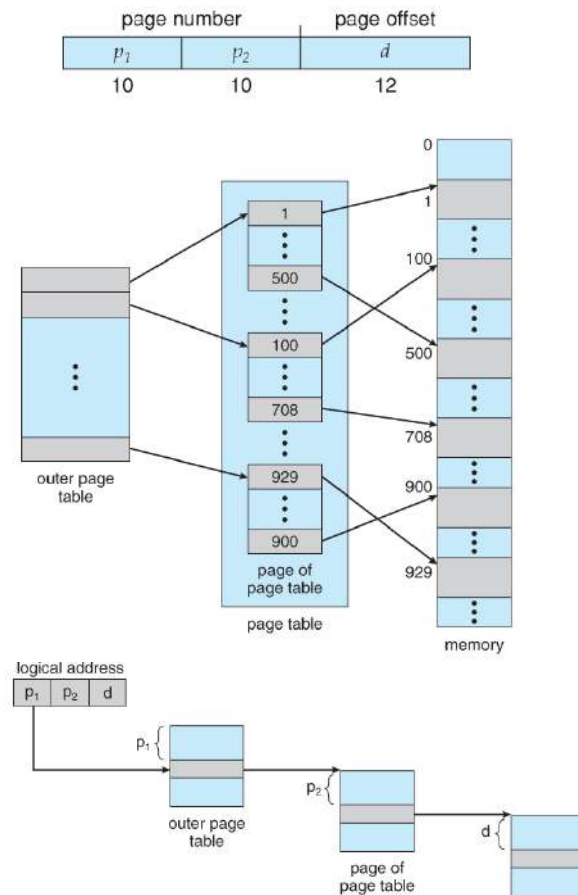
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More advanced paging structures are needed!

Advanced Paging: Two-Tier Page Table

Let's page the page table!

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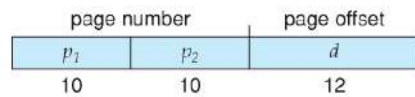
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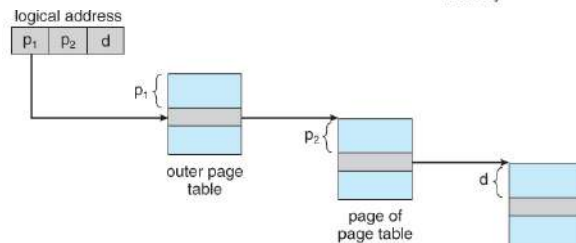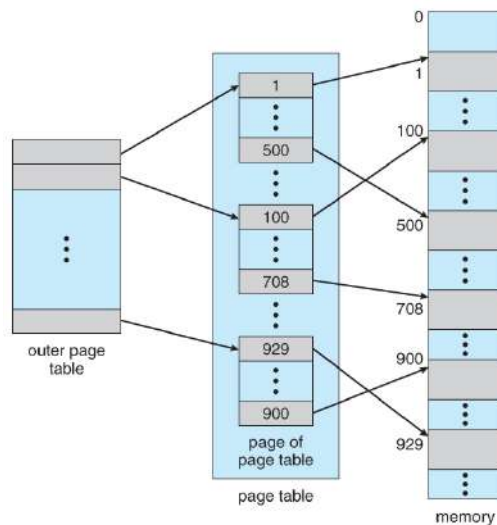20-bit page number broken into 2 10-bit page numbers
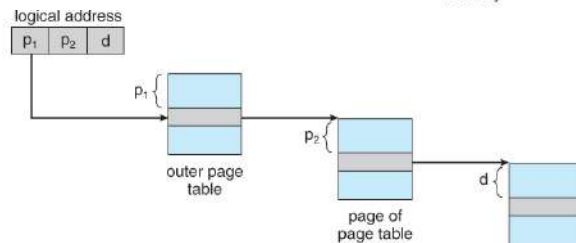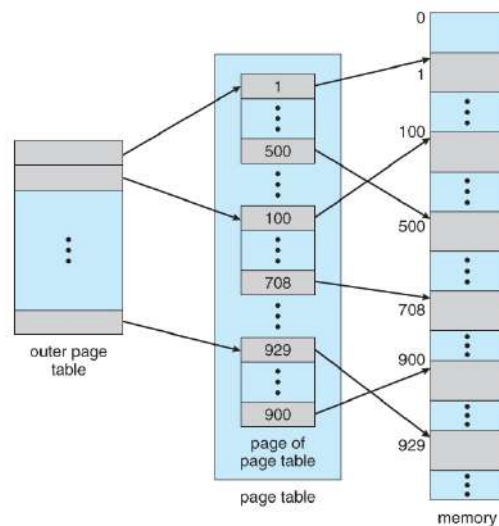
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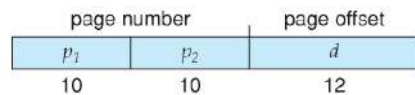
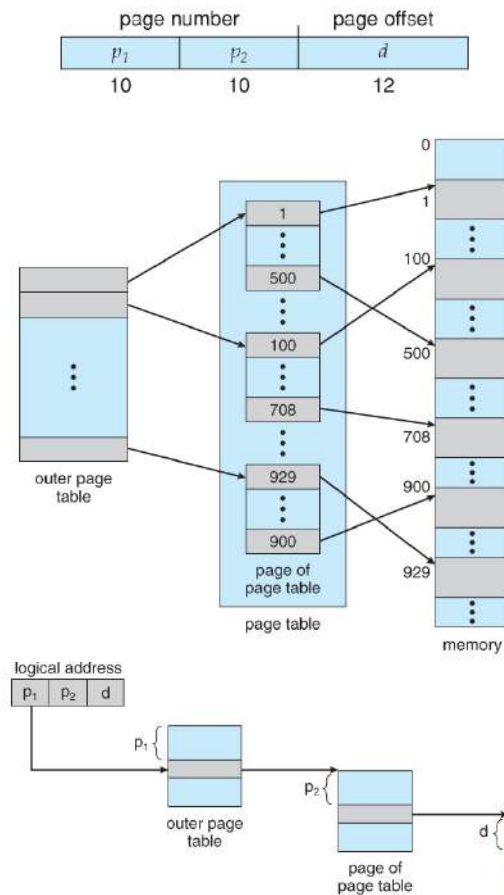

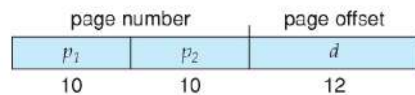**Let's page the page table!**

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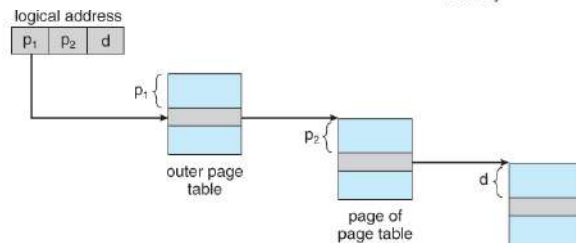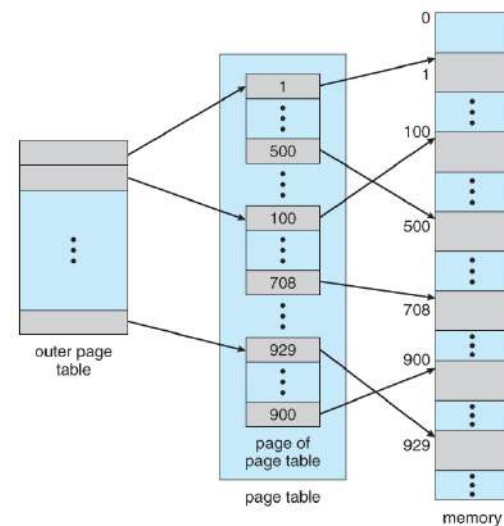20-bit page number broken into 2 10-bit page numbers

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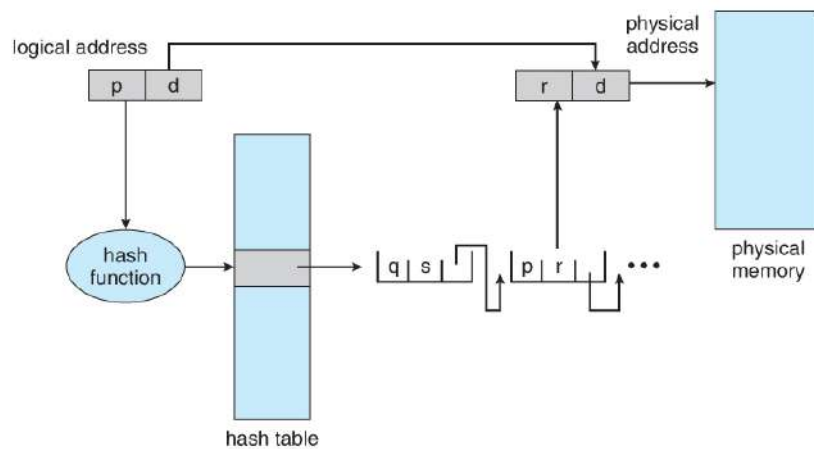
The remaining 12 bits of the 32-bit logical address are still the offset within the 4KiB frame

Advanced Paging: Hashed Page Table
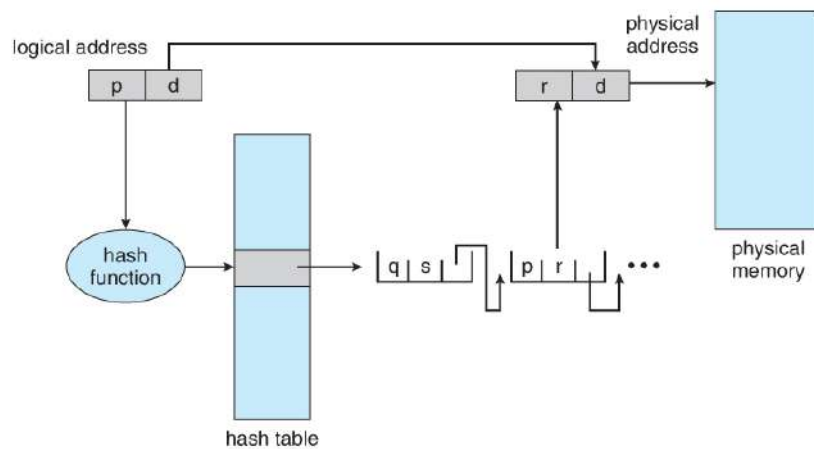
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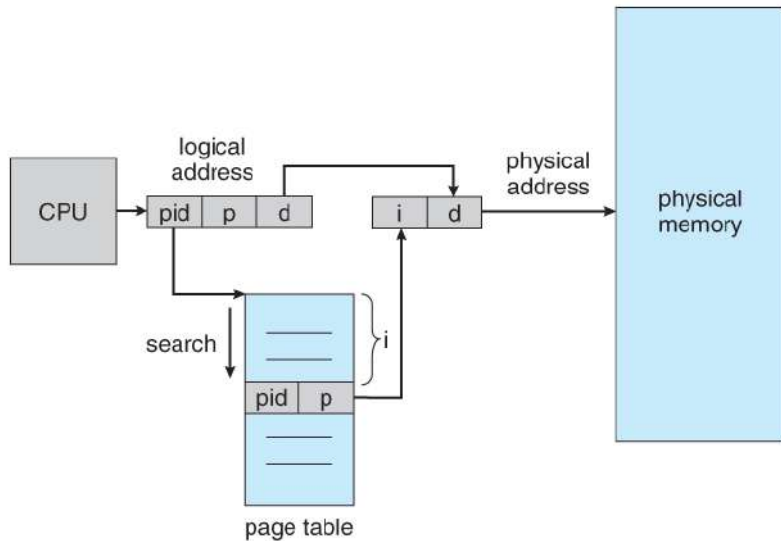
Advanced Paging: Hashed Page Table

Use hash tables to store highly sparse page tables

Indexing via hash function rather than integers

Advanced Paging: Inverted Page Table

An inverted page table lists all of the frames currently loaded in memory, for all processes

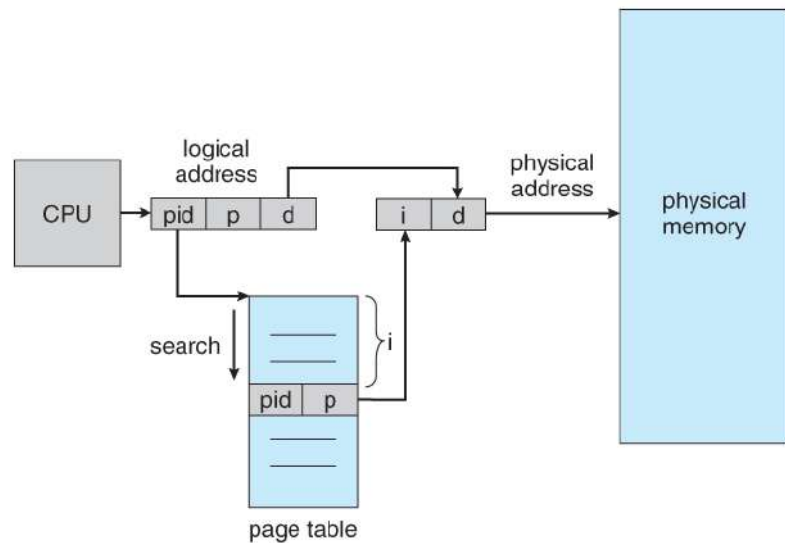Instead of a table listing all of the pages for a particular process

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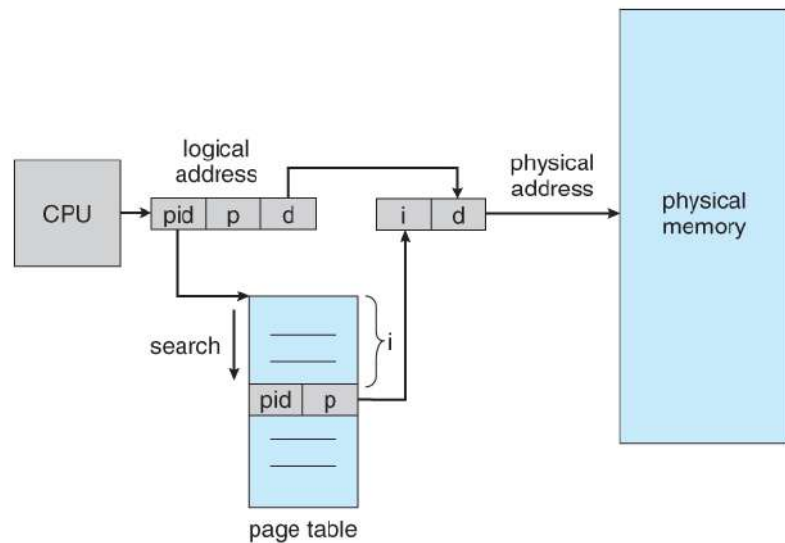
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Inverted page tables do not easily allow mapping multiple logical pages to a common physical frame (page sharing)

Each frame is mapped to exactly one process

logical
address

physical
address

CPU

pid | p | d

i | d

physical
memory

search

i

pid | p

page table

Summary

- **Relocation** using base and limit registers
  - Simple yet inflexible

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  - Simple yet inflexible

- **Segmentation**
  - Compiler's logical view of memory presented to the OS
  - Segment tables tend to be small enough to be stored in registers
  - Contiguous memory allocation is expensive and complicated (first-fit, best-fit, or worst-fit)
  - Compaction is needed to solve external fragmentation

Summary

- ## Paging

  - Simplifies memory allocation by relaxing contiguous assumption

  - Each logical page can be allocated to any physical frame

  - Page tables can be extremely large

Summary

- **Segmentation + Paging**
  - Only need to allocate as many page table entries an needed
  - Sharing either at the segment or at the page level
  - Might increase internal fragmentation over pure paging
  - 2 lookups per memory reference are needed