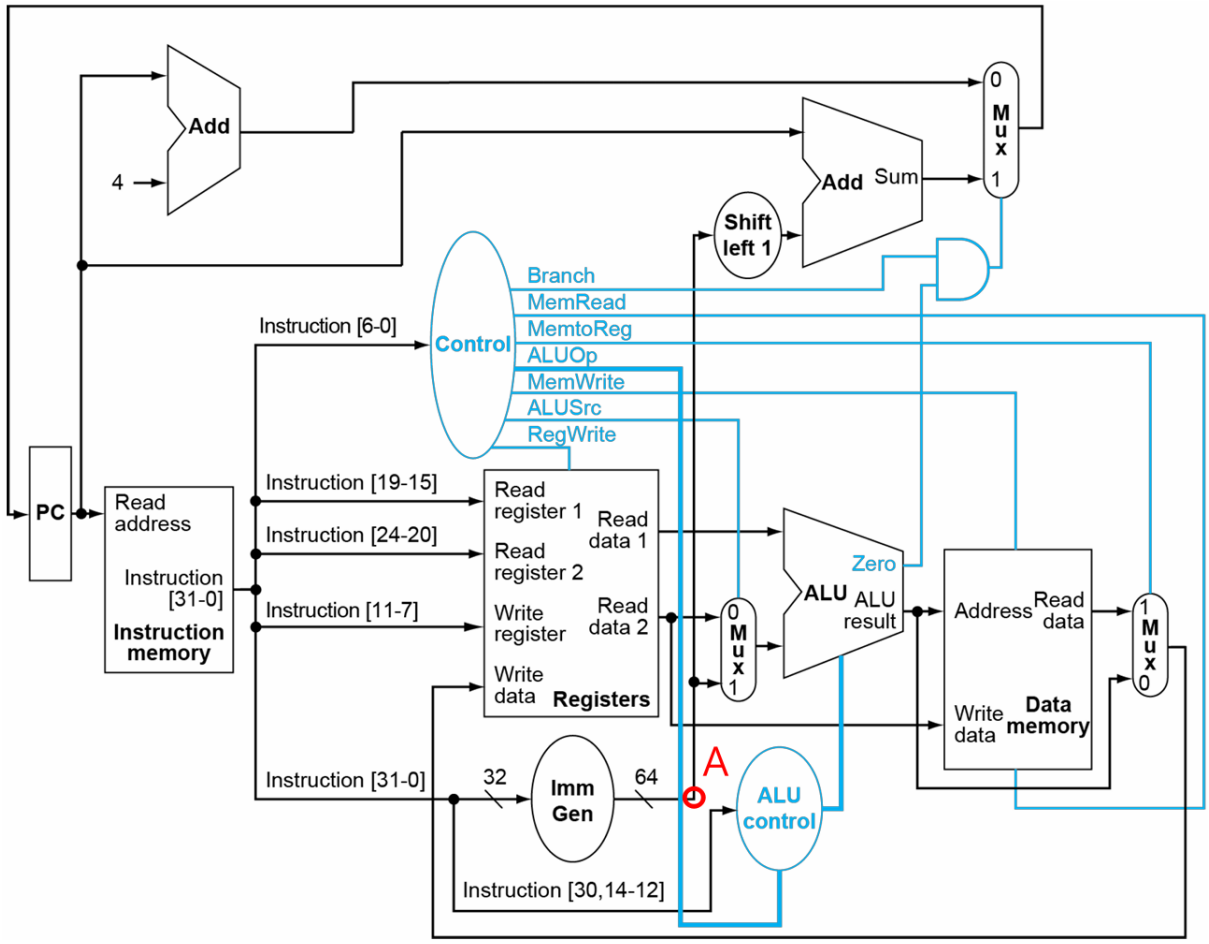
**CS4100 Computer Architecture**

Spring 2025, Homework 4

Due: 23:59, 5/10/2024

1. (14%) Consider the single-cycle processor below:




(a) (4%) What instruction(s) may fail to run correctly if the interconnections labeled **A** above have been cut? Choose the answer from add, sub, and, sd, ld, and beq.

(b) (4%) What instruction(s) would still be correct if the input signals of **Read register 1** and **Read register 2** were swapped? Choose the answer from add, sub, and, sd, ld, and beq.

(c) (6%) What control signal(s) must be set to 0 when the program runs the instruction **ld x10 8(x12)**? What are the **respective** consequences if they are set to 1? Choose the answer from Branch, MemRead, MemtoReg, MemWrite, ALUSrc, and RegWrite.

2. (11%) Consider the execution of the machine instruction $015A07B3_{hex}$ on the single-cycle processor.

(a) (7%) What are the values of the signals: Branch, MemRead, MemtoReg, ALUOp, MemWrite, ALUSrc and RegWrite?

(b) (4%) What are the input values of the ALU? You can use Reg[x] to denote the value of register x.

3. (8%) Assume that the logic blocks used to implement the single-cycle processor have the following delay values:

| I-Mem/ D-Mem | Register File | Mux | ALU | Adder |
|---|---|---|---|---|
| 200ps | 120ps | 10ps | 150ps | 100ps |
| Single Gate | PC Read | Register Setup | Imm Gen | Control |
| 5ps | 20ps | 10ps | 25ps | 25ps |

"I-Mem/D-Mem" is the amount of time to access the Instruction or Data Memory.
"Register File" is the amount of time to read rs1 and rs2.
"PC Read" is the amount of time needed after a rising clock edge for the new PC value to appear on the output; this delay value applies to the PC only.
"Register Setup" is the amount of time a register's data input must be stable before a rising clock edge; this delay value applies to both the PC and Register File.
"Control" is the total amount of time for the Control unit and the ALU control unit to produce the 4-bit "ALU operation".

(a) (4%) Consider the four instructions: add, ld, sd, beq. Which has the least execution time and how much time does it take?

(b) (4%) What is the minimum clock period for this processor? Justify your answer.

4. (10%) In a multi-cycle processor, each instruction executes over multiple clock cycles, with each cycle handling a distinct step (e.g., fetch, decode, execute, etc.). Unlike a single-cycle processor, where all instructions complete in the same cycle time, a multi-cycle processor allows different instructions to require varying numbers of cycles. Additionally, unlike a pipelined processor, which executes multiple instructions in parallel, a multi-cycle processor processes one instruction at a time, completing all required steps before starting the next instruction. Now consider executing a program with the instruction mix provided below on a single-cycle processor and a multi-cycle processor, respectively.

| Class | statistics |
|---|---|
| ALU | 50% |
| Load | 20% |
| Store | 14% |
| Branch | 12% |
| Jump | 4% |

The critical path, which is 60 ns, exists in the Load-type instruction class for the single-cycle processor. In the multi-cycle processor, the Load-type instruction is evenly divided into 6 steps, reducing the clock period. Assume that the step register introduces additional 2 ns delay to each

step. Adopting the multi-cycle processor, the number of clock cycles for each instruction class is listed as follows:

| Class | Load | Store | ALU | Branch | Jump |
|---|---|---|---|---|---|
| Cycles | 6 | 5 | 4 | 4 | 3 |

(a) (5%) What is the ratio between the total numbers of clock cycles for the multi-cycle processor and the single-cycle processor to execute this program? Justify your answer.

(b) (5%) What is the performance speedup of the multi-cycle processor compared to the single-cycle processor for this program? Justify your answer.

5. (20%) Consider the instruction sequence below:

```
ld   x12, 8(x3)
addi x13, x4, 7
or   x14, x12, x13
sd   x14, 0(x5)
```

(a) (3%) List all the data dependencies, regardless of whether they cause any hazard or not.

(b) (5%) How many clock cycles does the five-stage pipelined processor take to complete the execution of this instruction sequence? Justify your answer.

(c) (3%) Assume that this instruction sequence is executed on a five-stage pipelined processor with the forwarding unit but without the hazard detection unit. Are there any data hazards that will require the pipeline to stall because they cannot be resolved by forwarding? Justify your answer.

(d) (4%) Assuming that this instruction sequence is executed on a five-stage pipelined processor without the forwarding unit and the hazard detection unit, insert a minimum number of NOP (no operation) instructions to ensure correct execution.

(e) (5%) How many clock cycles does the processor take to complete the execution of the instruction sequence in (d)? Justify your answer.

6. (10%) Consider the instruction sequence below:

```
add x3, x1, x2
sub x4, x1, x2
ld x5, 4(x3)
sub x1, x4, x5
```

(a) (5%) What is the average CPI for the five-stage pipelined processor to execute this instruction sequence?

(b) (5%) Is it possible to reorder the code so that the average CPI for the five-stage pipelined processor to execute the new instruction sequence is less than that in (a)? Justify your answer.

7. (12%) Consider the following sequence of branch outcomes: T, NT, T, NT, T, NT, NT, NT, where NT denotes not-taken and T denotes taken.

(a) (4%) What are the respective accuracy rates of the always-not-taken predictor and the always-taken predictor for the sequence of branch outcomes?

(b) (4%) Assume that a 1-bit dynamic predictor starts at the T state. Complete the following table and write down the accuracy rate of this predictor for the sequence of branch outcomes.

| Ground truth | T | NT | T | NT | T | NT | NT | NT |
|---|---|---|---|---|---|---|---|---|
| State | | | | | | | | |
| Decision | | | | | | | | |
| Correctness | | | | | | | | |

(c) (4%) Assume that a 2-bit dynamic predictor starts at the "strongly predict taken" state. Complete the following table and write down the accuracy rate of this predictor for the sequence of branch outcomes.

| Ground truth | T | NT | T | NT | T | NT | NT | NT |
|---|---|---|---|---|---|---|---|---|
| State | | | | | | | | |
| Decision | | | | | | | | |
| Correctness | | | | | | | | |

8. (10%) Consider the execution of the following sequence of four instructions on a five-stage pipelined processor which uses the always-not-taken strategy for branch prediction and has both the forwarding unit and hazard detection unit.

**add x12, x6, x5**
**sub x10, x11, x12**
**beq x11, x12, LABEL**
**sd x11, 0(x12)**

Suppose the third instruction is detected to have an invalid target address and cause an exception in the ID stage. Fill in the following table by showing what instructions are in the IF, ID, EX, MEM and WB stages. Note that each instruction in your answer should be one chosen from the given four instructions, the NOP instruction (or bubble), and the first instruction of the exception handler.

| | IF | ID | EX | MEM | WB |
|---|---|---|---|---|---|
| Cycle 1 | | - | - | - | - |
| Cycle 2 | | | - | - | - |
| Cycle 3 | | | | - | - |
| Cycle 4 | | | | | - |
| Cycle 5 | | | | | |

9. (5%) Consider the two-issue processor introduced in class, where one instruction can be an integer ALU operation or a branch, and the other can be a load or store operation. Determine whether the instruction sequence below can be scheduled on this processor to issue all instructions within four clock cycles. Justify your answer.

```
add x12, x6, x5
ld x31, 0(x12)
sub x10, x11, x12
sub x5, x11, x31
sd x11, 0(x10)
ld x30, 0(x13)
add x30, x10, x30
sd x30, 0(x10)
```