<- This means this lab is on your local computer

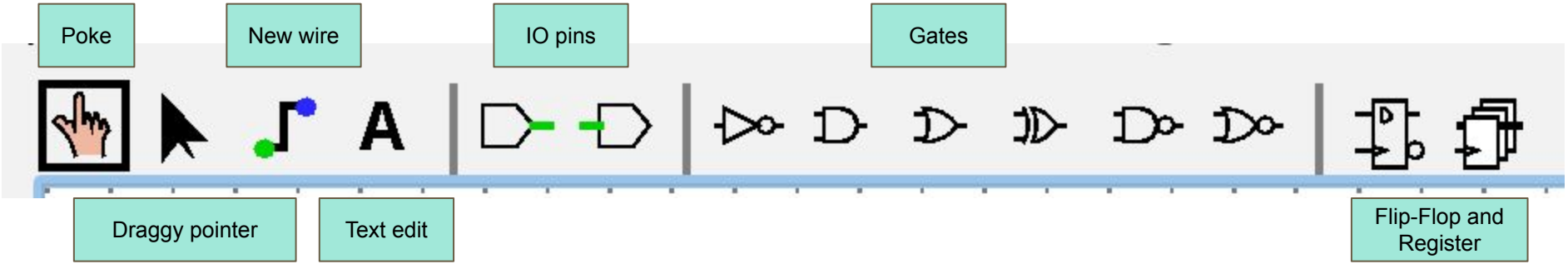
# Lab 5: Logisim

CS61C FA24

# Topics

- Logisim tools
- Basic logic gates in Logisim
- Advanced (and useful) Logisim components
- Wire colors in Logisim

# Logisim Basics




- Don’t forget about debugger finger!!

# AND Gate

2 - input AND gate

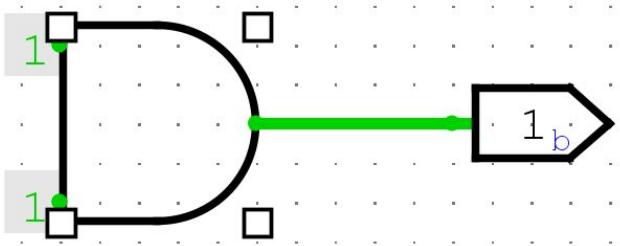

| A | B | Output |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

# AND - logisim

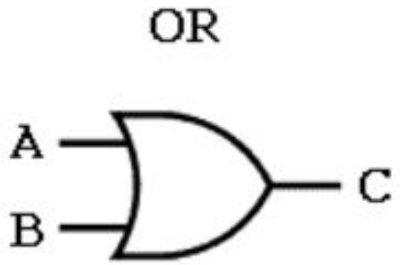
**Properties** **State**

**AND Gate (120,360)**

| | |
|---|---|
| FPGA supported: | Supported |
| Facing | → East |
| Data Bits | 1 |
| Gate Size | Medium |
| Number Of Inputs | 2 |
| Output Value | 0/1 |
| Label | |
| Label Font | SansSerif Bold 16 |
| Negate 1 (↑ Top) | No |
| Negate 2 (↓ Bottom) | No |



# OR Gate



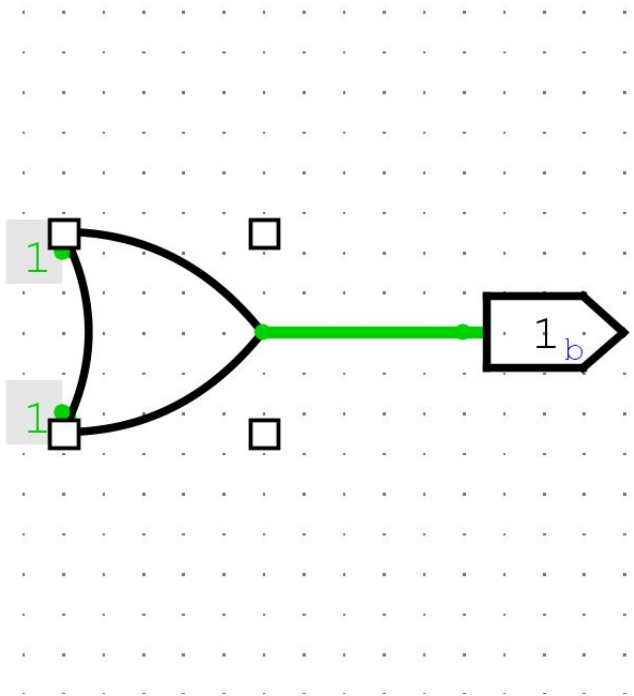

| Inputs | | Output |
|---|---|---|
| A | B | C |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

# OR - logisim

**Properties** | **State**

**OR Gate (120,360)**

| | |
|---|---|
| FPGA supported: | Supported |
| Facing | → East |
| Data Bits | 1 |
| Gate Size | Medium |
| Number Of Inputs | 2 |
| Output Value | 0/1 |
| Label | |
| Label Font | SansSerif Bold 16 |
| Negate 1 (↑ Top) | No |
| Negate 2 (↓ Bottom) | No |

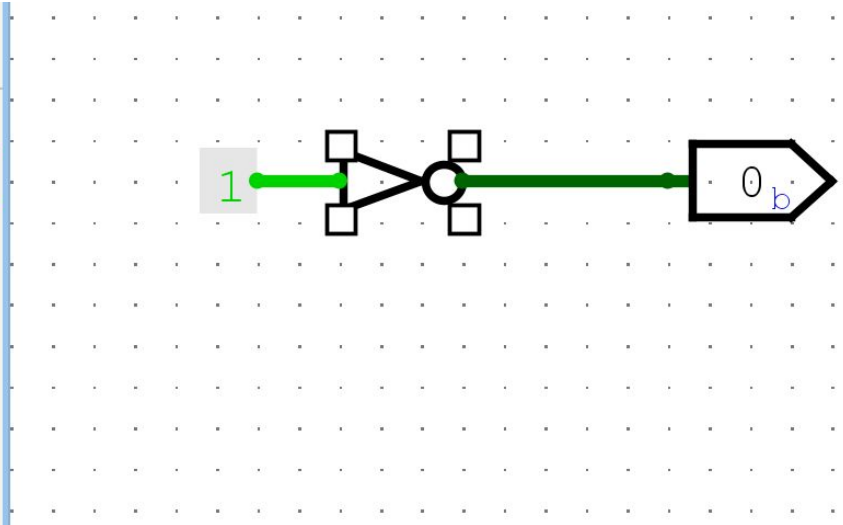


# NOT Gate

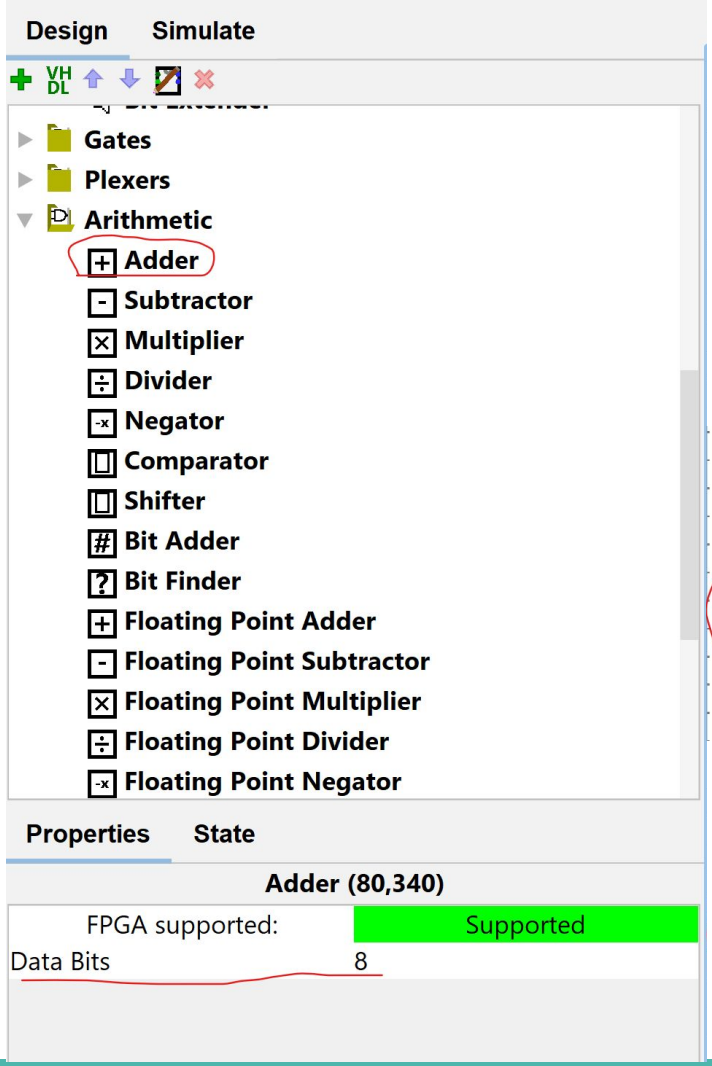
**Properties** **State**

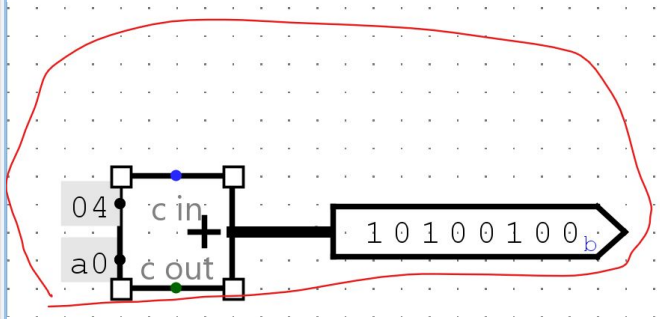
**NOT Gate (110,320)**

| | |
|---|---|
| FPGA supported: | Supported |
| Facing | → East |
| Data Bits | 1 |
| Gate Size | Wide |
| Output Value | 0/1 |
| Label | |
| Label Font | SansSerif Bold 16 |

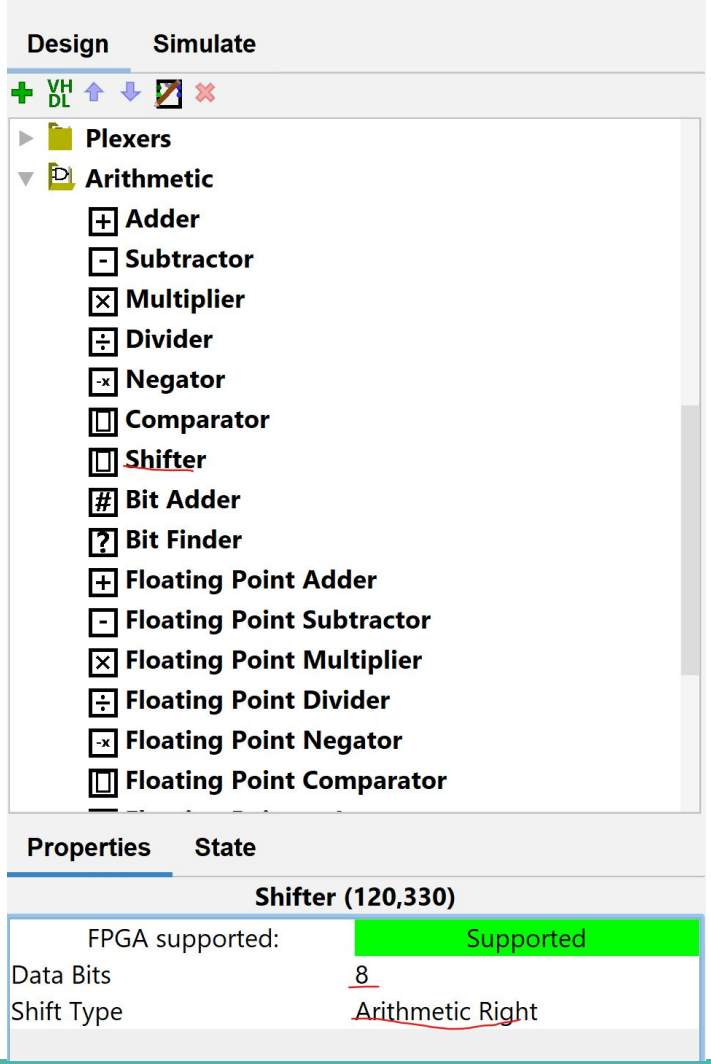


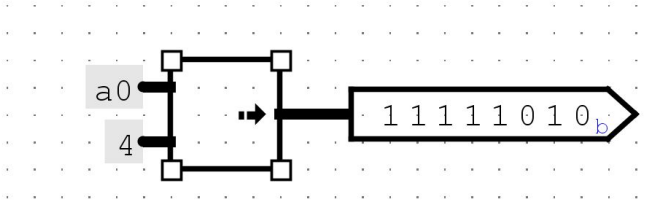
# Adder


Design
Simulate
Gates
Plexers
Arithmetic
Adder
Subtractor
Multiplier
Divider
Negator
Comparator
Shifter
Bit Adder
Bit Finder
Floating Point Adder
Floating Point Subtractor
Floating Point Multiplier
Floating Point Divider
Floating Point Negator
Properties
State
Adder (80,340)
FPGA supported:
Supported
Data Bits
8

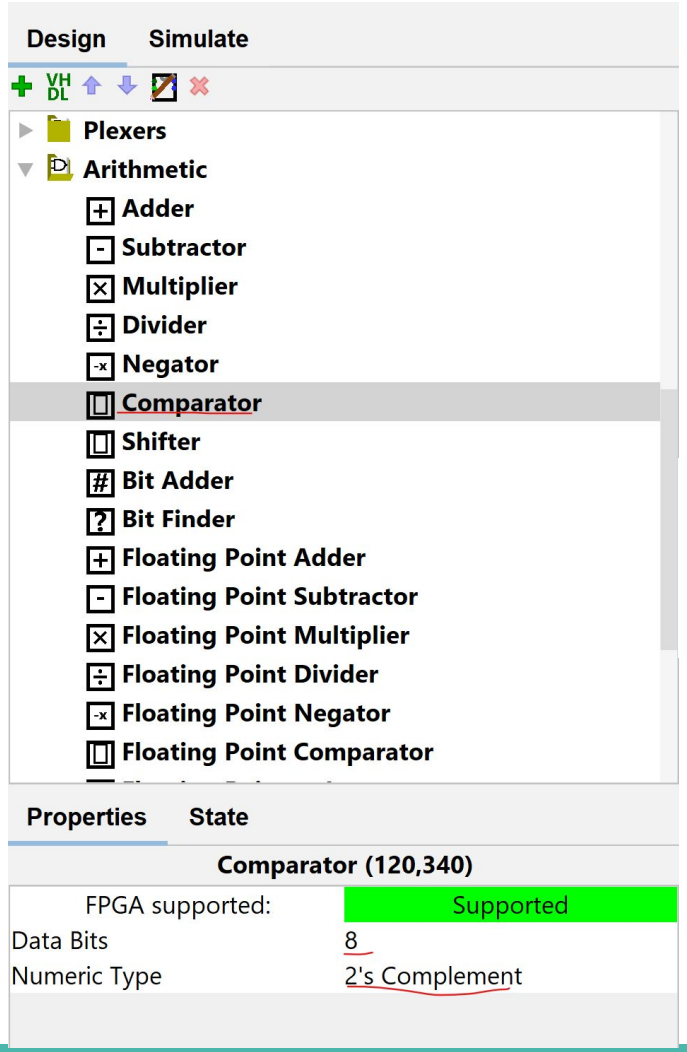

04
a0
c in
c out
10100100b

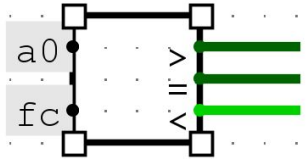
# Shifter


Design
Simulate
Plexers
Arithmetic
Adder
Subtractor
Multiplier
Divider
Negator
Comparator
Shifter
Bit Adder
Bit Finder
Floating Point Adder
Floating Point Subtractor
Floating Point Multiplier
Floating Point Divider
Floating Point Negator
Floating Point Comparator
Properties
State
Shifter (120,330)
FPGA supported:
Supported
Data Bits
8
Shift Type
Arithmetic Right

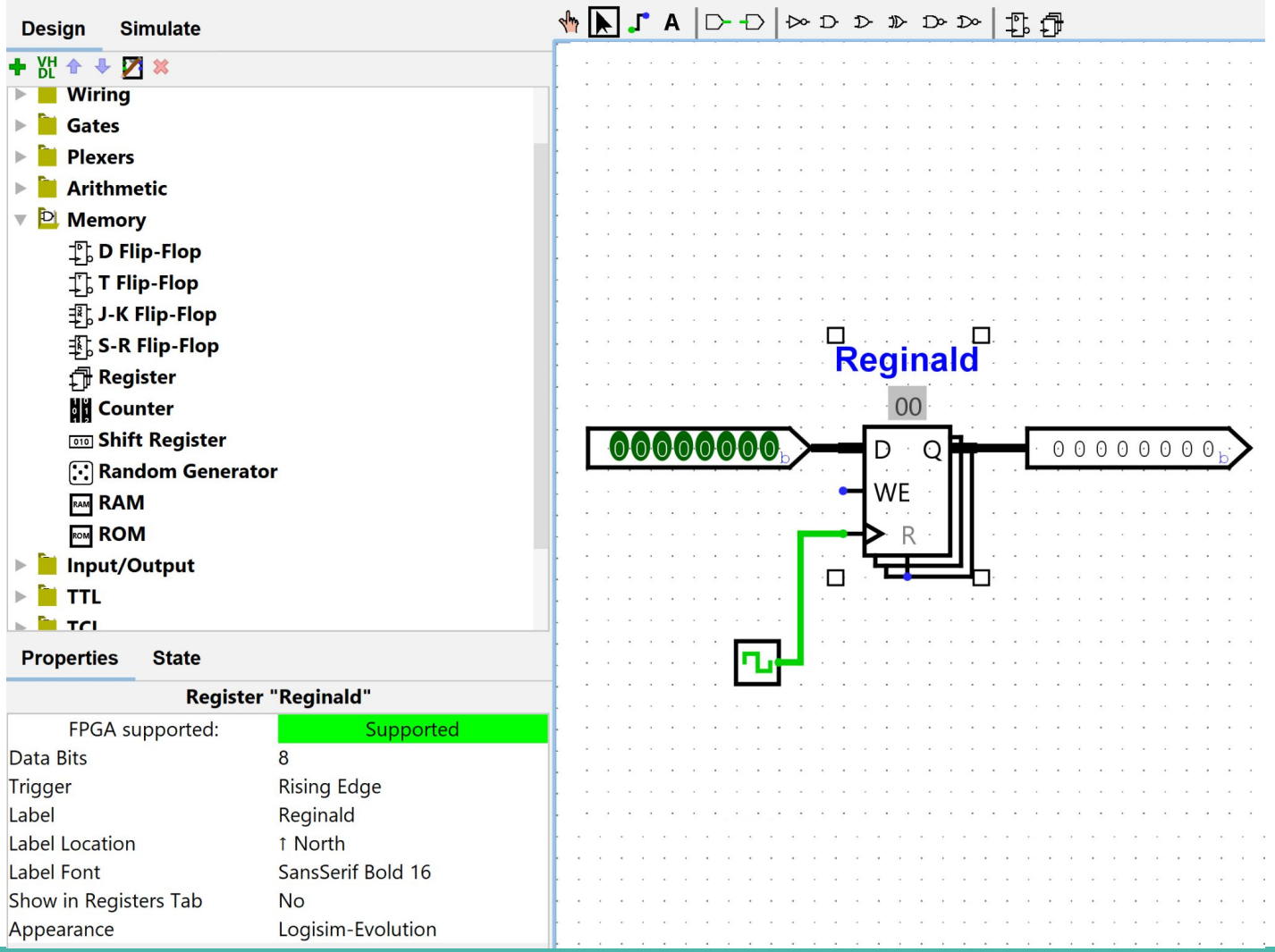

a0
4
1 1 1 1 1 0 1 0 b

# Comparator


Design
Simulate
Plexers
Arithmetic
Adder
Subtractor
Multiplier
Divider
Negator
Comparator
Shifter
Bit Adder
Bit Finder
Floating Point Adder
Floating Point Subtractor
Floating Point Multiplier
Floating Point Divider
Floating Point Negator
Floating Point Comparator
Properties
State
Comparator (120,340)
FPGA supported:
Supported
Data Bits
8
Numeric Type
2's Complement

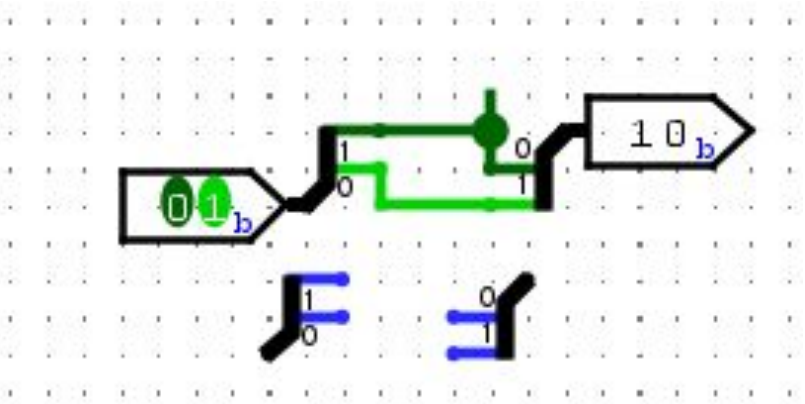

a0
fc
>
=
<

# Register


Design
Simulate
Wiring
Gates
Plexers
Arithmetic
Memory
D Flip-Flop
T Flip-Flop
J-K Flip-Flop
S-R Flip-Flop
Register
Counter
Shift Register
Random Generator
RAM
ROM
Input/Output
TTL
Properties
State
Register "Reginald"
FPGA supported: Supported
Data Bits 8
Trigger Rising Edge
Label Reginald
Label Location ↑ North
Label Font SansSerif Bold 16
Show in Registers Tab No
Appearance Logisim-Evolution
Reginald
00
D
Q
WE
R

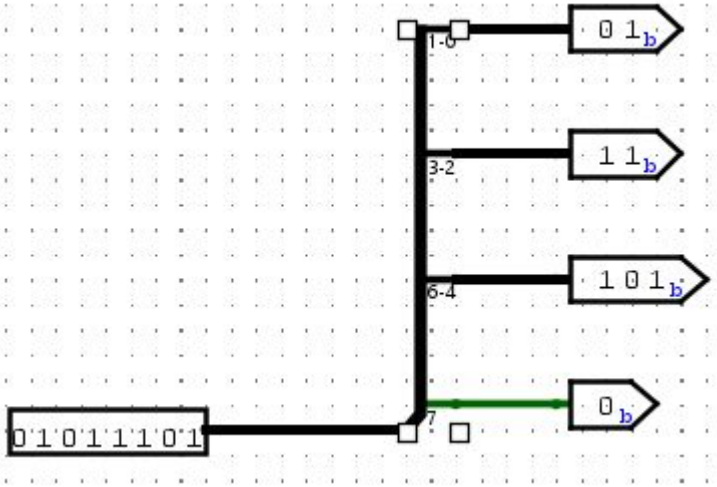
# Splitter

| Splitter (270,270) | |
|---|---|
| FPGA supported: | Supported |
| Facing | ← West |
| Fan Out | 2 |
| Bit Width In | 2 |
| Appearance | Left-handed |
| Spacing | 1 |
| Bit 0 | 0 (↑ Top) |
| Bit 1 | 1 (↓ Bottom) |



# Splitter cont.

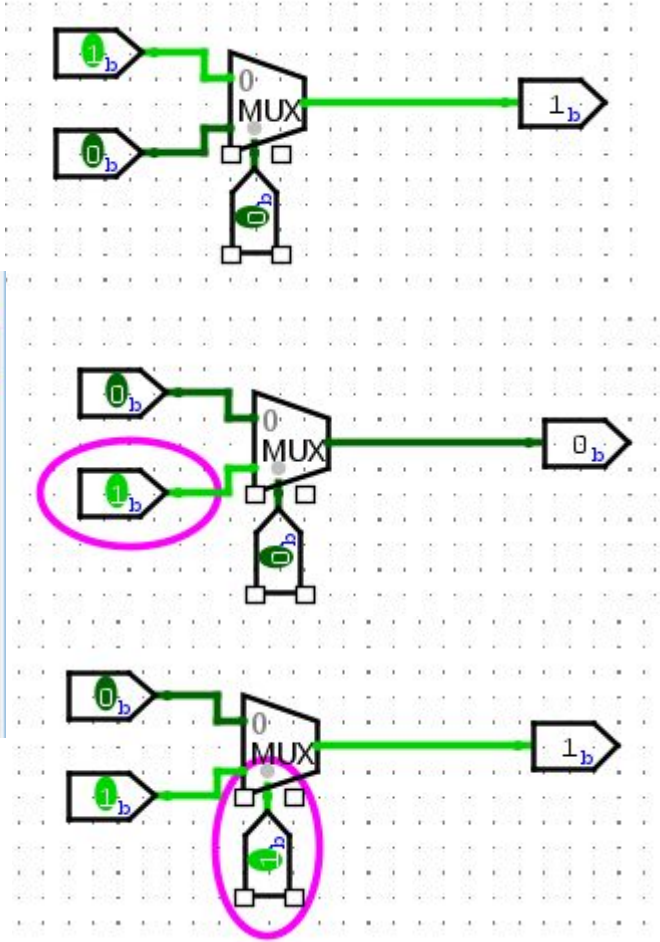
| Splitter (590,720) | |
|---|---|
| FPGA supported: | Supported |
| Facing | → East |
| Fan Out | 4 |
| Bit Width In | 8 |
| Appearance | Left-handed |
| Spacing | 5 |
| Bit 0 | 0 (↑ Top) |
| Bit 1 | 0 (↑ Top) |
| Bit 2 | 1 |
| Bit 3 | 1 |
| Bit 4 | 2 |
| Bit 5 | 2 |
| Bit 6 | 2 |
| Bit 7 | 3 (↓ Bottom) |




Tip: You can shift-click the bit rows to select multiple bits. Editing one bit's pins will then edit the pins for multiple bits at once! This can save lots of time.

# Mux

| Multiplexer (180,430) | |
|---|---|
| FPGA supported: | Supported |
| Facing | → East |
| Gate Size | Wide |
| Select Location | Bottom/Left |
| Select Bits | 1 |
| Data Bits | 1 |
| Disabled Output | Zero |
| Include Enable? | No |



# Wire colors and their meanings (from spec)

| Color | Meaning |
| --- | --- |
| Dark green | 1-bit wire has a value of 0 |
| Bright green | 1-bit wire has a value of 1 |
| Black | Multi-bit wire (many components have bit width attributes which can be configured in the attributes menu on the bottom left) |
| Red (values with `EEEE`) | The wire has multiple values on it (in this case, a `0` and `1` from the 2 inputs). Also, remember that a big circle appears at wire junctions. |
| Blue (values with `UUUU`) | The wire is floating (i.e. has no known value) |
| Orange | The wire is connected to components that have different bit widths. A simple example is a 1-bit input pin connected to a 2-bit output pin. In the shown example, there's a slightly hidden wire behind the `MUX` connecting the 2-bit lower data line to the 1-bit select line. Watch out for these! |

# Demo

- DEMO TIME