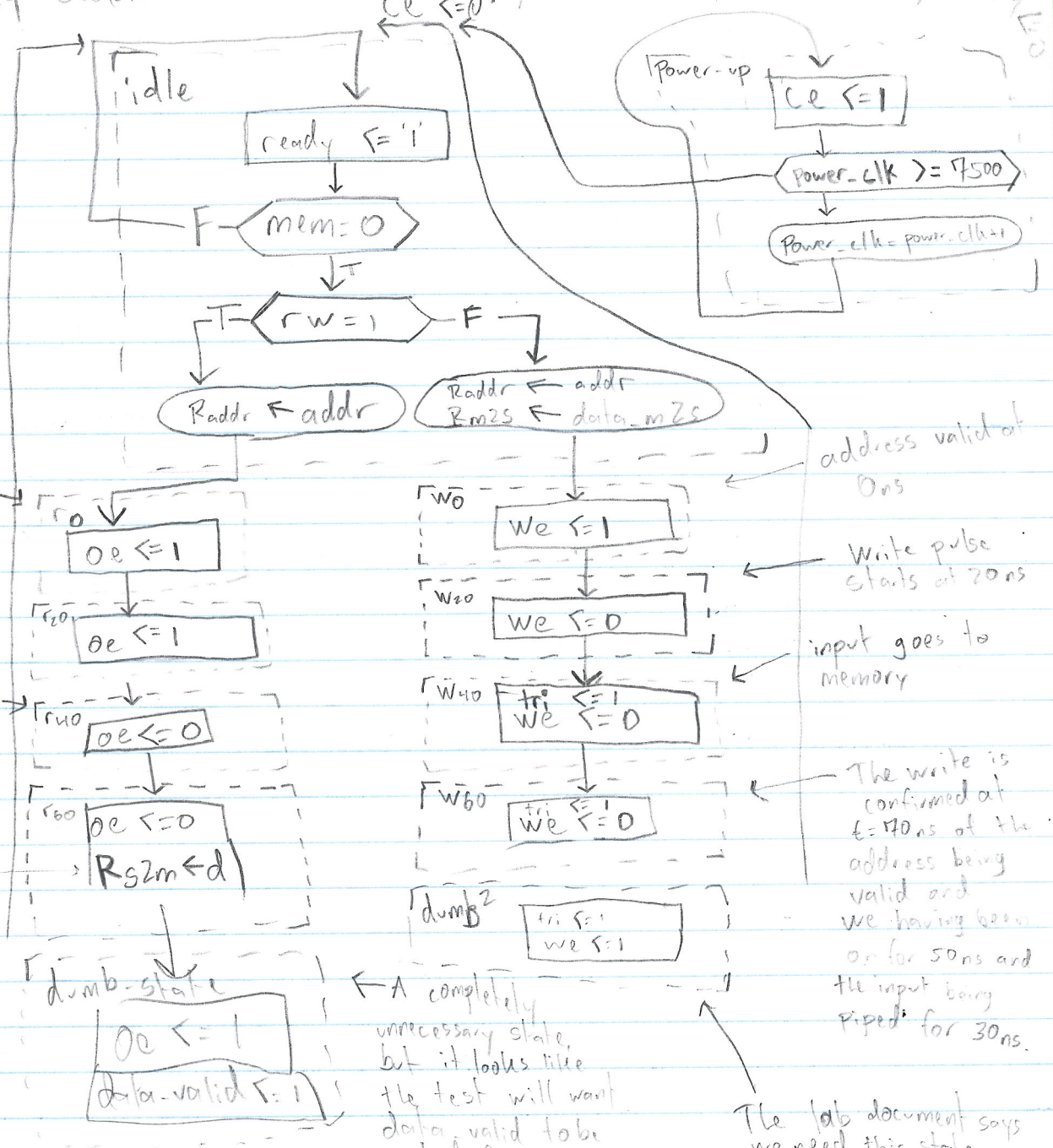
Taylor Conley Lab 9

default: data_valid 0, oe <= 1, we <= 1, tri_en <= 0, ready <= 0, ce <= 0



Address valid at 0ns

oe to be on 20ns before read

data not valid until 40ns, so Rs2m will initially get an invalid value but it will get a good one by the end.

address valid at 0ns

Write pulse starts at 20ns

input goes to memory

The write is confirmed at t = 40ns of the address being valid and we having been on for 50ns and the input being piped for 30ns.

A completely unnecessary state, but it looks like the test will want data_valid to be asserted for only 1 clock cycle... Maybe I will change the turning off of data_valid to the end of the idle state so we can get rid of this state.
The reason we can't put this in r60 (unless at the end) is because the data won't be valid

The lab document says we need this state to do the data_hold time, but for this chip the data hold time is 0ns - so this is unnecessary

Edit: I was correct - those states were unnecessary. But I was missing important signals in the process sensitivity list, so it took me a whole extra clock cycle to get the data