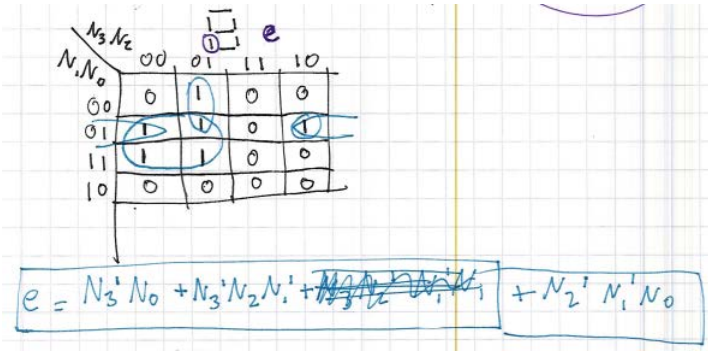
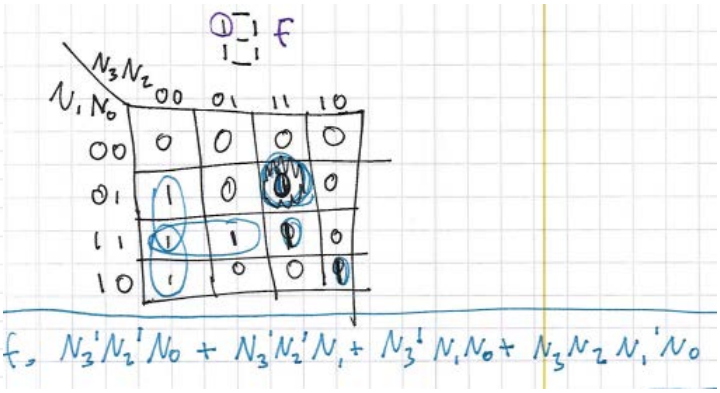
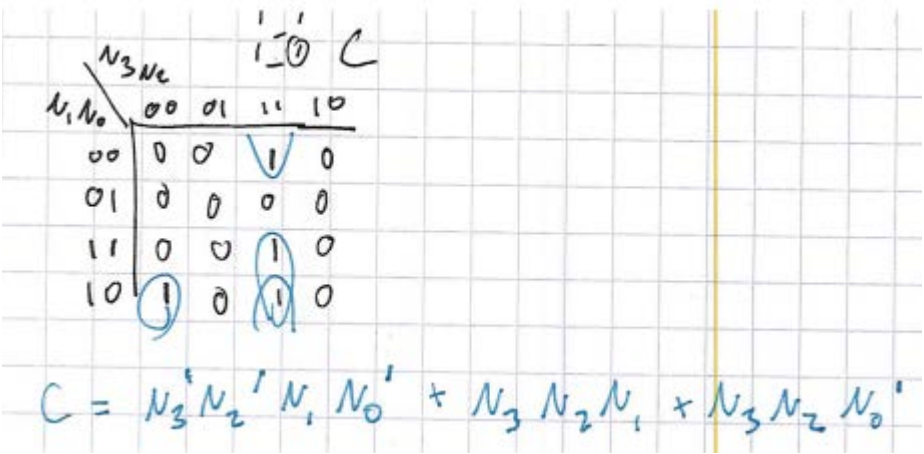
Taylor Cowley
Lab 04: CAD Schematic Entry and Simulation
May 12 2016

Input				(total)	Output						
N3	**N2**	**N1**	**N0**		**a**	**b**	**c**	**d**	**e**	**f**	**g**
0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	1	1	0	0	1	1	1	1
0	0	1	0	2	0	0	1	0	0	1	0
0	0	1	1	3	0	0	0	0	1	1	0
0	1	0	0	4	1	0	0	1	1	0	0
0	1	0	1	5	0	1	0	0	1	0	0
0	1	1	0	6	0	1	0	0	0	0	0
0	1	1	1	7	0	0	0	1	1	1	1
1	0	0	0	8	0	0	0	0	0	0	0
1	0	0	1	9	0	0	0	0	1	0	0
1	0	1	0	A	0	0	0	1	0	0	0
1	0	1	1	b	1	1	0	0	0	0	0
1	1	0	0	C	0	1	1	0	0	0	1
1	1	0	1	d	1	0	0	0	0	1	0
1	1	1	0	E	0	1	1	0	0	0	0
1	1	1	1	F	0	1	1	1	0	0	0
					2812	D860	9004	8492	02BA	208E	1083
High Asserted					**Low Asserted**						

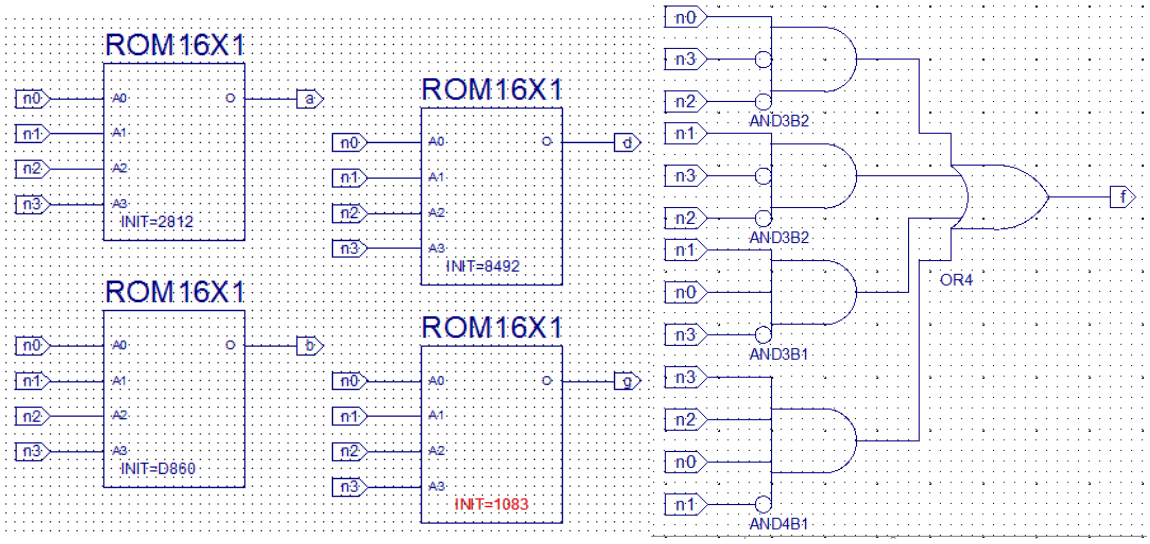


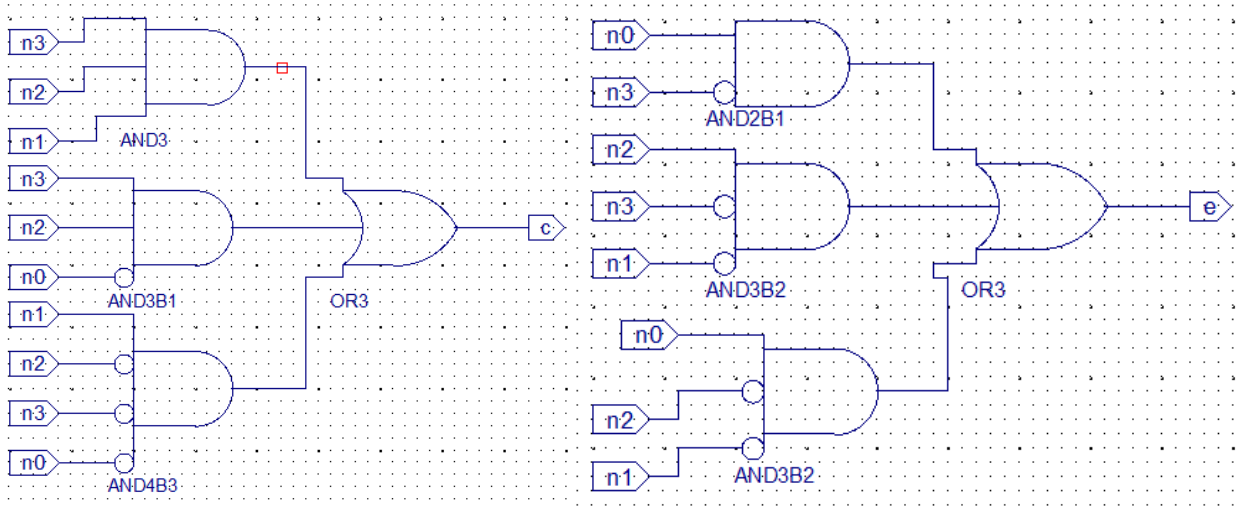




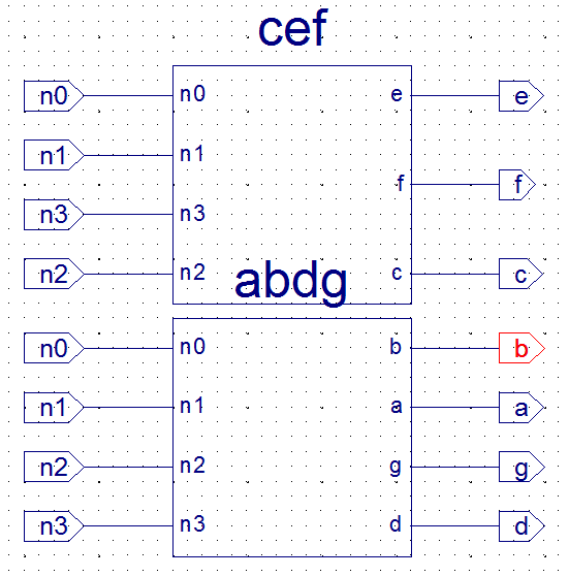
Procedure

ROM schematic and Combinational Logic Schematic





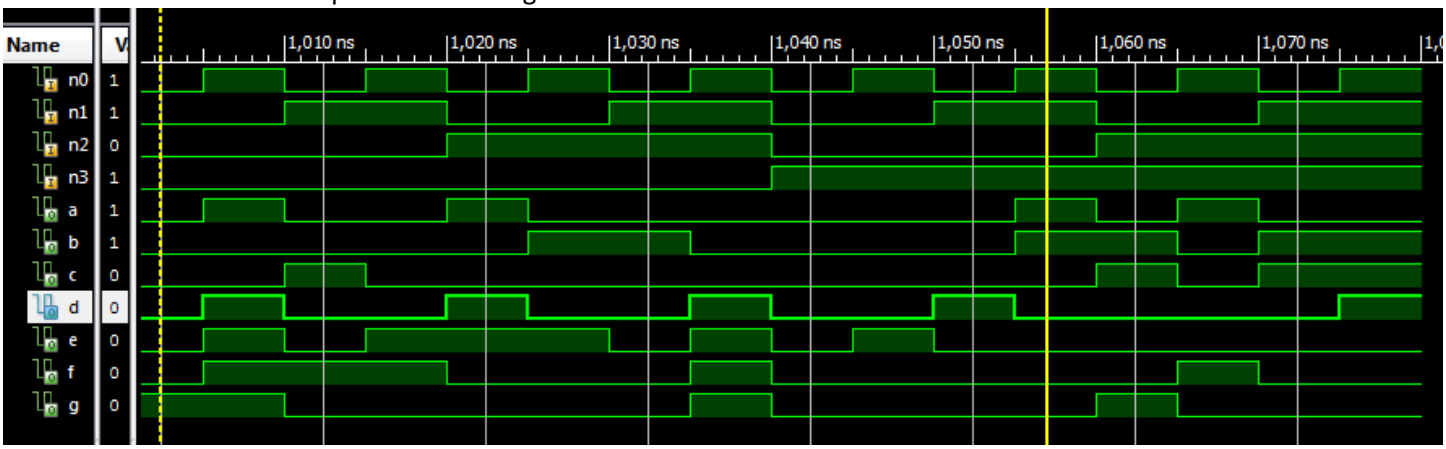
Seven Segment Decoder Schematic



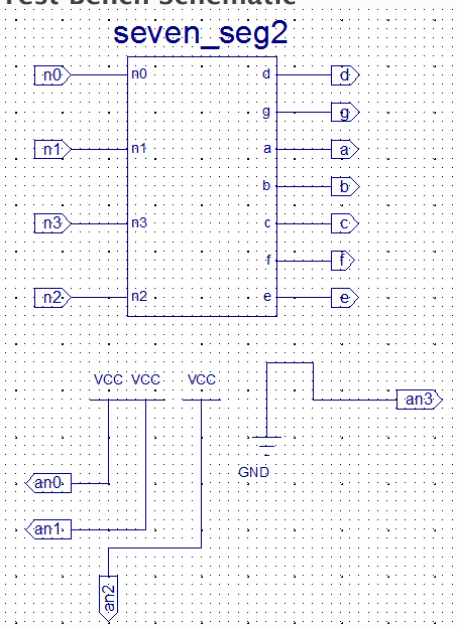
TCL File for simulation

```
isim force add n3 0
isim force add n2 0
isim force add n1 0
isim force add n0 0
run 5ns
isim force add n0 1
run 5ns
isim force add n1 1
isim force add n0 0
run 5ns
isim force add n0 1
run 5ns
isim force add n2 1
isim force add n1 0
isim force add n0 0
run 5ns
isim force add n0 1
run 5ns
isim force add n1 1
isim force add n0 0
run 5ns
isim force add n0 1
run 5ns
isim force add n3 1
isim force add n2 0
isim force add n1 0
isim force add n0 0
run 5ns
isim force add n0 1
run 5ns
isim force add n1 1
isim force add n0 0
run 5ns
isim force add n0 1
run 5ns
isim force add n1 1
isim force add n0 0
run 5ns
isim force add n0 1
run 5ns
isim force add n2 1
isim force add n1 0
isim force add n0 0
run 5ns
isim force add n0 1
run 5ns
```

Simulation waveform for top-level seven-segment schematic



Test Bench Schematic



Test Bench UCF

```
## Switches
NET "n0" LOC = "L14";
NET "n1" LOC = "L13";
NET "n2" LOC = "N17";
NET "n3" LOC = "R17";
## 7 segment display
NET "a" LOC = "L18";
NET "b" LOC = "F18";
NET "c" LOC = "D17";
NET "d" LOC = "D16";
NET "e" LOC = "G14";
NET "f" LOC = "J17";
NET "g" LOC = "H14";
NET "an0" LOC = "F17";
NET "an1" LOC = "H17";
NET "an2" LOC = "C18";
NET "an3" LOC = "F15";
```

Anomalies (bugs, problems, and suggestions)(5pts possible)

Well the first time I did the K-maps, I did it all correct, but I did not implement the schematic according to the k-map. So I had to redo the schematic. Also, I got confused on how to initialize the ROM to the proper value- I was reading the truth table backwards to make the Hexadecimal values.