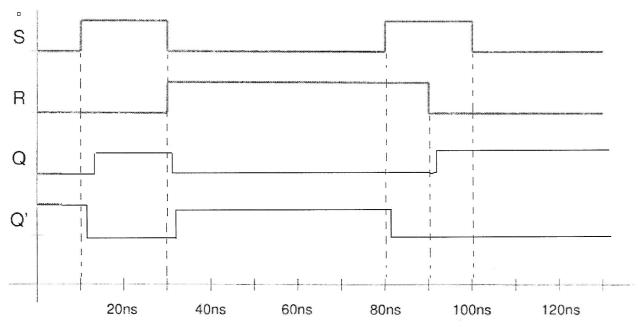
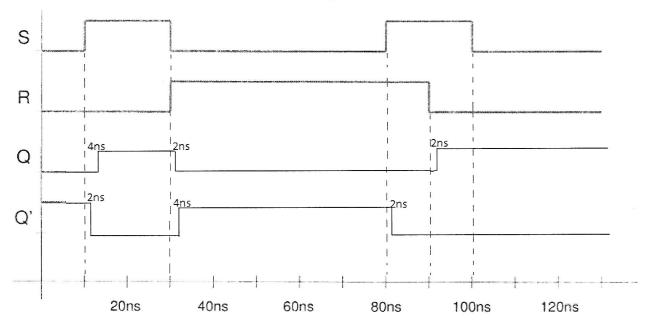
Taylor Cowley EE220 May 25 2016

HW 08 ch11

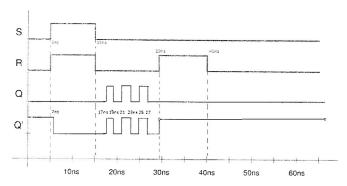
11.1. Below is a timing diagram for the SR latch of Figure 11.1. Fill in the output waveform. Reflect approximate timing. See Section 11.6 to remind you what is meant by *approximate timing*.



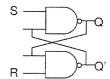
11.2. Repeat Problem 11.1 but with detailed timing. You may simply label each output signal transition in the timing diagram with the time it occurs. Delays of the various gates include: $t_{NOT}=1ns, t_{AND}=3ns, t_{NOR}=2ns$.



11.3. Complete the timing diagram below for an SR latch. In this case, the circuit oscillates. Use $t_{NOR}=2ns$ and accurately reflect the Q and Q' waveforms in the drawing (complete with timing).

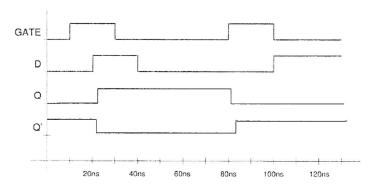


11.5. Shown in the figure below is a storage circuit made from NAND gates instead of NOR gates. Experiment with values on the *S* and *R* inputs to determine how it works. Hint: start with *S=R=*'1'. Write a transition table to summarize the operation of the gate.

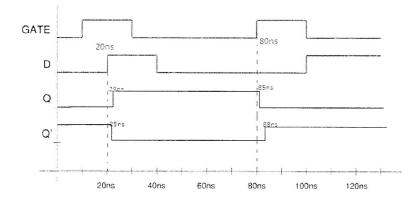


e to				
S	R	σ	Q+	Comment
1	1	1	1	Stable
1	1	0	0	
1	0	1	0	Reset
1	0	0	0	
0	1	1	1	Set
0	1	0	1	
0	0	1	n/a	unstable
	0	0	n/a	
0				

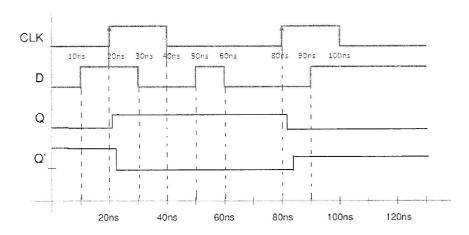
11.6. Below is a timing diagram for the circuit of Figure 11.7. Fill in the output waveform. Reflect approximate timing.



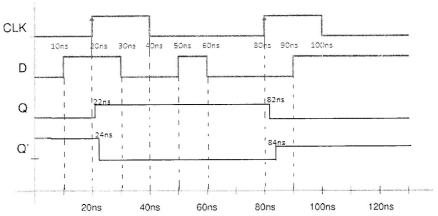
11.7. Repeat Problem 11.6 but with detailed timing. Use the following delays: $t_{NOT} = 1ns, t_{AND} = 3ns, t_{NOR} = 2ns$.



11.11. Below is a timing diagram for the circuit of Figure 11.18. Fill in the output waveform. Reflect approximate timing.



11.12. Repeat Problem 11.11 but with detailed timing. For your delays use the following: $t_{CLK-Q}=2ns,\,t_{setup}=4ns,\,t_{hold}=3ns.$ Which of these delays is actually needed in order to complete the timing diagram?



11.14. Befow is a toggle circuit along with a timing diagram. Complete the associated timing diagram complete with detailed timing. Use the delays from Problem 11.12. Also, use $t_{NOT}=2ns$.

