

# Computer Organization Homework 4 Cache Design





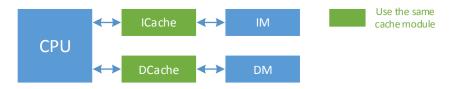


Figure 1. Relationship between CPU, ICache, DCache, IM, and DM

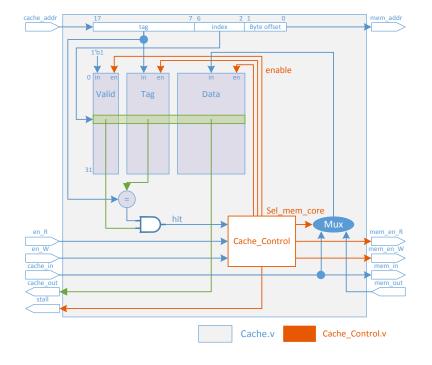


Figure 2. Cache Datapath used in this homework



## General rules for deliverables



- Complete this homework INDIVIDUALLY.
- When submitting your homework, compress all files into a single zip file, and upload the compressed file to Moodle.

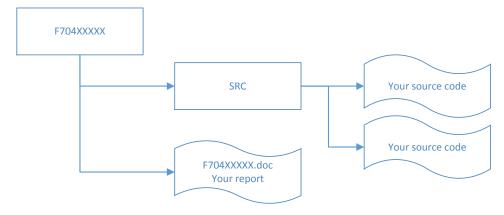


Figure 1. File hierarchy for homework submission



## Deadline



# • Due: 6/23(─) PM 9:50

#### HW Announcement:

- HW0 Self Introduction <u>Student\_info\_v1.pptx</u> Due: 3/1 9:50PM. If the course is not in your moodle account, you can mail homework 1 to nckuco@gmail.com
- · HW1 MIPS Instruction Due: 4/6
- HW2 Single-cycle Due:4/27 moved to 5/1 9:50PM
- HW3 Pipeline Due: 5/22->5/25 9:50 PM
- HW4 Cache Due:6/15-> 6/23 (Friday) 9:50PM

#### 繳交狀態

徽交狀態	沒有繳交作業		
評分狀態	尚未評分		
規定繳交時間	2017年 06月 12日(一) 21:55	Moodle will be update soon	!!!
剩餘時間	10 日 7 小時		



# 作業重點 - Outline



I/D Cache Size

Read Data From IM or DM

Cache Read Miss/Hit

Cache Write Miss/Hit (Write Through)

Modify CPU: Stall & MemRead



# I/D Cache Size

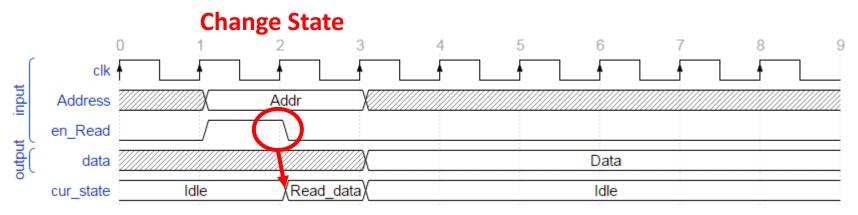


Cache Size	Cache Line	Cache Block	Way	Write Policy
128Byte	32	4Byte	Direct Map	Write Through

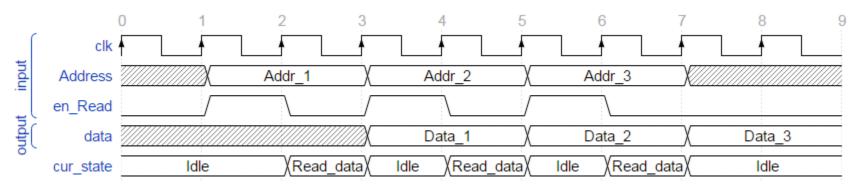


## Read Data From IM or DM





### Read One Data From I/D Memory



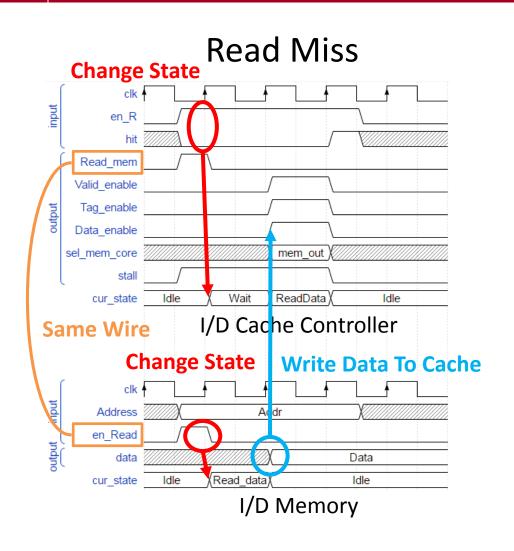
Read Three Datas From I/D Memory

Waveform:
<a href="ReadOneData">ReadOneData</a>
ReadThreeDatas

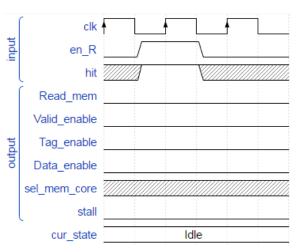


# Cache Read Miss/Hit





### Read Hit



I/D Cache Controller

Waveform:

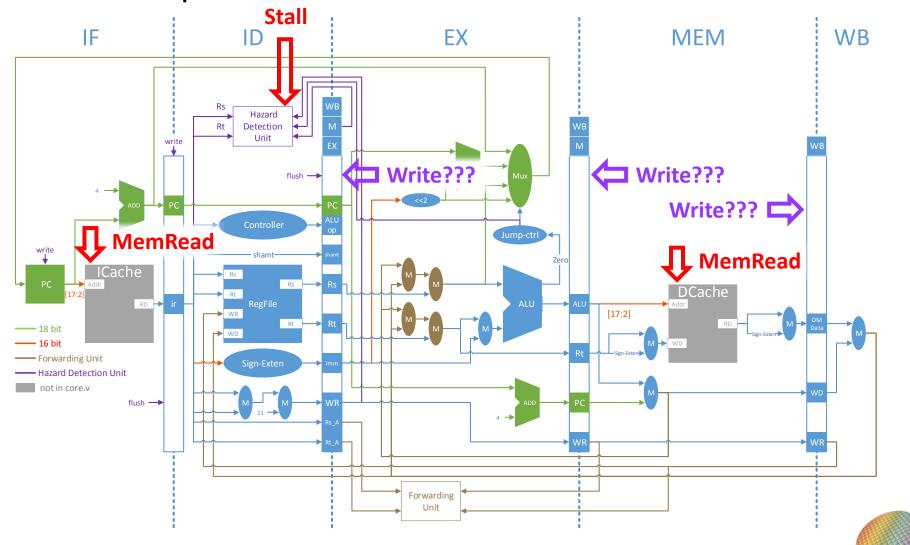
 $\frac{\text{ReadMiss}}{\text{ReadHit}}$ 





# Modify CPU: Stall & MemRead

HW3 top.v => HW4 Core.v



# Q&Atime

