Design and Modeling of Planar Power Switching Inductors for Monolithic and Single Chip DC-DC Power Converters

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Abstract— Engineers are continuously trying to integrate active circuit components of dc-dc converters on chip, while leaving behind the passive components because of their limited capabilities under small-scale integration. This document describes several key issues and design considerations relating to dc-dc converters under high frequencies. Inductor modeling and design of a buck converter are investigated, and a performance plot of the inductor under high switching frequency is presented.

1. INTRODUCTION

As handheld electronic hardware become smaller in size, higher demands for low voltage operation and high output current are becoming a necessity. The main unit in portable devices responsible for such functionality is the dc-dc converter. This means that the converter should maintain high efficiency in order to achieve a longer battery life, while shrinking it to fit on a smaller silicon die. The key to achieve full integration, which will reduce size and cost, is to operate these converters at high frequencies, typically greater than 5 MHz, while maintaining the required specs.

High switching frequency is becoming essential to achieve designs that are required for next generation handheld electronics. An engineer has to understand the high frequency design constraints and their issues before initiating the step to design a high switch mode converter [1]. The system description, design philosophy, and key issues of operating the buck dc-dc converter under high frequency are presented in section II. Inductor equivalent circuit, modeling, and operation under high switching frequency are included in section III. In Section IV performance plot of the Inductor as the operating frequency increases is reported. Operating at high frequency will allow the engineer to integrate the passive components of the converter along with the active components to achieve a single chip dc-dc converter.

2. CIRCUIT DESCRITON

The circuit schematic of a buck dc-dc converter is shown in Fig. 1. In this converter topology, when M1 turns on, the input voltage will be applied on the left side of the inductor. Thus, the input voltage will induce current through the inductor and will cause the current of the inductor to rise. When M1 turns off and M2 turns on, a closed loop consisting of the transistor M2, the inductor, and the capacitor will be formed and the inductor current will decrease as the off time increases. The main essential parameter in designing dc-dc converters is efficiency. This means that the converter should perform the same along the full load range. Usually the best efficiency is achieved at maximum load, which corresponds to maximum current supplied. However, the engineer faces a huge difficulty in maintaining a high efficiency at low load operation. Different techniques such as PFM, which skips pulses generated by the control circuitry, have been developed to maintain the required efficiency. Nevertheless, this degrades the converter stability and puts it at the risk of failure under extreme conditions. Also, this defeats the purpose of operating the converter at high frequencies. In the end, the ultimate goal is to operate these converters at high frequencies in order to integrate the whole unit on a single chip.

Method and design approaches for a high frequency dc-dc converter operating in the range of 100 MHz have been reported [2]. However, the suggested design approach is not economical, since the bill of materials of the components needed is enormous. Thus, it is not feasible in industrial applications where cost is the main driving element. In general, one needs to operate at high frequency while marinating the same number of components and reducing their respective sizes, which eventually reduces the overall cost. A problem arises, however, by keeping the same number of components and increasing the switching frequency. [3] analyzes the main problems associated with high frequency operation. A high frequency parasitic model of the boost dc-dc converter has been studied. It has been reported that parasitic resistances, inductances, and capacitances

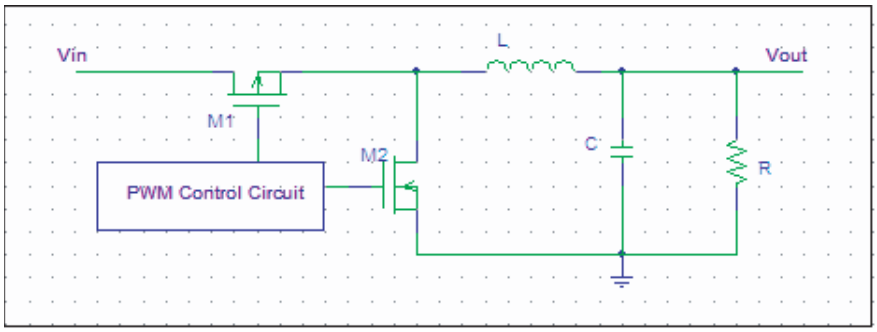

Figure 1: A buck dc-dc converter.

generated from packaging and interconnections of the converter arises at high frequencies. All these components will aid in degrading the converter efficiency. Thus, new packaging techniques should be introduced to overcome this major obstacle.

3. INDUCTOR MODELING

The inductor is the largest component in a dc-dc converter. Thus, innovative ideas of how to integrate the inductor on chip are necessary for achieving a miniaturized dc-dc converter. This is achieved by investigating the consequences of having a small inductor operating at a high frequency, and by modeling the inductor and its behavior under high frequency. Fig. 2 shows the equivalent circuit of an inductor at a frequency above 5 MHz.

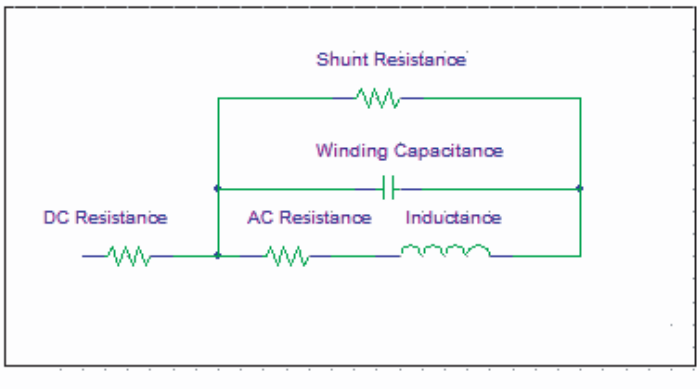

Figure 2: Inductor equivalent circuit.

The inductor in Fig. 2 consists of many frequency dependent elements: the AC resistance, the Inductance, and the shunt resistance. [1] illustrates that for small valued inductors, the resonance frequency occurs in the range of few GHz. This will ease defining the corner frequency of the LC filter in the converter when designing it. However, as shown in Fig. 2 above, the engineer should take into consideration the nonideality of the inductor under high frequency. One advantage of high frequency operation is that it allows reducing the size of the inductor, which will need less turns ratio which reduce resistive losses. Also, this will enable a faster dynamic response due to the wide bandwidth introduced in the control feedback circuit. The main problem with a smaller inductor is that the average rms current of the transistor switch will increase, and this will increase the conduction losses. This is because the peak-current rating of the inductor will increase, and this will force us to keep a large capacitor at the output. The Enpirion, EN5312QI 1A synchronous buck regulator, have achieved an integrated Inductor but on a separate die brought close to the converter's active circuitry die because of interference issues [1]. However, it was necessary to keep the capacitor as large as possible to eliminate voltage ripples at the output. Various methods and techniques on integrating the inductor on chip was studied in [4]. It was found that to minimize the AC resistance of the inductor at a high frequency range up to 10 MHz can be achieved by using "outof- plane" inductors constructed using PDMA. "The PDMA technology would have a smaller footprint and probably higher quality." [4].

4. HIGH FREQUENCY INDUCTOR PERFORMANCE

The power inductor in a commercial semiconductor process is designed using ANSOFT microwave modeling package including all of the electrical and thermal effects. The 3D HFSS model for the inductor designed is shown in Fig. 3. Fig. 4 illustrates a typical performance of the inductor at RF frequency. Inductors with values in excess of 100 nH capable of handling more than 1A current have been designed with a Q value of 40.

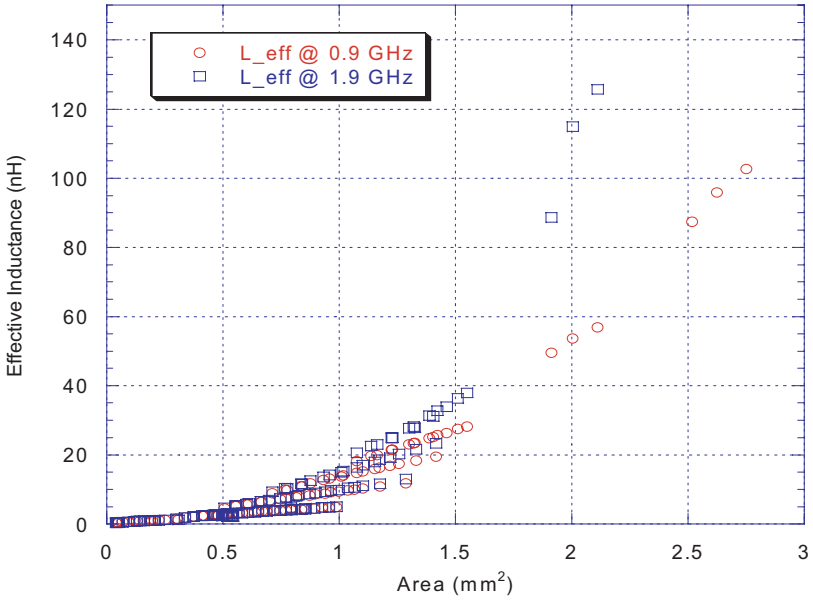

Figure 3: Inductor performance vs. frequency.

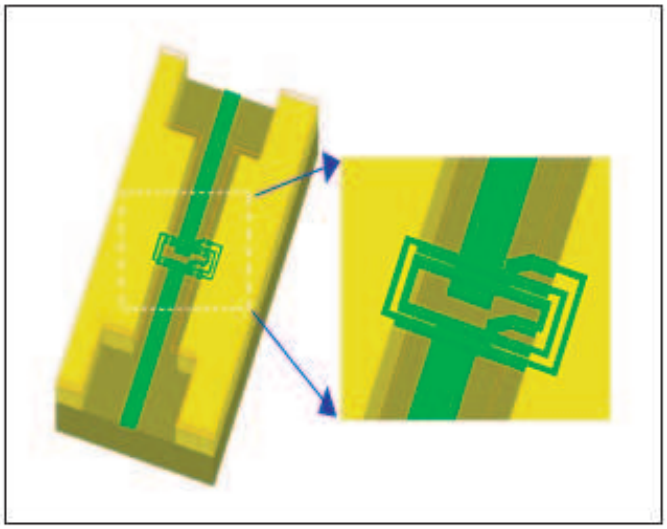

Figure 4: HFSS 3D inductor model.

The inductor is fabricated using a thick film Cu process with air as the dielectric. Experimental results are validated with 3D model calculations.

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