HEF4040B

12-stage binary ripple counter Rev. 8 — 17 November 2011

Product data sheet

1. **General description**

The HEF4040B is a 12-stage binary ripple counter with a clock input (CP), an overriding asynchronous master reset input (MR) and twelve fully buffered outputs (Q0 to Q11). The counter advances on the HIGH-to-LOW transition of $\overline{\text{CP}}$. A HIGH on MR clears all counter stages and forces all outputs LOW, independent of CP. Each counter stage is a static toggle flip-flop. The clock input is highly tolerant of slow rise and fall times due to its Schmitt trigger action.

It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to $V_{\text{DD}},\,V_{\text{SS}},$ or another input.

2. **Features and benefits**

- Tolerant of slow clock rise and fall time
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from –40 °C to +85 °C
- Complies with JEDEC standard JESD 13-B

3. Applications

- Frequency dividing circuits
- Time delay circuits
- Control counters

Ordering information

Table 1. **Ordering information**

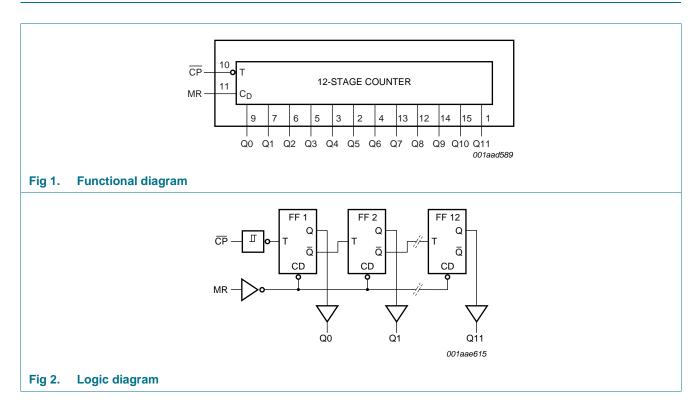
All types operate from $-40 \,^{\circ}\text{C}$ to $+85 \,^{\circ}\text{C}$.

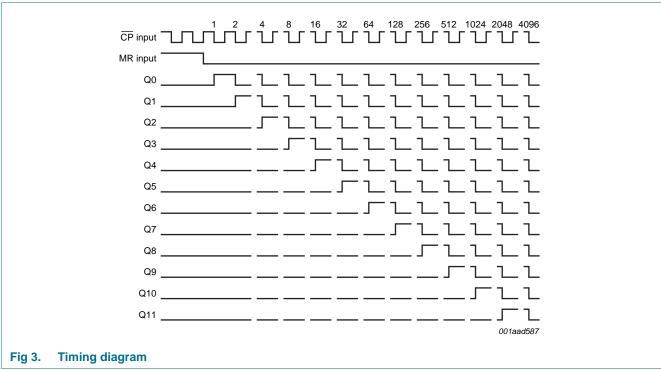
Type number	Package						
	Name	Description	Version				
HEF4040BP	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4				
HEF4040BT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1				



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5. Functional diagram

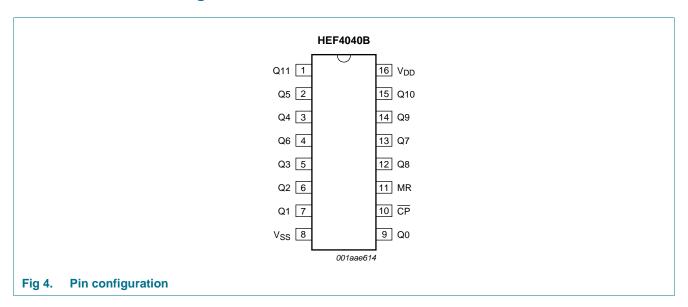




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6. Pinning information

6.1 Pinning



6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
V_{SS}	8	ground supply voltage
Q0 to Q11	9, 7, 6, 5, 3, 2, 4, 13, 12, 14, 15, 1	parallel output
CP	10	clock input (HIGH-to-LOW edge-triggered)
MR	11	master reset input (active HIGH)
V_{DD}	16	supply voltage

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7. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		-0.5	+18	V
I _{IK}	input clamping current	$V_I < -0.5 \text{ V or } V_I > V_{DD} + 0.5 \text{ V}$	-	±10	mA
V_{I}	input voltage		-0.5	$V_{DD} + 0.5$	V
I _{OK}	output clamping current	$V_O < -0.5 \text{ V or } V_O > V_{DD} + 0.5 \text{ V}$	-	±10	mA
I _{I/O}	input/output current		-	±10	mA
I _{DD}	supply current		-	50	mA
T _{stg}	storage temperature		- 65	+150	°C
T _{amb}	ambient temperature		-40	+85	°C
P _{tot}	total power dissipation	DIP16 package	<u>[1]</u> -	750	mW
		SO16 package	[2] _	500	mW
Р	power dissipation	per output	-	100	mW

^[1] For DIP16 package: P_{tot} derates linearly with 12 mW/K above 70 °C.

8. Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{DD}	supply voltage		3	-	15	V
VI	input voltage		0	-	V_{DD}	V
T _{amb}	ambient temperature	in free air	-40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	$V_{DD} = 5 V$	-	-	3.75	ms/V
		V _{DD} = 10 V	-	-	0.5	ms/V
		V _{DD} = 15 V	-	-	0.08	ms/V

9. Static characteristics

Table 5. Static characteristics

 $V_{SS} = 0 \ V$; $V_I = V_{SS}$ or V_{DD} ; unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	T _{amb} = -40 °C		T _{amb} = 25 °C		T _{amb} = 85 °C		Unit
				Min	Max	Min	Max	Min	Max	
V _{IH} HIGH	HIGH-level input voltage	$ I_{O} < 1 \mu A$	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
V _{IL} LO	LOW-level input voltage	I _O < 1 μA	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V

^[2] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

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 Table 5.
 Static characteristics ...continued

 $V_{SS} = 0 \ V$; $V_I = V_{SS} \ or \ V_{DD}$; unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	T _{amb} =	–40 °C	T _{amb} = 25 °C		T _{amb} = 85 °C		Unit
				Min	Max	Min	Max	Min	Max	
V _{OH} HIGH-level output voltage	HIGH-level output voltage	$ I_{O} < 1 \mu A$	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
		15 V	14.95	-	14.95	-	14.95	-	V	
V _{OL}	LOW-level output voltage	$ I_{O} < 1 \mu A$	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
I _{OH} HIC	HIGH-level output current	$V_0 = 2.5 \text{ V}$	5 V	-	-1.7	-	-1.4	-	-1.1	mΑ
		$V_0 = 4.6 \text{ V}$	5 V	-	-0.52	-	-0.44	-	-0.36	mΑ
		$V_0 = 9.5 \ V$	10 V	-	-1.3	-	-1.1	-	-0.9	mΑ
		$V_0 = 13.5 \text{ V}$	15 V	-	-3.6	-	-3.0	-	-2.4	mΑ
I _{OL}	LOW-level output current	$V_0 = 0.4 \ V$	5 V	0.52	-	0.44	-	0.36	-	mΑ
		$V_0 = 0.5 \ V$	10 V	1.3	-	1.1	-	0.9	-	mΑ
		V _O = 1.5 V	15 V	3.6	-	3.0	-	2.4	-	mΑ
ILI	input leakage current		15 V	-	±0.3	-	±0.3	-	±1.0	μΑ
I _{DD}	supply current	I _O = 0 A	5 V	-	20	-	20	-	150	μΑ
			10 V	-	40	-	40	-	300	μΑ
			15 V	-	80	-	80	-	600	μΑ
Cı	input capacitance		-	-	-	-	7.5	-	-	pF

10. Dynamic characteristics

Table 6. Dynamic characteristics

 $V_{SS} = 0 \text{ V; } T_{amb} = 25 \text{ °C; unless otherwise specified; for test circuit see } \underline{Figure 6}.$

Symbol	Parameter	Conditions	V_{DD}		Extrapolation formula[1]	Min	Тур	Max	Unit
t _{PHL}	HIGH to LOW	$\overline{CP} \to Q0$	5 V		78 ns + $(0.55 \text{ ns/pF})C_L$	-	105	210	ns
	propagation delay	see <u>Figure 5</u>	10 V		34 ns + (0.23 ns/pF)C _L	-	45	90	ns
			15 V		27 ns + (0.16 ns/pF)C _L	-	35	70	ns
		$Qn \rightarrow Qn + 1$	5 V	[2]	(0.55 ns/pF)C _L	-	35	70	ns
			10 V	[2]	(0.23 ns/pF)C _L	-	15	30	ns
			15 V	[2]	(0.16 ns/pF)C _L	-	10	20	ns
		$MR \rightarrow Qn$ see Figure 5	5 V		63 ns + $(0.55 \text{ ns/pF})C_L$	-	90	180	ns
			10 V		29 ns + (0.23 ns/pF)C _L	-	40	80	ns
			15 V		22 ns + (0.16 ns/pF)C _L	-	30	60	ns
t _{PLH}	LOW to HIGH	$\overline{CP} \to Q0$	5 V		58 ns + $(0.55 \text{ ns/pF})C_L$	-	85	170	ns
	propagation delay	see <u>Figure 5</u>	10 V		29 ns + (0.23 ns/pF)C _L	-	40	80	ns
			15 V		22 ns + (0.16 ns/pF)C _L	-	30	60	ns
		$Qn \rightarrow Qn + 1$	5 V	[2]	(0.55 ns/pF)C _L	-	35	70	ns
			10 V	[2]	(0.23 ns/pF)C _L	-	15	30	ns
			15 V	[2]	(0.16 ns/pF)C _L	-	10	20	ns

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 Table 6.
 Dynamic characteristics ...continued

 $V_{SS} = 0 \text{ V}$; $T_{amb} = 25 \,^{\circ}\text{C}$; unless otherwise specified; for test circuit see <u>Figure 6</u>.

Symbol	Parameter	Conditions	V_{DD}	Extrapolation formula[1]	Min	Тур	Max	Unit
t _t	transition time	see Figure 5	5 V	3 10 ns + (1.00 ns/pF)C _L	-	60	120	ns
			10 V	9 ns + (0.42 ns/pF)C _L	-	30	60	ns
			15 V	6 ns + (0.28 ns/pF)C _L	-	20	40	ns
t _W pulse	pulse width	CP input HIGH;	5 V		50	25	-	ns
		minimum width;	10 V		30	15	-	ns
		see <u>Figure 5</u>	15 V		20	10	-	ns
		MR input HIGH; minimum width; see <u>Figure 5</u>	5 V		40	20	-	ns
			10 V		30	15	-	ns
			15 V		20	10	-	ns
t _{rec}	recovery time	MR input;	5 V		40	20	-	ns
		see Figure 5	10 V		30	15	-	ns
			15 V		20	10	-	ns
f _{max}	maximum	CP input;	5 V		10	20	-	MHz
	frequency	see Figure 5	10 V		15	30	-	MHz
			15 V		25	50	-	MHz

^[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF).

Table 7. Dynamic power dissipation P_D

 P_D can be calculated from the formulas shown. $V_{SS} = 0$ V; $t_r = t_f \le 20$ ns; $T_{amb} = 25$ °C.

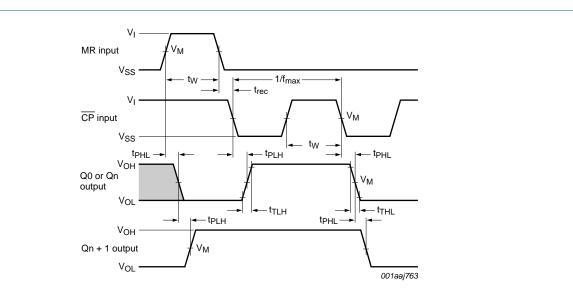
Symbol	Parameter	V_{DD}	Typical formula for P_D (μ W)	where:
P_D	dynamic power	5 V	$P_D = 400 \times f_i + \Sigma (f_o \times C_L) \times V_{DD}^2$	f_i = input frequency in MHz,
dis	dissipation	10 V	$P_D = 2000 \times f_i + \Sigma (f_o \times C_L) \times V_{DD}^2$	f _o = output frequency in MHz,
		15 V	$P_D = 5200 \times f_i + \Sigma (f_o \times C_L) \times V_{DD}^2$	C_L = output load capacitance in pF,
				V_{DD} = supply voltage in V,
				$\Sigma(f_0 \times C_L)$ = sum of the outputs.

^[2] For loads other than 50 pF at the n^{th} output, use the slope given.

^[3] t_t is the same as t_{THL} and t_{TLH} .

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11. Waveforms



Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Transition times: transition time (t_t) = HIGH LOW (t_{THL}) or LOW HIGH (t_{TLH}) transition times.

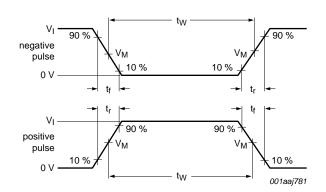
Measurement points are given in $\underline{\text{Table 8}}$, test circuit in $\underline{\text{Figure 6}}$ and test data in $\underline{\text{Table 9}}$

Fig 5. Waveforms showing propagation delays for MR to Qn and $\overline{\text{CP}}$ to Q0, minimum MR and $\overline{\text{CP}}$ pulse widths

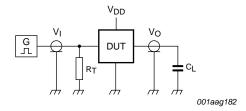
Table 8. Measurement points

Supply voltage	Input	Output	
V_{DD}	V _I	V _M	V _M
5 V to 15 V	V _{DD} or V _{SS}	0.5V _{DD}	0.5V _{DD}

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a. Input waveforms



b. Test circuit

Test data is given in Table 9.

Definitions test circuit:

DUT = Device Under Test;

C_L = load capacitance, including the jig and probe capacitance;

 R_L = load resistance, which should be equal to the output impedance of the pulse generator.

Fig 6. Test circuit for measuring switching times

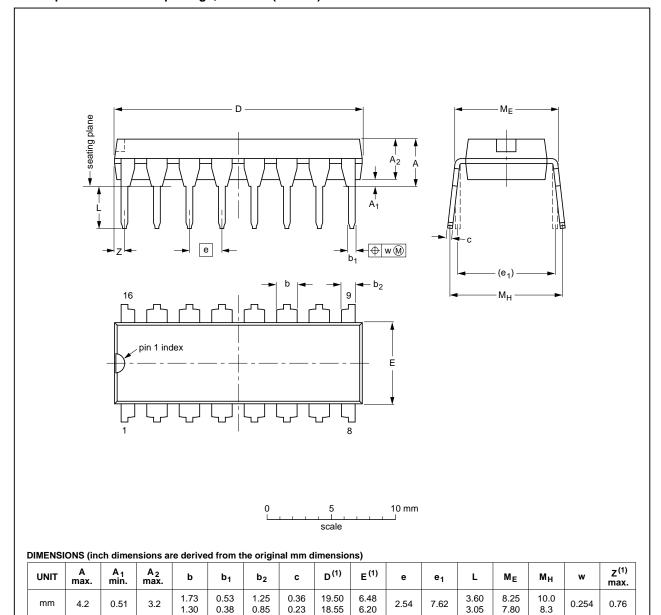
Table 9. Test data

Supply voltage	Input	Load	
V_{DD}	VI	t _r , t _f	CL
5 V to 15 V	V _{SS} or V _{DD}	≤ 20 ns	50 pF

12. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



inches

0.17

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

0.015

0.049

0.033

0.014

0.068

0.051

OUTLINE	OUTLINE REFERENCES					ISSUE DATE	
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT38-4						95-01-14 03-02-13	

0.77

0.26

0.1

0.14

0.32

Fig 7. Package outline SOT38-4 (DIP16)

0.02

0.13

HEF4040B

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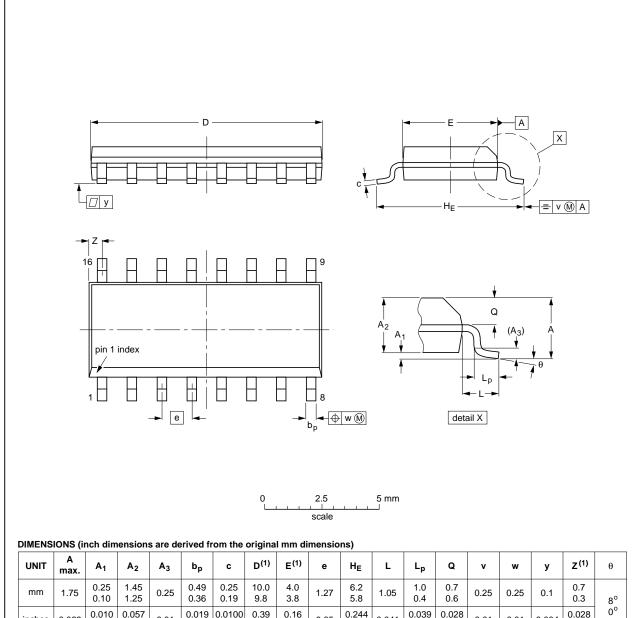
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0.01

0.03

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	ø	v	w	у	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069	0.010 0.004	0.057 0.049	0.01	l	0.0100 0.0075		0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016		0.01	0.01	0.004	0.028 0.012	0°

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT109-1	076E07	MS-012				99-12-27 03-02-19	

Fig 8. Package outline SOT109-1 (SO16)

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13. Revision history

Table 10. Revision history

	-			
Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4040B v.8	20111117	Product data sheet	-	HEF4040B v.7
Modifications:	 Legal page: 	s updated.		
	 Changes in 	"General description" and "F	eatures and benefits".	
HEF4040B v.7	20111010	Product data sheet	-	HEF4040B v.6
HEF4040B v.6	20091125	Product data sheet	-	HEF4040B v.5
HEF4040B v.5	20090709	Product data sheet	-	HEF4040B v.4
HEF4040B v.4	20090304	Product data sheet	-	HEF4040B_CNV v.3
HEF4040B_CNV v.3	19950101	Product specification	-	HEF4040B_CNV v.2
HEF4040B_CNV v.2	19950101	Product specification	-	-

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14. Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions"
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