計算機結構 HW2　　b08901019 吳冠緯

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Test function of multiplication...
Multiplication task correct
Test function of division...
Division task correct
Test function of AND...
AND task correct
Test function of OR...
OR task correct
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-   Success!! You passed the simulation   -
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```

```
================================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
================================================================================
|      shreg_reg      | Flip-flop |  64   |  Y  | N  | Y  | N  | N  | N  | N  |
|     alu_in_reg      | Flip-flop |  32   |  Y  | N  | Y  | N  | N  | N  | N  |
|      state_reg      | Flip-flop |   3   |  Y  | N  | Y  | N  | N  | N  | N  |
|     counter_reg     | Flip-flop |   5   |  Y  | N  | Y  | N  | N  | N  | N  |
================================================================================
Presto compilation completed successfully.
Current design is now '/home/raid7_2/userb08/b08019/1101_CA_HW2/ALU.db:ALU'
Loaded 1 design.
Current design is 'ALU'.
```