Hi3861 V100 / Hi3861L V100 / Hi3881 V100 Wi-Fi Chip

Hardware User Guide

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About This Document

Purpose

This document describes the package pins, electrical characteristics, schematic diagram design recommendations, printed circuit board (PCB) design recommendations, thermal design recommendations, soldering process, moisture-sensitive parameters, interface timings, and precautions of Hi3861 V100, Hi3861L V100, and Hi3881 V100, providing hardware design reference for hardware development engineers.

Related Versions

The following table lists the product versions related to this document.

Product Name	Version
Hi3861	V100
Hi3861L	V100
Hi3881	V100

Intended Audience

The document is intended for:

- PCB hardware development engineers
- Software engineers
- Technical support engineers

Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description
DANGER	Indicates a hazard with a high level of risk which, if not avoided, will result in death or serious injury.
WARNING	Indicates a hazard with a medium level of risk which, if not avoided, could result in death or serious injury.
CAUTION	Indicates a hazard with a low level of risk which, if not avoided, could result in minor or moderate injury.
NOTICE	Indicates a potentially hazardous situation which, if not avoided, could result in equipment damage, data loss, performance deterioration, or unanticipated results. NOTICE is used to address practices not related to personal injury.
NOTE	Supplements the important information in the main text. NOTE is used to address information not related to personal injury, equipment damage, and environment deterioration.

Change History

Issue	Date	Change Description
01	2020-04-30	This issue is the first official release. • In **1.1.2 Pinout**, **Table 1-2** is updated. • In **1.2.3 RTC Pins**, the description of the two external RTC clock input solutions supported by Hi3861L V100 is updated. • In **Table 1-6** of **1.2.4 PMU Control Pin**, the description of PMU_PWRON is updated. • In **1.2.11 CLK Pins**, the voltages of **Table 1-12** are updated. • In **1.4.1 Pin Multiplexing In Hardware**, the description of reset signal 1 for GPIO_00, GPIO_01, GPIO_02, GPIO_03, GPIO_04, and GPIO_06 is updated. • In **2.5 Power-Up/Down Sequences**, **Step 4** is updated. The description of the VDDIO pins is updated. • In **3.2.2 VBAT Power Supplies**, the description of the TX power (output power) is updated. • In **3.2.6 Buck/LDO Power Supplies**, the description of the saturation current of the recommended inductor is updated. • Section 8.1 "SFC Interface Timings" is deleted. • In **Table 8-15** and **Table 8-16** of **8.4 SDIO Interface Timing**, the descriptions of t_{ODLY} and t_{OH} are updated.
00B04	2020-04-08	• In **2.5 Power-Up/Down Sequences**, the description in **Step 3** is updated. • In **4.3 PCB Layout**, the precautions in **Figure 4-3** are updated. • In **4.5 RF Trace Routing**, the RF routing recommendations for VDD_WL_RF_PA2G_3P3 and filter capacitors are updated. • In **6.2 Parameter Requirements on Lead-Free Reflow Soldering**, **Figure 6-2** is updated.
00B03	2020-02-12	In section 8.1 "SFC Interface Timings", the parameters (output data signal delay and output CS signal delay) are updated in the SFC output timing parameter table

Issue	Date	Change Description
00B02	2019-12-19	• In **Table 1-11**, the description of multiplexed signal 6 of pin 32 is updated. • In **Table 3-4**, the RTC clock of the drive level is updated. • In **7.1 Storage and Usage**, The moisture sensitivity level of the product is level 3 in [Usage of Moisture-Sensitive Products].
00B01	2019-11-15	This issue is the first draft release.

Contents

1 Package and Pins

1.1 Package and Pinout

1.1.1 Package

Hi3861 V100/Hi3861L V100/Hi3881 V100 uses the QFN-32 package. The package size is 5 mm x 5 mm (0.20 in. x 0.20 in.), and the ball pitch is 0.5 mm (0.02 in.). For details about the package, see **Figure 1-1** to **Figure 1-3**.

Figure 1-1 Package top view

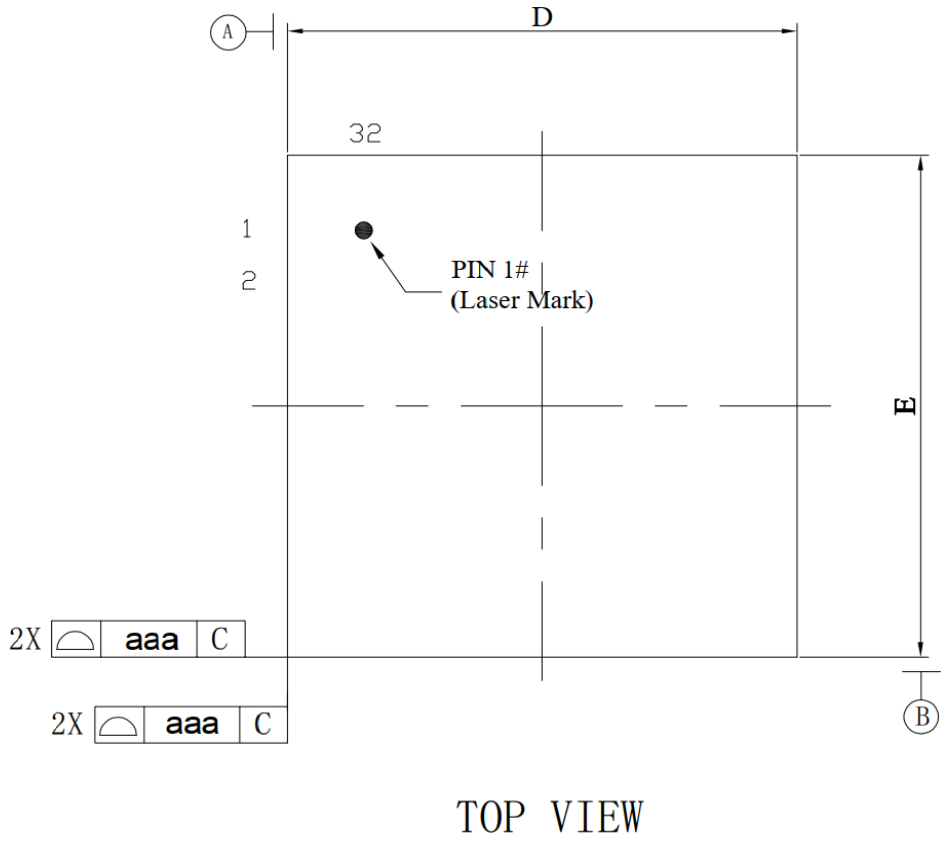


Figure 1-2 Package bottom view

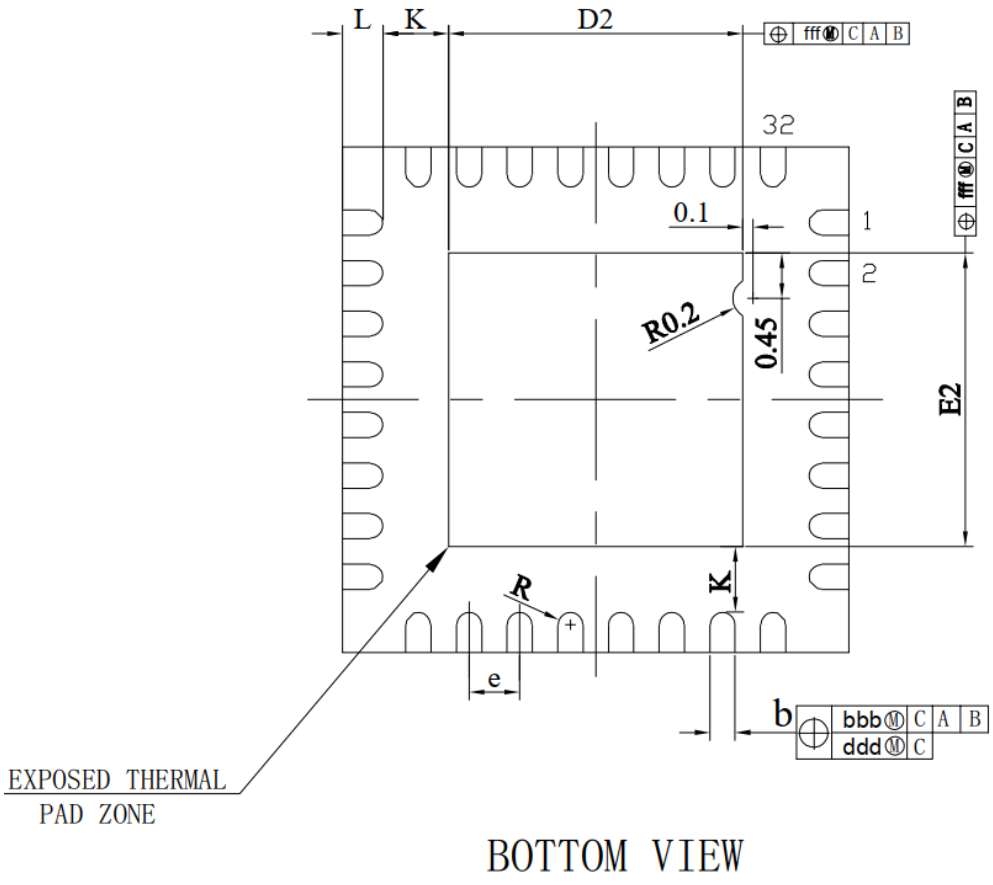


Figure 1-3 Package side view (enlarged)

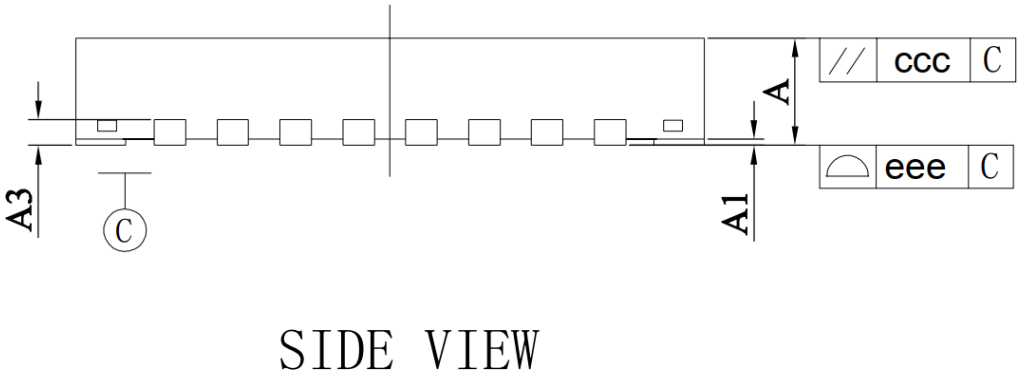


Table 1-1 describes the package dimensions.

Table 1-1 Package parameters of the chip

Parameter	Dimensions (mm)			Dimensions (in.)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D	4.93	5.00	5.07	0.194	0.197	0.200
E	4.93	5.00	5.07	0.194	0.197	0.200
D2	2.80	2.90	3.00	0.110	0.114	0.118
E2	2.80	2.90	3.00	0.110	0.114	0.118
e	0.50 BSC			0.020 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.65REF			0.026		
R	0.075	0.125	0.175	0.003	0.005	0.007
aaa	0.15			0.006		
bbb	0.10			0.004		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D	4.93	5.00	5.07	0.194	0.197	0.200
E	4.93	5.00	5.07	0.194	0.197	0.200
D2	2.80	2.90	3.00	0.110	0.114	0.118
E2	2.80	2.90	3.00	0.110	0.114	0.118
e	0.50 BSC			0.020 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

Parameter	Dimensions (mm)			Dimensions (in.)		
K	0.65REF			0.026		
R	0.075	0.125	0.175	0.003	0.005	0.007
aaa	0.15			0.006		
bbb	0.10			0.004		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

1.1.2 Pinout

Figure 1-4 shows the pin map of Hi3861 V100/Hi3861L V100/Hi3881 V100.

Figure 1-4 Pin map of Hi3861 V100/Hi3861L V100/Hi3881 V100 (top view)

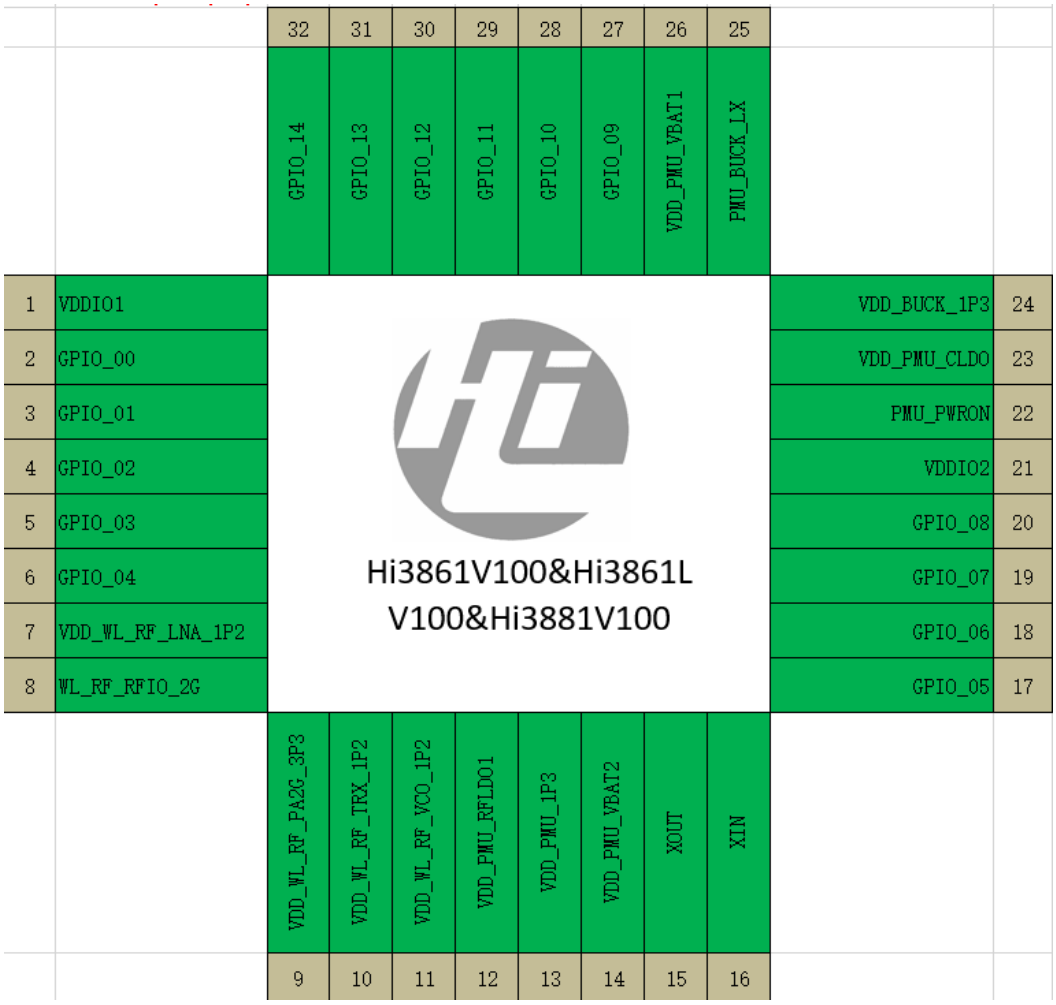


Table 1-2 Hi3861 V100/Hi3861L V100/Hi3881 V100 key features

Chip	External RTC Support	Flash Support
Hi3861V100	Not supported	Built-in 2 MB flash memory
Hi3861LV100	Supported	Built-in 2 MB flash memory
Hi3881V100	Not supported	Not supported

1.2 Pin Description

1.2.1 Pin Types

Table 1-3 describes the I/O types of the pins.

Table 1-3 I/O types

I/O	Description
I	Input signal
I_{PD}	Input signal, internal pull-down
I_{PU}	Input signal, internal pull-up
I_S	Input signal with a Schmitt trigger
I_{SPD}	Input signal with a Schmitt trigger, internal pull-down
I_{SPU}	Input signal with a Schmitt trigger, internal pull-up
O	Output signal
O_{OD}	Output open drain (OD)
I/O	Bidirectional (I/O) signal
I_{PD}/O	Bidirectional signal, input pull-down
I_{PU}/O	Bidirectional signal, input pull-up
I_{SPD}/O	Bidirectional signal with a Schmitt trigger, input pull-down
I_{SPU}/O	Bidirectional signal with a Schmitt trigger, input pull-up
I_{PD}/O_{OD}	Bidirectional signal, input pull-down and output OD
I_{PU}/O_{OD}	Bidirectional signal, input pull-up and output OD

I/O	Description
I_S/O	Bidirectional signal, input with a Schmitt trigger
I_S/O_{OD}	Bidirectional signal, input with a Schmitt trigger and output OD
CIN	Crystal oscillator input
COUT	Crystal oscillator output
P	Power supply
G	Ground (GND)

1.2.2 Pin Assignments

Hi3861 V100/Hi3861L V100/Hi3881 V100 uses the QFN-32 package. **Table 1-4** describes the pin assignments.

Table 1-4 Pin assignments of Hi3861 V100/Hi3861L V100/Hi3881 V100

Pin No.	Pin Name	Pin No.	Pin Name
1	VDDIO1	18	GPIO_06
2	GPIO_00	19	GPIO_07
3	GPIO_01	20	GPIO_08
4	GPIO_02	21	VDDIO2
5	GPIO_03	22	PMU_PWRON
6	GPIO_04	23	VDD_PMU_CLDO
7	VDD_WL_RF_LNA_1P2	24	VDD_BUCK_1P3
8	WL_RF_RFIO_2G	25	VDD_BUCK_LX
9	VDD_WL_RF_PA2G_3P3	26	VDD_PMU_VBAT1
10	VDD_WL_RF_TRX_1P2	27	GPIO_09
11	VDD_WL_RF_VCO_1P2	28	GPIO_10
12	VDD_PMU_RFLDO1	29	GPIO_11
13	VDD_PMU_1P3	30	GPIO_12
14	VDD_PMU_VBAT2	31	GPIO_13
15	XOUT	32	GPIO_14
16	XIN	33	EPAD

Pin No.	Pin Name	Pin No.	Pin Name
17	GPIO_05	-	-

1.2.3 RTC Pins

Hi3861L V100 supports two external RTC input solutions:

- Crystal oscillator single-ended input: multiplexed with GPIO_00
- 32.768 kHz crystal input: XIN_OUT is multiplexed with GPIO_00, and XIN_IN is multiplexed with GPIO_01.

Table 1-5 RTC pins

Pin	Name	Type	Frequency (MHz)	Level (V)	Description
2	GPIO_00	I/O	< 10	3.3/1.8	Crystal oscillator single-ended mode: input Crystal mode: output
3	GPIO_01	I/O	< 10	3.3/1.8	Crystal mode: input

1.2.4 PMU Control Pin

Table 1-6 describes the global control pin.

Table 1-6 Global control pin

Pin	Name	Type	Frequency (MHz)	Level (V)	Description
22	PMU_PWRON	I	<1	3.3/1.8	PMU power-on enable pin (following the VDDIO level) 0: powered off 1: powered on

1.2.5 GPIO Pins

Table 1-7 describes the GPIO pins. All I/Os support the fail-safe (FS) function.

Table 1-7 GPIO pins

Pin	Name	Type	Level (V)	Description
2	GPIO_00	I/O	3.3/1.8	Common GPIO
3	GPIO_01	I/O	3.3/1.8	Common GPIO
4	GPIO_02	I/O	3.3/1.8	Common GPIO
5	GPIO_03	I/O	3.3/1.8	Common GPIO. In ultra deep sleep mode, wakeup can be triggered at the I/O rising edge.
6	GPIO_04	I/O	3.3/1.8	Common GPIO
17	GPIO_05	I/O	3.3/1.8	Common GPIO. In ultra deep sleep mode, wakeup can be triggered at the I/O rising edge.
18	GPIO_06	I/O	3.3/1.8	Common GPIO
19	GPIO_07	I/O	3.3/1.8	Common GPIO. In ultra deep sleep mode, wakeup can be triggered at the I/O rising edge.
20	GPIO_08	I/O	3.3/1.8	Common GPIO
27	GPIO_09	I/O	3.3/1.8	Common GPIO
28	GPIO_10	I/O	3.3/1.8	Common GPIO
29	GPIO_11	I/O	3.3/1.8	Common GPIO
30	GPIO_12	I/O	3.3/1.8	Common GPIO
31	GPIO_13	I/O	3.3/1.8	Common GPIO
32	GPIO_14	I/O	3.3/1.8	Common GPIO. In ultra deep sleep mode, wakeup can be triggered at the I/O rising edge.

1.2.6 Power Supply Pins

Table 1-8 describes the power supply pins.

Table 1-8 Power supply pins

Pin	Name	Type	Voltage (V)	Description
26	VDD_PMU_VBAT1	P	2.3–3.6	Internal buck power supply input
25	VDD_BUCK_LX	P	Duty cycle output	Buck power tube output with 2.2 µH output inductance, connected to the board-level 4.7 µF capacitor for filtering
24	PMU_BUCK_1P3	P	1.3	Buck power supply output, supplying power to RFLDO1/2/3/4/5
13	VDD_PMU_1P3	P	1.3	1.3 V voltage input, supplying power to CLDO
23	VDD_PMU_CLDO	P	1.0	CLDO output, connected to an external 1 µF filter capacitor
1	VDDIO1	P	3.3/1.8	I/O power supply input
21	VDDIO2	P	3.3/1.8	I/O power supply input
7	VDD_WL_RF_LNA_1P2	P	1.15	RF LNA power supply input
10	VDD_WL_RF_TRX_1P2	P	1.15	RF TRX power supply input
12	VDD_PMU_RFLDO1	P	1.15	RF LDO1 power supply output, connected to an external 1 µF filter capacitor
11	VDD_WL_RF_VCO_1P2	P	1.15	RF VCO PLL power supply input, connected to an external 1 µF filter capacitor
14	VDD_PMU_VBAT2	P	2.3–3.6	VABT power supply input
9	VDD_WL_RF_PA2G_3P3	P	2.3–3.6	VABT power supply input

NOTE

When VDD_PMU_VBAT1 and VDD_PMU_VBAT2 are powered by 2.3 V supplies, the RF TX power decreases by about 3 dB when the error vector magnitude (EVM) remains unchanged.

1.2.7 RF Pin

Table 1-9 describes the RF pin.

Table 1-9 RF pin

Pin	Name	Type	Level (V)	Description
8	RF_WL_RFO_2G	ANA	-	WLAN 2.4 GHz RF input/ output

1.2.8 GND Pin

Table 1-10 describes the GND pin.

Table 1-10 GND pin

Pin	Name	Voltage (V)	Description
Epad	GND	-	The exposed pad (EPAD) is the only GND pin.

1.2.9 SFC Interface Pins

In Hi3861/Hi3861L, the SFC is an internal interface. Hi3881 does not support the SFC interface.

1.2.10 GPIO Pins

Table 1-11 describes the general-purpose input/output (GPIO) pins.

NOTE

- Multiplexed signal 0 is the default function after power-on reset (POR) of the chip.
- Multiplexed signal 0 of a single-die package is the corresponding SFC signal.

Table 1-11 GPIO pins

Pin	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
2	GPIO_00	I_{SPU}/O	1	3.3/1.8	• Multiplexed signal 0: GPIO_00 • Multiplexed signal 1: UART1_TXD • Multiplexed signal 2: SPI1_CLK • Multiplexed signal 3: PWM3_OUT • Multiplexed signal 4: I2C1_SDA • Multiplexed signal 5: RTC_OSC_32K • Multiplexed signal 6: RTC32K_XOUT • Multiplexed signal 7: reserved
3	GPIO_01	I_{SPU}/O	1	3.3/1.8	• Multiplexed signal 0: GPIO_01 • Multiplexed signal 1: UART1_RXD • Multiplexed signal 2: SPI1_RXD • Multiplexed signal 3: PWM4_OUT • Multiplexed signal 4: I2C1_SCL • Multiplexed signal 5: reserved • Multiplexed signal 6: RTC32K_XIN • Multiplexed signal 7: reserved
4	GPIO_02	I_{SPU}/O	1	3.3/1.8	• Multiplexed signal 0: GPIO_02 • Multiplexed signal 1: UART1_RTS, UART1 flow control pin, transmit (TX) request signal, output • Multiplexed signal 2: SPI1_TXD • Multiplexed signal 3: PWM2_OUT • Multiplexed signal 4: reserved • Multiplexed signal 5: SSI_CLK, internal RF debugging interface • Multiplexed signal 6: reserved • Multiplexed signal 7: reserved

Pin	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
5	GPIO_03	I_{SPU}/O	1	3.3/1.8	• Multiplexed signal 0: UART0_LOG_TXD, data transmission, debugging and download serial port • Multiplexed signal 1: UART1_CTS, UART1 flow control pin, TX clear signal, input • Multiplexed signal 2: SPI1_CS1 • Multiplexed signal 3: PWM5_OUT • Multiplexed signal 4: I2C1_SDA • Multiplexed signal 5: SSI_DATA, internal RF debugging interface • Multiplexed signal 6: GPIO_03 • Multiplexed signal 7: reserved
6	GPIO_04	I_{SPU}/O	1	3.3/1.8	• Multiplexed signal 0: UART0_LOG_RXD, data receiving, debugging and download serial port • Multiplexed signal 1: reserved • Multiplexed signal 2: reserved • Multiplexed signal 3: PWM1_OUT • Multiplexed signal 4: I2C1_SCL • Multiplexed signal 5: reserved • Multiplexed signal 6: GPIO_04 • Multiplexed signal 7: ADC1
17	GPIO_05	I_{SPU}/O	1	3.3/1.8	• Multiplexed signal 0: UART1_RXD, data receiving, communication serial port • Multiplexed signal 1: GPIO_05 • Multiplexed signal 2: I2S0_MCK • Multiplexed signal 3: PWM2_OUT • Multiplexed signal 4: reserved • Multiplexed signal 5: BT_STATUS, that is, a signal of the PTA interface which co-exists with the BT interface • Multiplexed signal 6: SPI0_CS1 • Multiplexed signal 7: ADC2

Pin	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
18	GPIO_06	I_{SPU}/O	1	3.3/1.8	• Multiplexed signal 0: UART1_TXD, data transmission, communication serial port • Multiplexed signal 1: GPIO_06 • Multiplexed signal 2: I2S0_TX • Multiplexed signal 3: PWM3_OUT • Multiplexed signal 4: reserved • Multiplexed signal 5: COEX_SWITCH, that is, a signal of the PTA interface which co-exists with the BT interface • Multiplexed signal 6: SPI0_CLK • Multiplexed signal 7: reserved
19	GPIO_07	I_{SPU}/O	1	3.3/1.8	• Multiplexed signal 0: UART1_CTS, TX clear signal, communication serial port • Multiplexed signal 1: GPIO_07 • Multiplexed signal 2: I2S0_CLK • Multiplexed signal 3: PWM0_OUT • Multiplexed signal 4: reserved • Multiplexed signal 5: BT_ACTIVE, that is, a signal of the PTA interface which co-exists with the BT interface • Multiplexed signal 6: SPI0_RXD • Multiplexed signal 7: ADC3
20	GPIO_08	I_{SPU}/O	1	3.3/1.8	• Multiplexed signal 0: UART1_RTS, TX request signal, communication serial port • Multiplexed signal 1: GPIO_08 • Multiplexed signal 2: I2S0_WS • Multiplexed signal 3: PWM1_OUT • Multiplexed signal 4: reserved • Multiplexed signal 5: WLAN_ACTIVE, that is, a signal of the PTA interface which co-exists with the BT interface • Multiplexed signal 6: SPI0_TXD • Multiplexed signal 7: reserved

Pin	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
27	GPIO_09	I_{SPU}/O	1	3.3/1.8	• Multiplexed signal 0: GPIO_09 • Multiplexed signal 1: UART2_RTS, TX request signal, communication serial port, output signal • Multiplexed signal 2: SPI0_TXD • Multiplexed signal 3: PWM0_OUT • Multiplexed signal 4: I2C0_SCL • Multiplexed signal 5: I2S0_MCK • Multiplexed signal 6: SDIO_D2 • Multiplexed signal 7: ADC4 Note: In the single-die package, I/O is multiplexed as the SFC interface by default. For details, see **1.2.9 SFC Interface Pins**.
28	GPIO_10	I_{SPU}/O	1	3.3/1.8	• Multiplexed signal 0: GPIO_10 • Multiplexed signal 1: UART2_CTS, TX clear signal, communication serial port, input signal • Multiplexed signal 2: SPI0_CLK • Multiplexed signal 3: PWM1_OUT • Multiplexed signal 4: I2C0_SDA • Multiplexed signal 5: I2S0_TX • Multiplexed signal 6: SDIO_D3 • Multiplexed signal 7: reserved Note: In the single-die package, I/O is multiplexed as the SFC interface by default. For details, see **1.2.9 SFC Interface Pins**.

Pin	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
29	GPIO_11	I_{SPU}/O	1	3.3/1.8	• Multiplexed signal 0: GPIO_11 • Multiplexed signal 1: UART2_TXD • Multiplexed signal 2: SPI0_RXD • Multiplexed signal 3: PWM2_OUT • Multiplexed signal 4: reserved • Multiplexed signal 5: I2S0_RX • Multiplexed signal 6: SDIO_CMD • Multiplexed signal 7: ADC5 Note: In the single-die package, I/O is multiplexed as the SFC interface by default. For details, see **1.2.9 SFC Interface Pins**.
30	GPIO_12	I_{SPU}/O	1	3.3/1.8	• Multiplexed signal 0: GPIO_12 • Multiplexed signal 1: UART2_RXD • Multiplexed signal 2: SPI0_CS1 • Multiplexed signal 3: PWM3_OUT • Multiplexed signal 4: reserved • Multiplexed signal 5: I2S0_CLK • Multiplexed signal 6: SDIO_CLK • Multiplexed signal 7: ADC0 Note: In the single-die package, I/O is multiplexed as the SFC interface by default. For details, see **1.2.9 SFC Interface Pins**.
31	GPIO_13	I_{SPU}/O	1	3.3/1.8	• Multiplexed signal 0: GPIO_13 • Multiplexed signal 1: UART2_RTS • Multiplexed signal 2: UART0_LOG_TXD • Multiplexed signal 3: PWM4_OUT • Multiplexed signal 4: I2C0_SDA • Multiplexed signal 5: I2S0_WS • Multiplexed signal 6: SDIO_D0 • Multiplexed signal 7: ADC6 • Multiplexed signal 8: SSI_DATA Note: In the single-die package, I/O is multiplexed as the SFC interface by default. For details, see **1.2.9 SFC Interface Pins**.

Pin	Pin Name	Type	Drive Current (mA)	Voltage (V)	Description
32	GPIO_14	I_{SPU}/O	1	3.3/1.8	• Multiplexed signal 0: GPIO_14 • Multiplexed signal 1: UART2_CTS • Multiplexed signal 2: UART0_LOG_RXD • Multiplexed signal 3: PWM5_OUT • Multiplexed signal 4: I2C0_SCL • Multiplexed signal 5: reserved • Multiplexed signal 6: SDIO_D1 • Multiplexed signal 7: reserved • Multiplexed signal 8: SSI_CLK Note: In the single-die package, I/O is multiplexed as the SFC interface by default. For details, see **1.2.9 SFC Interface Pins**.

1.2.11 CLK Pins

Table 1-12 describes the CLK pins.

Table 1-12 CLK pins

Pin	Pin Name	Type	Voltage (V)	Description
15	XIN	I	1.8	Crystal clock input, supporting 24 MHz and 40 MHz
16	XOUT	O	1.8	Crystal clock output, supporting 24 MHz and 40 MHz

1.3 Pin Multiplexing in Software

For details, see the description of pin multiplexing in software in the *Hi3861/ Hi3861L/Hi3881 V100 Wi-Fi Chip Data Sheet*.

For details about the pin drive strength configuration, see the register description in the *Hi3861/ Hi3861L/Hi3881 V100 Wi-Fi Chip Data Sheet*.

1.4 Pin Multiplexing In Hardware

NOTE

- During power-on, the hardware automatically straps **HW_IDx** and **JTAG_ENABLE**. No software configuration is required.
- **HW_IDx**: hardware version number. This pin is used to identify the hardware product form. The pin level is automatically strapped during chip power-on or reset. **x** can be 0–7.

1.4.1 Pin Multiplexing In Hardware

Table 1-13 describes the pin multiplexing configuration of Hi3861/ Hi3861L/ Hi3881 V100 in hardware. **HW_ID** can be ignored if it is not used.

Table 1-13 Pin multiplexing and configuration in hardware

Pin	Pad Signal	Multiplexed Signal 1	Multiplexed Signal 2
2	GPIO_00	JTAG_TDO: JTAG data output.	HW_ID0: hardware version number. The pin level is automatically strapped during chip power-on or reset. The user-defined hardware version is reserved.
3	GPIO_01	JTAG_TCK: JTAG clock.	HW_ID1: hardware version number. The pin level is automatically strapped during chip power-on or reset. The user-defined hardware version is reserved.
4	GPIO_02	JTAG_TRSTN: JTAG reset pin.	REFCLK_FREQ_STATUS: frequency status select of the crystal clock. • Low level (default): 40 MHz • High level: 24 MHz The pin level is automatically strapped during chip power-on or reset.
5	GPIO_03	JTAG_TDI: JTAG input signal.	-

Pin	Pad Signal	Multiplexed Signal 1	Multiplexed Signal 2
6	GPIO_04	JTAG_TMS: JTAG TMS signal.	HW_ID3: hardware version number. The pin level is automatically strapped during chip power-on or reset. The user-defined hardware version is reserved.
17	GPIO_05	HW_ID4: hardware version number 4. The pin level is automatically strapped during chip power-on or reset.	HW_ID4: hardware version number. The pin level is automatically strapped during chip power-on or reset. The user-defined hardware version is reserved.
18	GPIO_06	JTAG_MODE: hardware JTAG mode select. • Pull-down: normal mode (default) • Pull-up: DFT test mode	-
19	GPIO_07	HW_ID5: hardware version number 5. The pin level is automatically strapped during chip power-on or reset.	HW_ID5: hardware version number. The pin level is automatically strapped during chip power-on or reset. The user-defined hardware version is reserved.
20	GPIO_08	JTAG_ENABLE: JTAG enable input. Pull-down: determined by the configuration of the I/O multiplexing register Pull-up: JTAG function The pin level is automatically strapped during chip power-on or reset.	-
29	GPIO_11	HW_ID6: hardware version number 6. The pin level is automatically strapped during chip power-on or reset.	HW_ID6: hardware version number. The pin level is automatically strapped during chip power-on or reset. The user-defined hardware version is reserved.

Pin	Pad Signal	Multiplexed Signal 1	Multiplexed Signal 2
30	GPIO_12	HW_ID7: hardware version number 7. The pin level is automatically strapped during chip power-on or reset.	- HW_ID7: hardware version number. The pin level is automatically strapped during chip power-on or reset. The user-defined hardware version is reserved.
32	GPIO_14	HW_ID2: hardware version number 2. The pin level is automatically strapped during chip power-on or reset.	HW_ID2: hardware version number. The pin level is automatically strapped during chip power-on or reset. The user-defined hardware version is reserved.

1.4.2 Hardware Configuration Words for Power-on

After the chip system is started normally, the hardware configuration words must be correct. There are two types of hardware configuration words:

- Words that are closely related to the chip hardware startup (such as REFCLK_FREQ_STATUS/ JTAG_MODE/ JTAG_ENABLE). For details, see **Table 1-14**.
- Words that are closely related to the reserved hardware configuration word (such as HW_ID) of the solution and the product solution. The pin level is automatically strapped during chip power-on or reset.

Table 1-14 Hardware configuration words of the pins

Signal	Low Level	High Level
REFCLK_FREQ_STATUS (The signal is pulled down by default. If it is pulled up externally, the level is the same as the VDDIO level.)	40 MHz (default)	24 MHz
JTAG_ENABLE (The signal is pulled down by default. If it is pulled up externally, the level is the same as the VDDIO level.)	Common I/O (default)	JTAG enable
JTAG_MODE (The signal is pulled down by default. If it is pulled up externally, the level is the same as the VDDIO level.)	Normal mode (default)	Design for test (DFT) mode
VDD_PMU_LX (The signal is pulled down by default. If it is pulled up externally, the level is the same as the VBAT level.)	Buck (default)	LDO

2 Electrical Characteristics

2.1 Current Distribution

Table 2-1 describes the power consumption distribution of Hi3861/Hi3861L/ Hi3881 V100.

Table 2-1 Current parameters

Symbol	Description	Min.	Typ.	Max.	Unit
VDD_PMU_VBAT1 VDD_PMU_VBAT2	Buck and PA input power supplies	-	300	TBD	mA
VDDIO	I/O input power supply	TBD	30	TBD	mA
PMU_1P3	CLDO, RFLDO1/2/3/4 input power supply	-	200	-	mA

2.2 Rated Operating Voltages

⚠ WARNING

If the rated operating voltages in **Table 2-2** are exceeded, the chip may not work stably or even be damaged.

Table 2-2 Rated operating voltages

Symbol	Parameter	Min.	Max.	Unit
VDD_PMU_VBAT	Battery power supply	2.3	3.6	V
VDDIO	I/O input power supply	1.71	3.6	V

2.3 Recommended Operating Conditions

Table 2-3 describes the recommended operating conditions of Hi3861/Hi3861L/ Hi3881 V100.

Table 2-3 Recommended operating conditions

Symbol	Description	Min.	Typ.	Max.	Unit
VDD_PMU_VBAT1, VDD_PMU_VBAT2	Battery power supplies	2.3	3.3	3.6	V
VDDIO1, VDDIO2	I/O input power supplies	1.71	1.8/3.3	3.6	V
PMU_1P3, BUCK_1P3	CLDO, RFLDO1/2/3/4 input power supplies	1.1	1.3	1.5	V

2.4 DC/AC Electrical Specifications

Table 2-4 DC electrical specifications (VDDIO1/VDDIO2 = 1.8 V GPIO)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Description
VDDIO1/ VDDIO2	Interface voltage	1.71	1.8	1.89	V	-
V_{IH}	High-level input voltage	1.2	-	3.63	V	Incompatible with 5 V input
V_{IL}	Low-level input voltage	–0.3	-	0.6	V	-
I_L	Input leakage current	-	-	±10	μA	-

Symbol	Parameter	Min.	Typ.	Max.	Unit	Description
I_{OZ}	Tristate output leakage current	-	-	±10	μA	-
V_{OH}	High-level output voltage	(VDDIO1/2)-0.45	-	-	V	-
V_{OL}	Low-level output voltage	-	-	0.45	V	-
R_{PU}	Internal pull-up resistor	19	25	31	kΩ	-
R_{PD}	Internal pull-down resistor	19	25	31	kΩ	-
I_{OH}	High-level output current	2.04	-	-	mA	IO4_level 1
		4.08	-	-	mA	IO4_level 2
		6.13	-	-	mA	IO4_level 3
		8.16	-	-	mA	IO4_level 4
I_{OL}	Low-level output current	1.9	-	-	mA	IO4_level 1
		3.79	-	-	mA	IO4_level 2
		5.64	-	-	mA	IO4_level 3
		7.54	-	-	mA	IO4_level 4
I_{OH}	High-level output current	1.94	-	-	mA	IO8_level 1
		3.89	-	-	mA	IO8_level 2
		5.84	-	-	mA	IO8_level 3
		7.79	-	-	mA	IO8_level 4

Symbol	Parameter	Min.	Typ.	Max.	Unit	Description
		9.73	-	-	mA	IO8_level 5
		11.67	-	-	mA	IO8_level 6
		13.62	-	-	mA	IO8_level 7
		15.57	-	-	mA	IO8_level 8
I_{OL}	Low-level output current	2.01	-	-	mA	IO8_level 1
		4.02	-	-	mA	IO8_level 2
		6.02	-	-	mA	IO8_level 3
		8.03	-	-	mA	IO8_level 4
		10.04	-	-	mA	IO8_level 5
		12.04	-	-	mA	IO8_level 6
		14.05	-	-	mA	IO8_level 7
		16.06			mA	IO8_level 8

Table 2-5 DC electrical specifications (VDDIO1/VDDIO2 = 3.3 V GPIO)

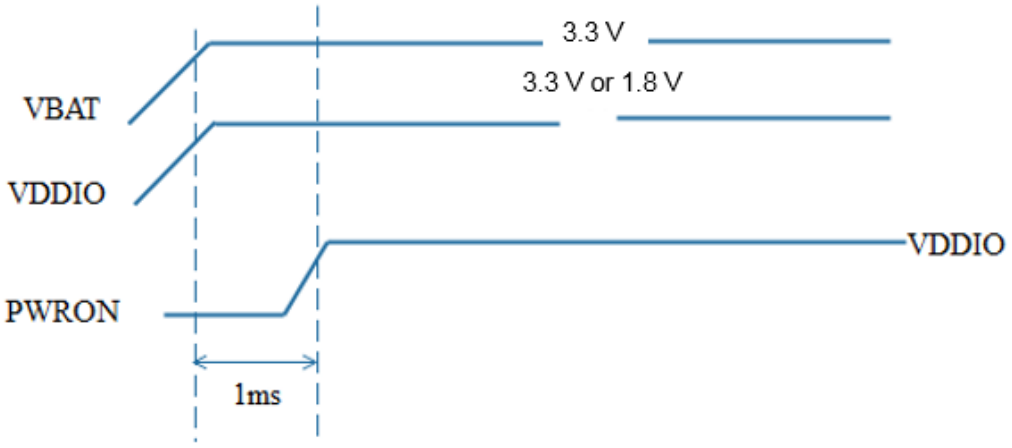
Symbol	Parameter	Min.	Typ.	Max.	Unit	Description
VDDIO1/ VDDIO2	Interface voltage	3.125	3.3	3.6	V	-
V_{IH}	High-level input voltage	2.4	-	3.63	V	Incompatible with 5 V input
V_{IL}	Low-level input voltage	–0.3	-	0.8	V	-

Symbol	Parameter	Min.	Typ.	Max.	Unit	Description
I_L	Input leakage current	-	-	±10	μA	-
I_{OZ}	Tristate output leakage current	-	-	±10	μA	-
V_{OH}	High-level output voltage	2.4	-	-	V	-
V_{OL}	Low-level output voltage	-	-	0.4	V	-
R_{PU}	Internal pull-up resistor	19	25	31	kΩ	-
R_{PD}	Internal pull-down resistor	19	25	31	kΩ	-
I_{OH}	High-level output current	5.61	-	-	mA	IO4_level 1
		11.21	-	-	mA	IO4_level 2
		16.83	-	-	mA	IO4_level 3
		22.43	-	-	mA	IO4_level 4
I_{OL}	Low-level output current	3.58	-	-	mA	IO4_level 1
		7.16	-	-	mA	IO4_level 2
		10.7	-	-	mA	IO4_level 3
		14.29	-	-	mA	IO4_level 4
I_{OH}	High-level output current	5.27	-	-	mA	IO8_level 1
		10.55	-	-	mA	IO8_level 2
		15.83	-	-	mA	IO8_level 3

Symbol	Parameter	Min.	Typ.	Max.	Unit	Description
		21.1	-	-	mA	IO8_level 4
		26.37	-	-	mA	IO8_level 5
		31.64	-	-	mA	IO8_level 6
		36.92	-	-	mA	IO8_level 7
		42.2	-	-	mA	IO8_level 8
I_{OL}	Low-level output current	3.76	-	-	mA	IO8_level 1
		7.51	-	-	mA	IO8_level 2
		11.27	-	-	mA	IO8_level 3
		15.03	-	-	mA	IO8_level 4
		18.79	-	-	mA	IO8_level 5
		22.54	-	-	mA	IO8_level 6
		26.3	-	-	mA	IO8_level 7
		30.06			mA	IO8_level 8

2.5 Power-Up/Down Sequences

Figure 2-1 Power-up sequence



The power-up sequence is as follows:

Step 1 The external battery power supply VBAT [1] and I/O power supply VDDIO [2] are disconnected, PWRON is invalid, and the chip is powered off.

Step 2 The external power supplies VBAT and VDDIO power up (with no requirement on the power-up sequence). In this case, the external control signal PMU_PWRON is at low level.

Step 3 The external control signal PMU_PWRON is set to high level. PWRON needs to be pulled up (to VDDIO) 1 ms after VBAT and VDDIO are powered up.

Step 4 In Hi3861L V100/Hi3861 V100/Hi3881 V100, after the power management unit (PMU) detects that the PMU_PWRON signal is at high level for 1 ms, the chip starts the reset deassertion process and powers on the power supplies in sequence. The reset deassertion time is 1.1 ms. The hardware configuration word is latched within 100 μs after the reset is deasserted. Then the chip works properly.

----End

NOTE

- [1]: VBAT pins are VDD_PMU_ VBAT1 and VDD_PMU_VBAT2.
- [2]: VDDIO pins are VDDIO1 and VDDIO2.
- This chip has no requirement on the power-down sequence.

3 Recommendations on Schematic Diagram Design

3.1 Minimum System

The minimum system refers to the minimum peripheral circuit configurations required for proper chip operation. The circuits of the minimum system include: clock circuit, reset circuit, watchdog, JTAG debugging circuit, and flash circuit.

3.1.1 Clock Reference Design

3.1.1.1 Reference Clock

3.1.1.1.1 Crystal Input Mode

Figure 3-1 shows the circuit structure when an external crystal is used.

Figure 3-1 Reference circuit diagram of the crystal input reference clock

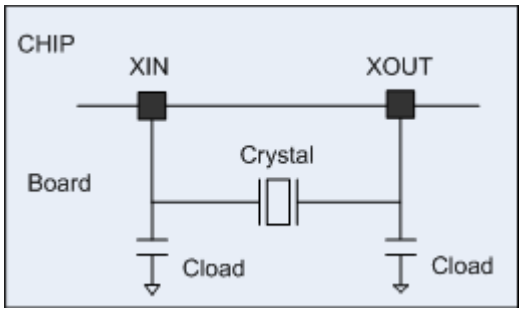


Table 3-1 describes the electrical specifications of the external crystal.

Table 3-1 Electrical specifications of the crystal

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Nominal frequency	f	-	24/40		MHz	-
Frequency tolerance	L_m	-10	-	+10	ppm	-
Equivalent resistance	Rr		40	45	Ohm	The vibration is affected.
Load capacitance	CL	-	11	15	pF	The vibration is affected.
Drive power consumption	Wl	-	100	300	μW	-
Operating temperature	T	–40		85	℃	

In the preceding information:

- CL: load capacitance in the crystal
- Rr: equivalent resistance in the crystal
- The vibration requirements can be met when (Rr x CL x CL) is less than 9000.
- Q = Wl/Rr, where **Q** indicates the quality factor. If the Q value is too small, the frequency stability will be affected.
- Load capacitance of the crystal oscillator = [(Cd x Cg)/(Cd + Cg)] + Cic + △C, where **Cd** and **Cg** respectively connect to the two pins of the crystal oscillator and to ground. The empirical value of **Cic** (capacitor in the IC) + △C (capacitor on the PCB) is 3 to 5 pf.

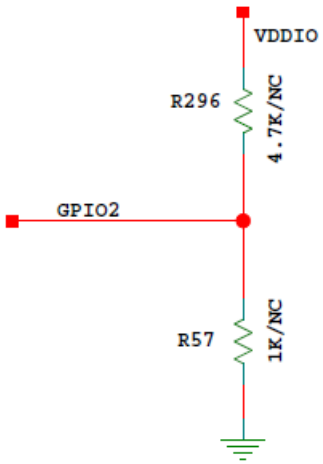
3.1.1.1.2 Reference Clock Frequency Select

Hi3861 V100/Hi3861L V100/Hi3881 V100 supports the 24 MHz and 40 MHz reference clock frequencies. The reference clock frequency is determined by the hardware configuration word of GPIO02. During power-on, the internal frequency divider is selected by reading the high and low levels of GPIO02. Table 3-2 describes the truth values of the external clock.

Table 3-2 Truth table of external clock selection

Clock Frequency	REFCLK_FREQ_STATUS	Remarks
40 MHz	0	Pulled down internally by default
24 MHz	1	Pulled up to VDDIO through a 4.7-kilohm resistor

Figure 3-2 Reference circuit diagram of the frequency selection pin



3.1.1.2 RTC

Hi3861L V100 needs to provide an external 32.768 kHz real-time clock (RTC) for low-power processing. However, Hi3861 V100 and Hi3881 V100 do not support the external RTC low-power application.

Table 3-3 and Table 3-4 describe the electrical specifications of the 32.768 kHz RTC.

Table 3-3 Electrical specifications of the active RTC

Parameter	RTC	Unit
Clock frequency	32.768	kHz
Clock accuracy	≤±200	ppm
Duty cycle	45–55	%
Input signal amplitude (peak-to-peak)	900–1800	mV

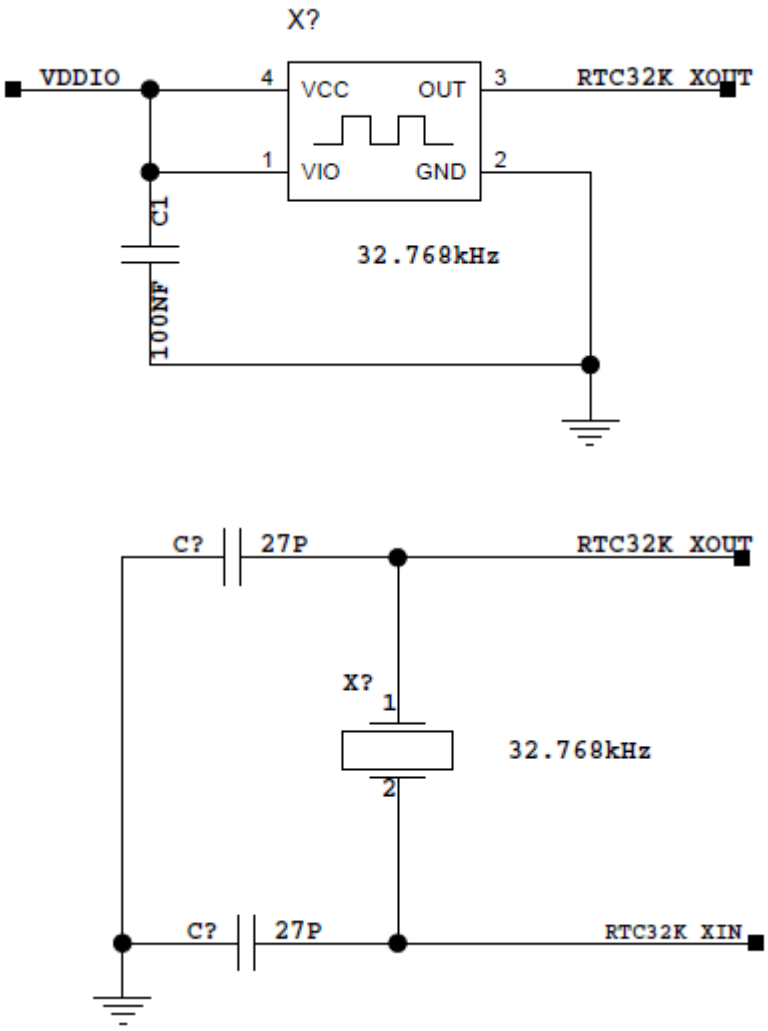
Parameter	RTC	Unit
Clock jitter	±10000	ppm

Table 3-4 Electrical specifications of the passive RTC

Parameter	RTC	Unit
Clock frequency	32.768	kHz
Load capacitance	12.5	pF
Frequency tolerance	≤±50	ppm
Series resistance	≤ 70	kΩ
Drive level	≥ 0.5	μW

Figure 3-3 shows the RTC reference circuit. The upper part is the reference design of the crystal oscillator. The level of the VCC supply is the same as that of VDDIO. The lower part is the reference design of the crystal.

Figure 3-3 RTC reference circuit



3.1.2 Reset and Watchdog Circuits

Hi3861 V100/Hi3861L V100/Hi3881 V100 integrates the internal POR and watchdog circuits. The board is reset by powering off the PMU_PWRON.

3.1.3 JTAG Debugging Interface

The Hi3861 V100/Hi3861L V100/Hi3881 V100 JTAG interface complies with the IEEE1149.1 standard. A PC can be connected to the Realview ICE emulator over this interface for debugging the CPU. **Table 3-5** describes the signals of the JTAG debugging interface.

Table 3-5 Signals of the JTAG debugging interface

Signal	Description
TCK	JTAG clock input. It is connected to a 1-kilohm pull-down resistor on the board and then to GND.
TDI	JTAG data input. It is connected to a 4.7-kilohm pull-up resistor on the board and then to VDDIO.
TMS	JTAG mode select input. It is connected to a 4.7-kilohm pull-up resistor on the board and then to VDDIO.
TRSTN	JTAG reset input. It is connected to a 1-kilohm pull-down resistor on the board and then to GND. If a PC is connected to an emulator such as the Realview ICE over the JTAG interface, it is recommended that this pin be connected to a 4.7-kilohm pull-up resistor on the board and then to VDDIO.
TDO	JTAG data output, direct connection

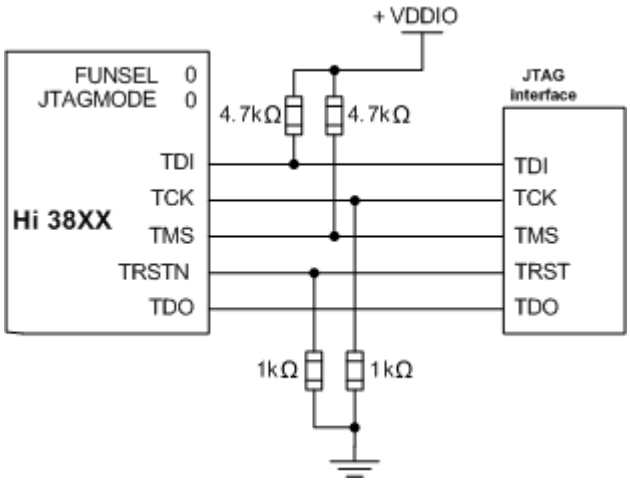
For Hi3861 V100/Hi3861L V100/Hi3881 V100, JTAG_ENABLE can be used to enable the JTAG function by pulling the level high, and the JTAG_MODE pin can be used to select the normal or test mode. For details, see **Table 3-6**.

Table 3-6 Description of the JTAG_ENABLE mode

JTAG_MODE	Description
0	Normal mode, in which the software can be debugged over the JTAG interface
1	Test mode, in which the DFT or board interconnection test can be performed

Figure 3-4 shows the JTAG connection mode and standard connector pins.

Figure 3-4 JTAG connection mode and standard connector pins



3.1.4 System Configuration Circuit for Hardware Initialization

Hi3861 V100/Hi3861L V100/Hi3881 V100 integrates a Huawei-developed CPU, supporting the following features:

- Booting from the SPI flash
- 24 MHz or 40 MHz clock input
- JTAG enable and mode selection
- Buck 1.3 V and LDO 1.3 V output modes

For Hi3861 V100/Hi3861L V100/Hi3881 V100, the hardware needs to be configured as required during hardware initialization, which is implemented by connecting pull-up or pull-down resistors on the board.

Table 3-7 describes the hardware configuration word signals.

Table 3-7 Hardware configuration word signals

Description	Low Level	High Level	Remarks
REFCLK_FREQ_STATUS	40 MHz	24 MHz	The signal is pulled down by default. If it is pulled up externally, the level is the same as the VDDIO level.
JTAG_ENABLE	Common I/O	JTAG enable	The signal is pulled down by default. If it is pulled up externally, the level is the same as the VDDIO level.
JTAG_MODE	Normal mode	DFT test mode	The signal is pulled down by default. If it is pulled up externally, the level is the same as the VDDIO level.
VDD_PMU_LX	Buck output	Internal LDO output	The signal is pulled down by default. If it is pulled up externally, the level is the same as the VDDIO level.

3.2 Power Supply Reference Design

NOTE

For details about the system power supply design, see the schematic diagram of the Hi3861 V100/Hi3861L V100/Hi3881 V100 demo board.

3.2.1 Power Supply Specifications

Hi3861 V100/Hi3861L V100/Hi3881 V100 requires the following external power supplies:

- Battery power supply VBAT
- I/O power supply VDDIO

The chip integrates the buck and multiple low-dropout regulators (LDOs).

- Buck: As an intermediate power plane, it supplies power to multiple LDOs.
- LDO: There are the digital power supply LDO and low-noise LDO.
- A buck in the PMU provides 1.3 V power supply.
  Table 3-8 describes the recommended operating conditions.

Table 3-8 Recommended operating conditions

Symbol	Parameter Description	Min. (V)	Typ. (V)	Max. (V)
VDD_PMU_VBAT1, VDD_PMU_VBAT2	External power supplies	2.3	3.3	3.6
VDDIO1, VDDIO2	External I/O power supplies	1.71	1.8/3.3	3.6
VDD_BUCK_1P3, VDD_PMU_1P3	1.3 V power supplies provided externally or internal power supplies provided by the buck	1.1	1.3	1.5
VDD_PMU_CLDO	Internal LDO power supply, connected to an external 1 µF filter capacitor	-	1.0	-
VDD_PMU_RFLDO1	Internal LDO power supply, for VDD_WL_RF_LNA_1P2 and VDD_WL_RF_TRX_1P2	-	1.15	-
VDD_WL_RF_VCO_1P2	Internal RF_VCO power supply, connected to an external 1 µF filter capacitor	-	1.15	-

1P3 power can be generated in the following modes:

- Generated by the internal DC-DC converter
- Generated by the internal LDO

Table 3-9 Peripheral requirements for the 1P3 power generated by the internal DC-DC converter

Component	Size
Inductor	2.2 µH
Capacitor	4.7 µF, withstand voltage ≥ 4 V

Table 3-10 Peripheral requirements for the 1P3 power generated by the internal LDO

Component	Size
Capacitor	2.2 μF, withstanding voltage ≥ 4 V
Resistor	0 ohms, pulled up to VBAT

Whether BUCK_LX is pulled up or pulled down serves as the condition for determining whether to use the DC-DC mode or the LDO mode:

- Pull-up: LDO mode
- Pull-down: buck mode

See **Table 3-11**.

Table 3-11 Checking whether the DC-DC or LDO mode is used

Clock Frequency	BUCK_LX	Remarks
DC-DC mode	0	Pulled down internally by default
LDO mode	1	Connected to a 0-ohm pull-up resistor and then to VBAT

3.2.2 VBAT Power Supplies

Hi3861 V100/Hi3861L V100/Hi3881 V100 has two VBAT power input pins:

- VDD_PMU_VBAT1: provides buck input voltage.
- VDD_PMU_VBAT2: provides PALDO input voltage.

The VBAT supports the 2.3–3.6 V input. The VBAT power supplies can be generated and provided by an external PMU chip or external buck circuit.

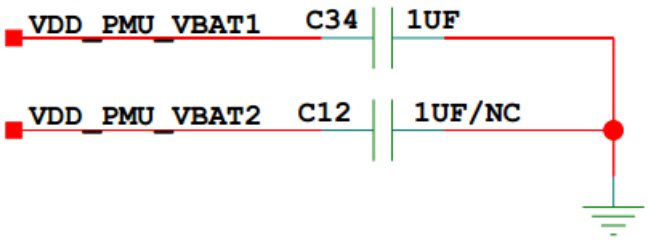
The output power must meet the following requirements: When the EVM of 2.3 V is the same as that of 3.3 V, the output power changes. The change amplitude varies according to the target power and rate. Take 11n_MCS7_HT20 as an example. At normal temperature, when the target power is 15 dBm at 3.3 V, the output power decreases by about 1–1.5 dB when the voltage decreases to about 2.3 V.

3.2.2.1 VBAT Reference Circuit

VBAT supplies power to the chip. Each of VDD_PMU_VBAT1 and VDD_PMU_VBAT2 connects to a capacitor for energy storage and filtering. **Figure 3-5** shows the reference circuit diagram.

Name	Design Recommendation
VDD_PMU_VBAT1	Connected to an external 1 µF capacitor, withstand voltage ≥ 6.3 V
VDD_PMU_VBAT2	Connected to an external 1 µF capacitor (reserved), withstand voltage ≥ 6.3 V

Figure 3-5 Hi3861 V100/Hi3861L V100/Hi3881 V100 VBAT input circuit



3.2.2.2 VBAT Input Power Supply

Hi3861 V100/Hi3861L V100/Hi3881 V100 has the following VBAT power supply requirements:

- The power supply ripple must be less than or equal to 50 mV.
- The power supply can be generated by an external buck circuit. The buck power supply chip with a high switching frequency (better greater than 1 MHz) is recommended.
- Appropriate inductors and output filter capacitors can suppress ripple and harmonic interference more effectively.

3.2.3 VDDIO Power Supplies

Hi3861 V100/Hi3861L V100/Hi3881 V100 has two VDDIO power input pins:

- VDDIO1
- VDDIO2

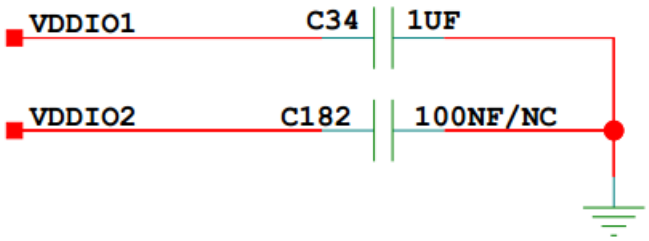
The 1.8 V/VBAT voltage and the power ripple less than or equal to 50 mV are supported. **Table 3-12** describes the design recommendations, and **Figure 3-6** shows the reference circuit diagram. It is recommended that the 1.8 V/VBAT voltage be generated by an external buck circuit or LDO circuit.

Table 3-12 Design recommendations on the VDDIO power supplies

Name	Design Recommendation
VDDIO1	Connected to an external 1 µF capacitor, withstand voltage ≥ 6.3 V

Name	Design Recommendation
VDDIO2	Connected to an external 100 nF capacitor (reserved), withstand voltage ≥ 6.3 V

Figure 3-6 VDDIO input circuit



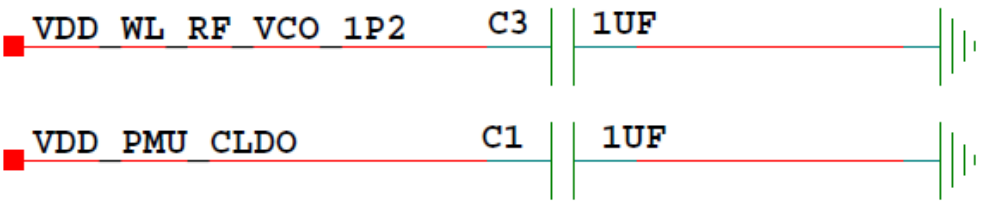
3.2.4 Filter Circuits of the Internal Power Supplies

The internal power supplies VDD_PMU_CLDO and VDD_WL_RF_VCO_1P2 must connect to external filter capacitors. **Table 3-13** shows the design recommendations, and **Figure 3-7** shows the reference circuit diagram.

Table 3-13 Design recommendations on the filter circuits of the internal power supplies

Name	Design Recommendation
VDD_PMU_CLDO	Built-in LDO output that supplies power to some digital baseband (DBB) components, and connected to an external 1 µF filter capacitor
VDD_WL_RF_VCO_1P2	1.15 V RF VCO, internal LDO power supply, and connected to an external 1 µF filter capacitor

Figure 3-7 Filter circuits of the internal power supplies



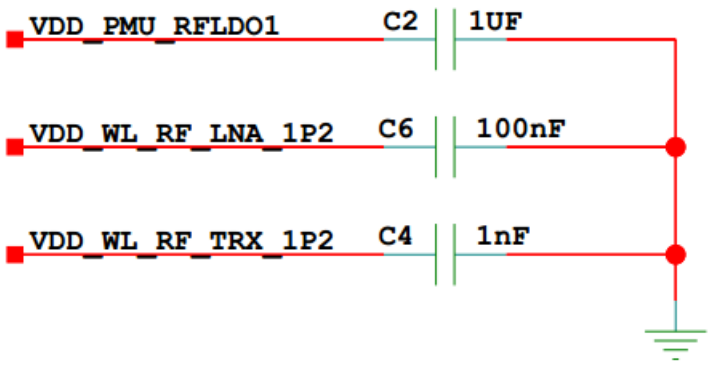
3.2.5 RFLDO1

The RFLDO1 power is output from the Hi3861 V100/Hi3861L V100/Hi3881 V100 pin VDD_PMU_RFLDO1, and the output filter capacitance is 1 µF. RFLDO1 supplies power to two pins: VDD_WL_RF_LNA_1P2 and VDD_WL_RF_TRX_1P2. **Table 3-14** shows the recommended design, and **Figure 3-8** shows the reference circuit.

Table 3-14 Design recommendations on the RFLDO1 power supply

Name	Description
VDD_PMU_RFLDO1	RFLDO1 output, connected to an external 1 µF filter capacitor
VDD_WL_RF_LNA_1P2	RFLDO1 input. On the 2-layer PCB, an external 100 nF filter capacitor is connected. On the 2-layer PCB, a capacitor position can be reserved. The radiation spurious emission can be reduced by debugging the capacitor.
VDD_WL_RF_TRX_1P2	RFLDO1 input. On the 2-layer PCB, an external 1 nF filter capacitor is connected. On the 2-layer PCB, a capacitor position can be reserved. The radiation spurious emission can be reduced by debugging the capacitor.

Figure 3-8 RFLDO1 reference circuit



3.2.6 Buck/LDO Power Supplies

Hi3861 V100/Hi3861L V100/Hi3881 V100 has two 1P3 power input pins:

- VDD_BUCK_1P3
- VDD_PMU_1P3

The 1P3 power supply may be provided by an internal buck or LDO.

Table 3-15 Design recommendations on the buck power supplies

Name	Description
PMU_BUCK_LX	Buck LX output, connected to an external 2.2 µH inductor
VDD_BUCK_1P3	Voltage input, supplying power to CLDO, connected to an external 4.7 µF capacitor
VDD_PMU_1P3	Supplying power to the internal RFLDO of the chip, connected to an external 1 µF capacitor (reserved)

VDD_PMU_VBAT1 provides input voltage for the internal buck, and PMU_BUCK_LX outputs on-off signals. Therefore, an external inductor and an output capacitor are required.

- Recommended inductor specifications: 2.2 µH, saturation current ≥ 0.8 A, DCR ≤ 0.2 ohm (a smaller DCR indicates higher efficiency)

Figure 3-9 shows the reference circuit diagram.

Figure 3-9 Internal buck reference circuit

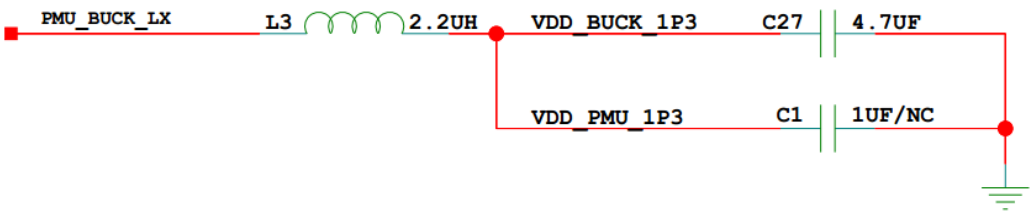
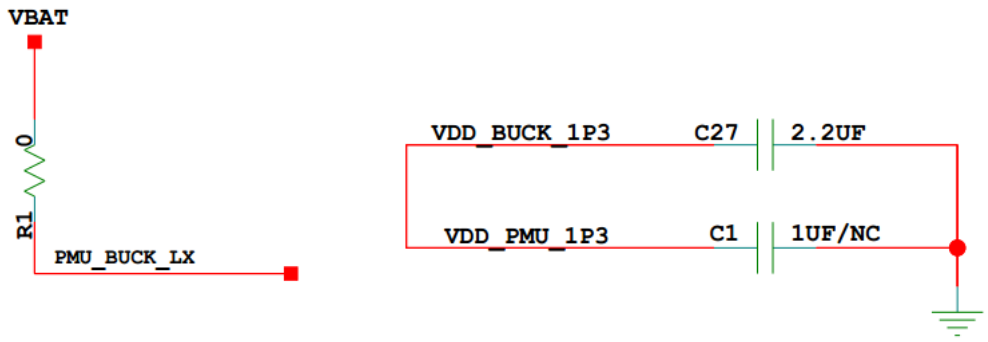


Table 3-16 Design recommendations on the LDO power supplies

Name	Description
PMU_BUCK_LX	Connected to a 0-ohm pull-up resistor and then to VBAT, set to the LDO mode
VDD_BUCK_1P3	Supplying power to the CLDO, output to VDD_PMU_1P3, and connected to an external 2.2 µF capacitor
VDD_PMU_1P3	Supplying power to the internal RFLDO of the chip, connected to an external 1 µF capacitor (reserved)

Figure 3-10 Internal LDO reference circuit



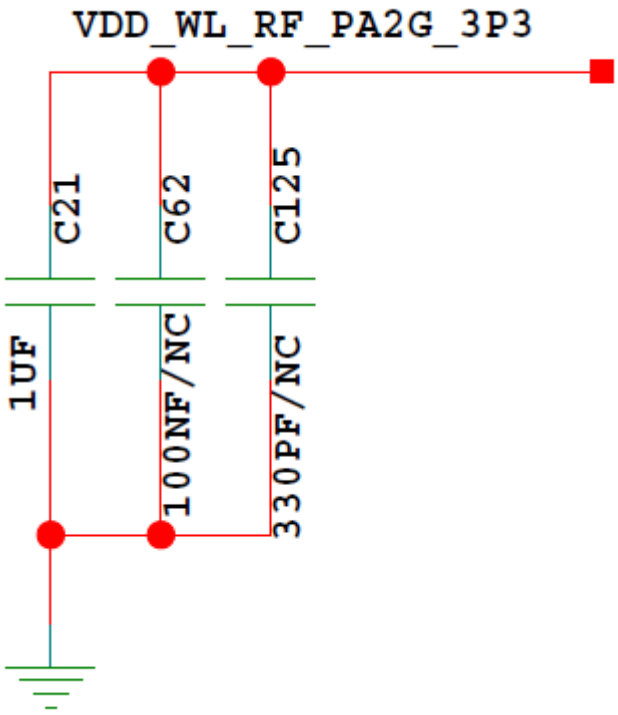
3.2.7 PA Power Supply

The VDD_WL_RF_PA2G_3P3 power can be supplied externally and can be connected to the VBAT power supply. **Table 3-17** shows the design recommendation, and **Figure 3-11** shows the reference circuit diagram.

Table 3-17 Design recommendations on the PA power supply

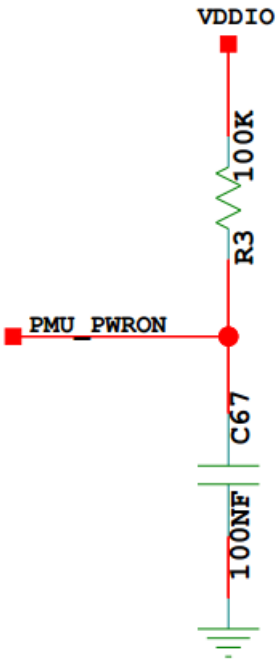
Name	Design Recommendation
VDD_WL_RF_PA2G_3P3	Supplied by VBAT, with a 1 μF capacitor, a 100 nF capacitor (reserved), and a 330 pF capacitor (reserved) connected near the chip in ascending order. If the space is insufficient, only one 1 μF capacitor can be added.

Figure 3-11 Circuit reference design of the PA power supply



3.2.8 Precautions

1. PMU_PWRON is a power-on enable pin. This pin must be powered on 1 ms later than VBAT and VDDIO. It is recommended that the RC delay circuit be reserved in PMU_PWRON. R = 100 kilohms, C = 100 nF. For Hi3881 V100, PMW_PWRON is controlled by the host. In normal cases, the boot time of the host is far greater than 1 ms, and the corresponding R and C pins can be reserved.



2. In internal LDO output mode, the filter capacitor of VDD_BUCK_1P3 must be greater than or equal to 2.2 µF. If the capacitor is not properly soldered or the capacitance is too small, an error is reported.

3.3 Design Recommendations on Peripheral Interfaces

3.3.1 Reference Design of the SDIO Interface

Hi3861 V100/Hi3861L V100/Hi3881 V100 communicates with the host over the SDIO interface. The SDIO interface supports the 1.8 V and 3.3 V levels. The host must also use the 1.8 V or 3.3 V level. Otherwise, a level converter component must be added between them. The selected level converter chip must comply with the SDIO rate requirement (50 MHz). **Table 3-18** describes the design recommendations.

Table 3-18 Design recommendations on the SDIO interface

Signal	Pull-Up/ Down	VDDIO	Connection Mode (2- or 4-Layer PCB)
SDIO_CLK	N/A	3.3/1.8	Hi3861L and Hi3861: 4-layer PCB: Connect a 33-ohm resistor in series at the device end, ensure that the trace length ≤ 5 inches, and reserve a 10 pF capacitor at the chip end. 2-layer PCB: Connect a 50-ohm resistor in series at the device end, ensure that the trace length ≤ 5 inches, and reserve a 10 pF capacitor at the chip end. Hi3881: 4-layer PCB: Connect a 33-ohm resistor in series at the device end, ensure that the trace length ≤ 5 inches, and reserve a 10 pF capacitor at the chip end. 2-layer PCB: Connect a 50-ohm resistor in series at the device end, ensure that the trace length ≤ 5 inches, and reserve a 10 pF capacitor at the chip end.
SDIO_CMD	N/A	3.3/1.8	Hi3861L and Hi3861: 4-layer PCB: Connect a 33-ohm or 0-ohm resistor in series at the device end and ensure the trace length ≤ 5 inches. 2-layer PCB: Connect a 75-ohm or 0-ohm resistor in series at the device end and ensure the trace length ≤ 5 inches. Hi3881: 4-layer PCB: Connect a 33-ohm resistor in series at the device end and ensure the trace length ≤ 5 inches. 2-layer PCB: Connect a 75-ohm resistor in series at the device end and ensure the trace length ≤ 5 inches.

Signal	Pull-Up/ Down	VDDIO	Connection Mode (2- or 4-Layer PCB)
SDIO_D0 SDIO_D1 SDIO_D2 SDIO_D3	The chip has a built-in 20-kilohm pull-up resistor. It is recommended that a pull-up resistor be reserved on the PCB for debugging.	3.3/1.8	Hi3861L and Hi3861: 4-layer PCB: Connect a 33-ohm or 0-ohm resistor in series at the device end and ensure the trace length ≤ 5 inches. 2-layer PCB: Connect a 75-ohm or 0-ohm resistor in series at the device end and ensure the trace length ≤ 5 inches. Hi3881: 4-layer PCB: Connect a 33-ohm resistor in series at the device end and ensure the trace length ≤ 5 inches. 2-layer PCB: Connect a 75-ohm resistor in series at the device end and ensure the trace length ≤ 5 inches.

3.3.2 Reference Design of the UART Interface

Hi3861 V100 and Hi3861L V100 support three groups of UART signals. Hi3881 V100 supports only one UART0. UART0 is used for Hi3861 V100/Hi3861L V100/ Hi3881 V100 maintenance and test printing. UART1 and UART2 are used for device interconnection. The level of the pin is the same as that of VDDIO. **Table 3-19** describes the design recommendations.

Table 3-19 Design recommendations on the UART interface

Name	Design Recommendation
UART0_LOG_RXD	Directly connected, trace ≤ 5 inches
UART0_LOG_TXD	Directly connected, trace ≤ 5 inches
UART1_TXD / UART2_TXD	Directly connected, trace ≤ 5 inches
UART1_RXD / UART2_RXD	Directly connected, trace ≤ 5 inches
UART1_RTS / UART2_RTS	Directly connected, trace ≤ 5 inches

Name	Design Recommendation
UART1_CTS / UART2_CTS	Directly connected, trace ≤ 5 inches

3.3.3 Reference Design of the PWM Interface

Hi3861 V100/Hi3861L V100 supports the output of six pulse-width modulation (PWM) interface signals. The output level is the same as the VDDIO level. The duty cycle ranges from 1/65535 to 1. **Table 3-20** describes the design recommendations.

Table 3-20 Design recommendations on the PWM interface

Name	Design Recommendation
PWM0_OUT	Directly connected, trace ≤ 5 inches
PWM1_OUT	Directly connected, trace ≤ 5 inches
PWM2_OUT	Directly connected, trace ≤ 5 inches
PWM3_OUT	Directly connected, trace ≤ 5 inches
PWM4_OUT	Directly connected, trace ≤ 5 inches
PWM5_OUT	Directly connected, trace ≤ 5 inches

3.3.4 Reference Design of the I^2S Interface

Hi3861 V100/Hi3861L V100 supports one I^2S interface. The input/output level must be the same as the VDDIO level. **Table 3-21** describes the design recommendations.

Table 3-21 Design recommendations on the I^2S interface

Name	Design Recommendation
I2S0_MCK	Directly connected, and surrounded with GND traces
I2S0_TX	Directly connected
I2S0_RX	Directly connected
I2S0_CLK	Directly connected, and surrounded with GND traces
I2S0_WS	Directly connected, and surrounded with GND traces

3.3.5 Reference Design of the SPI Interface

Hi3861 V100/Hi3861L V100 supports two SPI interfaces. The input/output level must be the same as the VDDIO level. **Table 3-22** describes the design recommendations.

Table 3-22 Design recommendations on the SPI interface

Name	Design Recommendation
SPI0_CS1 / SPI1_CS1	Directly connected, trace ≤ 5 inches
SPI0_CLK / SPI1_CLK	2-layer PCB: trace ≤5 inches, a 50-ohm resistor connected in series at the chip end, and each trace surrounded with GND traces 4-layer PCB: VDDIO = 1.8 V, trace ≤ 5 inches, a 33-ohm resistor connected in series at the chip end, and each trace surrounded with GND traces 4-layer PCB: VDDIO = 3.3 V, trace ≤ 5 inches, a 50-ohm resistor connected in series at the chip end, and each trace surrounded with GND traces
SPI0_RXD / SPI1_RXD SPI0_TXD / SPI1_TXD	2-layer PCB: trace ≤ 5 inches, a 75Ω resistor connected in series, and each trace surrounded with GND traces 4-layer PCB: trace ≤ 5 inches, a 0-ohm or 33-ohm resistor connected in series, and each trace surrounded with GND traces

3.3.6 Reference Design of the I^2C Interface

Hi3861 V100/Hi3861L V100 supports two I^2C interfaces. The input/output level must be the same as the VDDIO level. **Table 3-23** describes the design recommendations.

Table 3-23 Design recommendations on the I^2C interface

Name	Design Recommendation
I2C0_SCL / I2C1_SCL	Directly connected, trace ≤ 5 inches, with a 2.2-kilohm resistor connected to pull up to VDDIO
I2C0_SDA / I2C1_SDA	Directly connected, trace ≤ 5 inches, with a 2.2-kilohm resistor connected to pull up to VDDIO

3.3.7 Reference Design of the ADC Interface

Hi3861 V100/Hi3861L V100 supports seven analog digital converter (ADC) interfaces. The ADC input voltage ranges from 0 V to 3.6 V. **Table 3-24** describes

the design recommendations. The level of the ADC input signal can be read through UART0.

Table 3-24 Design recommendations on the ADC interface

Name	Design Recommendation
ADC0	Directly connected, trace ≤ 5 inches
ADC1	Directly connected, trace ≤ 5 inches
ADC2	Directly connected, trace ≤ 5 inches
ADC3	Directly connected, trace ≤ 5 inches
ADC4	Directly connected, trace ≤ 5 inches
ADC5	Directly connected, trace ≤ 5 inches
ADC6	Directly connected, trace ≤ 5 inches

3.3.8 Reference Design of the PTA Interface

Hi3861 V100/Hi3861L V100 supports one packet traffic arbitration (PTA) interface for managing the coexistence of Wi-Fi and Bluetooth (BT), as shown in **Figure 3-12**. The input/output level must be the same as the VDDIO level. **Table 3-25** describes the design recommendations.

The PTA interface is located between the Wi-Fi MAC and the BT. It receives the TX/RX requests and status inputs from the Wi-Fi MAC and the BT and outputs the arbitration results to them. In addition, the PTA interface has an output pin coex_switch) for switching the antenna.

Figure 3-12 PTA interface design

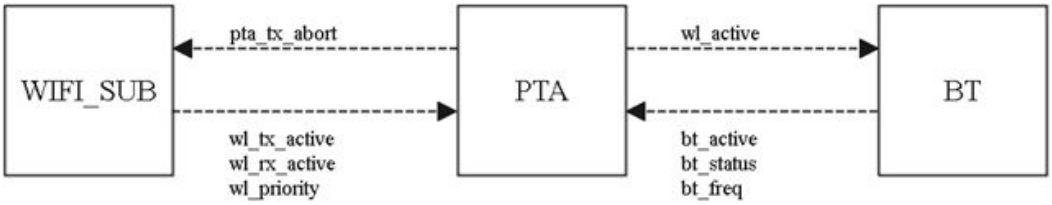


Table 3-25 Design recommendations on the PTA interface

Name	Design Recommendation
BT_FREQ	Directly connected, trace ≤ 5 inches
BT_STATUS	Directly connected, trace ≤ 5 inches
COEX_SWITCH	Directly connected, trace ≤ 5 inches
BT_ACTIVE	Directly connected, trace ≤ 5 inches

Name	Design Recommendation
WLAN_ACTIVE	Directly connected, trace ≤ 5 inches

3.3.9 Reference Design of the Ultra-low Power Interface

Hi3861 V100/Hi3861L V100 supports four ultra low-power interfaces. The input level must be the same as the VDDIO level. **Table 3-26** describes the design recommendations.

Table 3-26 Design recommendations on the ultra-low power interface

Name	Design Recommendation
GPIO_03	Directly connected, trace ≤ 5 inches, and valid on the rising edge. The function can be implemented by using the GPIO or external keys.
GPIO_05	Directly connected, trace ≤ 5 inches, and valid on the rising edge. The function can be implemented by using the GPIO or external keys.
GPIO_07	Directly connected, trace ≤ 5 inches, and valid on the rising edge. The function can be implemented by using the GPIO or external keys.
GPIO_14	Directly connected, trace ≤ 5 inches, and valid on the rising edge. The function can be implemented by using the GPIO or external keys.

3.4 Reference Design of Control Signals and Low-Power Applications

Hi3861 V100/Hi3861L V100/Hi3881 V100 provides multiple control signals, including:

- Global control signal: PMU_PWRON
- Mutual wakeup signals: HOST2DEV_WAKEUP and DEV2HOST_WAKEUP
- SDIO data interrupt: GPIO2 (which can be configured as another GPIO by using software)

The preceding control signals must be connected to the host.

Table 3-27 Design recommendations on control signals and low-power applications

Name	Design Recommendation
PMU_PWRON	Power-on enable. Low level triggers reset. This pin is connected to a 100-kilohm pull-up resistor and then to VDDIO, connected to a 100 nF capacitor and to GND, and also directly connected to the host chip.
GPIO2	GPIO2, used for the SDIO data interrupt, and directly connected to the host chip
DEV2HOST_WAKEUP	GPIO5, used for the device to wake up the host, and directly connected to the host chip
HOST2DEV_WAKEUP	GPIO6, used for the host to wake up the device, and directly connected to the host chip
RTC32K_XOUT	Clock output when an external 32.768 kHz crystal is connected, or clock input when a 32.768 kHz signal is injected
RTC32K_XIN	Clock input when an external 32.768 kHz crystal is connected

If low-power applications are required, the following design requirements must be considered:

- VBAT and VDDIO must be always powered on and cannot be disabled when the system enters standby mode.
- Only Hi3861L supports the external RTC clock input. For details about the specifications, see **3.1.1.2 RTC**.
- The PMU_PWRON and DEV2HOST_WAKEUP signals must be connected to the always-on GPIO. HOST2DEV_WAKEUP and GPIO2 connect to the host and can be powered off in standby mode. In addition, HOST2DEV_WAKEUP must retain low level before standby and active wakeup upon power-on to prevent the device from being woken up by mistake.

Figure 3-13 shows the reference circuit diagram of the control signal.

Figure 3-13 Reference circuit diagram of the control signal

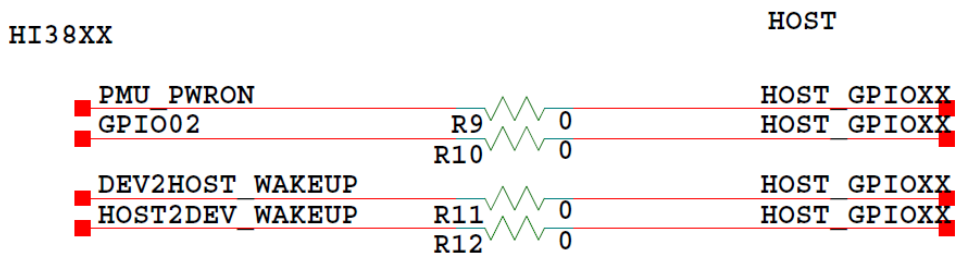
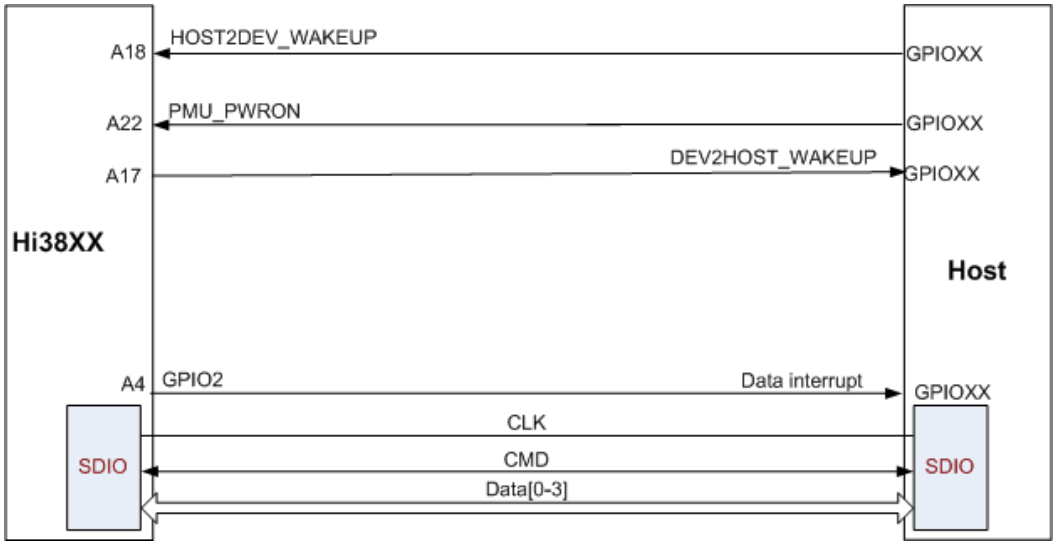


Figure 3-14 shows the reference connection diagram of the low-power application system.

Figure 3-14 Reference connection diagram of the low-power application system



The low-power application system has the following functions:

- HOST2DEV_WAKEUP: connects to the host, used for the host to wake up the device.
- GPIO2: connects to the host, used for the SDIO data interrupt.
- DEV2HOST_WAKEUP: connects to the host, used for the device to wake up the host. The host queries the device status by using the SDIO.
- PMU_PWRON: connects to the host, used to control the power-on and power-off of the device. This pin needs to connect to the RC delay circuit. For details, see **3.2.8 Precautions**.

4 PCB Design Recommendations

4.1 Stackup and Layout

Hi3861 V100/Hi3861L V100/Hi3881 V100 uses the QFN-32 package. The package size is 5 mm x 5 mm (0.20 in. x 0.20 in.). The PCB can have two or four layers. Single-sided surface-mount technology (SMT) is supported.

- Design recommendations on the 2-layer PCB

  Top layer: signal trace layer. Route signal traces and power traces at the top layer if possible.

  Bottom layer: GND plane layer. Keep the GND plane as complete as possible.
- Design recommendations on the 4-layer PCB

  Top layer: signal trace layer. Route signal traces at the top layer if possible.

  Internal layer 1: GND plane layer. Keep a complete GND plane layer.

  Inner Layer 2: power plane layer. Route power traces at the third layer, and separate power traces by GND traces.

  Bottom layer: Route a few signal traces. Ensure that the bottom layer is a complete GND plane.

Note the following during the PCB design:

- Recommendations: In the On Board solution, the PCB thickness should be greater than or equal to 1 mm to prevent warpage and the via should be 10 or 22 mils. The center distance of adjacent through-holes on the EPAD is about 23–40 mils. Usually, the recommended value is 25 mils to prevent solder leakage.
- The typical PCB material is FR4. The recommended thickness of the copper foil on the surface layer is 1.2 mils (0.5 oz+plating). Usually, the PCB thickness is greater than 1.0 mm. The typical value is 1.2 mm. The optional value can be 1.0 mm.

For common stackup design and impedance control, refer to the stackup information in **Table 4-1** and **Table 4-3**.

Table 4-1 Reference stackup information for the 2-layer PCB (1.0 mm in thickness)

Layer ID	Design requirement (oz/mil)		Adjusted design by the PCB vendor (oz/mil)	
	Stackup diagram	PCB thickness	PCB thickness	Stackup diagram
Art 1	0.5 oz+plating		0.5 oz+plating	
	CORE	XX	36.00	CORE
Art 2	0.5 oz+plating		0.5 oz+plating	
	Designed PCB thickness		1.0	(mm)
	Theoretical PCB thickness		1±0.1	(mm)

Table 4-2 Single trace width, impedance, and reference layer information

Layer ID	Designed Trace Width	Designed Impedance	Adjusted Trace Width	Adjusted Impedance	Reference Layer
Art 1	5/19/5 (Distance to GND/Trace width/Distance to GND)	50±10%	5.25/18.5/5.25 (Distance to GND/Trace width/ Distance to GND)	50±10%	2

Note: The measurement unit of trace width is mil, and the measurement unit of impedance is ohm.

Table 4-3 Reference stackup information for the 4-layer PCB (1.2 mm in thickness)

Layer ID	Stackup Diagram	RC	Designed PCB Thickness (μm)	Adjusted PCB Thickness (μm)	Internal Control Tolerance (μm)
Solder mask	-	-	-	20	20±15
Art01	-	-	1/2 oz+plating	40	40±15
	PP_7628	50%	208	215	215±20
Art02	-	-	30	30	30±5
	Core (excluding copper)	-	600	600	600±64
Art03	-	-	30	30	30±5
	PP_7628	50%	208	214	214±20
Art04	-	-	1/2 oz+plating	40	40±15
Solder mask	-	-	-	20	20±15
PCB thickness	-	-	1.2±0.12 mm	1.2±0.12 mm	-

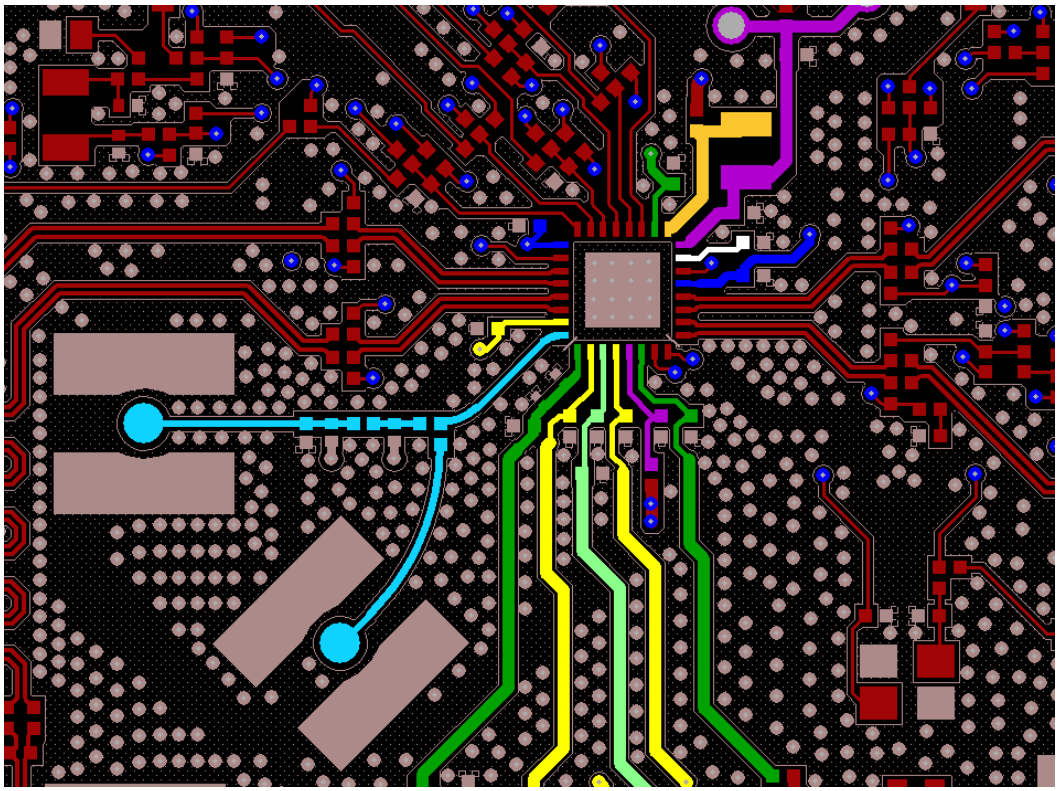
Table 4-4 Single trace width, impedance, and reference layer information

Signal Plane	GND Plane	Impedance Target	Impedance Tolerance	Designed Trace Width (mil)	Distance to Copper (mil)
L1	L1 & L2	50 ohms	10%	11	6

4.2 Fanout Design Recommendations

Figure 4-1 shows the fanout of the Hi3861 V100/Hi3861L V100/Hi3881 V100 4-layer PCB.

Figure 4-1 Reference design of the fanout for the 4-layer PCB



In the figure:

- Yellow: VDD_WL_RF_LNA_1P2, VDD_WL_RF_TRX_1P2, and VDD_PMU_RFLDO1
- Green: VDD_WL_RF_PA2G_3P3, VDD_PMU_VBAT1, and VDD_PMU_VBAT2
- Blue: VDDIO1 and VDDIO2
- Purple: VDD_BUCK_1P3 and VDD_PMU_1P3
- White: VDD_PMU_CLDO
- Orange: PMU_BUCK_LX
- Light blue: RF
- Light green: VDD_WL_RF_VCO_1P2

4.3 PCB Layout

The Hi3861 V100/Hi3861L V100/Hi3881 V100 application supports the On Board solution and the module solution.

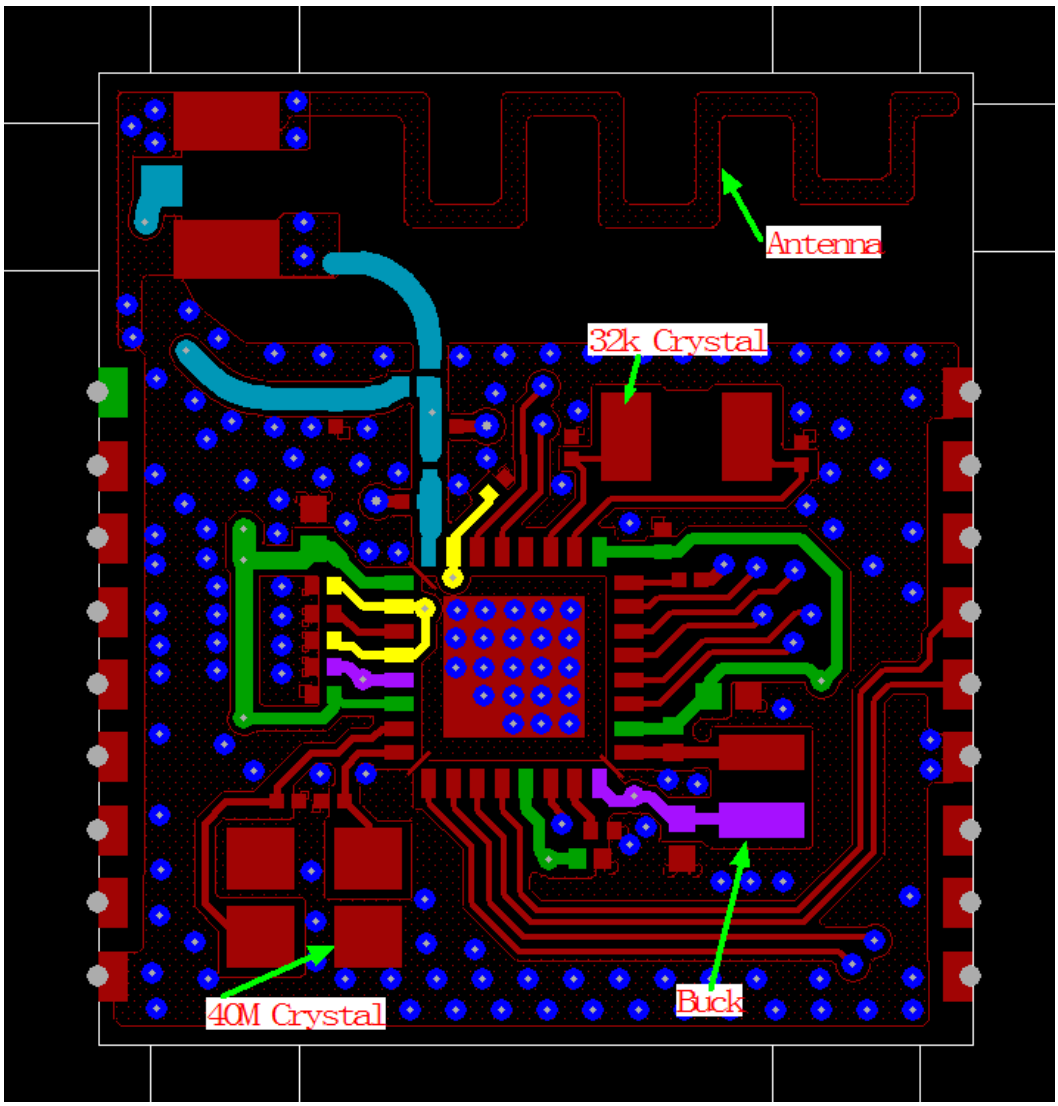
- On Board solution
  - The 2-layer PCB is supported.
  - The 0201 package (inch) is recommended for SMT components.
- SDIO module solution
  - The 4-layer PCB is recommended.
  - The 0201 package (inch) is recommended for SMT components. The mainstream module size in the market is 12 mm x 12 mm (0.47 in. x 0.47 in.).

- Set-top box (STB) application
  - The On Board solution supports double-sided SMT. If the space is sufficient, the 0402 package is suggested.
  - The module solution can be directly selected.
- IPC application

  The module solution can be directly selected for the miniaturization purpose.
- IoT products
  - 2-layer PCBs are recommended because IoT products are sensitive to costs.
  - The 0201 package with single-side SMT is recommended in view of the limited PCB space.

Figure 4-2 and **Figure 4-3** show the 2-layer PCB layout for IoT products and the 4-layer PCB for the SDIO module.

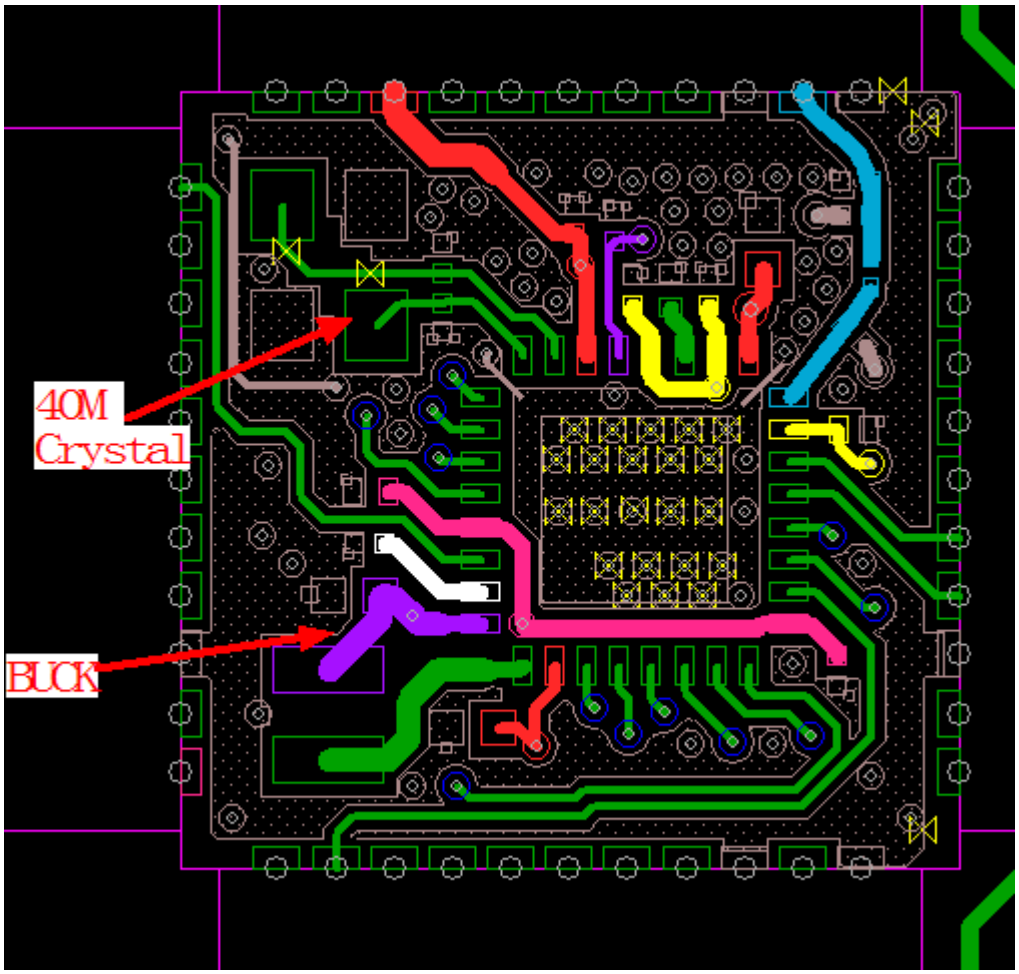
Figure 4-2 PCB layout reference 1 for IoT products



In the figure:

- Yellow: VDD_WL_RF_LNA_1P2, VDD_WL_RF_TRX_1P2, and VDD_PMU_RFLDO1
- Green: VDD_WL_RF_PA2G_3P3, VDD_PMU_VBAT1, VDD_PMU_VBAT2, VDDIO1, and VDDIO2. Because VDDIO is 3.3 V, VBAT and VDDIO are connected to the same network.
- Purple: VDD_BUCK_1P3 and VDD_PMU_1P3
- Light blue: RF

Figure 4-3 PCB layout reference 2 for the SDIO module



In the figure:

- Yellow: VDD_WL_RF_LNA_1P2, VDD_WL_RF_TRX_1P2, and VDD_PMU_RFLDO1
- Red: VDD_WL_RF_PA2G_3P3, VDD_PMU_VBAT1, and VDD_PMU_VBAT2
- Purple: VDD_BUCK_1P3 and VDD_PMU_1P3
- Pink: VDDIO1 and VDDIO2
- White: VDD_PMU_CLDO
- Light blue: RF
- Note: The RF components are compactly arranged. As a result, the two vias of the RF ground capacitor are close to each other, which affects the harmonic suppression performance of the RF. It is recommended that the two ground capacitors be located on both sides of the RF trace to improve the harmonic suppression effect of the RF circuit.

4.4 Power Supply

4.4.1 VBAT Trace Routing

The recommendations on VBAT trace routing are as follows:

- The current of VDD_PMU_VBAT1 is 400 mA. According to the principle of 100 mA/4 mils, the width of the VABT1 power trace must be greater than or equal to 16 mils. A 1 µF filter capacitor must be placed close to the pin.
- The current of VDD_PMU_VBAT2 is 500 mA. According to the principle of 100 mA/4 mils, the width of the VABT2 power trace must be greater than or equal to 20 mils. A 1 µF filter capacitor must be placed close to the pin. In addition, the power trace must pass through the filter capacitor before reaching the power pin of the chip.
- Place the VDD_PMU_CLDO filter capacitor close to the pin. The recommended trace width is greater than or equal to 8 mils.

Figure 4-4 shows the position of the filter capacitor on the VABT power trace (green), VDD_PMU_VBAT1, and VDD_PMU_VABT2.

Figure 4-4 VBAT trace routing reference for the 4-layer PCB

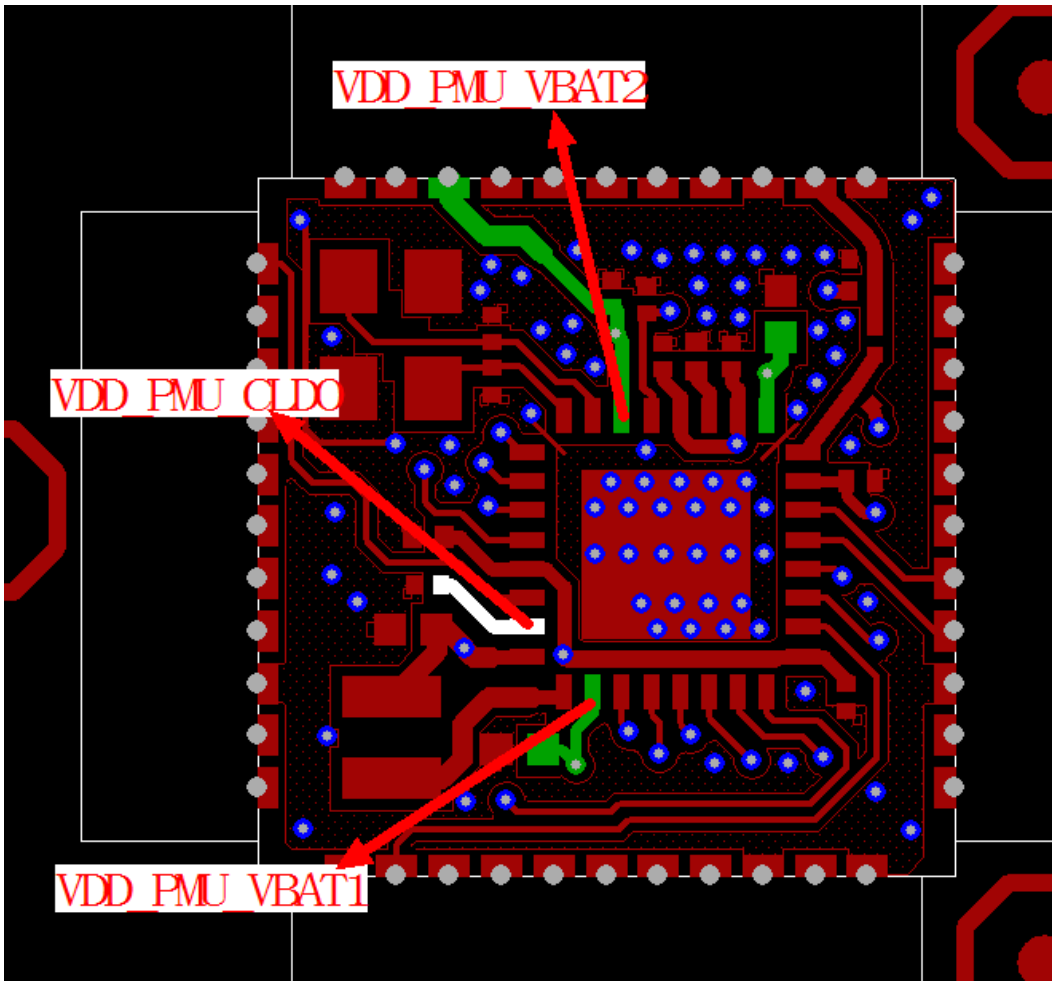
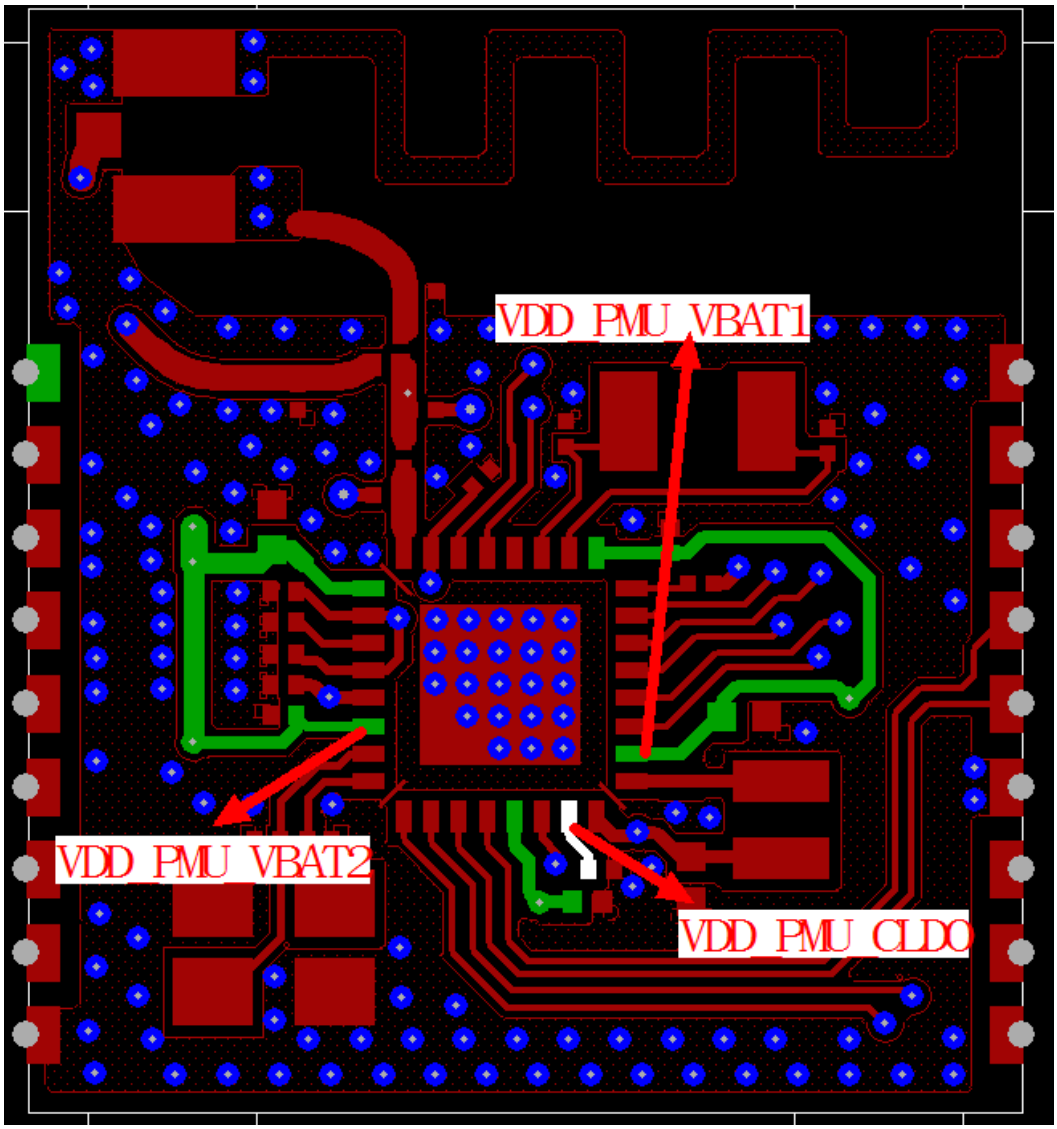


Figure 4-5 VBAT trace routing reference for the 2-layer PCB



4.4.2 Buck Trace Routing

The buck output, buck inductor, filter capacitor, and the shortest return current path formed by the terrain are very important. In the loop, there is much high-frequency switching current. Therefore, the loop area must be minimized during PCB routing. A larger return current loop area of the buck implies stronger magnetic field radiation, which will become the main source of noise diffusion.

The buck and RF are on a diagonal to avoid the impact of the buck power noise on the RF (lower left) and analog blocks. Therefore, the external power inductor should be placed far away from the RF and analog blocks of Hi3861 V100/ Hi3861L V100/Hi3881 V100 to reduce the impact of the buck converter on the RF performance.

The PCB routing restrictions are as follows:

- PMU_BUCK_LX: It is a strong-interference source and should be kept away from other sensitive signals. The output current should be 200 mA, the trace

width must be greater than or equal to 10 mils, and the traces should be accompanied by GND traces. The GND traces should be as thick as possible and have more GND vias.

- VDD_BUCK_1P3: The buck output is fed back to the internal CLDO input of the chip, with separate trace routing. The current should be 100 mA, the trace width must be greater than or equal to 10 mils, and a 4.7 µF filter capacitor must be placed close to the pin. The trace source obtains power from the output capacitor of 1P3. Both ends of the traces should be accompanied by GND traces if possible. The GND traces should be as thick as possible and have more GND vias.
- VDD_PMU_1P3: The buck input supplies power to the internal RFLDO of the chip. The current should be 100 mA, the trace width must be greater than or equal to 10 mils, and a 1 µF filter capacitor must be placed close to the pin. The trace source obtains power from the output capacitor of 1P3. Both ends of the traces should be accompanied by GND traces if possible. The GND traces should be as thick as possible and have more GND vias. Route the traces at the back side far away from the EPAD of the chip. Do not split the reference GND plane.

Figure 4-6 Buck trace routing reference for the 4-layer PCB

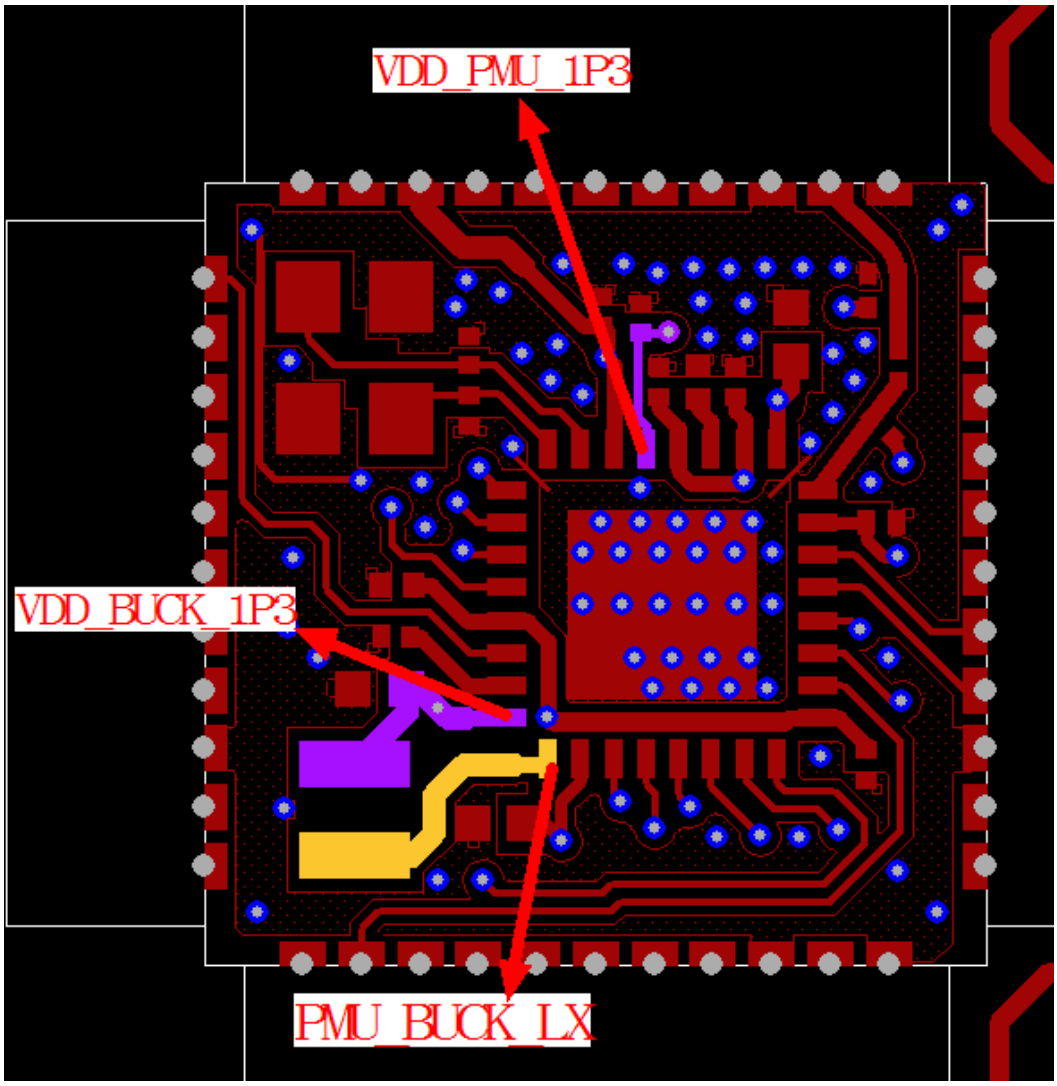
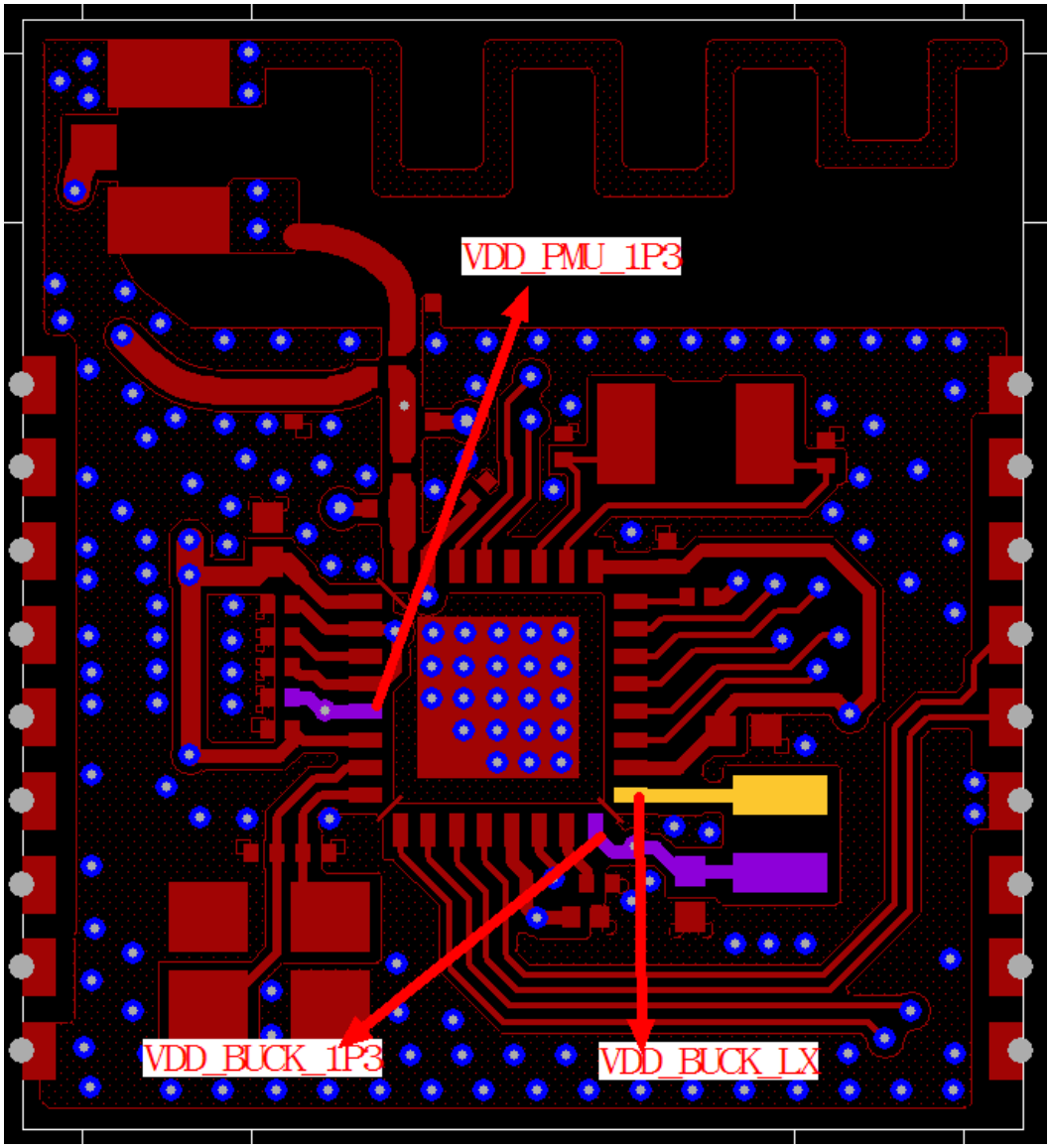


Figure 4-7 Buck trace routing reference for the 2-layer PCB



4.5 RF Trace Routing

The recommendations on RF trace routing are as follows:

- The RFLDO1 power traces can be routed in serial mode. A star topology provides better performance. For details, see the yellow traces in the following figure.
- VDD_WL_RF_VCO_1P2 connects to an external 1 µF capacitor to filter RFLDO2 in the chip.
- VDD_PMU_RFLDO1 is the LDO output in the chip. It outputs 1.15 V to supply power to the RF. The current should be 150 mA. The trace width must be greater than or equal to 8 mils.
- VDD_WL_RF_PA2G_3P3 supplies power to the Wi-Fi PA and can be directly connected to VBAT. A filter capacitor should be placed close to the chip pin.

- Ensure that no via is used for placing a filter capacitor of the PA power supply and routing traces. You are advised to route traces on the same layer as the chip to avoid parasitic parameters caused by vias. The voltage drop of the trace must be less than 30 mV. The current should be 400 mA, and the trace width must be greater than or equal to 16 mils.
- VDD_WL_RF_LNA_1P2 supplies power to the low noise amplifier (LNA). The traces must be routed away from RF signal interference.
- The power traces of VDD_PMU_RFLDO1, VDD_WL_RF_TRX_1P2, VDD_WL_RF_LNA_1P2, and VDD_WL_RF_PA2G_3P3 should be staggered to avoid mutual interference.
- Place the front-end matching circuit of the Wi-Fi RF close to the chip, and place the ESD protection inductor close to the antenna.
- Keep RF signal traces as short as possible, keep the impedance of 50 ohms, use the coplanar waveguide design for the 2-layer PCB, surround the traces with GND traces, and punch more ground holes on both sides.
- Keep RF traces away from high-speed clock traces and power traces and ensure that the reference plane for RF trace routing is complete. If this reference plane is split, use a 0-ohm resistor to ensure the connectivity.
- The reference GND of the RF traces must be properly connected to the main GND of the chip. If the GND loop is poor, the RF performance deteriorates. The EPAD needs to be led out from two pins to connect to the external GND.
- Connect the capacitor of the π-shaped RF matching filter circuit to GND over a single point instead of at the top layer. Punch a via for connecting the circuit to the bottom layer. If the PCB has multiple layers, do not connect the via to the GND of the middle layer. The via at the middle layer must be processed in the same way as that at the top layer. In this way, the processed via on the RF frequency is equivalent to a small inductor and a capacitor to form an LC circuit, thereby suppressing harmonic radiation. As mentioned in the PCB layout, the two vias cannot be too close to each other. It is recommended that the vias be distributed on different sides of the RF cable.

Figure 4-8 RFLDO1 and RF trace routing reference for the 4-layer PCB

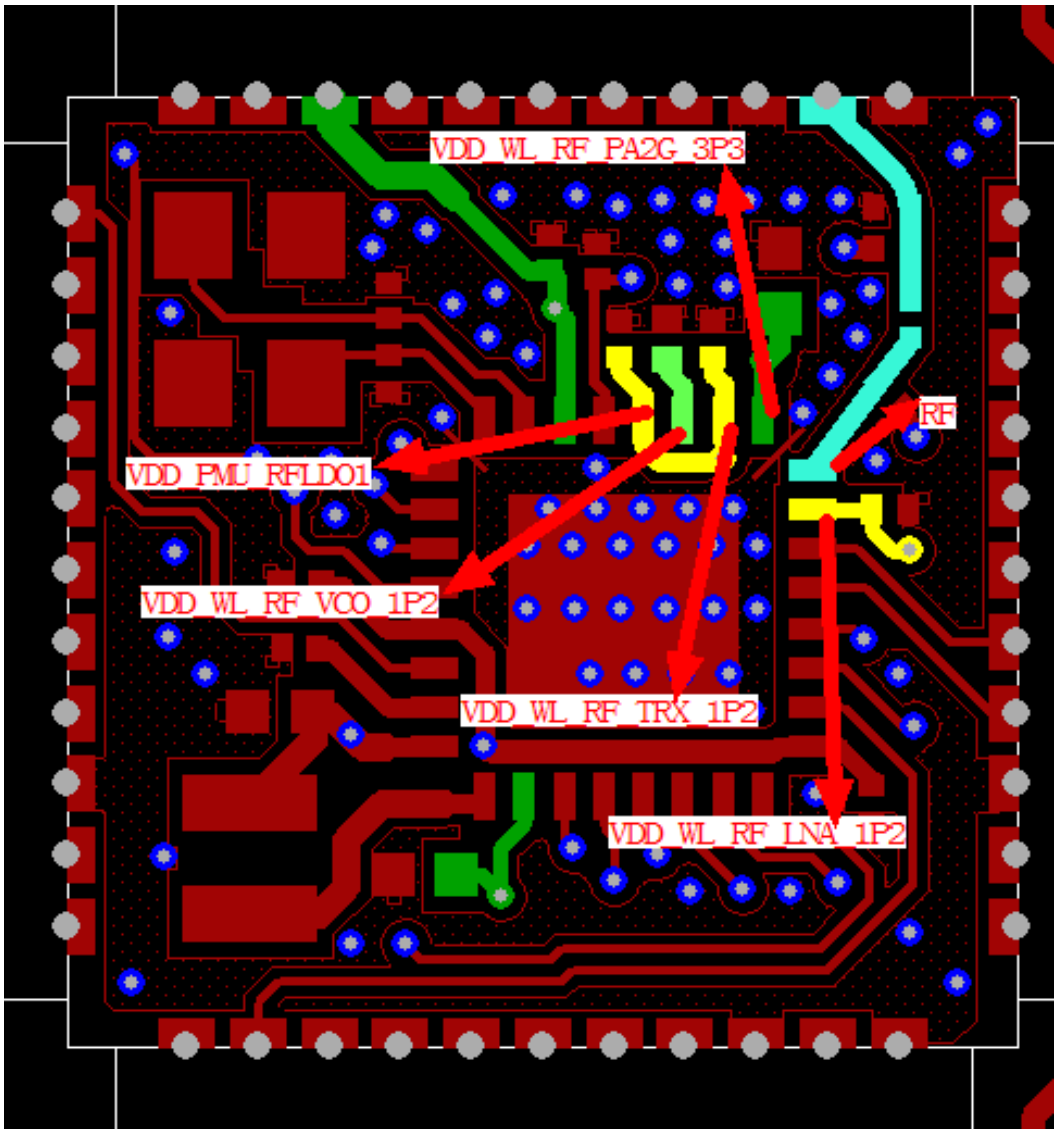
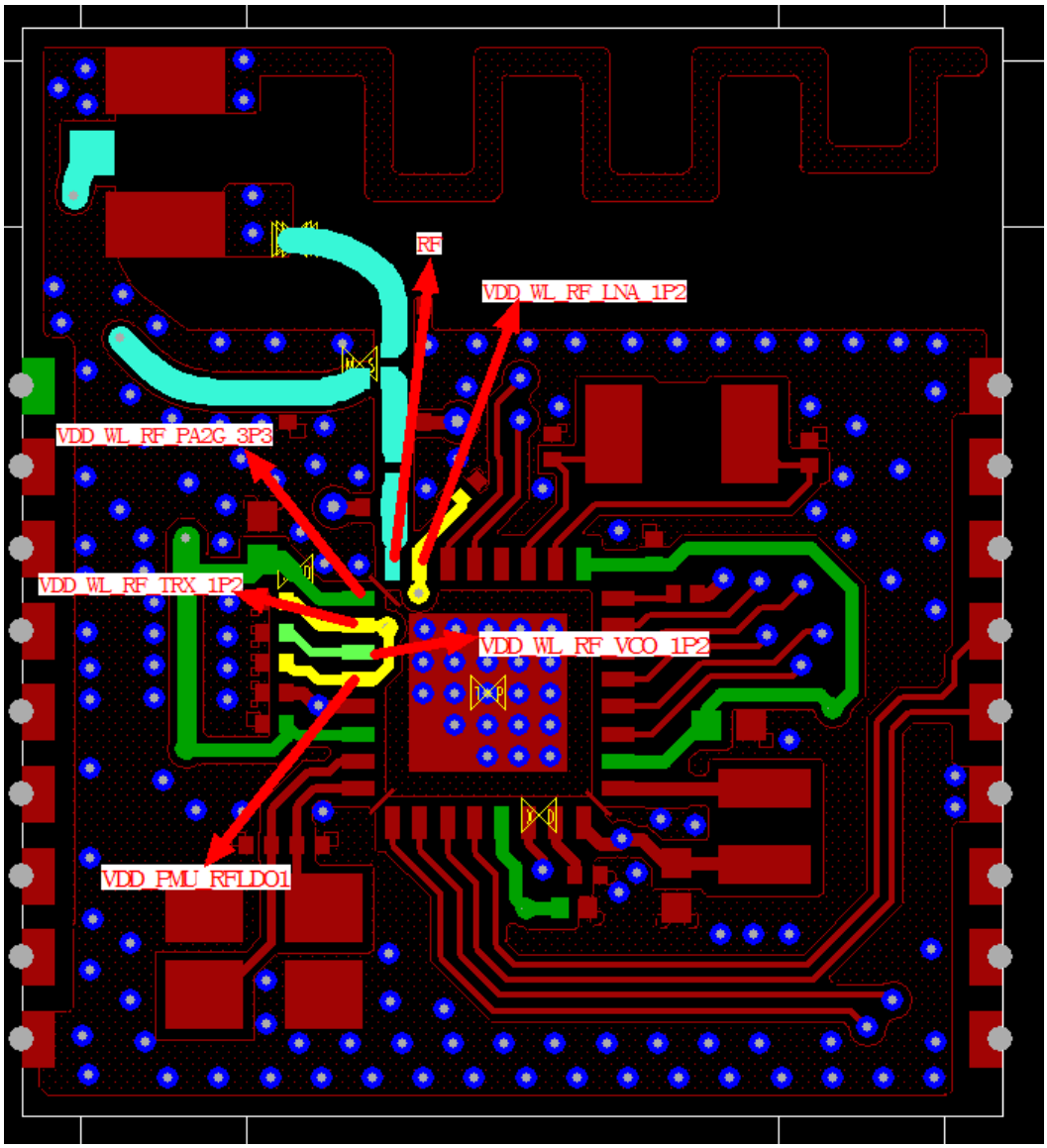


Figure 4-9 RFLDO1 and RF trace routing reference for the 2-layer PCB



4.6 CMU Trace Routing

The recommendations on clock managing unit (CMU) trace routing are as follows:

- The Wi-Fi system has high requirements on the clock. The crystal and XIN/XOUT traces must be far away from noise sources (RF and buck) and heat sources to avoid phase noise deterioration caused by noise interference or crystal temperature drift caused by heat source radiation.
- When the PCB space is small, the space between the crystal and the RF is small, and the clock may be coupled with the RF to interfere with the chip. You are advised to connect a 0-ohm resistor on the XIN trace close to the chip end for debugging.
- For a 4-layer PCB, it is recommended that the crystal GND pad be split from other GND at the top layer and be connected to the main GND through vias

to prevent the clock accuracy from being affected by the heat generated by the components on the board. Void under the signal pad to connect the main GND layer to reduce the parasitic capacitance of the pad.

- The XIN/XOUT traces should be as short as possible. It is recommended that the traces be surrounded with GND traces. The GND traces should be as thick as possible and more GND vias should be punched.
- If the On Board design and double-sided PCB are used, place the crystal at the bottom layer and punch vias close to the chip pin to connect XIN/XOUT to the chip.
- XIN/XOUT and VBAT should be separated by ground holes.

Figure 4-10 shows the CMU layout and trace routing.

Figure 4-10 CMU trace routing reference for the 4-layer PCB

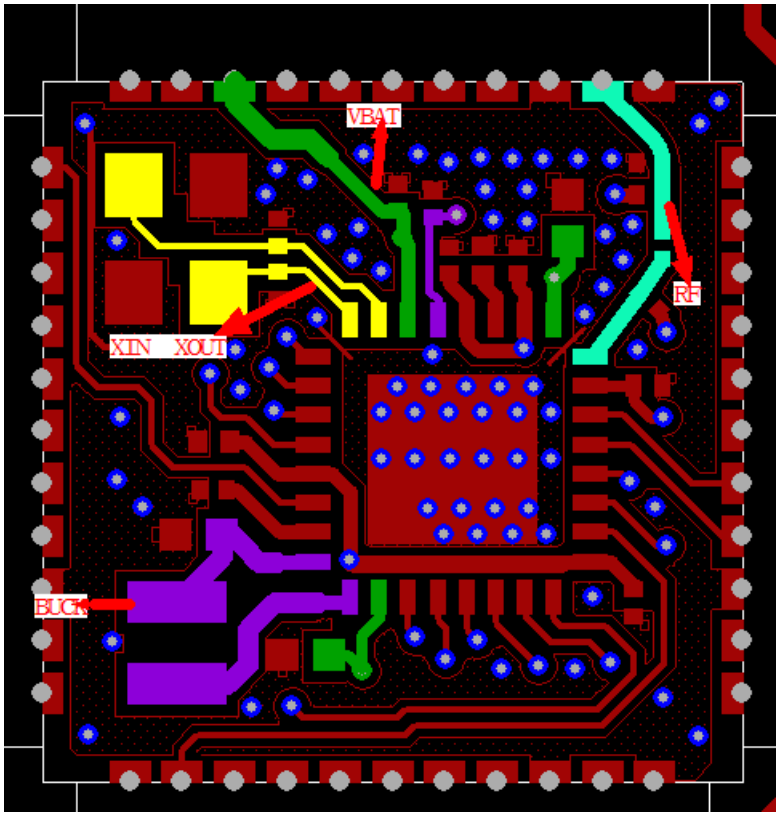
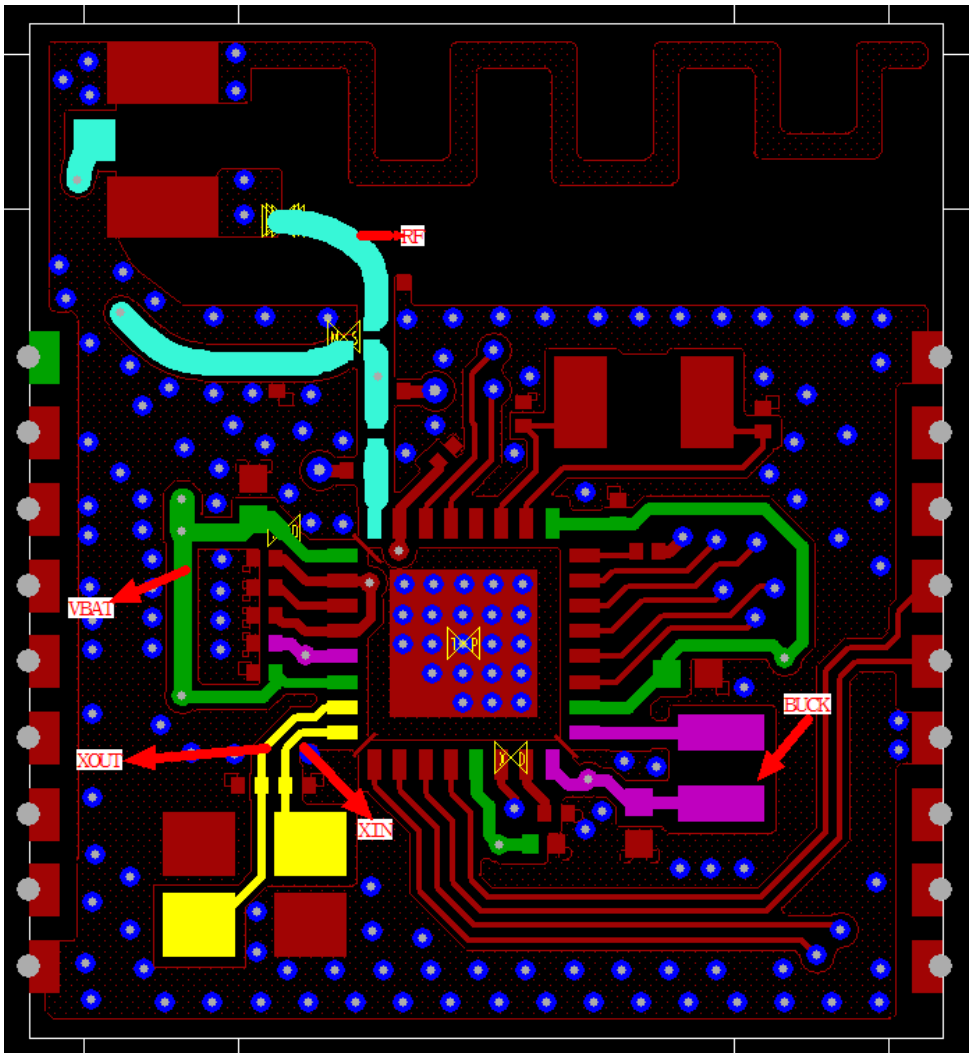


Figure 4-11 CMU trace routing reference for the 2-layer PCB



4.7 DBB Trace Routing

The recommendations on digital baseband (DBB) trace routing are as follows:

- Place the filter capacitor of the VDDIO power supply close to the pin.
- Avoid sensitive power supplies, RF, and analog blocks, which is the only rule for digital signal design.
- Route RTC clock traces far away from the RF and analog blocks, surround the RTC_CLK trace with GND traces, and punch as many vias as possible near the GND traces.

4.8 SDIO Trace Routing

The recommendations on SDIO trace routing are as follows:

- The SDIO interface supports up to 50 MHz. The traces must be far away from sensitive power supplies, RF, and analog part, and the trace length must be as short as possible and cannot exceed 5 inches.
- The SDIO trace spacing must comply with the 3W principle. That is, the distance measured between two trace center lines is at least 3 times the trace width to avoid crosstalk between signals. The SDIO_CLK signal trace should be surrounded by GND traces. Ensure that the GND traces are thick and that more GND vias are punched on both sides of the traces.
- Reserve a 10 pF capacitor close to the chip end for the SDIO_CLK pin to suppress radiation signals.
- Connect one end with the reserved pull-up resistors of SDIO_DATA (0–3) directly to the signal trace, and connect the other end to VDDIO. In this way, signal reflection can be reduced.

4.9 GND Trace Routing

In addition to GND pins, the exposed pad (EPAD) of the Hi3861 V100/Hi3861L V100/Hi3881 V100 must be grounded.

The recommendations on GND trace routing are as follows:

- Ensure that the reference GND plane is complete. Do not split the reference GND plane when routing traces on the back side of the 2-layer PCB. Ensure that grounded pins and capacitors have a good GND loop with the EPAD and the main GND of the system.
- Punch vias on the EPAD. The distance between the centers of adjacent vias is about 23–40 mils. Generally, 25 mils are recommended. At least 16 vias are required.

Figure 4-12 EPAD trace routing reference for the 2-layer PCB (top layer)

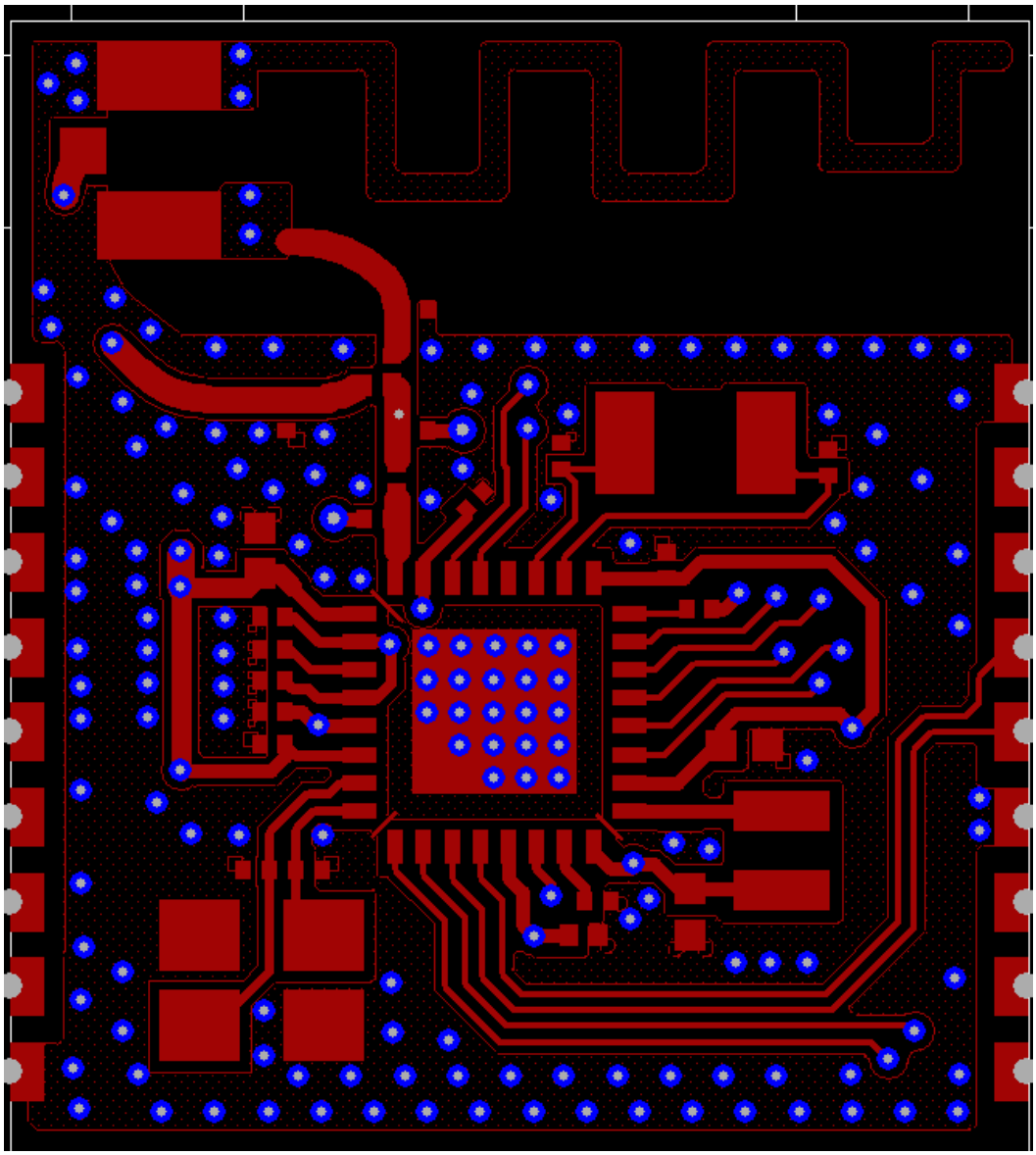
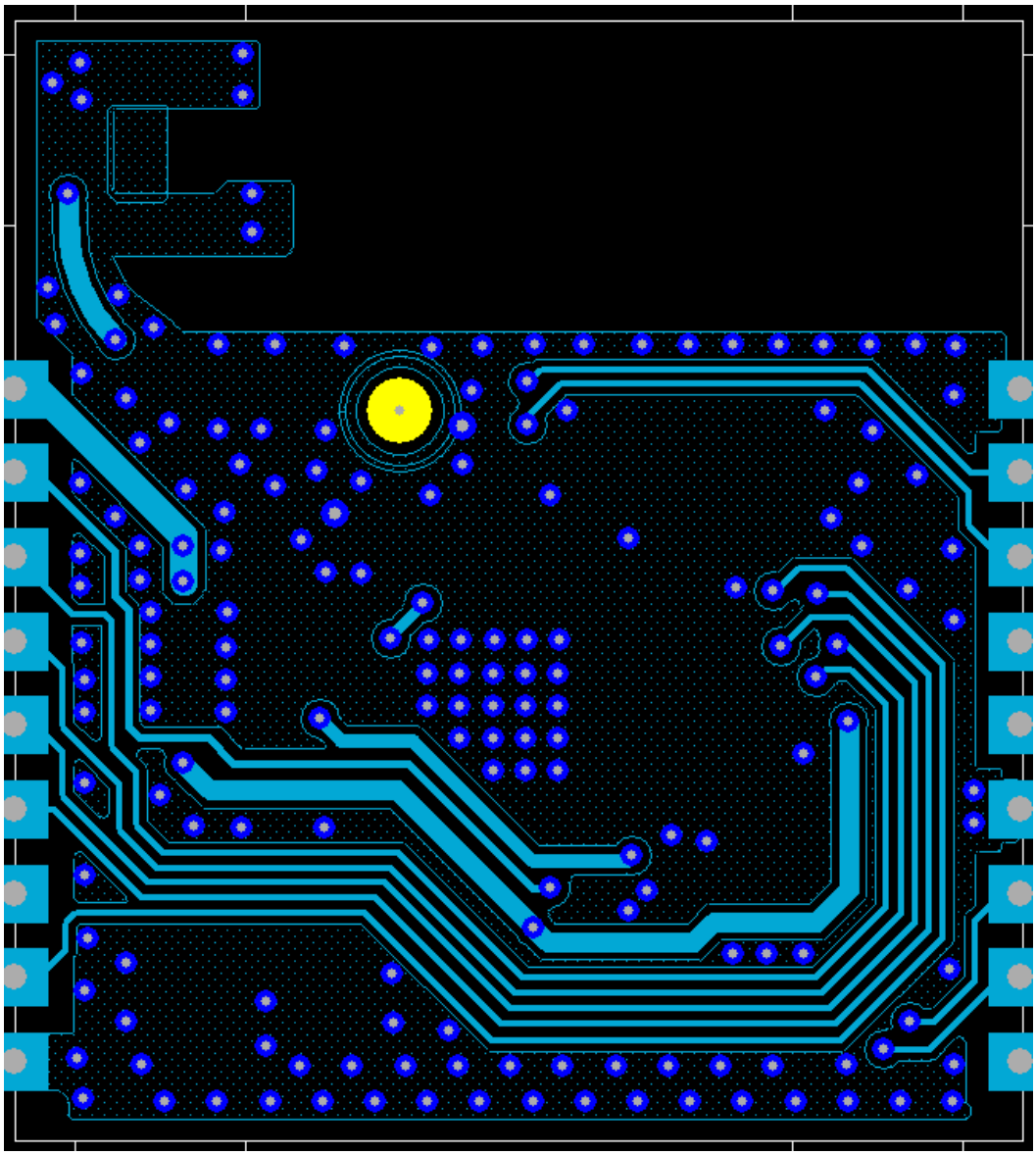


Figure 4-13 EPAD trace routing reference for the 2-layer PCB (bottom layer)



4.10 Strong-Current Interface Design (Optional)

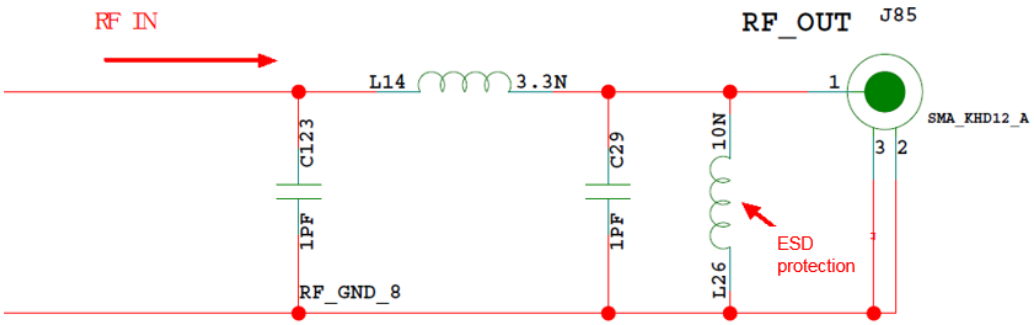
4.10.1 Power Supply Design

None

4.10.2 Security Specifications

Reserve a 10 nH inductor at the position where the RF connects to the antenna to enhance the ESD protection capability (≥ 4 kV). If the ESD protection capability greater than 8 kV is required, add a TVS diode.

Figure 4-14 Reference circuit diagram for ESD protection



5 Thermal Design Recommendations

5.1 Operating Conditions

NOTICE

- The maximum junction temperature of the chip is 125°C, which cannot be exceeded under any condition.
- The maximum long-term operating junction temperature of the chip is 105°C, which cannot be exceeded or equaled in normal working conditions.
- In short-term working conditions, the chip can tolerate a high temperature that is greater than 105°C (maximum long-term operating junction temperature) and less than 125°C (maximum junction temperature). However, if the chip works for a long time at a junction temperature greater than 105°C, the chip lifespan will be shortened.
- According to the GR-63-CORE standard, the short-term working conditions are defined as at most 96 consecutive hours each time and the accumulated duration of at most 15 days each year.

Table 5-1 Junction temperature requirements

Package	Minimum Junction Temperature for Normal Working (°C)	Maximum Junction Temperature for Long-Term Working (°C)	Maximum Junction Temperature for Short-Term Working (°C)	Destructive Maximum Junction Temperature (°C)	Lifecycle Definition
QFN	–40	105	125	125	5 years

Table 5-2 Package thermal resistance

Parameter	Symbol	Hi3861 single-die packaging	Hi3861 multi-die packaging	Unit
Junction-to-ambient thermal resistance	θ_{JA}	59.9	59.1	℃/W
Junction-to-case thermal resistance	θ_{JC}	37.2	35.7	℃/W
Junction-to-top center of case thermal resistance	Ψ_{JT}	-	-	℃/W
Junction-to-board thermal resistance	θ_{JB}	35.4	34.7	℃/W

Note: The thermal resistance is provided based on the JEDEC JESD51-2 standard, while the actual system design and environmental factors may vary according to actual situations.

The preceding package thermal resistance parameters are based on a 4-layer PCB compliant with the JEDEC standard, as shown in **Figure 5-1**.

Figure 5-1 Parameters of the 4-layer PCB compliant with the JEDEC standard

5.2 Reference Design on Heat Dissipation

None

5.3 Reference Design on Circuit Thermal

5.3.1 Component Layout

Based on the product architecture and thermal design, you are advised to lay out components as follows:

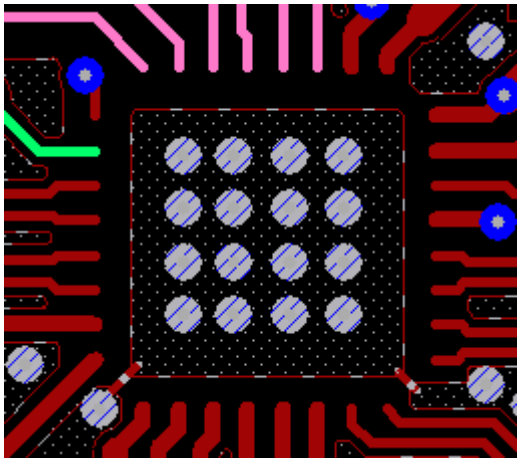
- On the PCB, evenly distribute components that consume high power and easily generate heat to avoid partial overheating, therefore ensuring the component reliability and efficiency.
- Properly design the product architecture to ensure that the internally produced heat can be dissipated.
- Perform temperature rise tests on key heating components of the PCB in extreme application scenarios to ensure that the components work reliably for a long time within a safe temperature range.
- If necessary, add heat sinks to key heating components to improve the heat dissipation effect.

5.3.2 PCB

You are advised to perform thermal design on routing traces as follows:

- Use full connection instead of common thermal connection for the vias under the chip to improve the heat dissipation efficiency of the board.
- Increase the area of the copper sheet right below or around the components with much heat, especially for the components on the double-sided PCB. Minimize the split of the GND plane on the back of the heating component. A complete GND plane can effectively disperse heat and improve the overall heat dissipation effect. In addition, if allowed by the structure, remove the solder mask near the GND plane on the back of the chip to further enhance the heat dissipation effect.

Figure 5-2 Ground hole design for EPAD heat dissipation



6 Soldering Process

6.1 Purpose

[Objective]

Define the zone temperatures for the surface mounting technology (SMT) applied in HiSilicon chips.

[Application Scope]

HiSilicon products

[Basic Information]

All HiSilicon products provided for customers comply with the Restriction of Hazardous Substances (RoHS). In the part number format HixxxxRBCVxxx, the letter **R** stands for RoHS, indicating that all the products are lead-free. The following sections describe the lead-free technology and mixing technology, which are used for process control when customers apply HiSilicon chips in reflow soldering.

[Reflow Chart]

Description:

- HiSilicon chips: All HiSilicon chips are ROHS products and meet lead-free requirements.
- Lead-free technology: All components (mainboards, ICs, capacitors, and resistors) are lead-free and apply lead-free solder paste.

6.2 Parameter Requirements on Lead-Free Reflow Soldering

Figure 6-1 shows the thermal profile of lead-free reflow soldering.

Figure 6-1 Thermal profile of lead-free reflow soldering

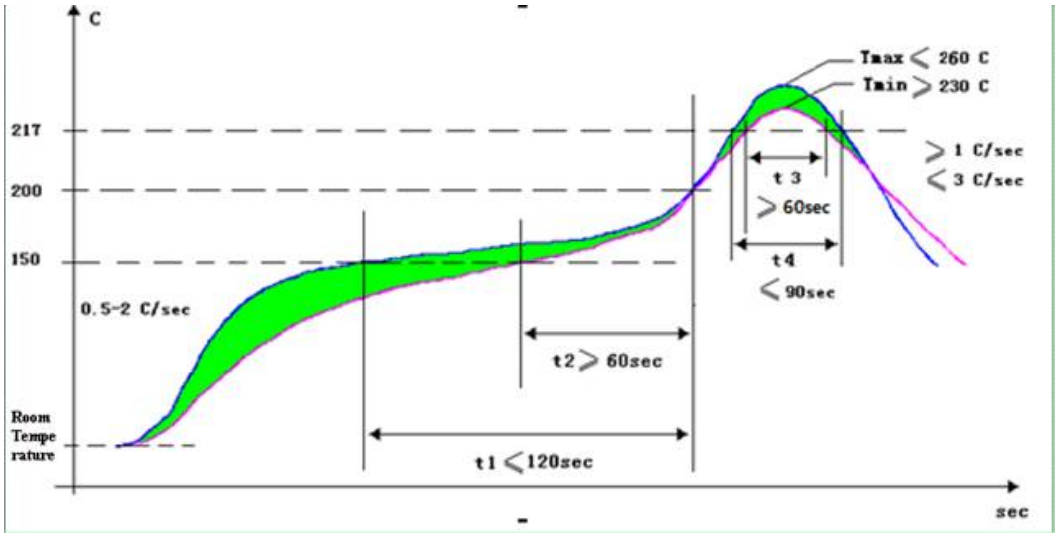


Table 6-1 describes the parameters of lead-free reflow soldering.

Table 6-1 Parameters of lead-free reflow soldering

Zone	Time	Heating Rate	Peak Temperature	Cooling Rate
Preheat zone (40–150°C or 104–302°F)	60–150s	≤ 2.0℃/s	-	-
Soak zone (150–200°C or 302–392°F)	60–120s	< 1.0 °C/s	-	-
Reflow zone (> 217°C or 423°F)	60–90s	-	230–260 °C (446–500°F)	-
Cooling zone (Tmax–180°C or 356°F)	-	-	-	1.0 °C/s ≤ Slope ≤ 4.0 °C/s

Note:

- Preheat zone: The temperate range is 40–150°C (104–302°F), the heating rate must be about 2.0°C/s (36°F/s), and the zone duration must be 60–150s.
- Soak zone: The temperature range is 150–200°C (302–392°F), the heating rate must be less than 1.0°C/s (34°F/s), and the zone duration must be 60–120s. **Slow heating is required; otherwise, soldering is poor.**
- Reflow zone: The zone temperature increases from 217°C (423°F) to Tmax and then decreases to 217°C (423°F) again. The zone duration must be 60–90s.
- Cooling zone: The zone temperature decreases from Tmax to 180°C (356°F). The cooling rate cannot exceed 4.0°C/s (39°F/s).
- It should take no more than 6 minutes for the ambient temperature to increase from 25°C (77°F) to 250°C (482°F).
- The thermal profile shown in the preceding figure provides recommended values. Customers need to adjust the values based on actual production.
- Typically, the duration of the reflow zone is 60–90s. For the boards with great heat capacity, the duration can be prolonged to 120s. For details about the requirements on package thermal resistance, see the IPC/JEDEC J-STD-020D standard. For details about the method of measuring the package temperature, see the JEP 140 standard.

Table 6-2 describes the thermal resistance standard for the lead-free package according to the IPC/JEDEC J-STD-020D standard.

Table 6-2 Thermal resistance standard for the lead-free package

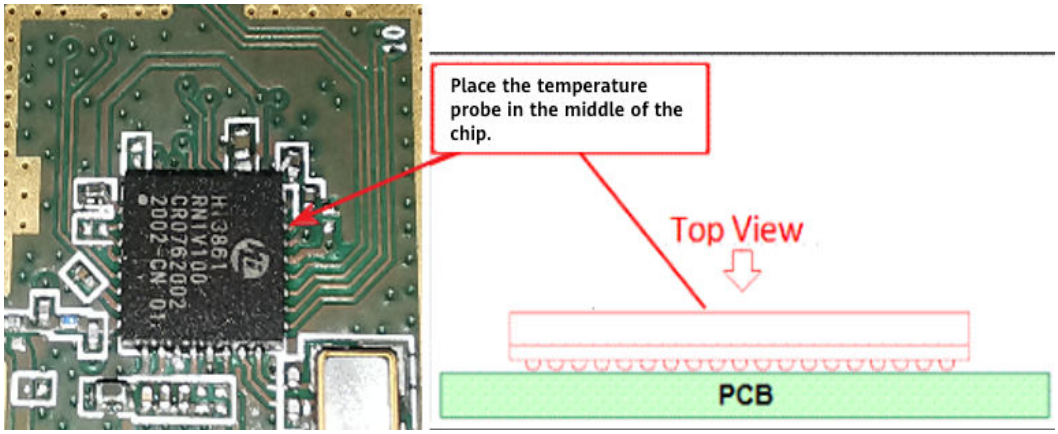
Package Thickness	Volume mm^3 < 350	Volume mm^3 350–2000	Volume mm^3 > 2000
< 1.6 mm	260℃	260℃	260℃
1.6–2.5 mm	260℃	250℃	245℃
> 2.5 mm	250℃	245℃	245℃

The component soldering terminals (such as the solder balls and pins) and external heat sinks are not considered for volume calculation.

The method of measuring the reflow soldering thermal profile is as follows:

According to the JEP140 standard, to measure the package temperature, you are advised to place the temperature probe of the thermocouple close to the chip surface if the chip package is thin, or to drill a hole on the package surface and place the temperature probe of the thermocouple into the hole if the chip package is thick. The second method is recommended based on the thickness of most chip packages. However, this method is not applicable if the chip package is too thin to drill a hole. See **Figure 6-2**.

Figure 6-2 Measuring the package temperature



NOTE

To measure the temperature of the QFP-packaged chip, place the temperature probe close to pins.

6.3 Parameter Requirements on Mixing Reflow Soldering

Lead-free components must be properly soldered if reflow soldering is applied to a mix of SMT and pin-through-hole (PTH) components. Table 6-3 describes the requirements.

Table 6-3 Reflow soldering parameters for a mix of SMT and PTH components

Zone		Lead BGA	Lead-Free BGA	Other Components
Preheat zone (40–150°C or 104–302°F)	Time	60–150s		
	Heating slope	< 2.5℃/s		
Soak zone (150–183°C or 302–361°F)	Time	30–90s		
	Heating slope	< 1.0 °C/s		
Reflow zone (> 183°C or 361°F)	Peak temperature	210–240°C	220–240°C	210–245°C
	Time	30–120s	60–120s	30–120s
Cooling zone (Tmax–150°C or 302°F)	Cooling slope	1.0 °C/s ≤ Slope ≤ 4.0 °C/s		

NOTE

The preceding parameter values are provided based on the soldering joint temperatures. The maximum and minimum soldering joint temperatures for the board must meet the requirements described in the preceding table.

During the adjustment of the thermal profile, the package thermal resistance requirements on the board components must be met. For details about the requirements on package thermal resistance, see the IPC/JEDEC J-STD-020D standard. For details about the method of measuring the package temperature, see the JEP 140 standard.

Table 6-4 describes the thermal resistance standard for the lead package according to the IPC/JEDEC J-STD-020D standard.

Table 6-4 Thermal resistance standard for the lead package

Package Thickness	Volume mm^3 < 350	Volume mm^3 ≥ 350
< 2.5 mm	235℃	220℃
≥ 2.5 mm	220℃	220℃

The component soldering terminals (such as the solder balls and pins) and external heat sinks are not considered for volume calculation.

According to the JEP140 standard, the method of measuring the temperature of the package soldered with the mixing technology is the same as that for measuring the temperature of the package soldered with the lead-free technology. For details, see **6.2 Parameter Requirements on Lead-Free Reflow Soldering**.

7 Moisture-Sensitive Specifications

7.1 Storage and Usage

[Application Scope]

All HiSilicon ICs (moisture-sensitive products)

[Storage Environment]

You are advised to use vacuum packaging and store products at ≤ 30°C (86°F) and 60% RH (relative humidity).

[Shelf Life]

The shelf life is no less than 12 months at ≤ 30°C (86°F) and 60% RH when vacuum packaging is used.

[Floor Life]

Table 7-1 lists the reference table for the floor life at ≤ 30°C/60% RH.

Table 7-1 Reference table for the floor life

Moisture Sensitivity Level (MSL)	Definition (Floor Life and Condition)
1	Unlimited at ≤ 30°C/85% RH
2	1 year, 30°C/60% RH
2a	4 weeks, 30°C/60% RH
3	1 week, 30°C/60% RH
4	72 hours, 30°C/60% RH
5	48 hours, 30°C/60% RH

Moisture Sensitivity Level (MSL)	Definition (Floor Life and Condition)
5a	24 hours, 30°C/60% RH
6	Time on Label, 30°C/60% RH

[Usage of Moisture-Sensitive Products]

- If a chip has been exposed to air for over 2 hours at ≤ 30°C/60% RH, rebake it and pack it into a vacuum bag.
- If a chip has been exposed to air for less than 2 hours at ≤ 30°C/60% RH, rebaking is not required. In this case, replace the desiccant and pack the chip into a vacuum bag.
- The moisture sensitivity level of the product is level 3.

For details about other storage modes and usage rules, see the JEDEC J-STD-033A standard.

7.2 Rebaking

[Applicable Product]

All HiSilicon ICs (moisture-sensitive products)

[Application Scope]

ICs that need to be rebaked (moisture-sensitive products)

[Reference Table for Rebaking]

Table 7-2 Reference table for rebaking

Chip Thickness	MSL	Baking at 125°C	Baking at 90°C/≤ 5% RH	Baking at 40°C/ ≤ 5% RH
≤ 1.4 mm	2a	3h	11h	5day
	3	7h	23h	9day
	4	7h	23h	9day
	5	7h	24h	10day
	5a	10h	24h	10day
≤2.0mm	2a	16h	2day	22day
	3	17h	2day	23day
	4	20h	3day	28day
	5	25h	4day	35day

Chip Thickness	MSL	Baking at 125°C	Baking at 90°C/≤ 5% RH	Baking at 40°C/ ≤ 5% RH
	5a	40h	6day	56day
≤4.5mm	2a	48h	7day	67day
	3	48h	8day	67day
	4	48h	10day	67day
	5	48h	10day	67day
	5a	48h	10day	67day

NOTE

- The preceding table lists the minimum baking time for damp products.
- Preferentially rebake products at low temperature.
- For details, see the JEDEC standard.

8 Interface Timings

8.1 UART Interface Timing

The UART interface of the chip implements the communication between the BFG subsystem and the host and supports the 4-wire protocols (RXD, TXD, CTS, and RTS). RXD and TXD are used for data transmission, and RTS and CTS are used for flow control.

The UART interface supports multiple baud rates. The baud rate is in direct proportion to the transfer rate. The supported baud rate ranges from 9600 bit/s to 4 Mbit/s, and the rate can be configured by configuring registers.

Table 8-1 lists the baud rates and bit error rates (BERs).

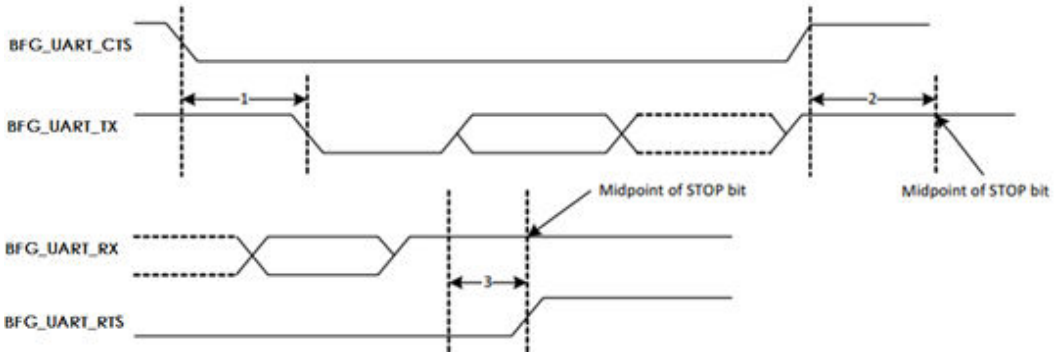
Table 8-1 Baud rates and BERs of the UART interface

Desired Rate	Actual Rate	Error (%)
4000000	4000000	0.00
3000000	3000000	0.00
2000000	2000000	0.00
1500000	1500000	0.00
1444444	1454544	0.70
921600	923077	0.16
460800	461538	0.16

Desired Rate	Actual Rate	Error (%)
230400	230796	0.17
115200	115385	0.16
57600	57692	0.16
38400	38400	0.00
28800	28846	0.16
19200	19220	0.00
14400	14423	0.16
9600	9600	0.00

Figure 8-1 shows the timing of the UART interface.

Figure 8-1 UART interface timing



Note: As marked by dotted lines, the rising edge is based on 0.7 x VDD, and the falling edge is based on 0.3 x VDD. The default VDDIO voltage is 1.8 V.

In the preceding figure:

- **1** indicates the maximum delay from the time when the CTS signal is pulled down to the time when the TXD signal is valid.
- **2** indicates the maximum duration from the midpoint of the stop bit to the time when the CTS signal is pulled up.
- **3** indicates the maximum delay from the midpoint of the stop bit to the time when the RTS signal is pulled up.

Table 8-2 describes the UART timing restrictions.

Table 8-2 UART timing restrictions

Ref No	Characteristics	Min.	Typical	Max.	Unit
1	CTS low to TXD valid	-	-	1.5	Bit period
2	CTS high before mid of stop bit	-	-	0.5	Bit period
3	Mid of stop bit to RTS high	-	-	0.5	Bit period

8.2 I²C Interface Timing

Figure 8-2 shows the I²C interface timing.

Figure 8-2 I²C interface timing

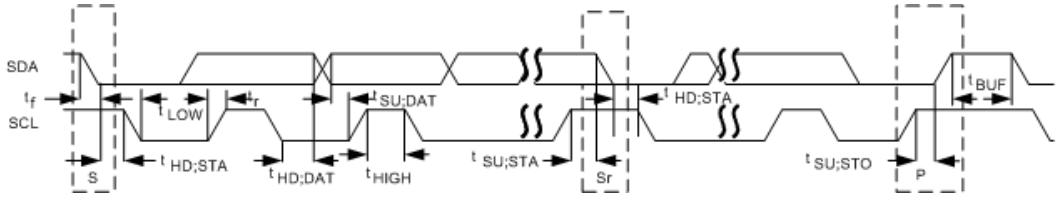


Table 8-3 describes the timing parameters of the I²C interface.

Table 8-3 Timing parameters of the I²C interface

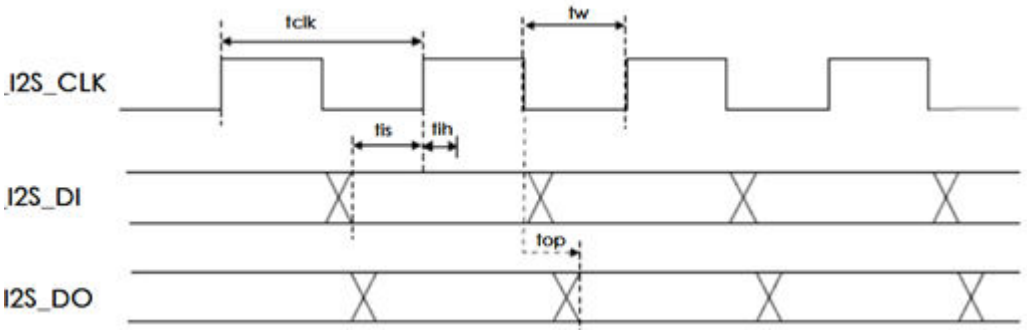
Parameter	Symbol	Standard Mode		Fast Mode		Unit
		Min.	Max.	Min.	Max.	
SCL clock frequency	f_{SCL}	-	100	-	400	kHz
Start hold time	$t_{HD;STA}$	4.0	-	0.6	-	µs
SCL low-level cycle	t_{LOW}	4.7	-	1.3	-	µs
SCL high-level cycle	t_{HIGH}	4.0	-	0.6	-	µs
Start setup time	$t_{SU;STA}$	4.7	-	0.6	-	µs
Data hold time	$t_{HD;DAT}$	0	3.45	0	0.9	µs
Data setup time	$t_{SU;DAT}$	250	-	100	-	ns

Parameter	Symbol	Standard Mode		Fast Mode		Unit
SDA and SCL rising time	t_r	-	1000	$20+0.1C_b$	300	ns
SDA and SCL falling time	t_f	-	300	$20+0.1C_b$	300	ns
End setup time	$t_{SU;STO}$	4.0		0.6	-	μs
Bus release time from start to end	t_{BUF}	4.7		1.3	-	μs
Bus load	C_b	-	400	-	400	pF
Low-level noise tolerance	V_{nL}	$0.1V_{DD}$	-	$0.1V_{DD}$	-	V
High-level noise tolerance	V_{nH}	$0.2V_{DD}$	-	$0.2V_{DD}$	-	V

8.3 I²S Interface Timing

The I²S interface supports the master or slave mode. **Figure 8-3** shows the I²S interface timing.

Figure 8-3 I²S interface timing



Note: As marked by dotted lines, the rising edge is based on 0.7 x VDD, and the falling edge is based on 0.3 x VDD. The default VDDIO voltage is 1.8 V.

In the preceding figure:

- **tclk**: one clock cycle of the I²S interface
- **tw**: duration of the high level or low level of the I²S interface in one clock cycle
- **tis**: setup time of the input signal, that is, the stability time required by the input data before clock sampling

- **tih**: hold time of the input signal, that is, the stability time required by the input data after clock sampling
- **t_{op}**: propagation time of the output signal

Table 8-4 describes the timing restrictions when the I²S acts as the master interface.

Table 8-4 Timing restrictions when the I²S acts as the master interface

Symbol	Parameter	Condition	Min.	Max.	Unit
t_{clk}	Cycle time	-	162	-	ns
t_w	Pulse width	-	$0.5\times t_{clk}-6.26$	$0.5\times t_{clk}+6.26$	
t_{is}	I2S_DI setup time	-	32	-	
t_{ih}	I2S_DI hold time	-	0	-	
t_{op}	I2S_DO propagation time	40 pF load	0	42.6	
t_{op}	I2S_WS propagation time	40 pF load	0	42.6	

Table 8-5 describes the Timing restrictions when the I²S acts as the slave interface.

Table 8-5 Timing restrictions when the I²S acts as the slave interface

Symbol	Parameter	Condition	Min.	Max.	Unit
t_{clk}	Cycle time	-	162	-	ns
t_w	Pulse width	-	$0.35\times t_{CLK}$	$0.65\times t_{CLK}$	
t_{is}	I2S_DI setup time	-	32	-	
t_{ih}	I2S_DI hold time	-	0	-	
t_{is}	I2S_WS setup time	-	32	-	
t_{ih}	I2S_WS hold time	-	0	-	

Symbol	Parameter	Condition	Min.	Max.	Unit
t_{op}	I2S_DO propagation time	40 pF load	0	24.5	

8.4 SDIO Interface Timing

The secure digital input/output (SDIO) interface supports three working modes:

- Default speed mode (DS)
  The maximum frequency of the interface clock is 25 MHz. The interface clock can work in 1-bit or 4-bit mode.
- High speed mode (HS)
  The maximum frequency of the interface clock is 50 MHz.
- SDR25 mode
  The maximum frequency of the interface clock is 50 MHz

DS Mode

The DS mode is the default mode after the SDIO is powered on. To ensure compatibility with various host components, the DS mode requires a low working rate and supports only the 25 MHz clock. **Table 8-6** describes the requirements on the clock.

Table 8-6 Clock parameters in DS mode (VDDIO = 3.3 V)

Parameter	Symbol	Min.	Max.	Unit	Remarks
Clock CLK (All values are referenced to min(V_{IH}) and max(V_{IL}))					
Clock frequency Date Transfer Mode	f_{PP}	-	25	MHz	C_{CARD} ≤ 10 pF
Clock frequency Identification Mode	f_{OD}	-	400	kHz	C_{CARD} ≤ 10 pF
Clock low time	t_{WL}	17	-	ns	C_{CARD} ≤ 10 pF
Clock high time	t_{WH}	17	-	ns	C_{CARD} ≤ 10 pF
Clock rise time	t_{TLH}	-	3	ns	C_{CARD} ≤ 10 pF
Clock fall time	t_{THL}	-	3	ns	C_{CARD} ≤ 10 pF

Table 8-7 Clock parameters in DS mode (VDDIO = 1.8 V)

Parameter	Symbol	Min.	Max.	Unit	Remarks
Clock CLK (All values are referenced to min(V_{IH}) and max(V_{IL}))					
Clock frequency Date Transfer Mode	f_{PP}	-	25	MHz	C_{CARD} ≤ 10 pF
Clock frequency Identification Mode	f_{OD}	-	400	kHz	C_{CARD} ≤ 10 pF
Clock low time	t_{WL}	14	-	ns	C_{CARD} ≤ 10 pF
Clock high time	t_{WH}	14	-	ns	C_{CARD} ≤ 10 pF
Clock rise time	t_{TLH}	-	6	ns	C_{CARD} ≤ 10 pF
Clock fall time	t_{THL}	-	6	ns	C_{CARD} ≤ 10 pF

Figure 8-4 shows the output data timing in DS mode. **tISU** is the setup time, that is, the stability time required by the data of the SDIO interface before clock sampling in this mode. **tIH** is the hold time, that is, the time required by the data of the SDIO interface to retain the original level after clock sampling in this mode.

Figure 8-4 Input timing in DS mode

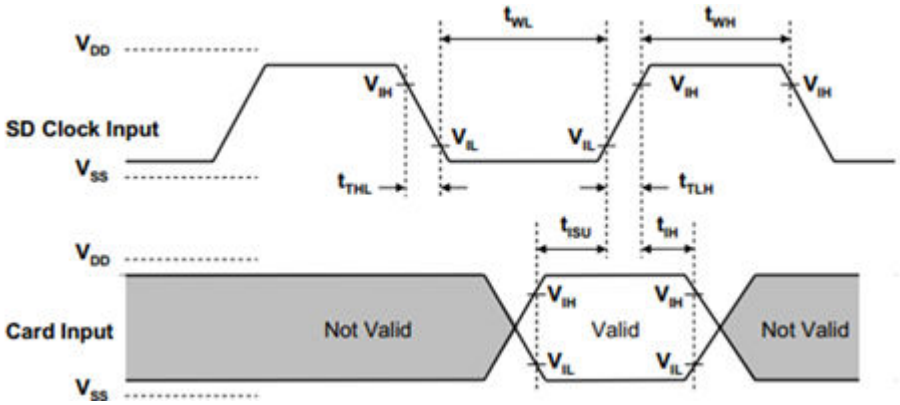


Figure 8-5 shows the input data timing in DS mode. Where, **tODLY(max)** is the maximum delay of the output data relative to the clock falling edge, and **tODLY(min)** is the minimum delay of the output data relative to the clock falling edge.

Figure 8-5 Output timing in DS mode

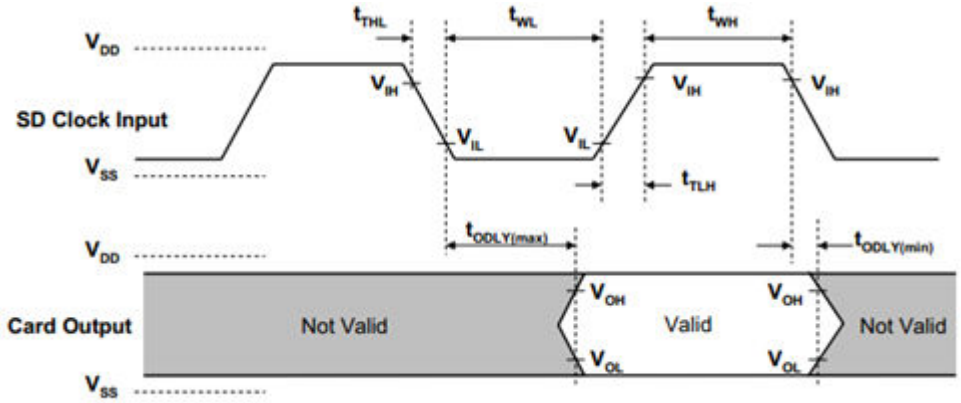


Table 8-8 describes the timing restrictions in DS mode.

Table 8-8 Timing restrictions in DS mode

Parameter	Symbol	Min.	Max.	Unit	Remarks
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3.5	-	ns	$C_{CARD} \leq 10$ pF
Input hold time	t_{IH}	0	-	ns	$C_{CARD} \leq 10$ pF
Outputs CMD, DAT(referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	-	11	ns	$C_L \leq 40$ pF
Output Delay time during Identification Mode	t_{ODLY}	-	11	ns	$C_L \leq 40$ pF

Note: In DS mode, the output data is referenced to the clock falling edge, and the input data is referenced to the clock rising edge.

HS Mode

The HS mode is entered after the SDIO is powered on and initialized because a higher working rate than the DS mode is required. In HS mode, the clock supports 50 MHz. For details about the restrictions on the clock, see Table 8-9.

Table 8-9 Clock parameters in HS mode (VDDIO = 3.3 V)

Parameter	Symbol	Min.	Max.	Unit	Remarks
Clock CLK (All values are referenced to min(V_{IH}) and max(V_{IL}))					
Clock frequency Date Transfer Mode	f_{PP}	-	50	MHz	C_{CARD} ≤ 10 pF
Clock low time	t_{WL}	7	-	ns	C_{CARD} ≤ 10 pF
Clock high time	t_{WH}	7	-	ns	C_{CARD} ≤ 10 pF
Clock rise time	t_{TLH}	-	3	ns	C_{CARD} ≤ 10 pF
Clock fall time	t_{THL}	-	3	ns	C_{CARD} ≤ 10 pF

Table 8-10 Clock parameters in HS mode (VDDIO = 1.8 V)

Parameter	Symbol	Min.	Max.	Unit	Remarks
Clock CLK (All values are referenced to min(V_{IH}) and max(V_{IL}))					
Clock frequency Date Transfer Mode	f_{PP}	-	50	MHz	C_{CARD} ≤ 10 pF
Clock low time	t_{WL}	4	-	ns	C_{CARD} ≤ 10 pF
Clock high time	t_{WH}	4	-	ns	C_{CARD} ≤ 10 pF
Clock rise time	t_{TLH}	-	6	ns	C_{CARD} ≤ 10 pF
Clock fall time	t_{THL}	-	6	ns	C_{CARD} ≤ 10 pF

Figure 8-6 shows the input data timing in HS mode. **tISU** is the setup time, that is, the stability time required by the data of the SDIO interface before clock sampling in this mode. **tIH** is the hold time, that is, the time required by the data of the SDIO interface to retain the original level after clock sampling in this mode.

Figure 8-6 Input timing in HS mode

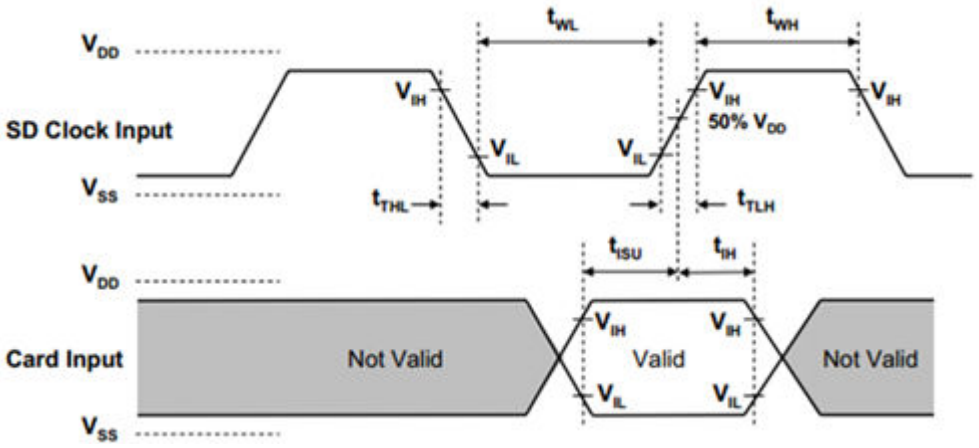


Figure 8-7 shows the input data timing in HS mode. Where, **tODLY(max)** is the maximum delay of the output data relative to the clock rising edge, and **tOH** is the minimum delay of the output data relative to the clock rising edge.

Figure 8-7 Output timing in HS mode

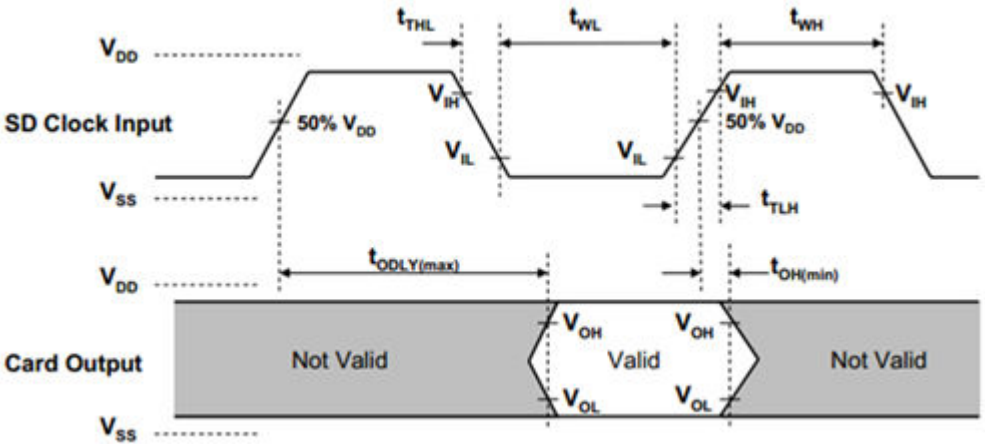


Table 8-11 describes the timing restrictions in HS mode.

Table 8-11 Timing restrictions in HS mode (VDDIO = 3.3 V)

Parameter	Symbol	Min.	Max.	Unit	Remarks
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3.5	-	ns	C_{CARD} ≤ 10 pF
Input hold time	t_{IH}	0	-	ns	C_{CARD} ≤ 10 pF
Outputs CMD, DAT(referenced to CLK)					

Parameter	Symbol	Min.	Max.	Unit	Remarks
Output Delay time during Data Transfer Mode	t_{ODLY}	-	12	ns	$C_L \leq 40$ pF
Output Hold time	t_{OH}	3	-	ns	$C_L \leq 40$ pF
Total System Capacitance for each line	C_L	-	40	pF	1 card

Table 8-12 Timing restrictions in HS mode (VDDIO = 1.8 V)

Parameter	Symbol	Min.	Max.	Unit	Remarks
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3.5	-	ns	$C_{CARD} \leq 10$ pF
Input hold time	t_{IH}	0	-	ns	$C_{CARD} \leq 10$ pF
Outputs CMD, DAT(referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	-	18	ns	$C_L \leq 40$ pF
Output Hold time	t_{OH}	4.5	-	ns	$C_L \leq 40$ pF
Total System Capacitance for each line	C_L	-	40	pF	1 card

Note: The data signal timing in HS mode is different from that in DS mode. The output data and input data are referenced to the clock rising edge.

SDR25 Mode

The SDR25 mode is entered only after the voltage of the SDIO is switched. In this mode, the maximum interface clock frequency is 50 MHz. **Table 8-13** describes the clock restrictions.

Table 8-13 Clock parameters in SDR25 mode (VDDIO = 3.3 V)

Parameter	Symbol	Min.	Max.	Unit	Remarks
Clock CLK (All values are referenced to min(V_{IH}) and max(V_{IL}))					

Parameter	Symbol	Min.	Max.	Unit	Remarks
Clock frequency Date Transfer Mode	f_{PP}	-	50	MHz	C_{CARD} ≤ 10 pF
Clock low time	t_{WL}	7	-	ns	C_{CARD} ≤ 10 pF
Clock high time	t_{WH}	7	-	ns	C_{CARD} ≤ 10 pF
Clock rise time	t_{TLH}	-	3	ns	C_{CARD} ≤ 10 pF
Clock fall time	t_{THL}	-	3	ns	C_{CARD} ≤ 10 pF

Table 8-14 Clock parameters in SDR25 mode (VDDIO = 1.8 V)

Parameter	Symbol	Min.	Max.	Unit	Remarks
Clock CLK (All values are referenced to min(V_{IH}) and max(V_{IL}))					
Clock frequency Date Transfer Mode	f_{PP}	-	50	MHz	C_{CARD} ≤ 10 pF
Clock low time	t_{WL}	4	-	ns	C_{CARD} ≤ 10 pF
Clock high time	t_{WH}	4	-	ns	C_{CARD} ≤ 10 pF
Clock rise time	t_{TLH}	-	6	ns	C_{CARD} ≤ 10 pF
Clock fall time	t_{THL}	-	6	ns	C_{CARD} ≤ 10 pF

Table 8-15 Timing restrictions in SDR25 mode (VDDIO = 3.3 V)

Parameter	Symbol	Min.	Max.	Unit	Remarks
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3.5	-	ns	C_{CARD} ≤ 10 pF
Input hold time	t_{IH}	0	-	ns	C_{CARD} ≤ 10 pF
Outputs CMD, DAT(referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	-	12	ns	C_L≤10pF
Output Hold time	t_{OH}	3	-	ns	C_L≤5pF

Parameter	Symbol	Min.	Max.	Unit	Remarks
Total System Capacitance for each line	C_L	-	40	pF	1 card

Table 8-16 Timing restrictions in SDR25 mode (VDDIO = 1.8 V)

Parameter	Symbol	Min.	Max.	Unit	Remarks
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3.5	-	ns	$C_{CARD} \leq 10$ pF
Input hold time	t_{IH}	0	-	ns	$C_{CARD} \leq 10$ pF
Outputs CMD, DAT(referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	-	18	ns	$C_L \leq 10$pF
Output Hold time	t_{OH}	4.5	-	ns	$C_L \leq 5$pF
Total System Capacitance for each line	C_L	-	40	pF	1 card

8.5 SPI Interface Timing

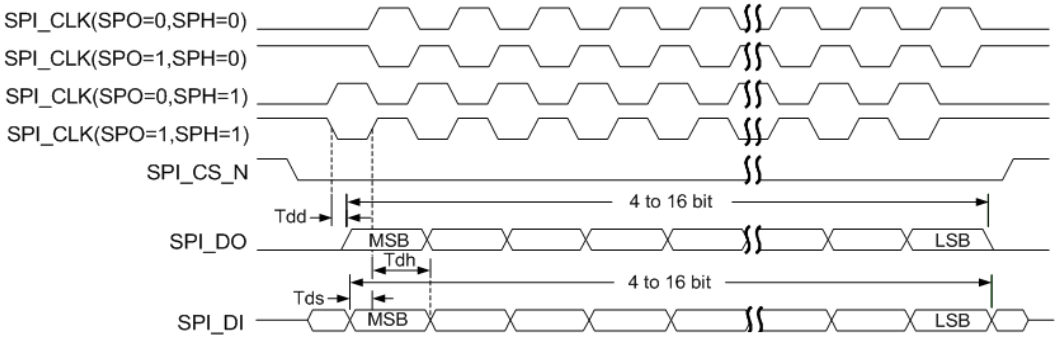
NOTE

Acronyms and Abbreviations:

- MSB: most significant bit
- LSB: least significant bit
- SPI_CK(0): spo = 0
- SPI_CK(1): spo = 1

Figure 8-8 shows the clock timing of the serial peripheral interface (SPI).

Figure 8-8 SPI interface timing



Note: When the SPI is used as the master interface, the minimum clock cycle is 80 ns. When the SPI is used as the slave interface, the minimum clock cycle is 80 ns.

SPO represents the SPICLKOUT polarity and SPH represents the SPICLKOUT phase.

Table 8-17 Timing parameters of the SPI interface

Parameter	Symbol	Min.	Max.	Unit
Output data delay	T_{dd}	3.5	17.5	ns
Setup time of the input control signal (master)	T_{ds}	4	-	ns
Hold time of the input control signal (master)	T_{dh}	1.6	-	ns
Setup time of the input control signal (slave)	T_{ds}	4	-	ns
Hold time of the input control signal (slave)	T_{dh}	1	-	ns

9 Precautions

9.1 Hardware Design

Pay attention to the following points during hardware design:

- When the hardware configuration words and power-on pins are used, external pull-up and pull-down resistors are required. To meet the low-power design requirements, 100-kilohm resistors are recommended.
- The Hi3861/Hi3861L/Hi3881 reference design board has passed the test on Wi-Fi RF specifications such as the transmit EVM, receive sensitivity, and authentication. Do not change the capacitance and position of the decoupling capacitors for the Hi3861, Hi3861L, and Hi3881 chips. If the capacitance and position must be changed, perform detailed tests on the mentioned Wi-Fi RF specifications.
- Do not change the π-shaped LC low-pass filter on the RF link. Pay special attention to the handling of the ground pad and ground hole of the ground capacitor.
- You are advised to add a grounded ESD RF inductor (10 nH) to the RF link and place the inductor close to the antenna.
- The reference design and component selection provided by HiSilicon are mainly based on lab and sample tests. During mass production design-in, you are advised to perform comprehensive product hardware testing and evaluation.

9.2 PCB Manufacturing Process

Pay attention to the following points during the PCB manufacturing process:

- Perform depaneling by using machines. Manual depaneling is prohibited.
- Before manual soldering, take ESD measures, for example, wear ESD bracelets.

- Recommended conditions for PCB storage:
  - Organic solderability preservative (OSP) PCB

    Storage conditions before and after vacuum packaging: The temperature range is 20°–30°C (68–86°F) and the relative humidity is 50%. The lifespan of a PCB in vacuum packaging ranges from three months to one year. If the storage duration exceeds six months, the PCB can be assembled after being unpacked. To prevent the PCB from being damaged due to moisture, you can bake the PCB. The baking temperature ranges from 110–120°C (230–248°F) and the baking lasts for about 1 hour (less than 1.5 hours).
  - Tin-coated PCB

    Storage conditions before and after vacuum packaging: The temperature is 25°C (77°F) and the relative humidity is 60%. The lifespan of a PCB in vacuum packaging is one year. If the storage duration exceeds six months, the PCB can be assembled after being unpacked. To prevent the PCB from being damaged due to moisture, you can bake the PCB. The baking temperature is 120°C (248°F) and the baking lasts for about 1 hour (less than 1.5 hours).