Hi3861 V100 / Hi3861L V100 Hardware Design

Checklist

Issue 01

Date 2020-04-30

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About This Document

Purpose

This document describes the checklist for the Hi3861 V100/Hi3861L V100 hardware board design, providing guidance for users to check the design during chip-based hardware board development.

Related Versions

The following table lists the product versions related to this document.

Product Name	Version
Hi3861	V100
Hi3861L	V100

Intended Audience

The document is intended for:

- PCB hardware development engineers
- Technical support engineers

Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description
DANGER	Indicates a hazard with a high level of risk which, if not avoided, will result in death or serious injury.
WARNING	Indicates a hazard with a medium level of risk which, if not avoided, could result in death or serious injury.

Symbol	Description
⚠ CAUTION	Indicates a hazard with a low level of risk which, if not avoided, could result in minor or moderate injury.
NOTICE	Indicates a potentially hazardous situation which, if not avoided, could result in equipment damage, data loss, performance deterioration, or unanticipated results. NOTICE is used to address practices not related to personal injury.
🕮 NOTE	Supplements the important information in the main text. NOTE is used to address information not related to personal injury, equipment damage, and environment deterioration.

Change History

Issue	Date	Change Description
01	2020-04-30	This issue is the first official release. • In **1 Schematic Diagram Design Checklist**, the specifications of the power supply (No.5), digital I/O (No.9), and others (No.15 and No. 16) is updated. • In **2 PCB Design Checklist**, the specifications of the digital I/O (No.2), crystals (No.12 and No.14), RF (No.16), integrated product and shielding cover (No.24 and No.26) are updated. The RF (No. 22) specifications are added.
00B04	2020-04-15	In **1 Schematic Diagram Design Checklist**, the crystal specifications when the PCB space is small are added.
00B03	2020-03-25	In **2 PCB Design Checklist**, the specifications of the digital I/Os (No. 2 and No. 5), power supplies (No. 10 and No. 14), RF (No. 21), integrated product and shielding cover (No. 28) are updated.
00B02	2020-02-12	In **2 PCB Design Checklist**, the description of the spacing between the shielding covers of the 5G RF circuit is deleted.
00B01	2020-01-15	This issue is the first draft release.

Contents

1 Schematic Diagram Design Checklist

Category	Subcategory	No.	Rule Details	Level		Result
				Rule	Suggestion	
Schematic Diagram	Crystal	1	For a selected crystal, the frequency offset must be less than ±10 ppm.	√		
		2	During crystal debugging, ask the supplier to provide a 0 ppm crystal sample. In this case, determine the load capacitors at both ends of the crystal in the R&D phase at room temperature 25°C. The load capacitors should be 0 ppm. An offset of –5 ppm is recommended.	√		
		3	If the PCB space is small (for example, the 12 mm x 12 mm module is used and the single-sided mounting solution is used), it is recommended that a 0-ohm resistor be connected in series to the XIN of the crystal to prevent external interference from affecting the system master clock.	√	√	
	Power supply	4	The chip supports the low-power BUCK mode and low-cost LDO mode. The mode selection is determined by the hardware configuration word **VDD_PMU_LX**. Pulling up to VBAT uses the low-cost LDO mode, and no inductor is required. Otherwise, the BUCK low-power mode is used.	√		
		5	In low-power buck mode, inductance = 2.2 µH, direct current resistance (Rdc) ≤ 0.1 ohms, saturation current ≥ 800 mA, output capacitor = 4.7 µF, rated voltage of the capacitor = 6.3 V (recommended)	√		

	Digital I/O	6	The debugging serial ports GPIO_03 and GPIO_04 are used by default on both hardware and software. You are advised not to use GPIO_13 and GPIO_14 as the debugging serial ports.	√		
		7	The chip has 15 GPIO pins. For details about the multiplexing of each GPIO pin, see the *Hi3861 V100/Hi3861L V100/Hi3881 V100 Wi-Fi Chip Hardware User Guide*.	√		
		8	The chip has four hardware configuration words: • Pin 4/REFCLK_FREQ_STATUS: working mode of the master clock 0: 40 MHz clock (default) 1: 24 MHz clock. • Pin 20/JTAG_ENABLE: JTAG mode enable 0: normal I/O mode (default) 1: JTAG enable • Pin 18/JTAG_MODE: JTAG mode 0: normal mode (default) 1: design for testability (DFT) mode • Pin 25/VDD_PMU_LX: switchover between the BUCK mode and LDO mode 0: BUCK (default) 1: LDO	√		
		9	If high level needs to be set, pin 25/VDD_PMU_LX can be directly pulled up to VBAT, and the other three pins must be pulled up to VDDIO through 4.7-kilohm resistors.	√		
		10	In UDSLEEP (ultra-deep sleep) mode, the chip can only be woken up by four I/O pins (GPIO03, GPIO05, GPIO07, and GPIO14) on the rising edge.	√	√	
	RF	11	The RF cable must be routed far away from the crystal (reference value > 5 mm).	√		
		12	The RF cable must be routed far away from strong interference such as DDR and CPU interference.	√		
		13	The RF test base is designed for compatibility. Whether to solder the RF test base depends on the user environment.	√		
		14	It is recommended that an ESD inductor (10 nH) be reserved close to the antenna on the RF link.	√	√	

	Others	15	To ensure that the chip can be normally initialized after power-on, you are advised to take the following measures: • Add an RC delay circuit (R = 100 kilohms, C = 100 nF) to the power-on pin in the module. If the internal space of the module is insufficient, you are advised to add the RC delay circuit on the EN signal of the peer microcontroller unit (MCU). • Pull up the power-on pin to VDDIO.	√	√	
		16	To prevent the impact of the external high-power equipment with motor on the UART port, reserve a grounding capacitor on the TRX signal cable of the UART port. The specific capacitance is determined by the surge of the high-power equipment at the peer end and the debugging result.	√	√	

2 PCB Design Checklist

Category	Subcategory	No.	Rule Details	Level		Result
				Rule	Suggestion	
PCB	Digital I/O	1	The lengths of CLK and data traces of the SDIO interface should be less than 5000 mils on the PCB.	√		
		2	Reserve matching resistors for the CLK and data traces of the SDIO interface. If space is sufficient, it is recommended that each trace be routed together with a GND trace.	√		
		3	Place a matching resistor of the SDIO interface based on the source-end matching principle. The closer the CLK series resistor is to the host component, the better. Place the data series resistor as close as possible to the connected host component.	√		
		4	The chip has 15 GPIO pins. The I/O overshoot must be less than 4.1 V. If not, a matching resistor is required.	√		
	Power supply	5	The BUCK energy storage inductor (especially the winding inductor) should be as far away from the antenna as possible (reference value > 10 mm).	√		

		6	The input and output traces of the BUCK energy storage inductor must be as short and thick as possible. Place the inductor and output capacitor close to the chip pin. The GND loop from the inductor and capacitor to the chip EPAD must be as short as possible.	√		
		7	Place the filter capacitor close to the filter network to avoid the inductance effect caused by long traces.	√		
		8	The component must be grounded through a nearby GND via instead of a long thin cable (except the via filter).	√		
		9	Place the decoupling capacitors for the power supply of the transceiver or power amplifier (PA) close to the pins. The smaller the capacitance, the closer to the pins. X7R materials are recommended.	√		
		10	It is recommended that the 1P2 trace for the RFLDO (pin 12 of the chip) to supply power to the LNA (pin 7 of the chip) be routed to the inner layer or bottom layer, and then be connected to the pin near the power pin of the LNA.	√	√	
		11	If possible, it is recommended that the VBAT power trace be routed together with GND traces on both sides.	√	√	
	Crystal	12	Keep the crystal far away from the antenna and PCB edge. (A distance of greater than 10 mm is recommended if space conditions permit.)	√		
		13	Keep the clock (MHz) and high-speed data cable away from the antenna (reference value > 5 mm).	√		
		14	Place the crystal far away from heat sources such as the PA.	√		
		15	The XIN/XOUT and 32 kHz crystal signal traces must be routed together with GND traces.	√		
	RF	16	The signal traces must be as far away from the RF port as possible and be routed together with GND traces.	√		
		17	Ensure that GND under the RF transceiver (pin 8 of the chip) is complete. The GND pad needs to be connected to the nearest main GND.	√		
		18	Ensure that the RF traces are routed by referring to the GND plane. Cross routing is not allowed.	√		

		19	For large-pad components such as the RF connector, the adjacent-layer GND of the pin corresponding to the RF signal must be void (except for the 2-layer PCB) to avoid parasitic capacitance effect. The RF signal is coupled to GND.	√		
		20	The impedance of the RF traces must be 50 ohms. Ensure that the traces are routed smoothly without sharp or right angles. In addition, punch a row of GND vias on both sides of the traces.	√		
		21	Punch a circle of GND vias around the hole through which the RF trace crosses layers, to form a coaxial-like structure.	√		
		22	If the RF components are compactly arranged, the two vias of the RF ground capacitor are close to each other, which affects the harmonic suppression performance of the RF. It is recommended that the two ground capacitors be located on both sides of the RF trace to improve the harmonic suppression effect of the RF circuit. For a multi-layer PCB, ensure that the GND via of the ground capacitor is punched to the bottom layer and then grounded. Do not punch the GND via at the corresponding position at other layers.	√		
		23	The IPEX connectors must be connected to GND and GND vias at the top layer and bottom layer.	√		
	Integrated product and shielding cover	24	It is recommended that the ground of the master chip EPAD at the top layer be connected to the surrounding ground by using a 4-mil trace.	√		
		25	Punch VSS vias around the layer-crossing positions of the high-speed signal interface traces (such as the SDIO).	√		
		26	A complete GND plane should be reserved for the integrated product to ensure that the signals of all chips share the GND and return current properly, to optimize the GND vias and avoid isolated copper sheets.	√		
		27	Punch GND vias around the PCB. Ensure that the GND of each layer is properly connected. It is recommended that two rows of GND vias be punched close to the pad of the shielding cover (that is, the first row of GND vias and the second row of GND vias are punched in a staggered manner). The distance between GND vias must be less than 1/50 wavelength.	√	√	

		28	The shielding cover must have the minimum openings. It is recommended that only one opening be used for RF traces. Other interface signal traces and power traces can be routed to the inner layer or bottom layer through vias and then connected to the module pins.	√		
		29	The spacing between the openings of the shielding frame must be less than 1/20 wavelengths. For the 2.4 GHz network gateway, the recommended spacing is less than 3 mm.	√		
		30	Ensure that the shielding frame is properly grounded. Punch at least three ground vias around each ground pad to connect to the main ground through the nearest path.	√		
	Heat dissipation	31	For a 2-layer PCB, it is recommended that more GND vias be punched on the EPAD of the master chip as long as the process technology requirements are met.	√		