Hi3861 V100 / Hi3861L V100 Board Key Components

Compatibility List

Issue 01

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About This Document

Purpose

This document describes the recommended parameters and selection guide for the key components of Hi3861 V100/Hi3861L V100.

Related Versions

The following table lists the product versions related to this document.

Product Name	Version
Hi3861	V100
Hi3861L	V100

Intended Audience

This document is intended for hardware development engineers, who are expected to have necessary skills in:

- Hardware board development
- Component selection

Change History

Issue	Date	Change Description
01	2020-04-30	This issue is the first official release. • In **1.1 Power Components**, the component description is updated. • In **1.2.1 Master Clock**, the recommended restrictions, components, and descriptions of the 40 MHz crystal and 24 MHz crystal are updated. • In **1.2.2 Real-Time Clock (RTC)**, the recommended restrictions, components, and descriptions of the 32.768 kHz crystal oscillator and 32.768 kHz crystal are updated. • In **1.3 ESD Components**, the recommended restrictions, components, and descriptions of the surface-mounted inductor and TVS diode are updated.
00B02	2020-02-12	• In **1.1 Power Components**, the component description is updated. • In **1.2.1 Master Clock**, the description of the ambient temperature that needs to be considered during crystal selection is added. • In **1.2.2 Real-Time Clock (RTC)**, the description of the 32.768 kHz crystal oscillator is deleted.
00B01	2020-01-15	This issue is the first draft release.

Contents

1 Classification of Key Components

Key components are classified into the following types based on their functions:

- Power components
- Clock components
- ESD protection components

1.1 Power Components

Component Type	Recommended Constraints	Recommended Components (Vendors/ Package)	Description
Buck inductor	• Inductance: 2.2 µH, ±20% • DC resistance (Rdc) ≤ 0.1 ohm • Saturation current: ≥ 0.8 A	• PCFE25201B-2R2MS (DELTA/2520) • 1239AS-H-2R2N=P2 (TOKO/2520) • WPN201610U2R2MTY01 (SUNLORD/2016)	Rdc can be greater than 0.1 ohm but cannot be greater than 0.2 ohm. If Rdc increases, the power consumption increases and the efficiency decreases. When Rdc increases from 0.1 ohm to 0.2 ohm, the heavy-load efficiency decreases by 1% to 2%.

1.2 Clock Components

1.2.1 Master Clock

Component Type	Recommended Constraints	Recommended Components (Vendors/Package/Temperature)	Description
40 MHz crystal	• Clock frequency = 24 or 40 MHz • Frequency tolerance ≤ ± 10 ppm • Temperature drift ≤ 15 ppm (–30°C to +85°C) • Temperature drift ≤ 25 ppm (–30°C to +105°C) • Serial resistance Rs = 40 ohms (typical value), 45 ohms (maximum value) • Load capacitance CL = 11 pF (typical value), 15 pF (maximum value) • DL = 100 µW (typical value), 200 µW (maximum value)	• E3SB40.0000F15G11 (HOSONIC/3225/Normal temperature) • 1C340000ZZ0D (KDS/3225/normal temperature) • 8Z40000056 (TXC/2520/normal temperature) • E3SB40E006400E (HOSONIC/3225/high temperature) • X3S040000BF1HB-Z (HARMONY ELECTRONICS CORP/3225/high temperature)	• Currently, the 3225 package is more cost-effective. As long as the space is sufficient, the 3225 package is recommended, superior to the 2520 package. • Vibration start condition: Rs x CL x CL < 9000. • The supplier needs to provide 0 ppm and ±10 ppm crystal samples. Use the 0 ppm crystal sample for debugging to ensure that the frequency offset after debugging is within –5 ppm to 0 ppm. Use the ±10 ppm crystal samples on the debugged circuit to verify that the maximum frequency offset is within ±20 ppm. • When the upper temperature limit is 85°C, a room-temperature crystal should be used. The frequency offset range is calculated as follows: Temperature drift + Frequency error ≤ ±25 ppm. • When the upper temperature limit is 105°C, a high-temperature crystal should be used. The frequency offset range

Component Type	Recommended Constraints	Recommended Components (Vendors/Package/Temperature)	Description
24 MHz crystal		• 1C224000AZ0A (KDS/3225/normal temperature)	is calculated as follows: Temperature drift + Frequency error ≤ ±35 ppm. The frequency offset can be adjusted to be within ±25 ppm through frequency offset compensation.

1.2.2 Real-Time Clock (RTC)

Component Type	Recommended Constraints	Recommended Components (Vendors)	Description
32.768 kHz crystal	• Clock frequency: 32.768 kHz • Load capacitor: 12.5 pF (typical value) • Frequency tolerance: ± 50 ppm • Temperature drift: ≤ 400 ppm • Series resistance Rs: ≤ 70 kilohms • Drive level (DL): ≥ 0.5 µW	• ETST003275700E (HOSONIC) • Q13FC1350000400 (Epson)	• According to the simulation result, the parasitic capacitance of the two pads of RTC-GPIO is about 2–5 pF, and the typical value is 2.7 pF. • The load capacitance on the PCB (C_pcb) depends on the CL value of the selected crystal. The calculation method is as follows: C_pcb = CL x 2 – C_pin. **C_pin** is the parasitic capacitor inside the I/O. Therefore, if the CL value is 12.5 pF, the recommended capacitance of the PCB is 22.3 pF (12.5 x 2 – 2.7), and 22 pF can be used. • The frequency offset within the operating range includes the nominal frequency tolerance at 25°C and the temperature drift (within the operating temperature range).

Component Type	Recommended Constraints	Recommended Components (Vendors)	Description
32.768 kHz crystal oscillator	• Clock frequency: 32.768 kHz • Frequency tolerance: ± 50 ppm • Temperature drift: ≤ 150 ppm • Duty cycle: 45% to 55% • Low level: 0–0.4 V • High level: (VDDIO – 0.4) to VDDIO • Clock jitter: ±10000 ppm	SG-3030CM (Epson)	-

1.3 ESD Components

Component Type	Recommended Constraints	Recommended Components (Vendors)	Description
Surface-mount inductor	• Package: 0201 or 0402 • Inductance: 10 nH • Error: ≤ ±5% • Frequency: ≥ 6 GHz	N/A	• Place the inductor close to the antenna end. Select the package (0402 or 0201) as required. • The use of 12 nH, 10 nH, and 8.2 nH can improve the ESD protection capability. As the inductance decreases, the ESD protection capability increases. However, the insertion loss increases and the RF output power decreases. A 10 nH inductor is recommended to improve the ESD protection capability to at least 4 kV. • After the ESD protection inductor is added, slightly adjust S11 of the RF circuit to increase or decrease the value of the series inductor. Ensure that S11 is less than or equal to 15 dB. Otherwise, the EVM deteriorates and the insertion loss increases.

Component Type	Recommended Constraints	Recommended Components (Vendors)	Description
TVS diode	• 10 V ≤ Breakdown voltage VBR ≤ 15 V (output power ≥ 20 dBm) • Package: 0201 or 0402 • Junction capacitance ≤ 0.35 pF	N/A	• Place the TVS diode close to the antenna end. Select the package (0402 or 0201) based on the actual situation. Currently, the 0402 package is the mainstream choice and its component price slightly lower than that of the 0201 package, but still higher than that of inductors. • The contact discharge ESD protection capability of the TVS diode can be greater than 8 kV. • The larger the junction capacitance, the larger the signal attenuation. When the output power requirement is met, you can increase the junction capacitance to 0.5 pF to expand the selection range.