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Actian

vectorwise

Actian Corporation Introduction

VectorWise Analytical Database Platform

October 2011

Presentation Outline

- Company Overview
- Ingres VectorWise Database Platforms
- Market and Industry Trends
- VectorWise Overview
  - VectorWise Architecture
  - VectorWise Performance Processing Architecture (VP^{2}A)
- Q & A

Corporate Overview:
Introduction Actian Corporation

- Global Company
  - Over 10,000 customers in 58 countries
  - Major offices in six countries
  - Mission critical 24x7 support

- Strong business
  - 3 Major Product Lines
  - Profitable and generating cash
  - Innovator in technology and business model

- Leader in Action Apps
  - Taking Action on Big Data
  - First to unveil cloud platform for delivering Action Apps

Corporate Overview:
Actian Product and Services Portfolio

Taking Action on Big Data

Ingres

- World class mission critical RDBMS
- CREDIBILITY, RELIABILITY, GLOBAL

Vectorwise

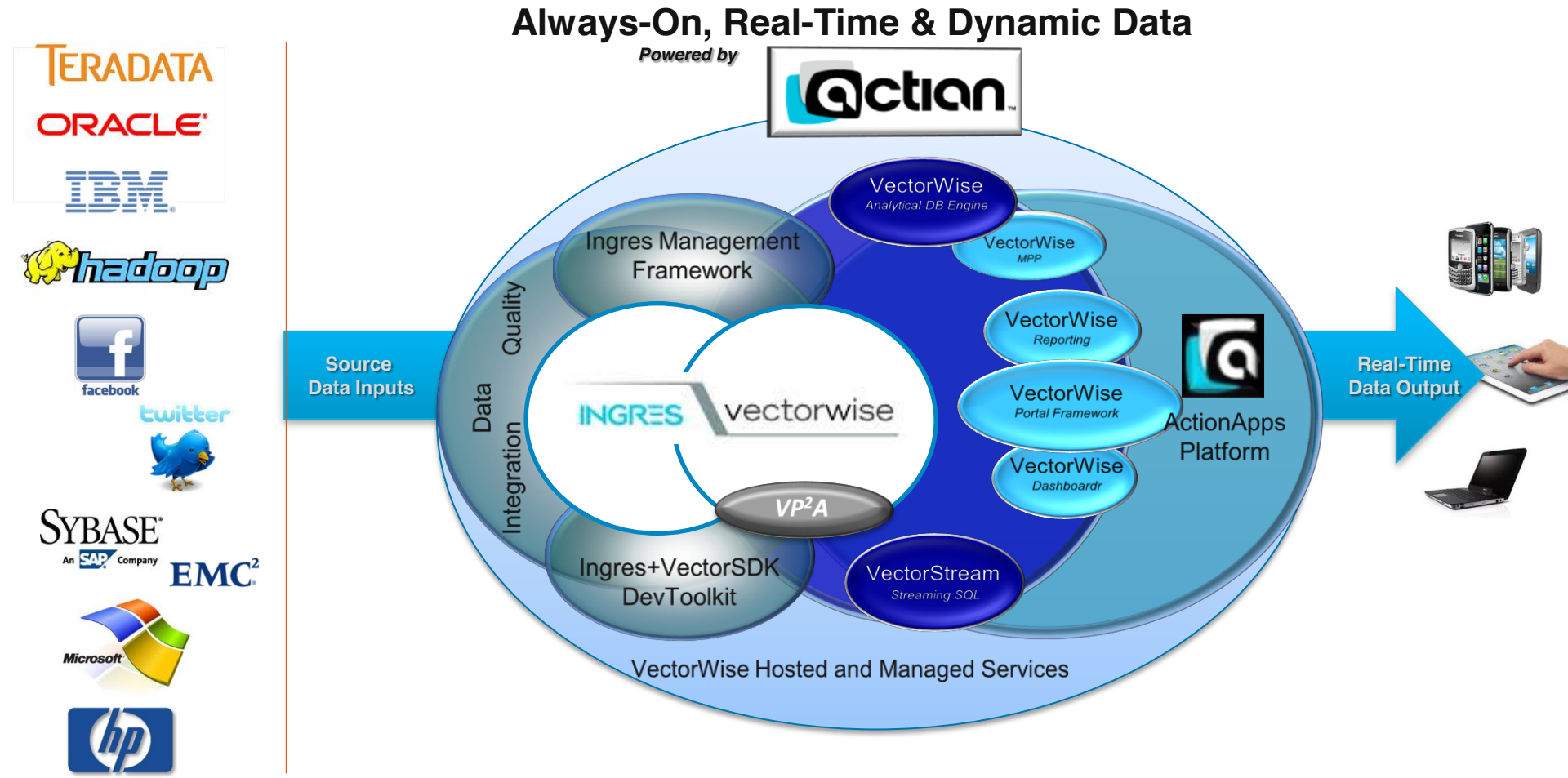
- World's fastest Big Data Analytics engine
- Always On, Real-Time and Dynamic
- PROVEN INNOVATION

Action Apps

- Turning the $2Tn opportunity into reality
- LEADERSHIP

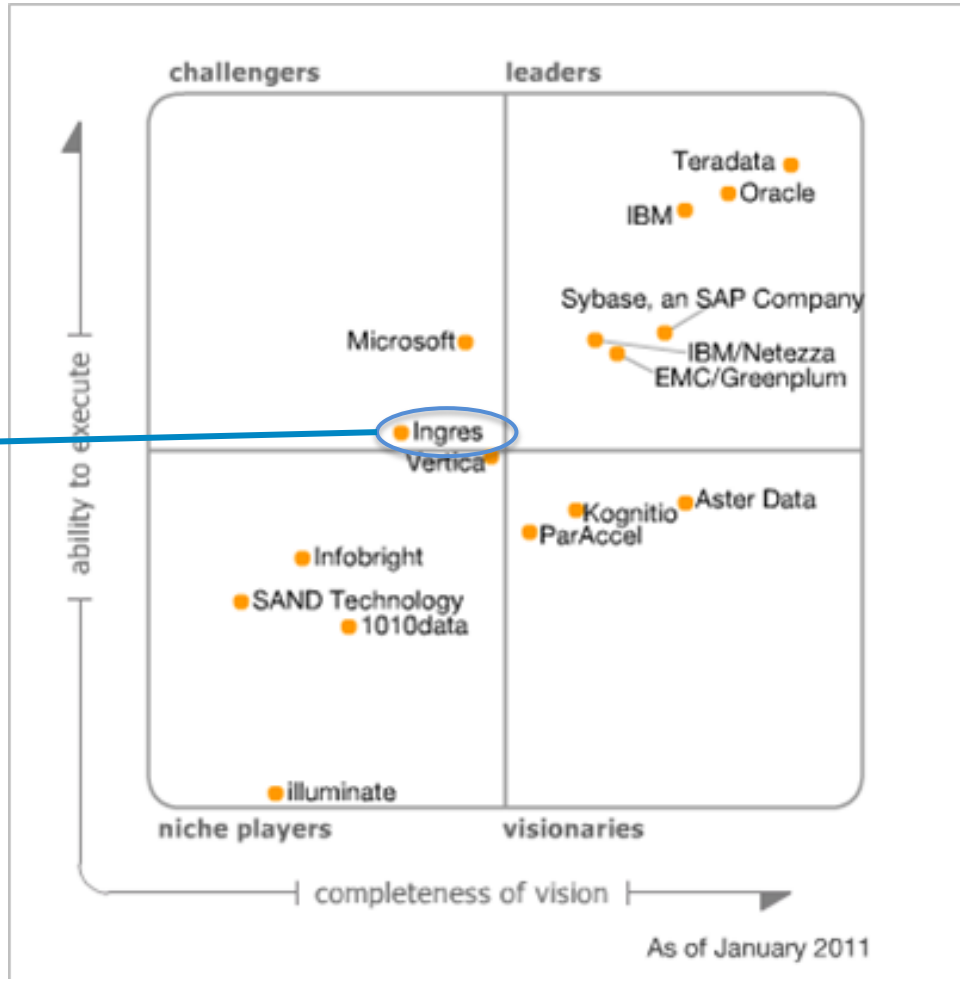
Actian Corporation

Ingres, VectorWise and Action App Platforms



Corporate Overview:
Actian 'Challenger' in 2011 Gartner Magic Quadrant

formerly INGRES



Highlight…..The World of Data is Changing…

Emergence of 'Big Data'-Infrastructure & Management Needs to Change

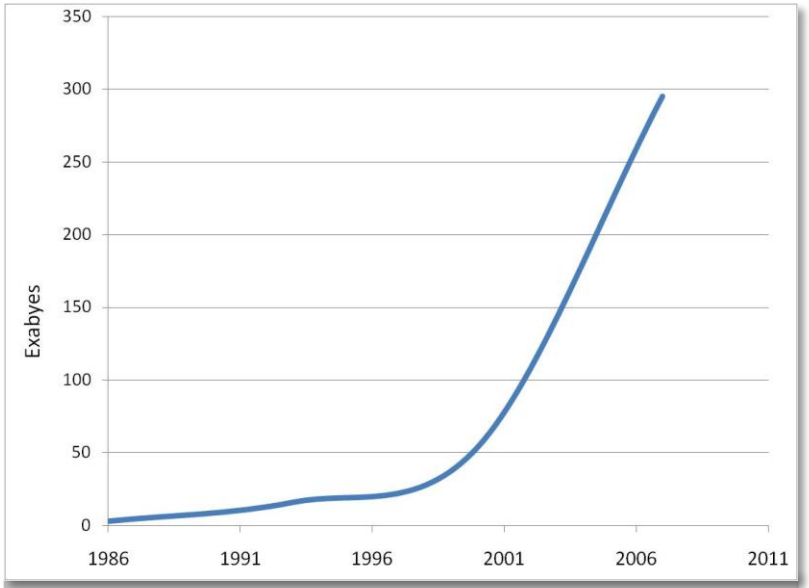
$2 Trillion Opportunity says McKinsey Group

- Economic value to businesses and citizens Over $10 Billion on BI Tools
- Over $8 Billion on Data Warehouse Software
- More than 10% annual growth

44x Increase in data by 2020 (1)

67x Increase in data files by 2020 (1)
new files such GPS and Facebook

450% Increase in connected devices that generate data, e.g. smart meters by 2015 (2)



(1) Source: **IDC**: The Digital Universe Decade – Are You Ready? May 2010, Sponsored by EMC
(2) Source: **McKinsey Global Institute**, Big Data: The next frontier…
(3) Source: **Hilbert and Lopez**, Science 2011.

VectorWise:
Why Fast Matters…Price (x) Performance Ratio

- High Performance 'Always On, Real-Time and Dynamic Data' Enables:
  - Interactive Analysis Against Raw Data (Unaggregated) Enables More Rapid and Deeper Insight
  - Enhanced Applications by Analyzing Larger Volumes of Data
  - Cost Optimized Infrastructure Enabling the Re-Deployment of Budgets to High Value IT Investments
  - Enables the Evolution of Next Generation Applications, Services and Utilities across Interfaces
    - Mobility is enabled with 'always on, real-time' analytical data infrastructure
- High Performance Computing at a Fraction of the Costs:
  - Enables your most Complex Business Requirements
  - Complex Data Analytical Requirements made Functional
  - Simplifies Project Design and Implementation
- Leverages Legacy Architectures and Infrastructure:
  - Enhances and Enables Legacy Capabilities
  - Optimizes Enterprise requirements for Big Data, Cloud, Unstructured Data and Mobile capabilities
  - Broad 3rd Party Developer Support
- Fast is 'Green'
  - Fast Data Processing Results in the Use of Less Processing Power

VectorWise:
Market and Industry Trends

- Cloud Computing, Big Data and the Emergence of ‘Analytical Data’:
  - Private Clouds Proliferate
  - Big Data Evolves in Requirements, Definition, Scope and Capability
  - Analytical Data or ‘Smart Data’, ‘Affiliated’ with Logic Emerges

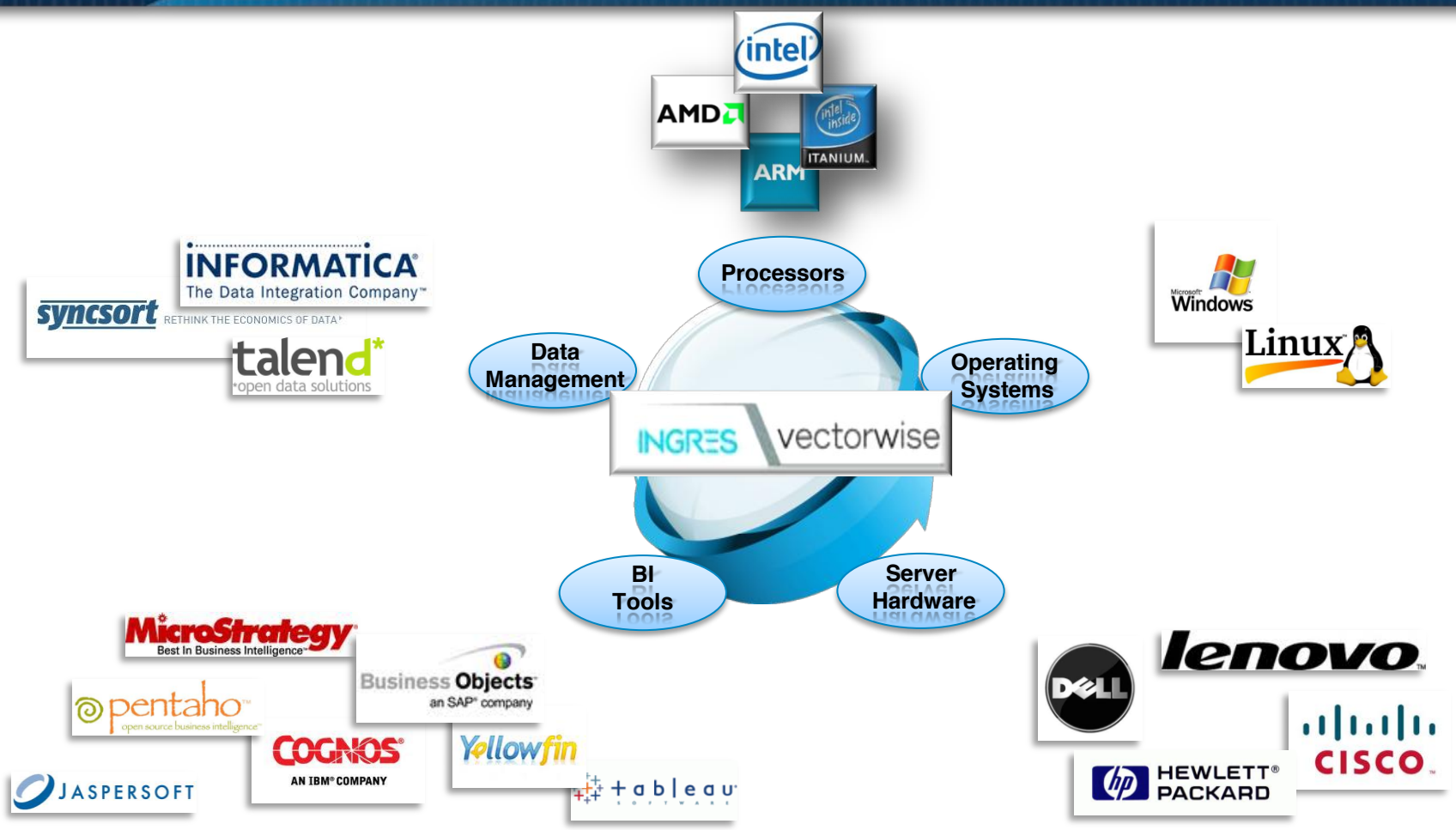
- Commoditization of, Increased Performance of Hardware Continues :
  - CPU’s
  - Memory
  - Storage

VectorWise:
Hardware Trends

- Hardware: Current Generation Hardware provides Specific Performance Optimizations
  - Processors have advanced execution capabilities
    - SIMD instructions for vector processing
    - Multiple execution elements in a core
    - Growing number of cores on a chip
  - Traditional databases do not benefit
    - Longer pipeline can be repeatedly flushed by poorly structured code resulting in inefficient processing – CPU utilization at 100% but mostly due to process overhead
    - Source code need proper structure for compliers to be able to invoke SIMD instructions
    - Most industry software was originally written in the 1970s or 1980s
- Memory: Memory size has Grown Enormously, but Not Memory Access Speed
  - Memory/processor bandwidth is a bottleneck
  - Traditional databases do not benefit
    - Processors implement multiple levels of cache to avoid idle cycles waiting for memory
    - Large poorly structure modules will cause frequent stalls waiting for memory
- Storage: External Storage Capacity are Substantially Improved
  - SSDs: high bandwidth but high price/GB and relatively low capacity
  - SAS: OK bandwidth for large reads and relatively high capacity but still pricy
  - SATA: low-cost, high capacity, but poor throughput
  - Modern disks can “feed” VectorWise consumption appetite
- Bandwidth: for Traditional Databases, Bandwidth between Storage and Memory is a Bottleneck

VectorWise 3rd Party Developer Ecosystem

Phase 1-2011: OS, Hardware, BI Tools and ETL Vendors



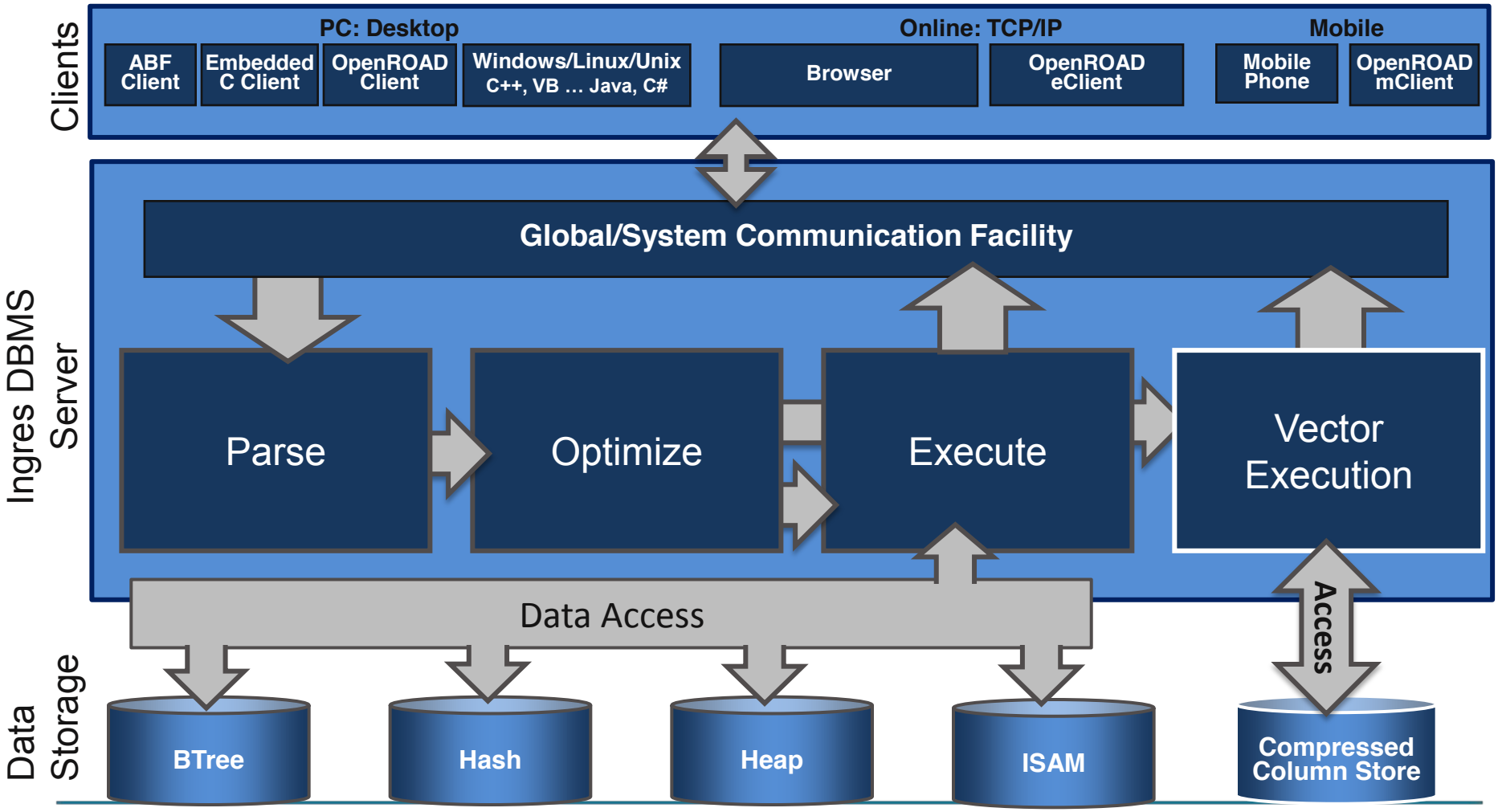
VectorWise Overview

October 2011

Authors: SReade/Rcovington/Fgallagher/Mzukowski | August, 2011 | Insight Delivered.

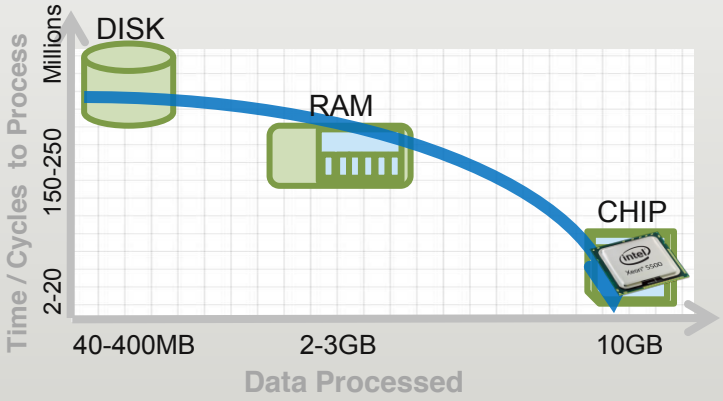
VectorWise Architecture:

Ingres10 Core Platform-Reliability + High Performance



Optimizing Processing:
What makes VectorWise Different?

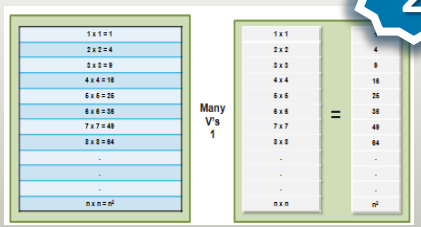
1 On Chip Computing



>100X Faster to process data on chip cache than in RAM.

Automatic optimization of full storage hierarchy

2 Vector Processing



Core level parallel processing – 100X
e.g. SIMD, Superscalar

3 2nd Gen Column Store

Limit I/O to specific columns. Efficient real time updates.

4 Smarter Compression

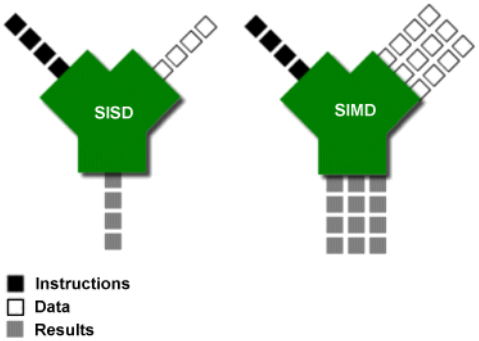
Maximizes throughput via automatically optimized on-chip compression

VectorWise Processor Strategic Partnerships

Modern CPU Capabilities and Collaboration

- Strategic Partnerships:
- Ongoing collaboration with Intel & AMD
  - Regular sharing of roadmap exchanges under NDA
  - Portability within x-64 so will work with past, current & future solutions from Intel and AMD
  - Ensure optimization of VectorWise for new chips & compiler architectures
  - Implementation of new performance features after looking at new chip features
  - Joint tests/whitepapers

- Evolution in Architecture:
  - Traditional CPU processing: Single Instruction, Single Data (SISD)
  - Modern CPU processing capabilities:
    - Single Instruction, Multiple Data (SIMD)



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VectorWise Processor Performance Architecture (VP²A)

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VectorWise Processor Performance Architecture (VP²A)

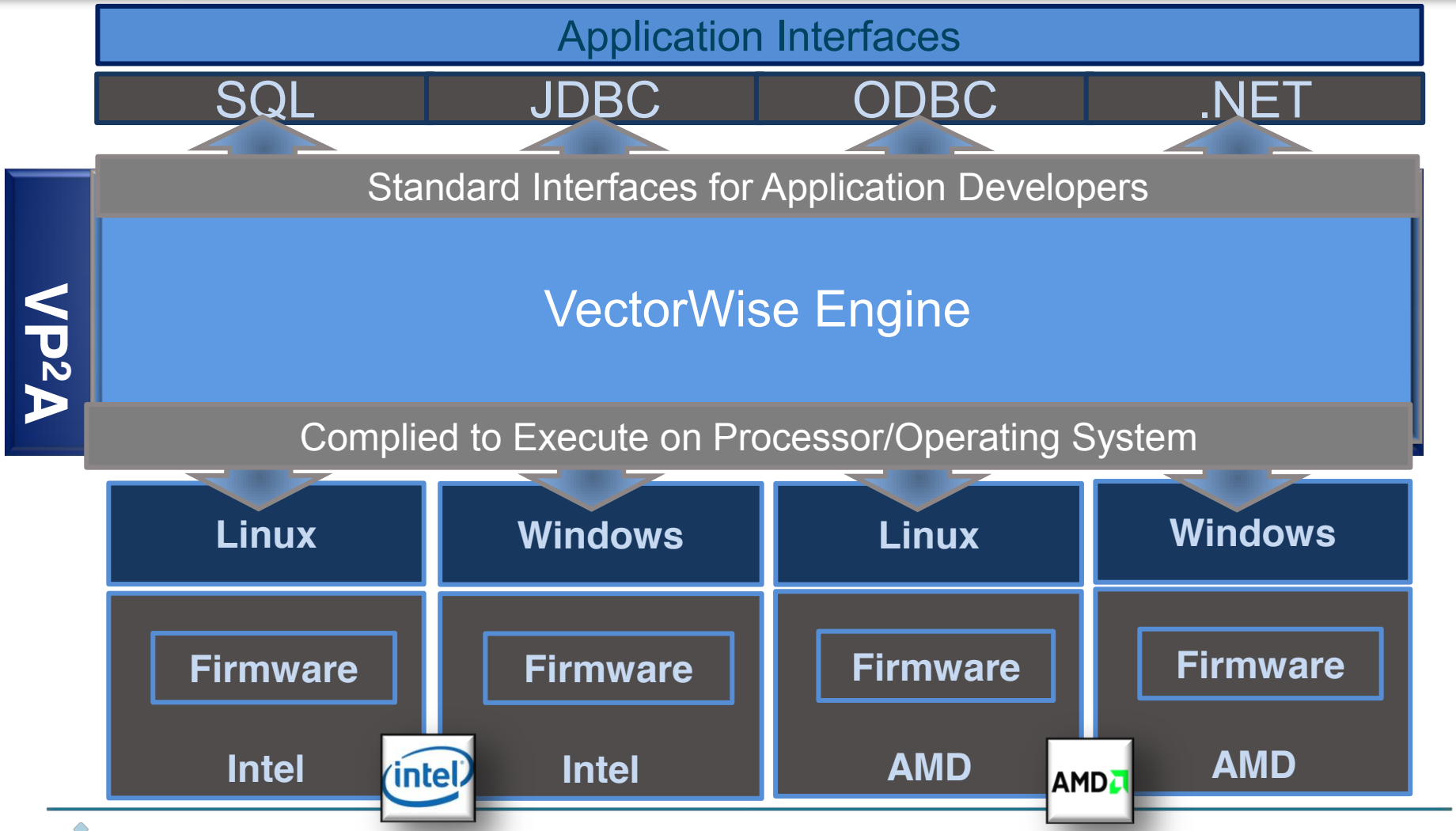
VP²A Interfaces Enable Standardization of Code

- VectorWise Processor Performance Architecture
  - Provides today's fastest analytic relational database
    - Runs analytic queries faster than any other RDBMS
    - Maximizes performance potential in today's CPUs
    - Installs on commodity hardware
  - Software-only implementation
    - Written in C
    - Design based on programming principles that unlock hardware potential
    - Compiled for different processor/system environments
  - Delivers improved hardware capabilities to applications
    - Proven query performance improvements over the last two generations of chips – ***without requiring application changes***
  - Result of years of research in analytic database performance and the exploitation of hardware capabilities.
  - IVW PPA roadmap exploits newly available hardware when available
    - SSE 4.2 leveraged since IVW 1.0, exploited if supported by the processors
    - As AMD enables SSE 4.2 in Bulldozer users will get the benefit of these instructions
    - IVW review roadmaps on a regular basis with both Intel and AMD

10x – 70x performance gains

VP²A Leverages Architectures and Optimizes Performance

Achieving Price+Performance + Standard Interfaces Protect Users



VP²A 3rd Party Support

Current and Planned Processor Support

August 2011

August 2011	Intel x64	AMD x64	Itanium
VectorWise v1.6	100% supported, main optimization target	100% supported, secondary optimization target	Prototype exist, not production ready
Database architecture optimized for analytical loads	Full Benefit	Full Benefit	Full Benefit
Automatic SIMDization	Full Benefit	Partial Benefit (1)	Partial Benefit
Exploitation of CPU Cache	Full Benefit	Full Benefit	Partial Benefit
SSE4.2 optimizations	Full Benefit	Full Benefit (from Bulldozer)	No Benefit
Wide-issue AVX instructions	Full Benefit	Full Benefit (from Bulldozer)	No Benefit
Multi-core	Full Benefit	Full Benefit	Unkown
Handling long CPU pipelines	Full Benefit	Full Benefit	Unkown

(1) Best compiler - ICC - works worse on AMD chips

(2) Recent ARM chips (Cortex-A8) has significantly longer pipelines than before

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Thank You
Q&A

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