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# Development of ASIC for Sine-Cosine to Position Code Conversion with High Resolution

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**Abstract**
The article deals with the problem of creating application specific integrated circuits transducer signal for position sensors with high resolution. The results of the work on the development of such chips, considered various solutions converters angle to code and justify the chosen architecture of the converter on the basis of a digital servo system with interpolation of the input signal. The results of modeling and experimental studies and comparison of developed angle to code converter with other known solutions are described.

**Keywords:** encoder ASIC, position sensor, rotary encoder, resolver, angle sensor

## INTRODUCTION

Position sensors are widely used in many industries, in particular, this throttle position sensor and electronic power steering in cars, the sensors of the angular position of the rotor brushless motors, position sensors of mobile elements in robotics, position sensors in machine tools and industrial equipment, etc. Such sensors consist from sensitive element and special electronic processing circuit for calculates position code. As sensitive elements of the sensors are used on different principles, including: magnetically elements (Hall-effect or magnetoresistive sensors), sine-cosine encoders, sine-cosine resolvers, linear differential transformers (LVDT) or optical sensor systems.

The main trend is the integration of all processing circuitry into a single chip for the purpose of miniaturization of sensors, reducing their costs and increasing the reliability [1]. Another major trend in the development of signal processing schemes is to increase the resolution of the conversion. For many of actual tasks necessary to provide an angular resolution of one period of sine-cosine signal 15-16 bits and higher.

Also, to ensure the greatest breadth of applications it is necessary to carry out the processing of the signals from all of the most common sine-cosine sensor systems, including resolver, LVDT, sine-cosine magnetic and optical systems.

## OBJECTIVE

The aim is to develop a single-chip application specific integrated circuit (ASIC), which provides processing of signals from the position sensors of all major types, with a resolution up to 16 bits per one period of the input sine-cosine signal.

## DEVELOPMENT OF THE CHIP ARCHITECTURE

To achieve the stated purpose is required to integrate the single chip system for generating a drive signal for resolver, LVDT and specialized signal demodulator with the secondary windings of the transformer, converter angle code, LVDT signal processing unit and a channel for generating a reference pulse for optical encoders.

Angle to code converters built on two basic principles - tracking loop converter that minimizes the error signal between the input signal and its image in the transmitter memory (table of sine and cosine) [2], and on the basis of direct calculation of the arc tangent of the angle, the most common of which is a system based on CORDIC-class algorithms [2, 3].

Angle to code converter with direct calculation has fixed the conversion delay is independent of the input signal phase. However, this architecture is sensitive to the quality of the input signal and does not guarantee monotonicity conversion that is necessary for most control systems where position sensors are used in the feedback. To improve the quality of the input signal in direct conversion systems, the provisional carry signal filtering and processing intensive use different algorithms, such as Wavelet transformation [4, 5].

Tracking architecture provides guaranteed monotonic conversion, as It represents the code position counter output count pulses from the generator, and the frequency of which depends on the polarity of the error signal between the input signal and the sine and cosine images placed in the transmitter memory [6]. Tracking system in the tracking mode provides maximum performance, but the time of entering the tracking depends on the current phase of the input signal, and in the worst case, equal to the time needed to iterate over all counter values. For most applications, this feature of the tracking system is not critical.

Tracking converter may be implemented as an analog-to-digital system, and completely in the digital domain. The analog-to-digital implementation of the error signal generated in analog form on the multiplied digital-analog converters (DACs). The maximum resolution of this architecture is around 13 bits, which is primarily due to the limited accuracy of the multiplied DACs because of the mismatch of their

elements, as well as with the size of such a high resolution DACs. As an example, commercial chips based on analog-to-digital tracking system can cause chip iC-NQC [7], as well as a single-chip encoder with a resolution up to 13 bits [8]. Can be realized high resolution analog-to-digital servo converters based on delta-sigma DAC, but this solution will provide low speed.

For conversion accuracy of 14 bits or more is already applied transformation angle code entirely in the digital domain [9]. This makes it easier to make a preliminary mathematical processing of the input signals to compensate for many of non-idealities of sensor system.

An analysis of architectural solutions in order to achieve high resolution and the lack of a guaranteed pass code has been selected on the basis of the architecture of the full digital tracking converter. A key element in determining the accuracy of digital processing is an analog-digital converter (ADC). The highest resolution of the ADC have performed on sigma-delta architecture [10]. For converter a multi-bit sigma-delta modulator of the second order have been developed, made by CIFF architecture (cascade of integrators with feed forward summation) [11]. The modulator converts the input analog signal into a 4-bit sample stream at a frequency of 8 MHz.

Structure of development Sine-Cosine to position code conversion ASIC (ENC_ASIC3) is show on figure 1.

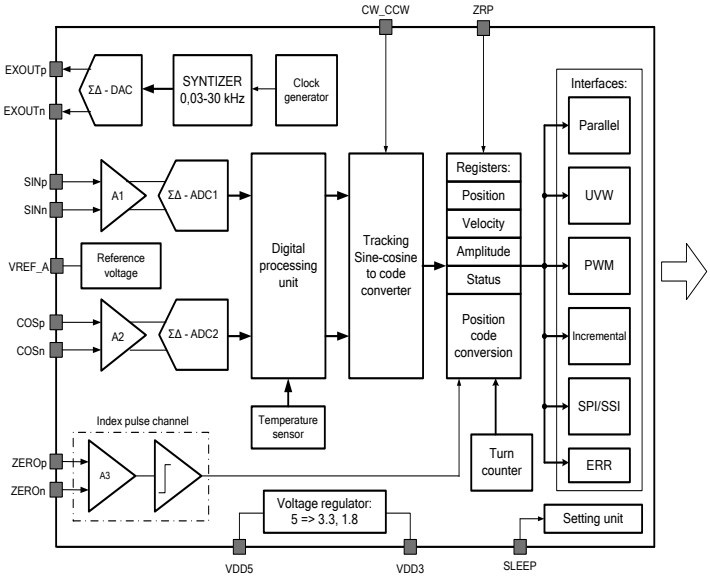


**Figure 1.** Structure of development Sine-Cosine to position code conversion ASIC

Structure of development Sine-Cosine to position code conversion ASIC (ENC_ASIC3) is show on figure 1.

ASIC is consist internal frequency synthesizer basis on direct digital synthesis, it generate sinusoidal signal with programmable frequency and signal amplitude. Reference clock signal generate from internal RC-oscillator, also can use external clock source. Synthesizer frequency programming in range 30 Hz-30 kHz with 1 Hz step. The sinusoidal signal is used to drive the primary winding of the transformer using a delta-sigma DAC.

Detailed conversion signal path for development ASIC show on figure 2.

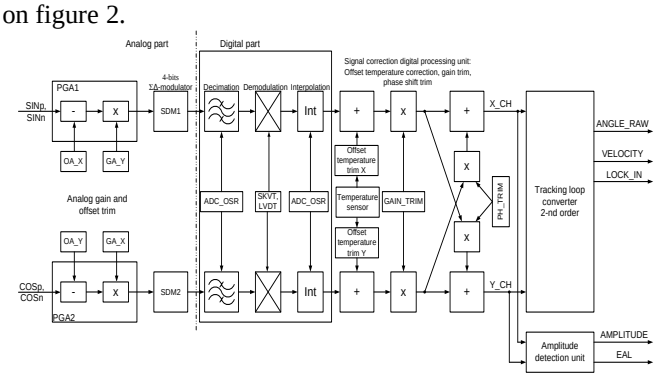


**Figure 2.** Conversion signal path for development ASIC

ASIC has two conversion channel, includes programmable differential amplifiers PGA1, PGA2 and sigma-delta modulators SDM1, SDM2. The output signal from modulators is fed processing unit provides quadrature demodulation, decimation and interpolation of the input signal with a resolution of 16 bits and a conversion time of 500 ns. The filter-decimator provides a programmable decimation from 32 to 4096 samples. For minimum decimation of the signal band of 62.5 kHz. A feature of implemented digital processing system is the interpolation algorithm of output of ADC samples, allowing providing a constant value in the sampling frequency of 2 MHz with 18-bit resolution conversion despite using high decimation of signal values (32 to 4096). Due to the input signal has harmonic type, using of interpolation applicable to the system. This allows the use of ADC with less speed and power consumption, at the same time providing a comparable conversion with converters with significantly more high-speed ADCs.

The filtered and demodulated signal is supplied to the signal correction circuit providing compensation for thermal drift of the offset voltage of input signals by the integrated temperature sensor, independently for each channel, channel gain adjustment, compensation for phase shift between channels.

The corrected signal is supplied to the tracking converter, which converts an input signal into position code with resolution of 13 to 16 bits. Next, the code position is adjusted depending on the user settings, counts the number of revolutions and the combined location code is supplied to interface circuit. The device delivers the next generation of output signals: digital serial SPI/SSI, incremental quadrature, pulse width modulated, three phase UVW with 120 degree phase shift for permanent magnet motor control system, parallel interface.

Structure of tracking loop converter show on figure 3. Tracking loop converter is minimize error signal Err with expression:

$$Err = \sin(\varphi) \cdot \cos(Addr) - \cos(\varphi) \cdot \sin(Addr)$$

where φ - phase of input signal, Addr - position counter code.

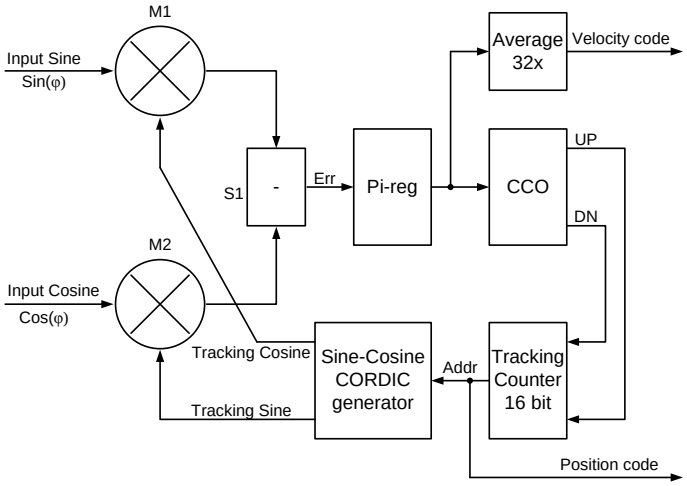


**Figure 3.** Structure of tracking loop converter

Error code integrated at Proportional-Integral controller Pi-reg and connect to code control oscillator CCO (analogous to voltage-control oscillator in analog domain). The CCO in depending on the magnitude and polarity of signal from PI controller generates a counting pulses UP and DN for reversive counter. For convert counter code into sine and cosine representations used generator based on CORDIC algorithm in rotation mode with pipelined architecture. For velocity calculation used averaged signal from PI-controller.

For amplitude calculation used amplitude detector based on iteration CORDIC converter in vector mode.

To connect the optical incremental sensor chip includes a channel reference pulse, consisting of a pre-amplifier and comparator. The channel reference pulse signal ensures the formation of the zero mark of the incremental interface.

## SIMULATION RESULTS

For developed ASIC conversion error of sine-cosine signal in the code was calculated. Testing circuit for determine conversion error show at figure 4. The input circuit model was applied sine-cosine signal frequency of 15 Hz and different amplitudes. Compared to the position code on the output circuit with a reference angle calculated from the input signal is determined by the conversion error.

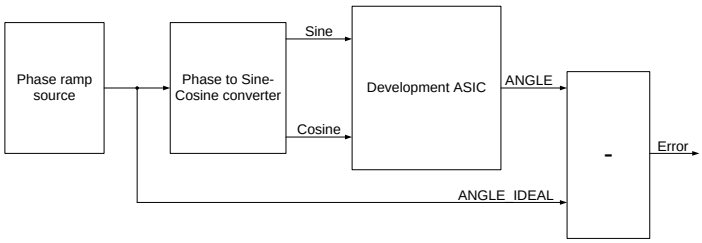


**Figure 4.** Conversion error testing circuit

Figure 5 shows the values of conversion error from the input signal amplitude (in% of the maximum possible signal amplitude) for the ADC 32 decimation mode (providing the maximum bandwidth of 62.5 kHz bandwidth ADC), and the nature of the error within the input period is shown in Figure 6.

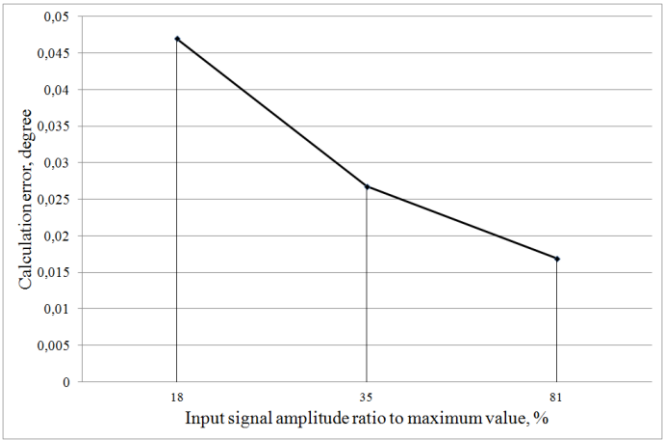


**Figure 5.** Conversion error versus amplitude of input signals

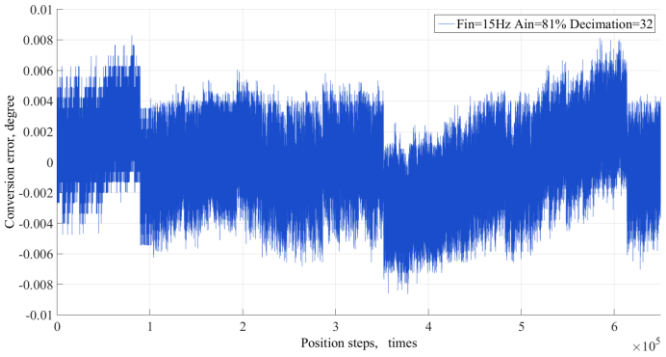


**Figure 6.** Simulated conversion error at full period of input signal

It was studied the effect of the filter characteristics of the digital signal processing unit (decimation factor and interpolation) on the accuracy of the development converter. The results are shown in Table 1.

**Table 1:** Simulation results for conversion error for various parameters of digital processing unit

| Decimation | Interpolation | ADC sampling frequency, at system clock 16 MHz, kHz | Total conversion error, degree |
|---|---|---|---|
| 32 | none | 250 | 0.0169 |
| 64 | none | 125 | 0.0209 |
| 128 | 32 | 2000 | 0.0167 |
| 256 | 64 | 2000 | 0.0170 |
| 1024 | 256 | 2000 | 0.0174 |
| 2048 | 512 | 2000 | 0.0173 |
| 4096 | 1024 | 2000 | 0.0174 |

Simulation results show that the use of interpolation ADC samples to increase the sample frequency has virtually no effect on the conversion tracking error transducer. This makes

it possible to obtain high performance converter code angle ADC sigma-delta type for large decimation signal. So for decimation in 4096 samples and at clock frequency of the modulator in 8 MHz we obtain nominal sampling frequency of 1953 Hz, but through the use of interpolation in 1024 points at the filter output we obtain sampling frequency 2 MHz. As shown by the simulation results, the conversion error will not be degraded compared with decimation 32 without using interpolation.

Algorithm of amplitude imbalance of sine-cosine signal correction was investigated. To do this, the input signals fed to the chip pattern relative amplitudes up to 0.45 sine signal and cosine signal for 0.4. Thus imbalance amplitude is about 12% - the amplitude of the sine signal at the output of interpolation unit is 23208, and 26111 samples for cosine signal.

Correction unit allows adjustment ratio sine and cosine signal by setting the 16-bit register GAIN_TRIM. High bit register performs handoff whose amplitude is attenuated in proportion, and the remaining 15 bits attenuation adjustment is performed on the selected channel signal.

For the values indicated above unbalance conversion error of 6.76 degrees, figure 7.

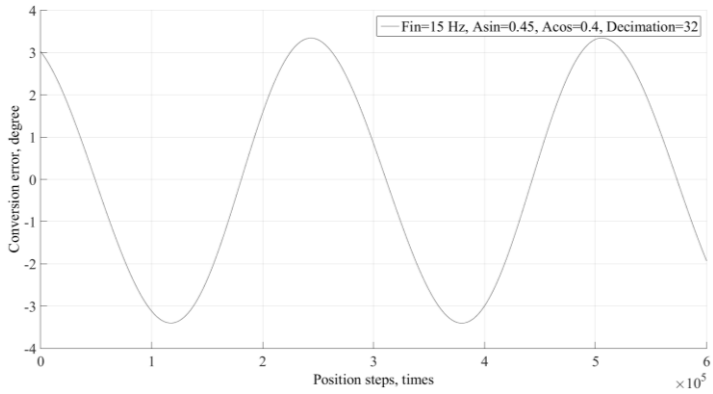


**Figure 7.** Position conversion error for amplitude imbalance of sine-cosine signal 12% without correction

For each channel, the correction algorithm defined by the following expression:

$$OUT = IN \cdot \frac{32768 + GAIN\_TRIM[14:0]}{2^{16}} \quad (1)$$

where *OUT* - output code after correction, *IN* - input code, *GAIN_TRIM[14:0]* - 15 bit register of gain correction.

Rate adjustment was determined that for this imbalance was 25481, and accordingly GAIN_TRIM register value was 58249. Error after correction reducet to 0.0206 degree, figure 86.

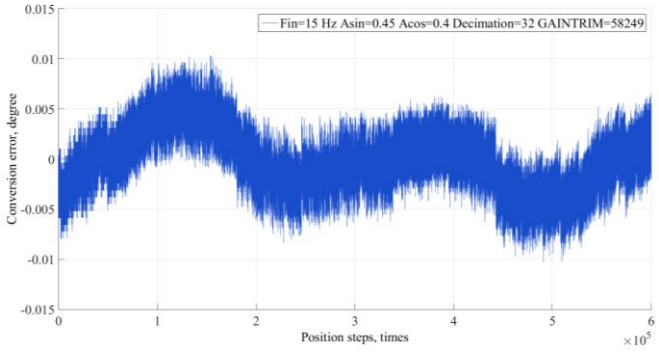


**Figure 8.** Position conversion error for amplitude imbalance of sine-cosine signal 12% without correction after correction (GAIN_TRIM=58249)

In accordance with expression (1) designed to adjust the system gain range for each channel is from 0.5-1.0 with 0.000015 adjusting step. This adjustment range covers most of the imbalance of the channel gain in real systems.

In real systems, there is often not a perfect phase relationship between the sine and cosine signals at 90 degrees. Due to mechanical error sensor placement, sensor moving parts, rotating windings of transformers the phase shift error may be from 2.3 units to tens of degrees in any direction. This necessitates the introduction of a correction unit of the phase shift system of sine and cosine signals.

The developed system includes a module correction of the phase shift of the input sine-cosine signal providing adjustment deviation of the phase shift between the sine and cosine signals in the range -37 ... + 37 degrees in increments of 0.00113 degrees. Phase adjusting unit operates in accordance with expressions:

$$OutX = InX + \frac{PH\_TRIM[15:0] \cdot InY}{2^{16}}$$
$$OutY = InY + \frac{PH\_TRIM[15:0] \cdot InX}{2^{16}} \quad (2)$$

where *OutX* - sine channel corrected output, *InX* - sine channel input, *InY* - cosine channel input, *OutY* - cosine channel corrected output, *PH_TRIM[15:0]* - phase shift correction code (signed).

According to the formula of addition of harmonic oscillations (2) that the introduced phase correction unit in the phase shift is defined as:

$$\Delta\varphi = 2 \cdot arctg\left(\frac{PH\_TRIM[15:0]}{2^{16}}\right) \quad (3)$$

It was simulated phase shift correction system operation. On the chip model input fed sine and cosine signals, in which an additional phase shift equal to π/16 or 11.25 degrees was introduced. The resulting conversion error was 11.3 degrees, the error graph shown in Figure 9.

For correction of phase shift by the expression (3) has been determined a correction factor PH_TRIM [15: 0] equal to 6455. This ratio has been loaded into the chip model; as a result of this adjustment of the conversion error has dropped to 0.0203 degrees, Figure 10. Thus, the developed chip construction provides phase deviation signals by 90 degrees, it is necessary to create precision position sensors.

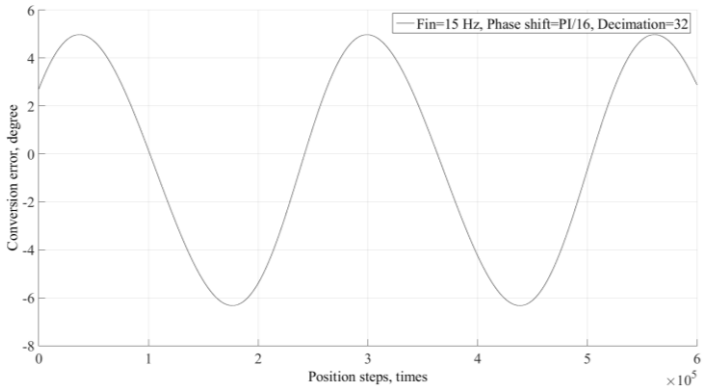


**Figure 9.** Conversion error for π/16 of sine-cosine phase shift error without correction

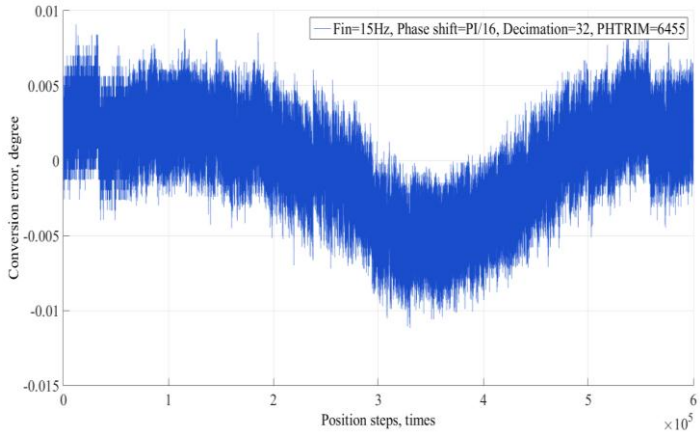


**Figure 10.** Conversion error for π/16 of sine-cosine phase shift error after correction (phase shift trim code PH_TRIM=6455)

**EXPERIMENTAL RESULTS**

Development ASIC was fabricated with 180 nm CMOS technology (X-FAB XH018 CMOS process). Die size 3.6x3.6 mm. Nominal clock frequency is 16 MHz. Photo of die of fabricated ASIC is show at figure 11.

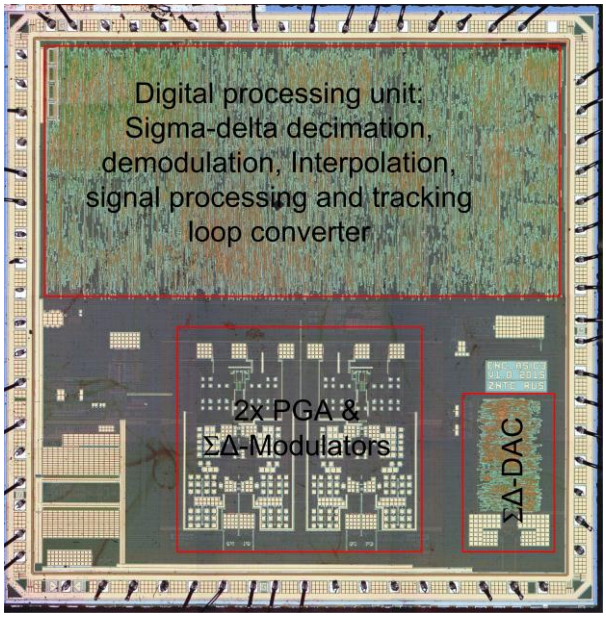


**Figure 11.** Photo of die of development ASIC

Measurements were conducted with connecting external precision sine-cosine source and with resolver LIR-158. Signal amplitude in both cases was within 90% from maximum value. Measurement results for conversion error show in table 2.

**Table 2.** Conversion error measurement results

| Decimation | Interpolation | Conversion error (stationary position), degree | |
|---|---|---|---|
| | | Sine-cosine mode | Resolver mode Modulation frequency 4.073kHz |
| 32 | 0 | 0.038 | - |
| 64 | 0 | 0.027 | - |
| 128 | 32 | 0.022 | - |
| 256 | 64 | 0.016 | - |
| 512 | 128 | 0.016 | 0.016 |
| 1024 | 256 | 0.011 | - |
| 2048 | 512 | 0.005 | - |
| 4096 | 1024 | 0.005 | - |

Comparison of development ASIC with others known sine-cosine to position code converter chips show in Table 3.

**Table 3.** Comparison of development ASIC with others sine-cosine to position code converter chips

| Parameter | Development ASIC | AD2S1210, Analog Devices | iC-TW8, iC-Haus | 2602PV2AP, NIIEMP | RD-19230, Data Device Corp. |
|---|---|---|---|---|---|
| Angle to code converter architecture | Tracking full digital, 2nd order | Tracking full digital, 2nd order | Direct conversion, CORDIC | Tracking, analog-digital, 2nd order | Tracking, analog-digital, 2nd order |
| Maximum resolution, bit | 16 | 16 | 16 | 16 | 16 |
| Tracking frequency at maximum resolution, Hz | 30 | 125 | n/a | 2 | 18 |
| Settling time at angle step $179^0$ for maximum resolution, ms | 16 | 45 | n/a | 40 | 50 |
| Conversion error, degree | 0.017 | 0.17 | 0.08 | 0.022 | 0.022 |
| Current consumption, mA | 48 | 49 | 35 | 270 | 50 |

## CONCLUSION

The research results show the correctness of the chosen chip architecture. According to the measurement results achieved conversion accuracy is less than 0.02 degrees at a current consumption of 48 mA and a conversion time of 500 ns. Using the algorithm of interpolation ADC samples allowed for a constant conversion rate does not depend on the value of decimation, without significant degradation of conversion accuracy. Research has shown that the use of interpolation ADC samples in order to increase the sample rate does not affect the conversion error of sine-cosine tracking converter. This makes it possible for the same ADC conversion rate to get a much higher sampling frequency, and thus, provide more speed of angle to code converter.

Developed ASIC will create angular and linear position sensors with high resolution. Due to the high degree of integration chip capable of processing the signal from the sensors of different types, which makes it fairly wide range of applications.

## ACKNOWLEDGEMENT

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## REFERENCES

[1] Sensor Trends 2014. 2010. Trends in future-oriented sensor technologies. AMA Association for Sensor Technology.

[2] Burke, J., Moynihan, J.F. & Unterkofler, K. 1999. Extraction of High Resolution Position Information from Sinusoidal Encoders. Proc. PCIM-Europe, Nuremberg, pp. 217-222.

[3] Meher, P.K., Valls, J., Juang, T.-B., Sridharan, K. & Maharatna K. 2009. 50 Years of CORDIC: Algorithms, Architectures, and Applications. IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS - I: REGULAR PAPERS. Vol. 56, No. 9, pp. 1893-1907.

[4] Kovtun, D.G., Sinyutin, C.A., Prokofev, G.V., Stakhin, V.G. & Obednin, A.A. 2015. Research of digital signal processing methods on the basis of the wavelet transformation for signal processing from a position sensor of the angle-component solvers. International Journal of Applied Engineering Research. Vol. 10, No. 18, pp. 38808-38811.

[5] Potekhin, D.S., Tarasov, I.E. & Potekhin, S.D. 2015. Improvement of Metrological Characteristics of Inductive Displacement Sensor of Movement Based on Digital Vector Diagram Reconstruction of Signals In Windings. International Journal of Applied Engineering Research. Vol. 10, No. 8, pp. 20343-20349.

[6] Nishimura, H. 2009. Tracking loop type digital angle converter and angle/digital converting apparatus. US Patent 7541951.

[7] iC-NQC, 13-bit Sin/D CONVERTER WITH SIGNAL CALIBRATION. iC-Haus GmbH, Germany. URL: [http://www.ichaus.de/NQC] (Accessed date: 11.09.2016).

[8] iC-MH, 12 BIT ANGULAR HALL ENCODER datasheet. iC-Haus GmbH, Germany. URL: [http://www.ichaus.de/upload/pdf/Mh_b1es.pdf] (Accessed date: 11.09.2016).

[9] High-Precision Sine/Cosine Interpolation. IC-Haus white paper. 2014. URL: [http://www.ichaus.de/upload/pdf/WP7en_High-Precision_Interpolation_140124.pdf] (Accessed date: 15.09.2016).

[10] Plassche, R. 2003. CMOS Integrated analog to digital and digital to analog converters. Kluwer Academic Publishers.

[11] Ziquan, T., Shaojun, Y., Yueming, J. & Naiying, D. 2013. The Design of a Multi-bit Quantization Sigma-delta Modulator. International Journal of Signal Processing, Image Processing and Pattern Recognition. Vol. 6, No. 5, pp.265-274.