ANALOG DEVICES

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APPLICATION NOTE

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Techniques for High Speed ADC PCB Layout

by Rob Reeder

INTRODUCTION

In today's industry, the layout of the system board has become an integral part of the design itself. Therefore, it is of paramount importance that the designer has an understanding of the mechanisms that affect the performance of a high speed signal chain design.

There are many options to consider when it comes to laying out a printed circuit board (PCB) in a high speed analog signal chain design. Some options matter more than others, and some are application dependent. In the end, the answer varies but in all cases the designer should try to lean on the error of best practice without becoming overly critical regarding every layout detail. This application note provides information that may be useful when starting the next high speed design.

EXPOSED PADDLES

Exposed paddles, or EPADs, are sometimes overlooked; however, they are essential to getting the most performance out of the signal chain as well as getting the most heat out of the device.

The exposed paddle, referred to at Analog Devices, Inc., as Pin 0, is the paddle found underneath most parts today. This is an important connection because it ties all internal grounds from the die to a central point under the part. Note the lack of ground pins in many converters and amplifiers today. The EPAD is the reason why.

The key is to tie this pin down, that is, soldered well to the PCB to make a robust electrical and thermal connection. When this connection is not solid, havoc can occur. In other words, the design may not work.

Achieving the Best Connection

There are three basic steps to take to achieve the best connection, electrically and thermally, with the EPAD. First, if possible, replicate the EPAD on each PCB layer. Doing so creates a thick thermal connection to all grounds and ground layers so that the heat can dissipate and spread out quickly. This is pertinent for high power parts and for applications that have high channel counts. Electrically, this gives a good equal connection to all the ground layers.

One can even replicate the EPAD on the bottom layer (see Figure 1). This can serve as a thermal relief ground point for decoupling and a placeholder to attach a heat sink on the bottom side.

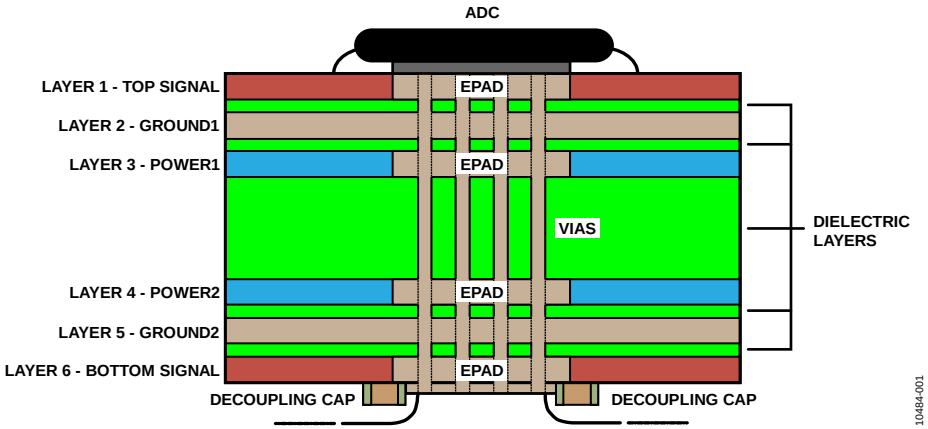

Figure 1. Exposed Pad Layer Layout Example

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REVISION HISTORY

1/12—Revision 0: Initial Version

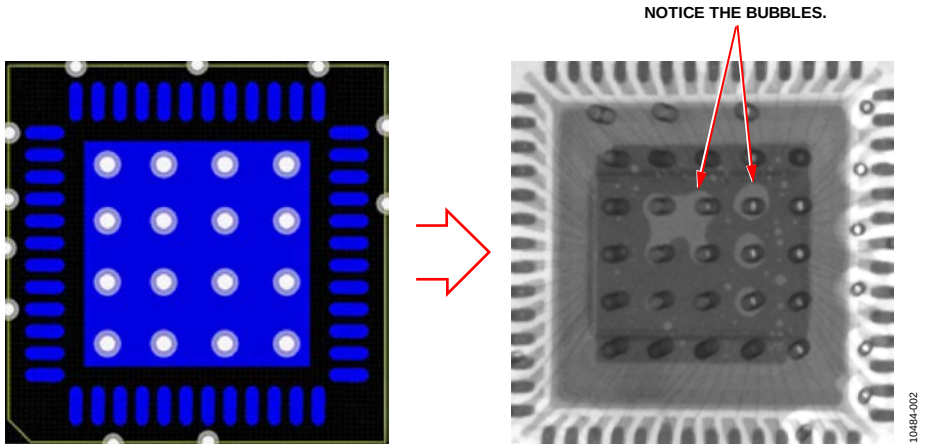

Figure 2. Poor EPAD Layout Example

Second, partition the EPAD into equal segments like a checkerboard. Use either a silkscreen crosshatch on the open EPAD or solder mask. This ensures a robust connection between the part and the PCB. During the reflow assembly process, there is no way to guarantee how the solder paste will flow and ultimately connect the part to the PCB. It is possible that the connection would be present, but not evenly distributed. It is possible to get only one connection and that connection could be small or, worse yet, situated in a corner. Dicing the EPAD into smaller partitions ensures a connection point in each separate area giving a more robust and evenly connected EPAD (see Figure 2 and Figure 3).

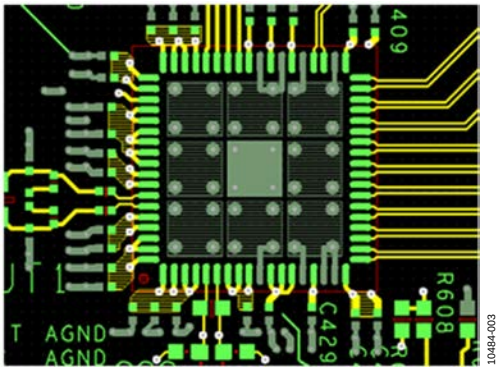

Figure 3. Better EPAD Layout Example

Finally, make sure that each of those partitions has via connections to ground. Usually, the partition is big enough so that several vias can be placed. Make sure each of these vias is filled with solder paste or epoxy before assembly. This important step ensures the EPAD solder paste will not be reflowed into those via voids thus possibly interfering with proper connection.

DECOUPLING AND PLANE CAPACITANCE

Sometimes engineers lose sight of why decoupling is used. Simply spreading many value capacitors across a board gives way to a lower impedance supply connection to ground. Yet the question remains: how many capacitors are needed? A good deal of the relevant literature states that lowering the power delivery system (PDS) impedance must be done with many capacitors and many values; however, that is not entirely true. Instead, simply select the right values and the right kinds of capacitors to make the PDS impedance low.

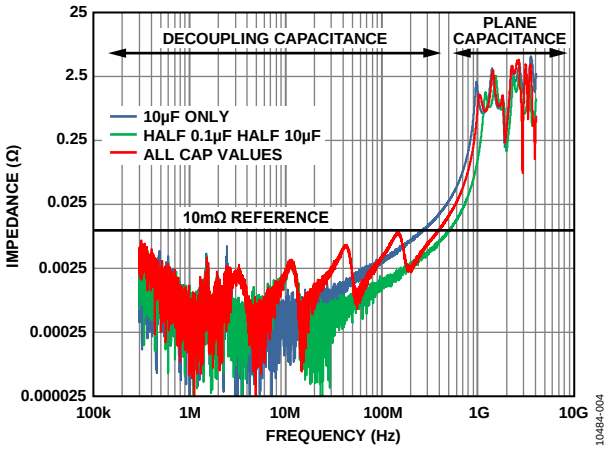

Figure 4. Capacitor Example

For example, consider designing a 10 mΩ reference plane, as shown in Figure 4. As indicated by the red curve, many capacitor values are employed on a system board, 0.001 µF, 0.01 µF, 0.1 µF, and so on. One can certainly lower the impedance across a 500 MHz frequency range; however, look at the green curve. In this case, there are only 0.1 µF and 10 µF capacitors used in the same design. This proves that if the right capacitors are used, then not as many capacitors values are needed. This also helps save on placement and BOM costs.

Note that not all capacitors are necessarily created equal even when purchased from the same vendor; make, size, and style matter. If the right capacitors are not used, and this applies to many capacitors or even just a few different types, then the result can have the opposite effect on the PDS than intended. The result may be inductance loops. Incorrect placement of

capacitors, or just using different capacitor makes and models that respond differently over frequency in the system, can resonate against each other (see Figure 5).

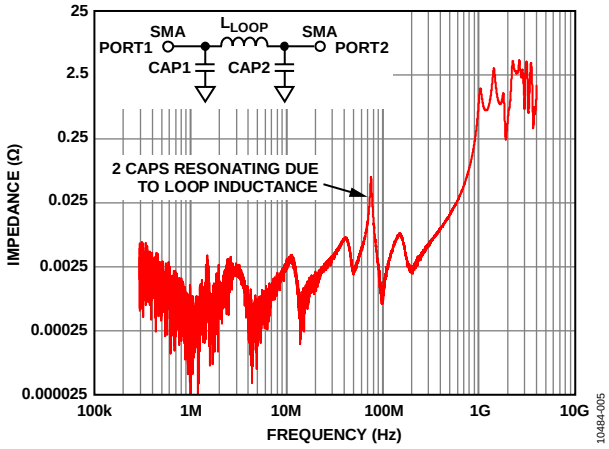

Figure 5. Resonating Capacitors

Taking the time to understand the frequency response of the capacitor types employed in the system is crucial. Do not undo all the hard work it took to design a low impedance PDS system by using just any capacitor.

High Frequency Plane Capacitance of a PDS

To design a good PDS, use a variety of capacitances (see Figure 4). Typical capacitor values used on the PCB only keep the impedance low between the frequency range of dc, or near dc, to about 500 MHz. Above 500 MHz frequencies the capacitance is dictated by the internal capacitance developed by the PCB. Note that stacking the power and ground plane tightly can help.

Design a PCB stack that supports a large plane capacitance. For example, a 6-layer stack may consist of a top signal, ground1, power1, power2, ground2, and bottom signal. Specify ground1 and power1 to be close in the stack—separating them by 2 mils to 4 mils forms an inherent high frequency plane capacitor. What is best about this capacitor is that it is free; it need only to be specified in the PCB fabrication notes. If the power planes must be divided, with multiple VDD rails on the same plane, use as much of the plane as possible. Do not leave voids, but be mindful of sensitive circuitry. This maximizes the capacitance for that VDD plane.

If the design allows for extra layers—from six to eight in the prior example—put those two extra ground planes between power1 and power2. This doubles the inherent capacitance in the stack given the same 2-mil to 3-mil core spacing (see Figure 6 for an example).

This can be much easier to design as opposed to adding more discrete high frequency capacitors to keep the impedance low at high frequencies.

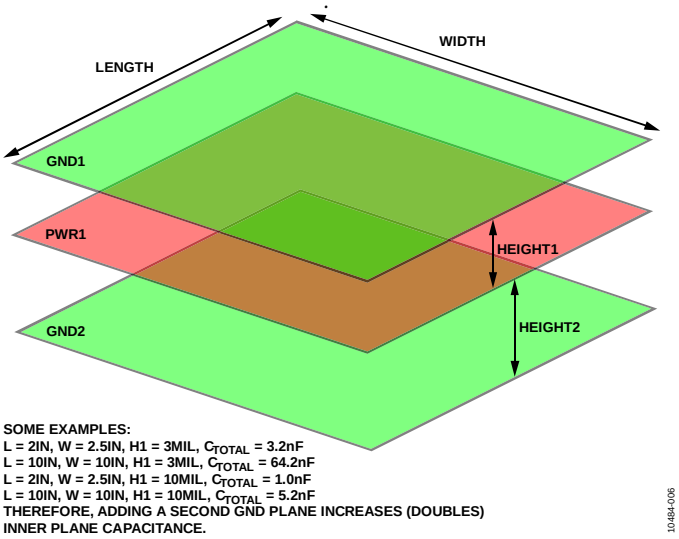

Figure 6. High Frequency Plane Capacitance Examples

Often overlooked, the task of the PDS is critical to minimize the voltage ripple that occurs in response to supply current demand. All circuits require current, some more than others and some at faster rates than others. A low impedance power or ground plane with adequate decoupling and a good PCB stack can help minimize the voltage ripple that occurs as a result of the circuit current demands. For example, if the system design has 1 A of switching current and the PDS is designed to have a 10 mΩ impedance based on the decoupling strategy used, then the maximum voltage ripple is 10 mV. It is that simple, V = IR.

With the perfect PCB stack up, the high frequency range can be covered, while the use of traditional decoupling at both the entry point, where the power plane originates, and around the devices that run at high power or surge currents can cover the lower frequency range (<500 MHz). This ensures the lowest PDS impedance across the entire frequency range. It is not necessary to sprinkle capacitors everywhere, butting them right up against every IC, thus breaking multiple manufacturing rules. If drastic measures of this sort are required, then this is an indication that something else is going on in the circuit.

PLANE COUPLING

It is inevitable that some layouts have a circuit plane overlapping another (see Figure 8). In some cases, this might be a sensitive analog plane (power or ground or signal, for example) where the next layer underneath is a noisy digital plane.

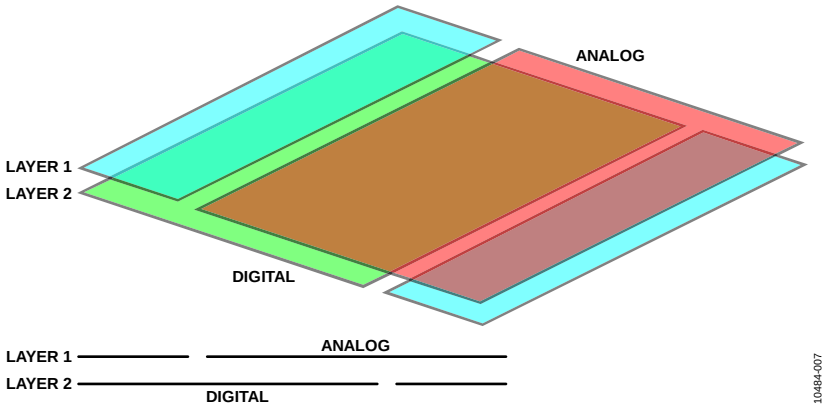

Figure 7. Cross Coupled Plane Example

This is commonly ignored because the noisy plane is on another layer (below) the sensitive analog layer. However, a simple test may prove otherwise. Take one of the layers and inject a signal on either plane. Next, connect the other layer that cross couples that adjacent layer to a spectrum analyzer. The amount of signal coupling through to the adjacent layer can be seen in Figure 8. Even if they are separated by 40 mil, it is still a capacitor in some sense; therefore, it still couples signals through to the adjacent plane at some frequency.

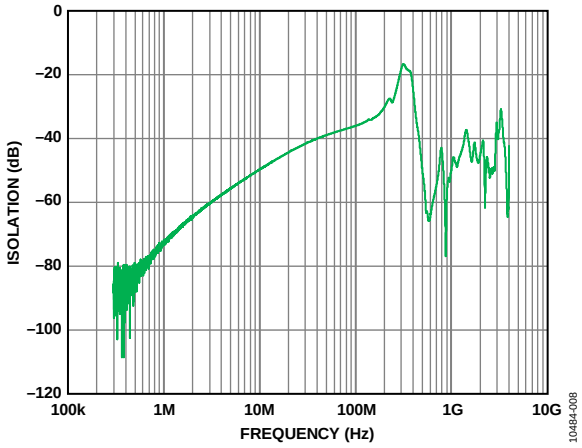

Figure 8. Measured Cross Coupled Plane Results

Figure 8 shows one such example. Assume, for example, that a noisy digital plane on one layer has a 1 V signal that switches at a high speed. This means the other layer will see 1 mV of coupling (~60 dB isolation). To a 12-bit ADC with a 2 V p-p full-scale swing, this is 2 LSBs of coupling. This may be fine for a particular system, but keep in mind that as the system's sensitivity increases by two bits, from 12 bits to 14 bits, the sensitivity of this coupling only quadruples to 8 LSBs.

Ignoring this type of cross plane coupling may neither make the system fail nor cripple the design. Simply note that more coupling exists between two planes than one may assume.

Keep this in mind when noisy spurs are seen coupling in the frequency spectrum of interest. Sometimes layouts dictate unintended signals or planes to be cross coupled to a different layer. Again, just keep this in mind when debugging sensitive systems. The issue may lay one layer below.

SPLITTING GROUNDS

The most popular question among analog signal chain designers is: should the ground plane be split into a AGND and DGND ground plane when using an ADC? The short answer is: it depends.

The long answer is: not usually. Why not? In most situations, a split ground plane can cause more harm than good because blindly splitting the ground plane only serves to increase the inductance for the return current.

Consider the equation V = L(di/dt). As the inductance is increased, so is the voltage noise. As the inductance increases, so does the PDS impedance, which the designer worked so hard to keep low. As the request for increasing ADC sampling rates continues, there is a minimal amount of effort the designer can make to decrease the switching current (di/dt). Thus, unless there is a reason to split the ground plane, keep those grounds connected.

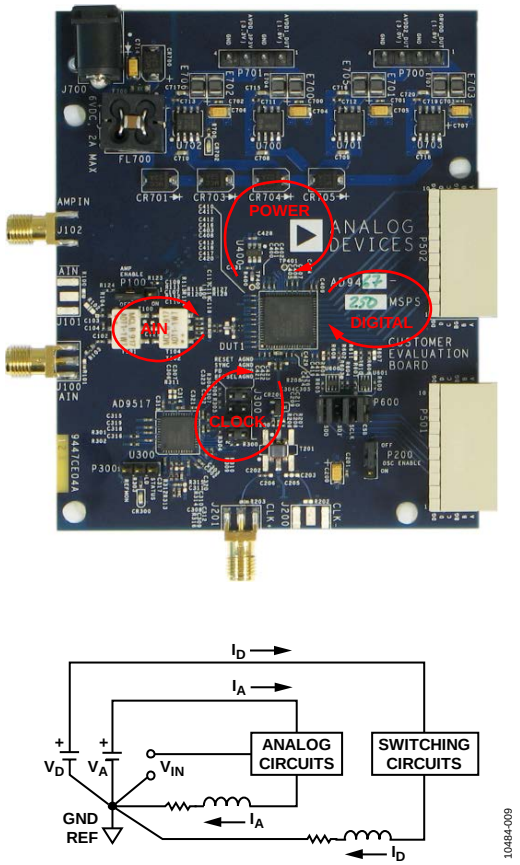

Figure 9. Example of Good Circuit Partitioning

Good circuit partitioning is key to not splitting ground planes as shown in Figure 9. Notice that if a layout allows you to keep the respective circuits in their own areas then there is no need to split the ground. Partitioning this way allows for a star ground, which keeps return currents localized to that particular circuit section.

For example, one reason to split ground planes occurs when a form factor restriction prohibits good layout partitioning. This may be because the dirty bus supplies or noisy digital circuits must be located in certain areas to conform with a legacy design or form factor. In that case, splitting the ground plane may make the difference in achieving good performance. However, to make the overall design work, a bridge or tie point is required to connect the grounds together somewhere on the board. In this case, spread the tie points evenly across the ground split planes.

One tie point on the PCB often ends up being the optimum place for the return current to pass without reducing performance or forcing return currents to couple to sensitive circuitry. If this tie point is at, near, or under the converter, it is not necessary to split the grounds.

CONCLUSION

Layout considerations are confusing because there are many differing opinions on the best strategy. Techniques and philosophy tend to become part of the design culture of a company. Engineers, who tend to use what worked in their previous designs, can be reluctant to change or try new techniques due to time-to-market pressures. This leaves the designer in the position of weighing trade-offs with risk until something goes wrong in the system.

At the evaluation board, module, and system level, a simple single ground works best. Good circuit partitioning is key. This also extends into plane and adjacent layer layout. Keep in mind that cross coupling can occur if sensitive planes are just above those noisy digital planes. Assembly is important too; use the fabrication notes given to the PCB or assembly house to your advantage to ensure a solid connection between the IC EPAD and the PCB.

Often, poor assembly leads to poor system performance. Decoupling close to both the power plane entry point and the VDD pins of the converter or IC is always good; however, for added inherent high frequency decoupling, take advantage of tight power and ground plains of 4 mils or less. There is no extra cost for this, only the extra few minutes it takes to update one's PCB fabrication notes.

It is not easy to cover all the specifics when designing a high speed, high resolution converter layout. Each application is unique. It is hoped that the key points provided in this application note are useful to the designer to better their understanding for future system designs.

REFERENCES

Griffin, Gary. 2006. AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP).*

Kester, Walt. 2004. *Analog-Digital Conversion: Seminar Series*, Analog Devices, ISBN 0-916550-27-3. (Also available as *The Data Conversion Handbook*, 2005, Elsevier/Newnes, ISBN 0-7506-7841-0)

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