

A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs

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INTRODUCTION

High sampling rate analog-to-digital converters (ADCs) are commonly used to sample complex modulated signals at intermediate frequencies in modern wireless receiver designs. Often CMOS switched-capacitor based ADCs are selected for such designs due to their attractive low cost and power dissipation. These ADCs utilize an unbuffered front end directly coupled to the sampling network, which presents time varying input track-and-hold impedances to the amplifier driving the ADC. To effectively drive the ADC with minimal noise and distortion degradation of the wanted signal, it is necessary to design a passive network interface, which helps to reject wideband noise and transforms the track-and-hold impedance to present a more benign load impedance to the driving amplifier. A resonant approach for transforming the track-and-hold impedance to a more predictable load allowing precise design of antialiasing filters is presented at several common IF frequencies.

SWITCHED-CAPACITOR ADCS

Switched-capacitor ADCs are different from buffered input ADCs because the buffer is stripped out of the ADC for lower power. The ADC sample-and-hold amplifier circuit (SHA) comprises an input switch, an input sampling capacitor, a sampling switch, and an amplifier. As shown in Figure 1, the input switch directly connects the driver to the sampling capacitor. When the input switch is on (track mode), the driver circuit drives the input capacitor. The input is sampled (captured) on the input capacitor at the end of this mode. When the input switch is off (hold mode), the driver is isolated from the input capacitor. The track-mode period and the hold-mode period of the ADC are approximately equal durations.

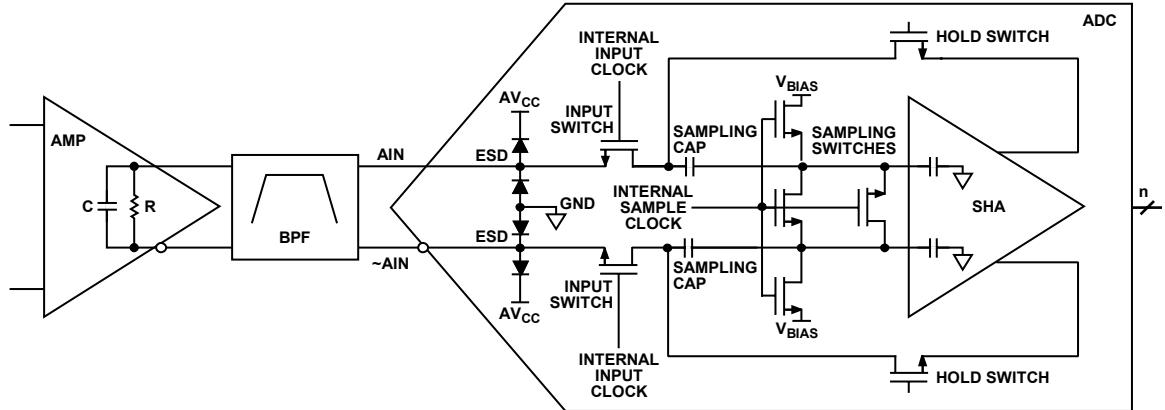


Figure 1. Simplified Input Model of a Switched-Capacitor ADC
Connected to Amplifier Driver

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The input impedance of the ADC during the track mode of the SHA is different from the input impedance of the ADC during the hold mode of the SHA. This makes it difficult to impedance match the ADC input with the driver circuit at all times.

Because the ADC only looks at the input signal during track mode, the input impedance should be matched for this mode. The frequency dependence of the input impedance is governed mainly by the sampling capacitor and any parasitic capacitance in the signal path. For accurate impedance matching, it is helpful to have an idea of the frequency dependence of the input impedance. Measurement results obtained from an AD9236 explain the behavior of the input impedance for input frequencies up to 1 GHz, as shown in Figure 2.

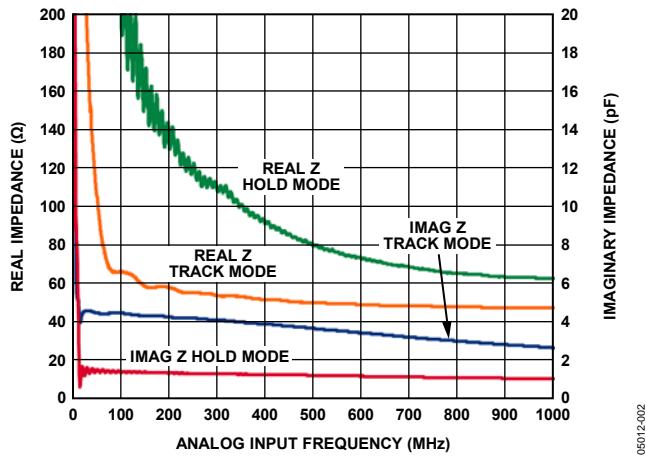


Figure 2. AD9236 Differential Input Frequency for Both Track Mode and Hold Mode

In Figure 2, the blue and red curves provide the imaginary input capacitance (right vertical axis) values for both the track mode and hold modes of the ADC input SHA network, respectively. Note that the imaginary impedance changes from a larger capacitance, greater than 4 pF at frequencies <100 MHz, to roughly 1 pF when in the hold mode. In Figure 2, the real portion of the input SHA network is seen by the orange and green curves (refer to the left vertical axis). Track mode yields a much lower impedance as expected vs. hold mode, where the input switch is opened. Unlike the impedance of buffered ADCs that stays constant over the entire rated bandwidth, the input impedance varies quite a bit with the first 100 MHz of input bandwidth. This presents a tough challenge to the designer to obtain an adequate match to the system's characteristic impedance over a given frequency range.

RESONANT MATCHING

To couple the wanted signal effectively into the desired Nyquist zone of a given ADC, it is necessary to understand the presented track-and-hold impedance of the ADC at the frequency of interest. Several ADC manufacturers are making scattering parameters and/or impedance parameters available for network analysis. The measured input impedance data can be used to design impedance transforming networks that improve coupling of the wanted signal while helping to provide rejection of unwanted signals at other frequencies.

When provided with the differential input impedance of any input system, it is possible to design a reactive matching network that offers low signal loss. If the presented input impedance is complex and is expressed as $Z_{IN} = R + jX$, where R is the equivalent series resistive portion of the complex input impedance and X is the imaginary series reactance, it is possible to find a network to transform the complex impedance to a more desirable load. Often it is desirable to describe the input impedance as an equivalent parallel RC network. To find the equivalent RC parallel network, convert the impedance to an admittance using the following equation:

$$Y_{IN} = Z_{IN}^{-1} = (R + jX)^{-1} \quad (1)$$

There are many software programs that can deal with the inversion of a complex quantity, such as MATLAB®, MathCAD™, and even the later versions of spreadsheet calculators such as Microsoft® Excel. It's easy to find the solution using basic complex algebra in the following manner:

$$(R + jX)^{-1} = \frac{1}{R + jX} \cdot \frac{R - jX}{R - jX} = \frac{R - jX}{R^2 + X^2} = G + jB \quad (2)$$

where

$$G = \frac{R}{R^2 + X^2} \text{ and is called the conductance.}$$

$$B = \frac{-X}{R^2 + X^2} \text{ and is called the susceptance.}$$

The complex admittance $Y_{IN} = G + jB$ has the units of Ω^{-1} (sometimes referred to as mhos, ohms spelled backwards, or siemens, abbreviated as S). To find the equivalent RC parallel network, invert G to find the parallel resistance and to find an equivalent capacitance that yields a susceptance equal to jB . The susceptance of a capacitor is equal to $j\omega C$. Therefore, the equivalent parallel RC network values are

$$R_{EQ} = \frac{1}{G} = \frac{R^2 + X^2}{R} \quad (3)$$

and

$$C_{EQ} = \frac{1}{\omega} \frac{-X}{R^2 + X^2} \quad (4)$$

where $\omega = 2\pi f$, the radian frequency at the frequency of interest.

Because admittances add in parallel, it is easy to find a resonant susceptance to cancel the jB imaginary component in Equation 2. The imaginary susceptance needs to have a magnitude of B with opposite polarity. The admittance of a shunt inductor is

$$\frac{1}{j\omega L} = \frac{-j}{\omega L} \quad (5)$$

An inductor equal to $1/\omega B$ resonates away the imaginary admittance, leaving only the conductive portion of the complex admittance. For example, the AD9236 presents a track impedance of $(59 - j270) \Omega$ at 140 MHz. Using Equation 1 and Equation 2, the complex admittance is $G + jB = (0.77 + j3.5) \text{ m}\Omega^{-1}$. The parallel RC equivalent resistance is $G^{-1} = (0.77 \times 10^{-3}) = 1300 \Omega$, with an equivalent parallel capacitance of $(B/\omega) = (3.5 \times 10^{-3}) / (2\pi f) = 4 \text{ pF}$. By applying a parallel inductor $L_P = 1/\omega B$, the capacitive susceptance can be resonated away leaving only the high impedance resistive portion of the RC parallel equivalent.

Proof:

$$(1/\omega B) = (2\pi f \times 3.5 \times 10^{-3})^{-1} = 322 \text{ nH} \quad (6)$$

and

$$R_{EQ}/C_{EQ}/L_P = ((1300 \Omega^{-1} + (j2\pi f C_{EQ}) + (j2\pi f L_P)^{-1})^{-1} = 1300 \Omega \quad (7)$$

IF SAMPLING AND NYQUIST CONSIDERATIONS

Baseband sampling is considered only when the signal or frequency of interest lies within the first Nyquist zone. However, some converters can sample in higher Nyquist zones above the first; this is called undersampling or IF sampling. Figure 3 shows the ADC Nyquist zones with a 140 MHz interest frequency (IF) relative to an 80 MHz sampling frequency (F_s). Essentially, the signal is in the forth Nyquist zone. The image or alias of the IF frequency can be seen reflected back to the first Nyquist zone; this looks like a 20 MHz signal as seen in the first Nyquist zone. Also note that most FFT analyzers, like the ADC Analyzer™, only plot an FFT of the first Nyquist zone or 0 F_s to 0.5 F_s . Therefore, if the frequency of interest is above 0.5 F_s , an image is reflected down to the first Nyquist zone or what is also known as baseband. This can make things confusing if spurious tones are in the band of interest.

So how does an ADC sample above 0.5 F_s and still hold true to the Nyquist criteria? Restated from Walt Kester's *High Speed Design Seminar*:

Nyquist Rule: A signal must be sampled at a rate equal to or greater than twice its bandwidth in order to preserve all the signal's information.

This is also seen in Equation 8, where F_s is the sample frequency and F_{BW} is the maximum frequency of interest:

$$F_s > 2 \times F_{BW} \quad (8)$$

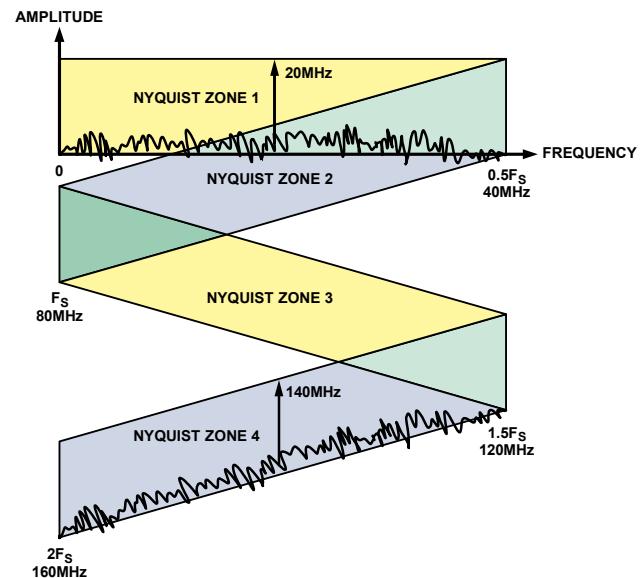


Figure 3. Nyquist Zone Definition

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The key here is the location of the frequencies of interest. As long as the signals do not overlap and stay within a single Nyquist zone, the Nyquist criteria is met. The only thing that changed is the location of the first Nyquist zone to a higher one.

IF sampling is becoming very popular because it allows the designer to eliminate a mix-down stage in the signal chain. This gives rise to better performance because the number of overall components in the signal chain is reduced, lessening the noise to the system. This in turn, better preserves the system's overall signal-to-noise ratio (SNR). In certain situations this can also improve the spurious-free dynamic range performance (SFDR) as well, because the local oscillator (LO) leakage through the mixer is reduced with the elimination of this stage.

The design of the antialiasing filter (AAF) at high frequencies is critical when doing IF sampling. In most cases, the AAF is designed and centered around the frequency band of interest. This could be anywhere from a few MHz to the entire bandwidth of the desired Nyquist zone. It all depends on the minimum analysis bandwidth required for the system. Correct filter design is critical in IF sampling applications so that lower frequency noise from lower Nyquist zones does not fall into the higher Nyquist zone where the frequency of interest lies. Poor filter design leads to excess noise seen in the baseband image of the noise floor. This can be summarized in Figure 4 where the antialiasing filter's stop-band attenuation characteristic depicts the system's overall dynamic range.

There is a direct relationship between the system dynamic range needed and the order of the band-pass filter. The same relationship exists depending on the system's resolution. The lower the resolution, the higher the noise floor. This means aliased signals are less effective, and therefore, the filter order

requirement is lower too. However, some higher order filters may give rise to more ripple in the pass band, which can also have an adverse effect on the system performance by introducing phase and amplitude distortion. In summary, care must be taken when designing the antialiasing filter.

ANTIALIASING FILTER DESIGN

An antialiasing filter helps to reduce signal content from unwanted Nyquist zones that would otherwise alias in-band and corrupt dynamic performance. Antialiasing filters are often designed using LC networks and need to have well-defined source and load impedances to achieve the desired stop-band and pass-band characteristics. To derive the filter network, a variety of cookbook filter synthesis approaches may be used. Often, Chebyshev or Butterworth polynomials are used to define the filter transfer function. Several software-based filter design programs are available to help simplify the problem, such as Filter Free 4.0 from Nuhertz Technologies or Agilent Technologies Advanced Design System (ADS).

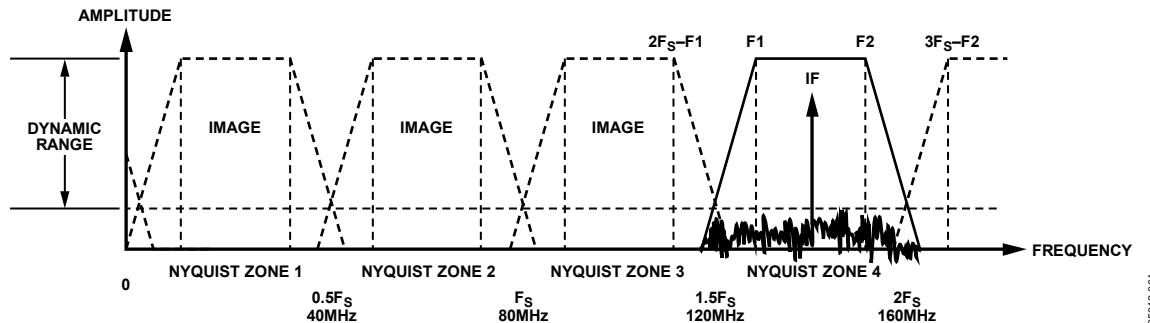


Figure 4. System Dynamic Range vs. Antialiasing Filter Stop-Band Attenuation

Alternatively, filter design handbooks can be used to find unit normalized prototype filter values, which can then be scaled for the desired cutoff frequency and load impedance. An example of a fourth-order unit normalized prototype filter is presented in Figure 5 (a). The filter obeys a Chebyshev polynomial and ideally provides less than 0.5 dB ripple for a 5:1 load-to-source impedance ratio. For a 144 MHz cutoff frequency and 600 Ω load impedance, the single-ended equivalent network is presented in Figure 5 (b). Most high speed ADCs capable of high dynamic range IF sampling utilize a differential input interface. Therefore, it is necessary to convert the single-ended network to a differential network, as shown in Figure 5 (c). The series impedances are halved when transforming to the final differential network. The final implementation using realistic L values and C values is shown in Figure 5 (d). It is wise to model the printed circuit board parasitics to select optimum Ls and Cs. The final implementation uses slightly lower inductor values to

accommodate for the series inductance of the circuit traces. Note that the load in Figure 5 (c) is replaced with the ADC interface in Figure 5 (d), including a shunt inductor and common-mode biasing resistors. The biasing resistors supply the needed DC offset into the individual differential inputs and work in combination with the raw track impedance and resonant shunt inductor to present a well-defined load for the filter.

It's important to respect the Q of the network. The greater the load-to-source impedance ratio, the more attention needs to be paid to component Q and layout parasitics. Often, some empirical trial and error is needed to optimize the network interface for the best combination of noise and distortion performance. It's advantageous to simulate the network response using realistic component models that accurately capture the parasitic effects of real-world Ls and Cs.

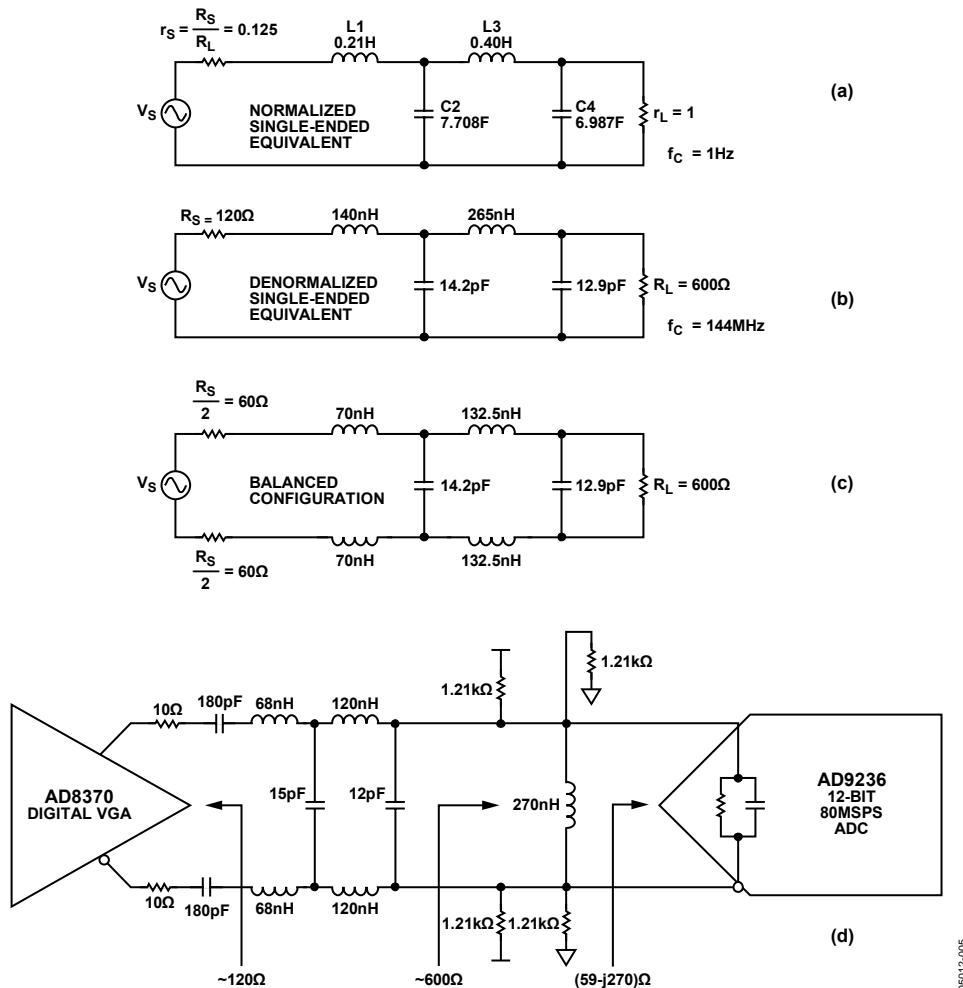


Figure 5. Matching a Switched-Capacitor ADC to Present a Defined Load

MEASURED PERFORMANCE

The circuit design in the previous example provides excellent dynamic performance, as shown in Figure 6. Note the difference in spurious-free dynamic range and total harmonic distortion with and without a properly designed interface network. The resonant shunt inductor transforms the raw impedance of the ADC, providing a predictable load impedance for the filter. Additionally, the shunt inductor helps to absorb any low frequency flicker noise and DC offsets that would otherwise corrupt the noise floor near 0 Hz. The antialiasing filter helps to reject high frequency wide-band noise that would otherwise alias in-band and helps to reject higher frequency harmonics present at the output of the driving amplifier. This provides a suitable solution for a high IF sampling receiver operating at a center frequency of 140 MHz. The frequency response is flat to within ± 0.2 dB over a 2 MHz bandwidth, with less than 10 ns of group delay.

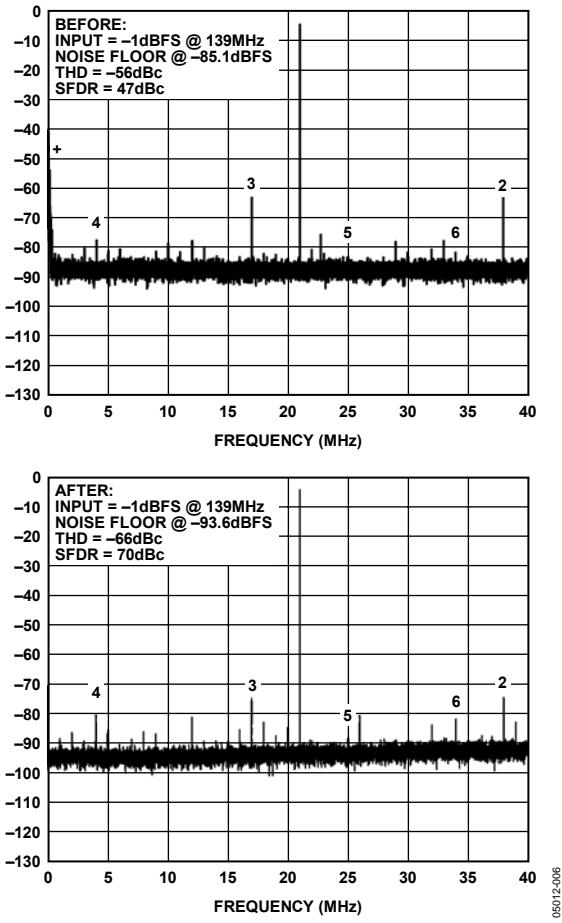


Figure 6. AD8370 Driving the AD9236 at 140MHz Before and After

A lower frequency example is provided in Figure 7. This solution is targeting a double-down conversion IF sampling design with 5 MHz of useful bandwidth with less than 100 ns of group delay and less than ± 0.25 dB of pass-band ripple. In this implementation, the AD8351 differential amplifier is used to

drive the AD9244 14-bit, 65 MSPS CMOS analog-to-digital converter. The same design approach is used as with the previous example. The cascaded noise floor is improved by more than 6 dB, while the SFDR improved by more than 10 dB.

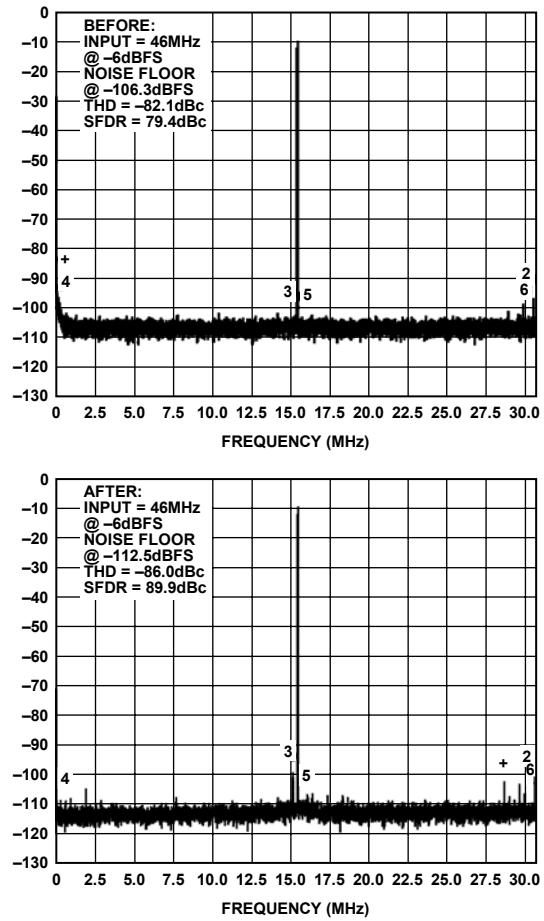


Figure 7. AD8351 Driving the AD9244 at 48MHz Before and After.

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SUMMARY

Providing an adequate match between the amplifier driving switched-capacitor ADCs can pose a challenge to any receiver designer. Here, a method has been described to match the amplifier properly. Using the track mode S-parameters given for a particular switched-capacitor ADC, it is possible to determine the resonant matching network to displace the dominate parasitic C terms inside the ADC's SHA. This provides a quick and easy solution by keeping the input impedance looking as resistive as possible. This yields better bandwidth, tighter passband flatness, and increased SFDR performance.

REFERENCES

- Chapter 4, *High Speed Design Seminar*, Walt Kester, Editor
- Filter Free 4.0, Nuhertz Technologies—online filter design software package
- MS Excel
- MATLAB
- MathCAD
- *RF Circuit Design*, Chris Bowick, page 66 to page 97
- AN-742, Frequency Response of Switched-Capacitor ADCs

For more information about switched-capacitor ADC input impedances for the AD9215/AD9226/AD9235/AD9236/AD9237/AD9244/AD9245, go to www.analog.com. On the product page, click the Evaluation Boards tab to download an Microsoft Excel spreadsheet for frequencies up to 1 GHz in track-and-hold modes.

