Fast and High Precision Motor Control for High Performance Servo Drives

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Abstract

This paper reports a new architecture of a fast current controller with two feedback signals for high performance motion control. Due to parallel processing inside the Field Programmable Gate Array (FPGA), the control algorithm computing time is significantly less than 1 µs. Together with advanced control technologies in combination with a new current observer the bandwidth of fast switching IGBT or MOSFET power stages is not limited by the delay time of high precision (integrating) current measurement any longer. Using that technology high control bandwidth in conjunction with high precision current control is now possible at no trade off. The control strategy relies on a simplified machine model without incurring performance degradations. The presented results have been produced with a high speed Computerized Numerical Controlled (CNC) machine.

1. Introduction

Low inertia permanent magnet (PM) synchronous motors are the preferred actuators in high performance machine tool or positioning systems. Owing to a large magnetic air gap the winding inductance is very low which favors a fast current rise. On the other hand, it makes the design of the current control system critical. The problem is even more pronounced with the new generation of ironless linear motors. Such motors are commonly used in high speed Computerized Numerical Controlled (CNC) machine tool applications.

When applied to low inductance machines the performance limits of existing current regulators are due to delay times of current measurement, DSP based algorithm computing and synchronizing with the PWM carrier signal. Regarding the current ripple, the low leakage inductance motors require operation at high switching frequencies, typically f_s = 8 – 50 kHz. The low phase shift especially of ironless motors with their extremely low electrical time constants allows very high current control bandwidth.

2. Current Loop

Usually, the control architecture of drive systems consists of three cascaded control loops. The innermost loop controls the current. Directly superposed to the current loop is the velocity controller. The outer loop is dedicated to control the position (fig. 1). The overall motion control system dynamics is limited by the achievable bandwidth of the current control loop. To achieve a very high current control bandwidth a fully analog power amplifier in conjunction with extremely fast (analog) control technology has been state of the art for a long time. These so called voice coil systems are characterized by two major drawbacks; the low power efficiency and the missing prediction capability. High efficiency is achievable with modern fast switched power electronics, prediction can be realized with digital control algorithms. Implementing a Smith Predictor for example, can increase the current loop bandwidth up to 70 % [1-4].

2.1 Pulse Width Modulation

In the following discussion PWM based current control schemes are divided in two categories:

Carrier based PWM

The most widely used pulsewidth modulation schemes are carrier based. Various industrial drives are built on this technique by utilizing Space Vector Modulation (SVM). Carrier based PWM have common characteristic subcycles of constant time duration $T_s = 1/2f_s$. Typically the actual current vector is only sampled at the beginning of each subcycle. During the sub

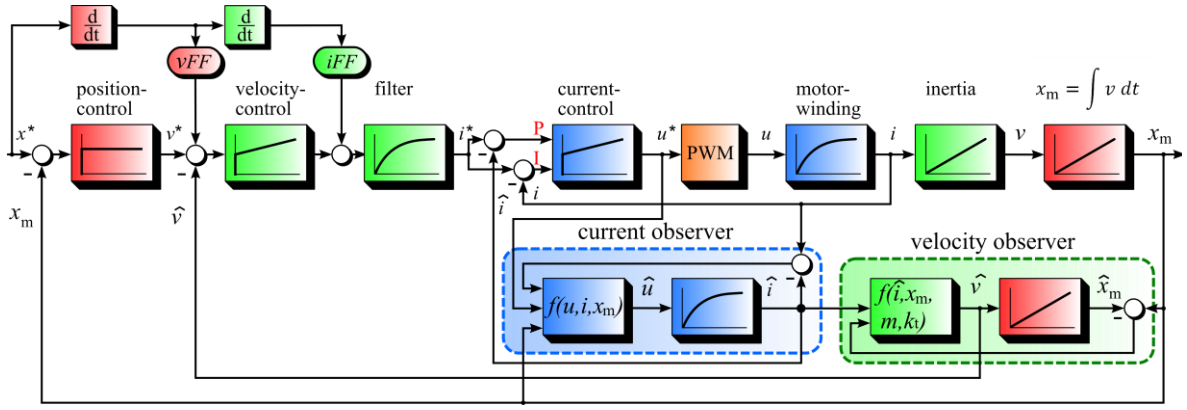

Fig. 1: Motion control with three cascaded feedback loops and two observers

cycle analog to digital conversion and computing the control algorithm are done. The resulting space vector voltage command defines the switching times for all three phases – as a switching sequence – for the next sub cycle. The behavior of such a sampling system can be described with a discrete z-transfer function $G(z)$. Due to analog to digital conversion and computing time for the control algorithm the resulting delay time of this z-transfer function is at least one sub cycle (z^{-1}). Very common is the implementation of a dead-beat controller to achieve the commanded current vector within a defined time frame. The required µcontroller computing power is reasonable for switching frequencies up to 10 kHz [3-5].

Carrier less PWM

Other control schemes like hysteresis control or trajectory based algorithms do without any carrier signal. Usually the switching events of the phases are determined separately for each motor phase. Especially hysteresis current control is still often realized with analog circuits to minimize the delay time. Typically predictive current control algorithms sample the current vector several times for each switching state. Due to the required high computing power the switching frequency is often below 2 kHz. For higher switching frequencies DSP or FPGA computing power is necessary. The Direct Torque Control (DTC) from ABB is the most common industrial drive utilizing a carrierless PWM. [5-7]

2.2 Phase current measurement

The quality of the analog-to-digital conversion is of great importance to servo controllers. The phase current measurements are especially critical. Traditionally, these currents are first converted by closed loop Hall Effect current transducers into electrically isolated voltages that can then be digitalized by 12-bit SAR ADCs (successive approximation). Sampling is usually carried out at certain harmonic-free times in order to minimize aliasing effects without using special low pass filters. Drawbacks are the offset voltage and the offset drift. Especially for low current applications size and cost of the devices are also issues.

Additional analog comparators are often used to rapidly detect overcurrent so that the power stage can be switched off immediately in order to protect it. A first order lag with approximately 2 µs is used to suppress EMI glitches due to the high voltage switching.

In carrier based PWM current control architectures two current measurement methods are common:

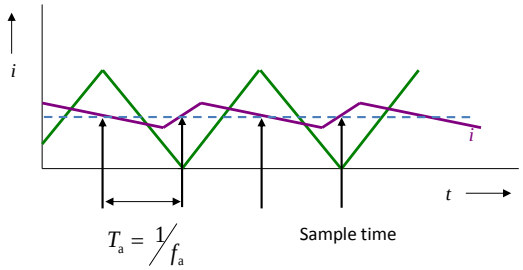

Fig. 2: Sampling the current synchronous to the carrier signal

a. Sampling the current synchronous to the carrier signal, fig. 2
   By sampling the current in synchronism with the ripple frequency the ripple current can be suppressed in an efficient way. This method is characterized by a low delay time but higher noise sensitivity. The current regulation is often realized with an

additional first order lag before the ADC with approximately 10 µs to reduce audible noise in high bandwidth systems.

b. Integrating the current over one PWM period (TPWM), fig. 3.
By integrating the current over one PWM period the ripple frequency, offset problems due to the sampling theorem and also noise are suppressed. In practical realizations the integration is replaced by a sum of several fast executed analog to digital conversions. This technique is called current oversampling. The drawback of this high precision acquisition is the additional delay time of $T_{PWM}/2$, which reduces the phase margin and accordingly the achievable bandwidth.

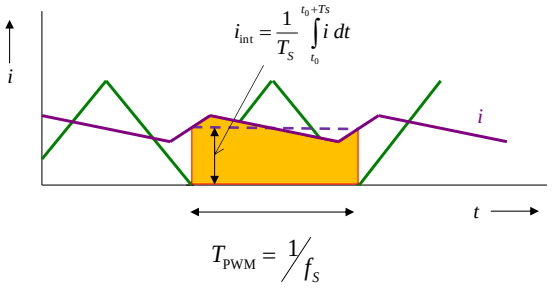

Fig. 3: Integrating the current over one PWM period (T_{PWM})

Thanks to the use of ΣΔ-ADCs, the control quality can be improved with considerably less effort [8]. Several semiconductor manufacturers offer integrated circuits specifically designed for potential-free current measurement. The differential analog input of these ICs can be directly connected to a shunt for current measurement; the electrically isolated, digital bit-stream is connected to an input of the FPGA. Signal transmission, filtering and sampling are carried out digitally. If the ΣΔ modulator is placed directly at the shunt, disruption as result of EMI of signal transmission, filtering or signal processing, as a matter of principle, is not possible [9].

2.3 A new Approach: FPGA based Multi Feedback Current Control

The modulators for each phase are generating a 20 MHz one bit data stream, which does not consist of digital words known from traditional A/D converters. In order to generate a digital word equivalent to the analog input voltage, this bit stream has to be processed by a digital filter. A very simple filter, built with minimal effort and hardware, is the Sinc³ filter: This filter provides the best output performance at the lowest hardware size (count of digital gates). For oversampling ratios M in the range of 16 to 256, this is a good choice. A Sinc³ filter step and pulse response is shown in fig. 4. The oversampling ratio M sets the conversion time and also the signal precision described with the signal to noise ratio (SNR) or the effective number of bits (ENOB) [9].

Due to the digital Sinc³ filtering analog noise filtering is not longer necessary. The bit-stream of the current signal is conditioned and processed further in the FPGA in up to three channels per motor phase:

1. Very fast decimation filtering for over-current detection.
   The oversampling ratio M is set to 16 with approx. 2 % precision.
2. Fast decimation filtering for the proportional component of the current controller with approx. 12-bit precision due to an oversampling ration of M = 64
3. High precision acquisition by means of integrating the signal over the specified PWM period $T_{PWM} = 1/f_s$

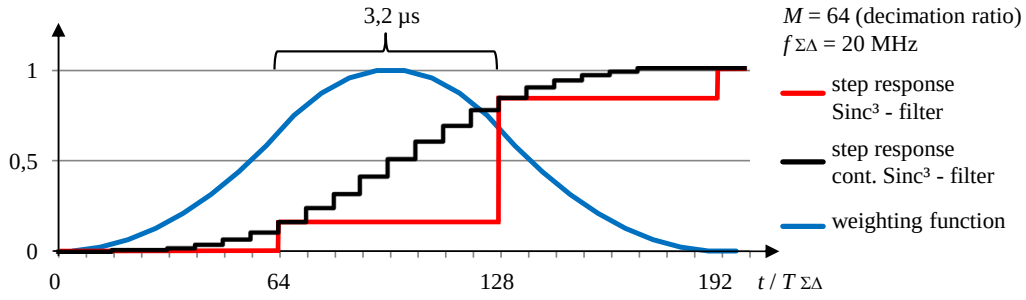

Fig. 4: Continuous Sinc³ decimation filter step and pulse response. Due to the pseudo interlaced operation the update frequency is 0.4 µs instead 3.2 µs.

This technique is comparable with a dual slope ADC used in digital multimeters.

Using the standard Sinc³ decimation filter architecture the output signal update rate depends on the modulator clock frequency $f_{\Sigma\Delta}$ and the decimation ratio M. Using a 20 MHz modulator in conjunction with a decimation ratio of 64 the current signal will be updated every $64 \cdot 50\,\mathrm{ns} = 3.2\,\mu s$. This conversion delay is acceptable for carrier based PWM control schemes, as long as this delay in addition to the delay for the control algorithm calculation does not exceed the subcycle time duration $T_s = 1/2f_s$.

By utilizing more FPGA resources a special pseudo interlaced operated Sinc³ filter provides the current value with only 0.4 µs update rate (3.2 µs / 8). This special decimation filter is for example required for hysteresis's control schemes to avoid a switching time discretization with the poor 3.2 µs time resolution.

2.4 FPGA based Current Observer

Thanks to the massive parallel execution inside an FPGA even complex algorithms can be executed in significantly less than 1 µs. A CPU with its sequential processing is much slower in executing complex signal condition and control algorithms.

The non desired influences of the Sinc³ filter on the measured current are the inherent attenuation and phase lag. By utilizing a new FPGA based current observer this attenuation and phase lag can be avoided. This observer relies on a simplified machine model described with the electrical motor parameters: inductance L_e and resistance R_e , fig. 5. Input data is – in addition to the measured and Sinc³ filtered phase currents and the rotor position signal – the output voltage of the power stage. It can be easily calculated from the dc link voltage v_{dc} in conjunction with the corresponding gate signals. The current observer delivers a current signal with effectively suppressed EMI noise, no attenuation and no phase lag at an update rate of 20 ns (50 MHz), fig. 6. This observer signal is perfect fitting for current regulation independent of the different control and modulation schemes (carrier / carrier less).

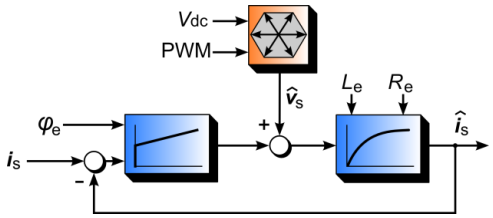

Fig. 5: Block diagram of the new current observer which is suppressing EMI noise and compensating the sinc³ filter delay

2.5 Dual Feedback Current Regulation

Various industrial current controllers are using more or less modified PI control schemes. The integral term in a PI controller causes the steady-state error to be zero. The problem with using an integral term is that it introduces a phase-lag. This means that the phase margin and also the damping of the system decrease. The immediately acting proportional term in a PI controller produces the control speed and decreases the phase lag at higher frequencies. This usually increases the phase margin.

The new multi-feedback current controller is designed to combine the advantages of the two current measurement methods with no drawback. The observed current signal is used as feedback signal for the proportional term of

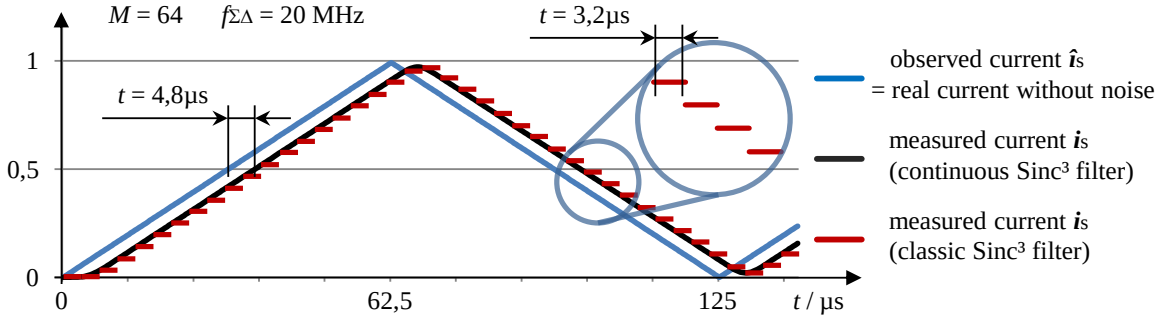

Fig. 6: Ramp response of the new current observer (= real current without noise) compared with classic and interlaced sinc³ filter output signals

the PI-current controller, fig. 7. This signal with suppressed EMI noise and no phase lag enables the requested high current control bandwidth. The integrated current signal is used as feedback signal for the integral term of the PI-current controller. The extremely low noise enables high precision operation of the current controller.

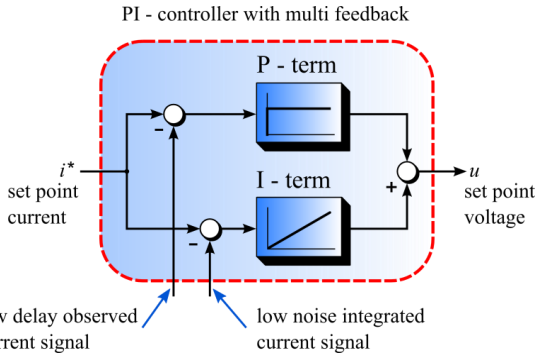

Fig. 7: Patented multi-feedback current control scheme [10]

This patented multi-feedback control scheme can also be implemented in a rotating reference frame which is used for field oriented control (FOC).

The system under discussion achieves 4 kHz current loop bandwidth at 8 kHz switching frequency [9].

3. Velocity Loop

Most modern controllers derive velocity feedback from the position sensor. In today's high performance digital servo drives the velocity signal is generated by utilizing a Luenberger Observer [11].

3.1 Position Feedback

The FPGA control board offers three feedback options: Resolver, digital Encoder and sin-cos-Encoder.

Resolvers are commonly used motor position sensing devices. Utilizing an FPGA based method to convert the analog resolver signals to a digital position signal using $\Sigma\Delta$ technology makes it possible to increase the resolution by 2-bit compared to sampling converters. The significantly better signal to noise ratio can be used to build a smoother motor current loop (less noisy), or to increase the tracking loop bandwidth. Due to the decimation filters the EMI noise from the IGBT Power stage is suppressed in a very efficient way. With this approach the flexibility of software RDC algorithms – observer with configurable bandwidth – are combined with the EMI ruggedness of a dedicated RDC circuit at no trade-off [11].

Optical sin-cos-encoders offer advantages in applications with special requirements:

- High precision / resolution
- High velocity loop bandwidth (high gain) and optionally
- Absolute position sensing (Multi-Turn).

The analog to digital conversion of rotary sin-cos-encoder signals for position acquisition is more and more accomplished within the encoder. Due to the digital link to the drive long cables do not reduce the feedback signal quality. The bidirectional digital sensor interface standards EnDAT®, BiSS® and Hiperface® DSL provide fast communication between position encoders and industrial drives. The logic for these digital Interfaces is usually implemented in an FPGA. Drawback is the additional signal delay due to the serial transmission of approximately 20 µs after sampling the position [12].

Using linear motors with special linear encoders still makes it often necessary to process the analog sin-cos-encoder signals. The FPGA based fine interpolation is utilizing two 12-bit SAR ADCs with 1 MHz sampling frequency. Conversion and interpolation – the effective signal delay – are executed in only 2 µs total. Optionally the sine and cosine analog offset and a gain correction can be configured for automatic on-line adjusting to compensate temperature drift effects of the analog signals [13].

3.2 Speed Control

The FPGA control card offers four speed loop configurations:

a) Closing the loop utilizing a VHLD coded PI controller is offering the fastest response time. The possible structures for anti resonance filtering are limited to the available FPGA resources.

b) Closing the loop with the embedded soft core CPU Nios® II including floating point extension allows limited utilization of Matlab®/Simulink® for an efficient control loop design.

c) Closing the loop in an IPC via EtherCAT allows Intellectual Property. TwinCAT® 3 from Beckhoff automation now features the possibility to use additional programming languages, such as C/C++ and Matlab®/Simulink® within the real time machine control task. Due to the very fast floating-point-unit, even complex control

algorithms can be programmed very easily [16].

d) Combining a VHLD coded controller in Hardware with an IPC control extension. For example a PI controller can be divided in two components:
   - The IPC can process the not time critical I-component via EtherCAT.
   - The P-component can be realized in hardware without any additional delay.

By utilizing the hardware (VHDL) PI-velocity-control scheme the system under discussion achieves more than 1 kHz velocity loop bandwidth. This is four times higher than industrial standard.

4. Position Loop

Today, many compact machine controllers use Intel®-compatible processors. The CX1030 Embedded PC from Beckhoff is such a device. Beckhoff TwinCAT PLC/NC software turns a PC with a Windows operating system into a real-time controller with cycle times from 50 µs, upwards.

Embedded PC with floating-point-unit

The task scheduler is configured in such a way that Windows operating system only receives the remaining CPU time that is not required by the real time controller. The motion control programming and path generation is always executed within a TwinCAT task utilizing the IPC floating-point-unit.

Performance wise there is not a large bandwidth improvement by closing the position in hardware, if the update frequency is high enough. The position loop bandwidth can achieve more than 300 Hz by using 62.5 µs position loop update rate. The position loop bandwidth is important to approximate the error compensation system dynamics. To build a system with an extreme low following error, a feed forward control structure is mandatory.

4.1 Feed Forward

By using a velocity feed forward signal the following error system bandwidth can be raised to the velocity loop bandwidth. The Bode-Plot of the closed loop shows significantly less phase and gain error up to 200 Hz.

Adding also acceleration (force / current) feed forward increases the position loop following error system bandwidth up to more than 1000 Hz.

The system under discussion uses double precision floating-point-math to calculate the feed forward signals, fig. 8. The position loop is closed by the IPC. The velocity command including the velocity feed forward comes as 32-bit signal via EtherCAT to the FPGA drive. The current feed forward requires only a 16-bit wide word.

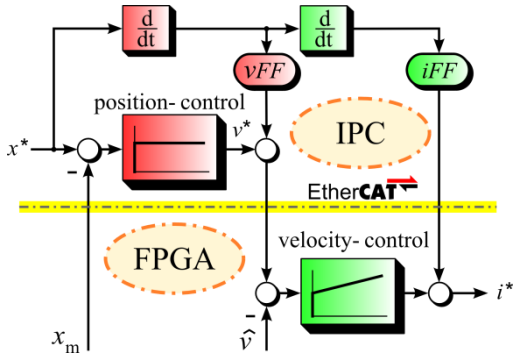

Fig. 8: Block diagram of the used motion control configuration

4.2 Intellectual Property

Until now, the use of intellectual property in motion control applications was rarely possible within the control loops. This is due to the limited calculation power of classical µcontrollers and DSPs. They were often programmed in “C” or “Assembler”. Time critical and interacting tasks often complicated the opening to application programmers. Today, due to the possibility of inherent parallel algorithm execution inside an FPGA most of these limitations disappear. The number of interacting tasks in motion control applications is reduced and complex algorithms can utilize the fast IPC processor.

An FPGA / IPC based motion controller offers following advantages.

- All standardized MS-Windows interfaces
- Programming and encapsulation of customer specific algorithms (IP) is possible
- The IPC can be used as development system on its own
- The development of customer specific algorithms can be done without knowledge of any programming language by using Matlab® Simulink®.

5. Experimental Results

Fig. 9 shows tool positioning plots from a fast tool lathe at three different frequencies. Even at an acceleration of 80 m/s² the following error is less than 1 µm.

The system is based on an ironless linear motor from Technotion, Netherland. Position feedback is realized with an optical 20 µm

linear encoder from Heidenhain. Current and velocity loop are closed in Hardware (VHDL). The FPGA is a Cyclone 3C40 from Altera. Approximately 30 000 logic elements are used. Motion programming, trajectory generation and feed forward calculation is done by a Beckhoff IPC at 20% CPU load (1.6 GHz, Core2duo, Windows XP, TwinCAT 2.11).

The IGBT based power electronics (3~400V_{ac} , 5 kW, Danfoss Model VLT FC-302P5K5) is operated with 300 V_{dc}, by a replaced FPGA-control-card designed by Cologne University of Applied Sciences.

IPC and FPGA drive are connected via EtherCAT fieldbus with 62.5 µs cycle time.

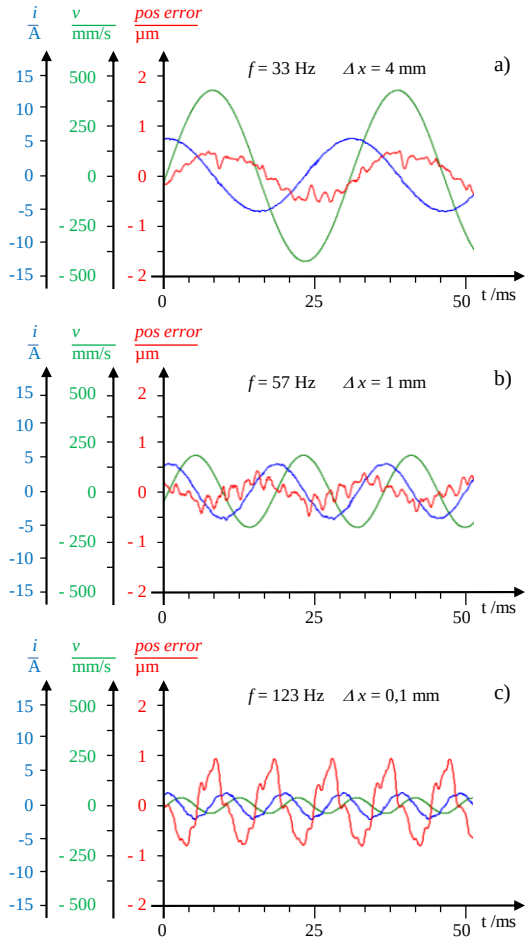

Fig. 9: Scope plot of current (acceleration) velocity and following error at three different frequencies.
Even at an acceleration of 80 m/s² the following error is less than 1 µm.

6. Summary

The paper describes a Field Programmable Gate Array (FPGA) based control system for low-inductance servo motors. The advantages of analog and digital control technology are combined due to digital signal processing in an FPGA. Generally, the control architecture of drive systems consists of three cascaded control loops. The innermost loop is the fastest, controlling the current. A new current observer generates a current signal with no attenuation and no phase lag.

Directly superposed to the new multi-feedback current loop is the velocity controller. It can be configured within the FPGA, in the embedded controller (IPC) or it can be separated between FPGA and IPC. The outer loop is the slowest controlling the position. The presented motion control system is implemented in conjunction with acceleration and velocity feed forward using a new developed control board with Altera Cyclone III FPGA technology connected via EtherCAT to an embedded controller. FPGA based control technology can combine the advantages of analog and digital control without any drawback. The new control board is driving a standard 5 kW frequency inverter power stage connected to an ironless linear motor with a linear measuring scale. Even with accelerations up to 80 m/s² the maximum following error is below 1 µm.

This new method provides an alternative to much higher switching frequencies, which stresses substantial power electronics, rarely available in cost optimized servo control environments, where the crucial requirement is always to provide high performance with minimized cost and size (= minimized swit-ching losses).

This innovative approach is based on several new technologies:

- ΣΔ-Bit-stream processing with three channels per current transducer
- New current observer without signal attenuation and phase lag
- Multi-feedback current controller (patented)
- Embedded PC with CNC functionality with Floating-Point-Unit and fast update rate via EtherCAT
- Standard µController based architectures would reduce the achievable precision and also the bandwidth due to the much slower current sampling and slower algorithm computing.

Acknowledgement

All implementation and testing of VHDL-algorithms was done on a Cyclone III FPGA control board developed at the Cologne University of applied since. The embedded controller (IPC) as well as the complete funding of this project was kindly provided by Beckhoff Automation GmbH, Verl, Germany.

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