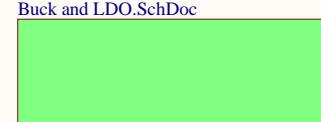


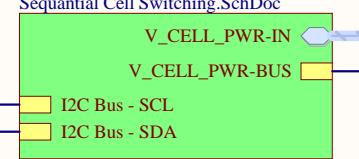
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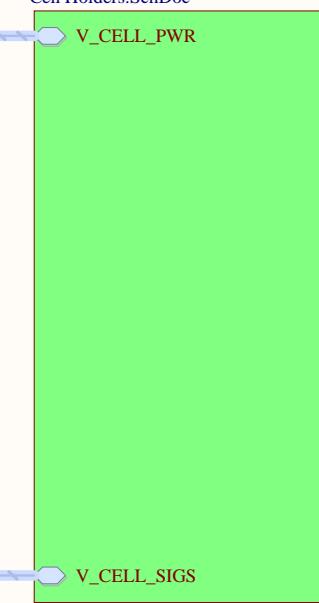
U_Buck and LDO
Buck and LDO.SchDoc



U_Sequential Cell Switching
Sequential Cell Switching.SchDoc



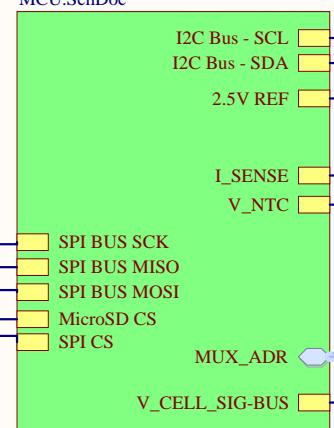
U_Cell Holders
Cell Holders.SchDoc



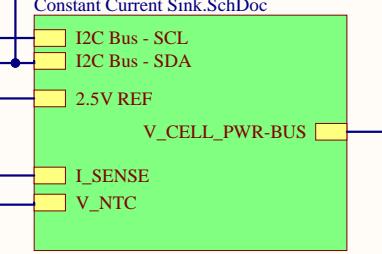
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B

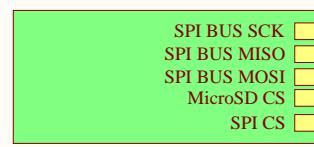
U MCU
MCU.SchDoc



U_Constant Current Sink
Constant Current Sink.SchDoc



U_MicroSD
MicroSD.SchDoc



C

C

Title

Size

Number

Revision

Date: 1-04-2026

Sheet of

File: C:\Users\..\TopLevel.SchDoc

Drawn By:

D

D

5V Buck / 3.3V LDO

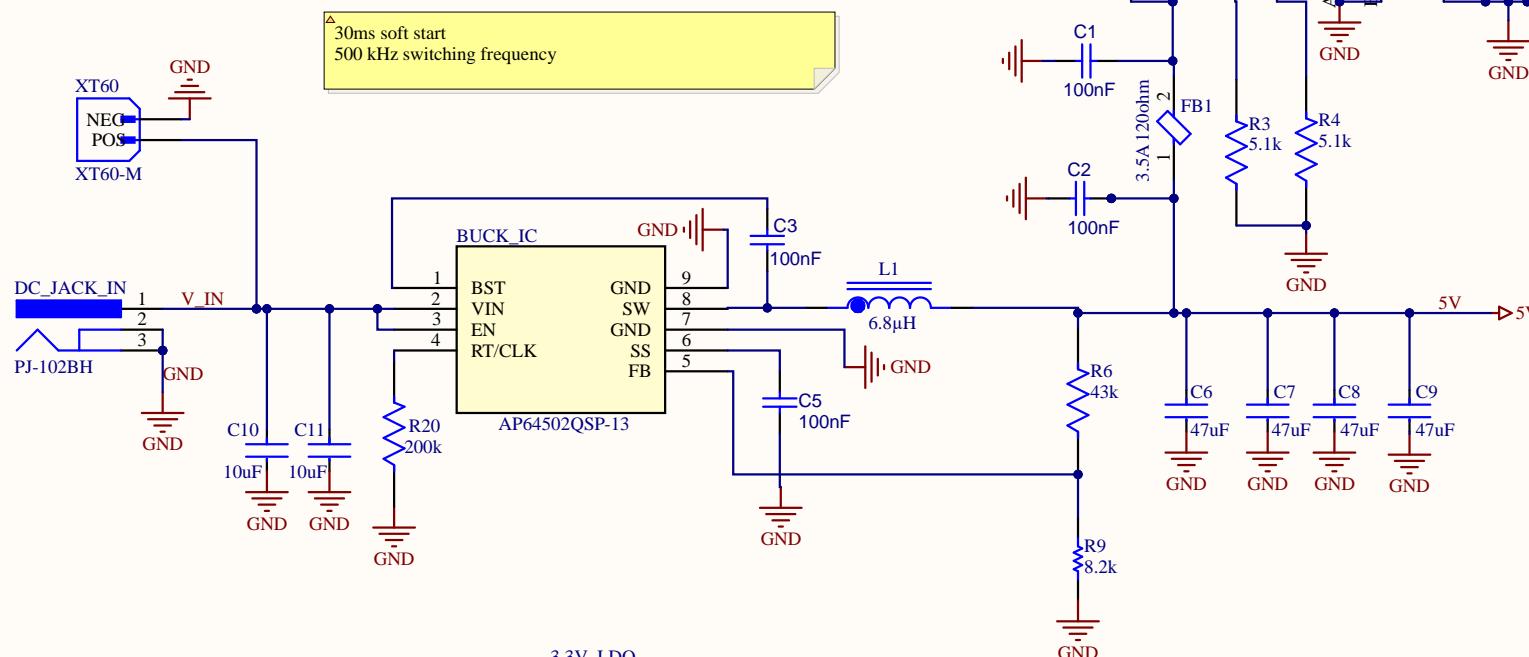
A

A

30ms soft start
500 kHz switching frequency

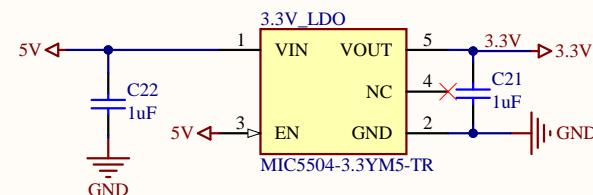
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B



C

C



D

D

Title

Size

A

Number

Revision

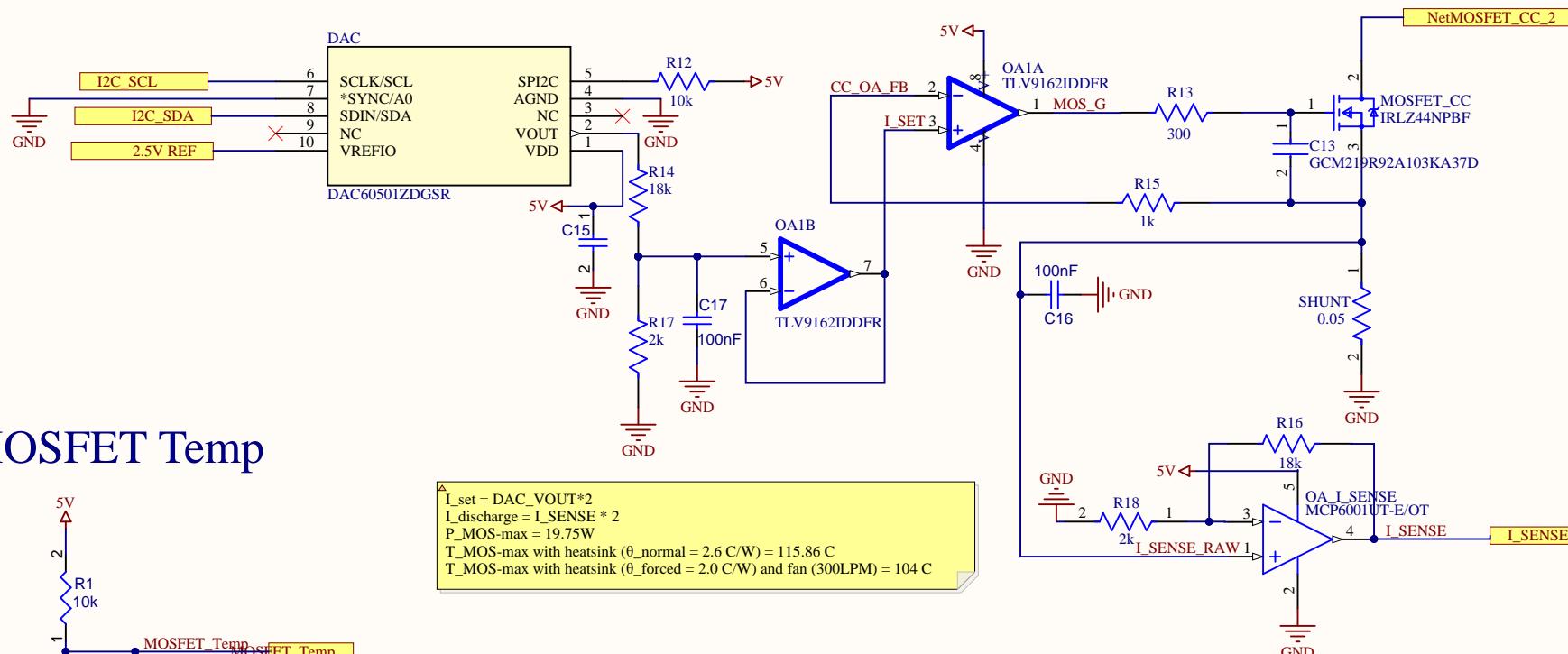
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Drawn By:

CONSTANT CURRENT SINK



Title		
Size	Number	Revision
A4		
Date: 1-04-2026	Sheet of	
File: C:\Users\.\Constant Current Sink.SchDoc		Drawn By:

CELL HOLDERS

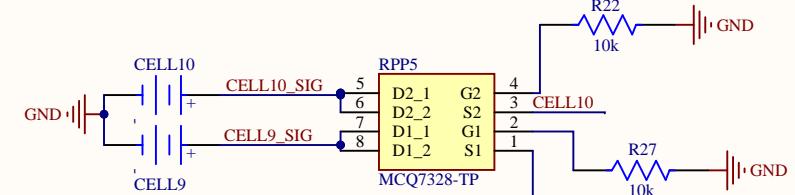
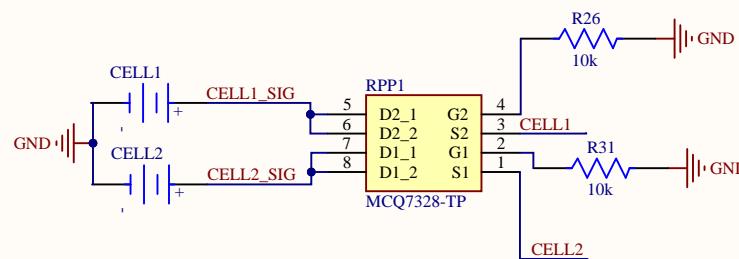
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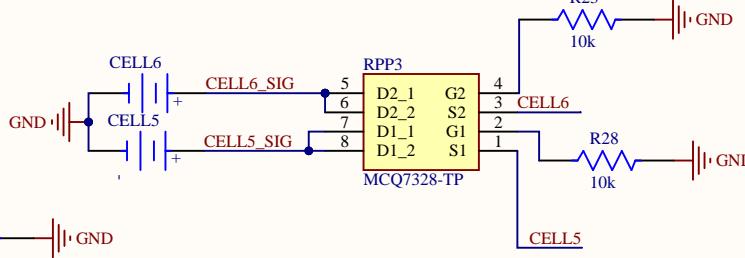
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4

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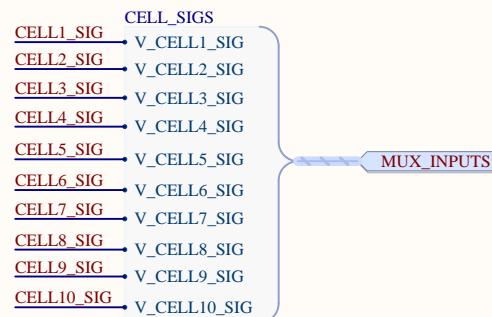
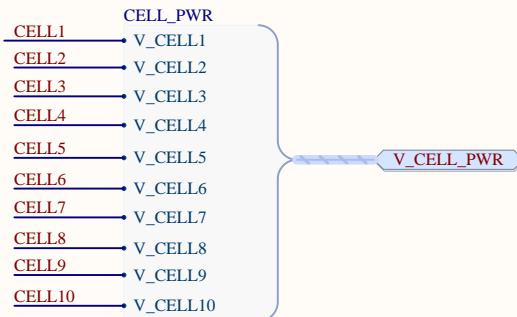
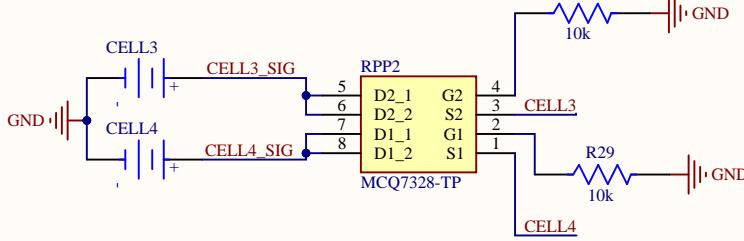


B



△ RPP1-5 are for reverse polarity protection. Approx voltage drop across D-S @ 5A is 140mv. SIG wires are added before RPP for kelvin sense

C



Title		
Size	Number	Revision
A4		
Date: 1-04-2026	Sheet of	
File: C:\Users\...\Cell Holders.SchDoc		Drawn By:

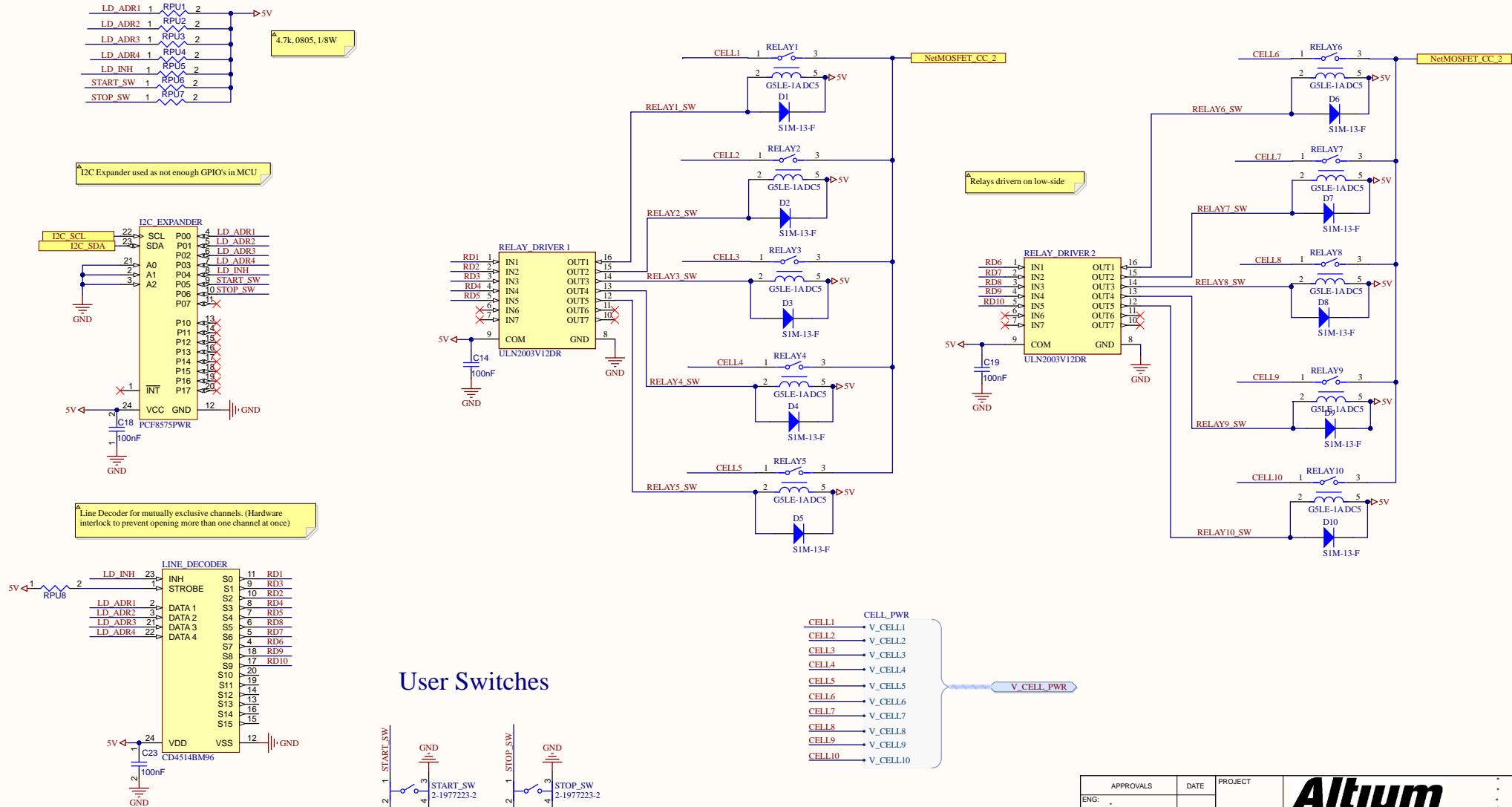
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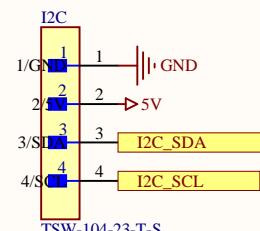
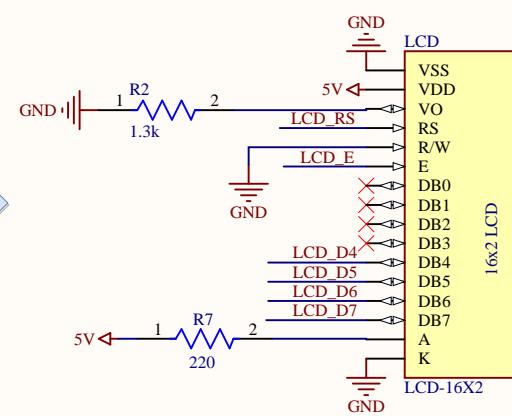
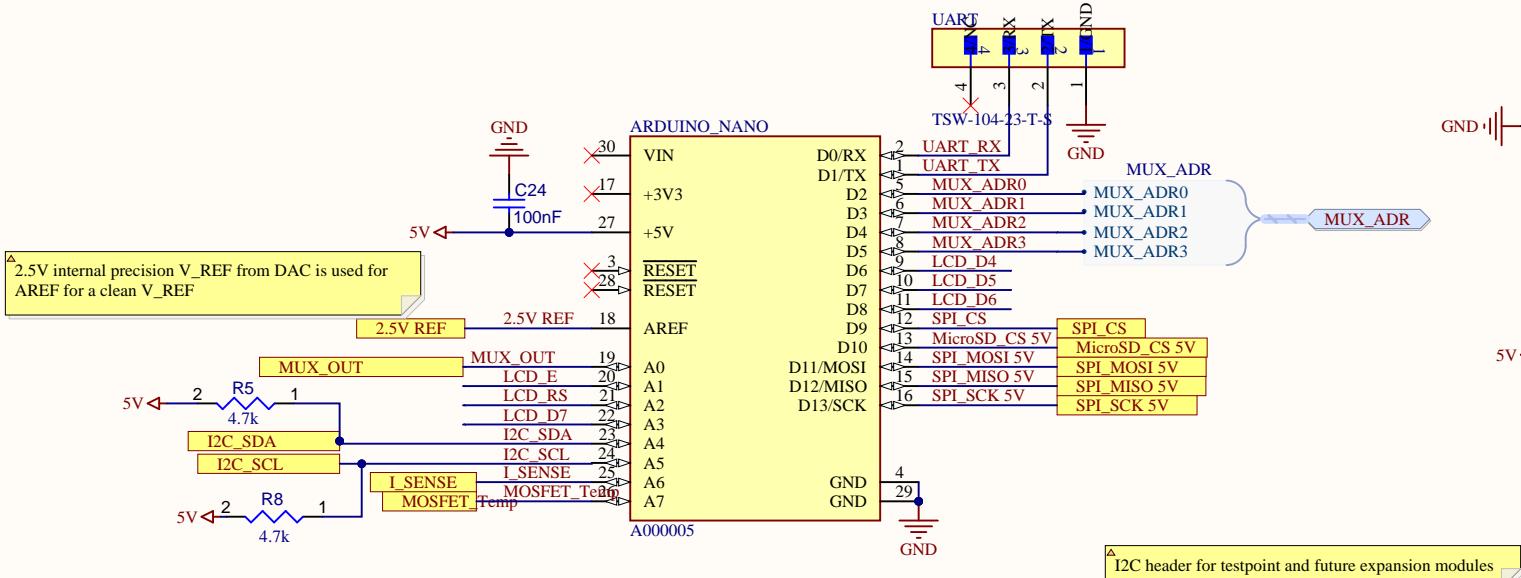
SEQUANTIAL CELL SWITCHING



APPROVALS	DATE	PROJECT
ENG: *		
DSN: *		
CHK: *		
REFERENCE DOCUMENTS		
BOM:	<BOM DOC NO>	
ASSY DWG:	<ASSY DWG NO>	
FAB DWG:	<FAB DWG NO>	
PCB DWG:	<PCB DWG NO>	
SIZE: B	CAGE CODE: ?????	DWG NO: <SCH DWG NO>
SCALE: 1:1	FILE NAME: Sequential Cell Switching.SchDoc	REV: 5 of 8

Altium

MCU (Nucleo / Nano)

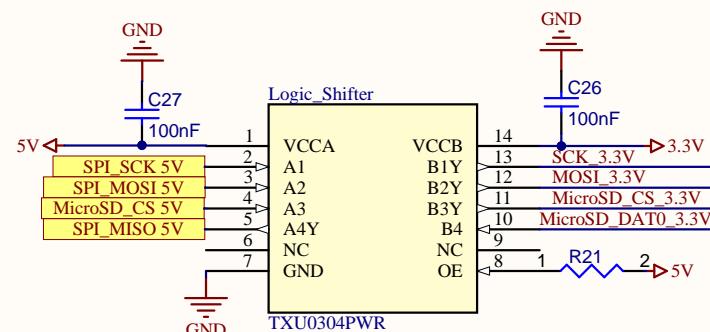


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Size A4	Number	Revision
Date:	1-04-2026	Sheet of
File:	C:\Users\...\MCU.SchDoc	Drawn By:

MicroSD

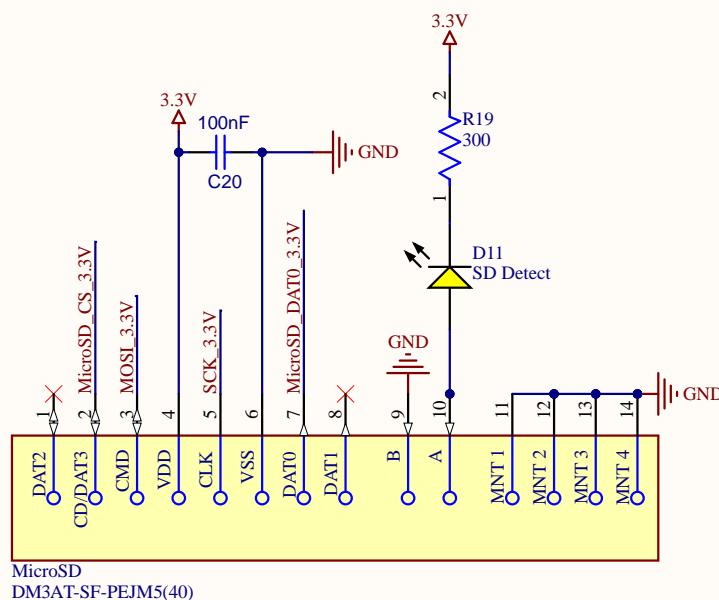
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B

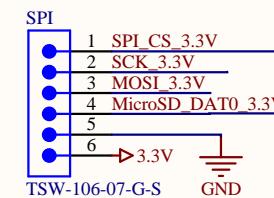
B



C

C

SPI header for testpoint and future expansion modules



D

D

Title

Size

Number

Revision

Date: 1-04-2026

Sheet of

File: C:\Users\...\MicroSD.SchDoc

Drawn By:

A

A

CELL MONITORING

B

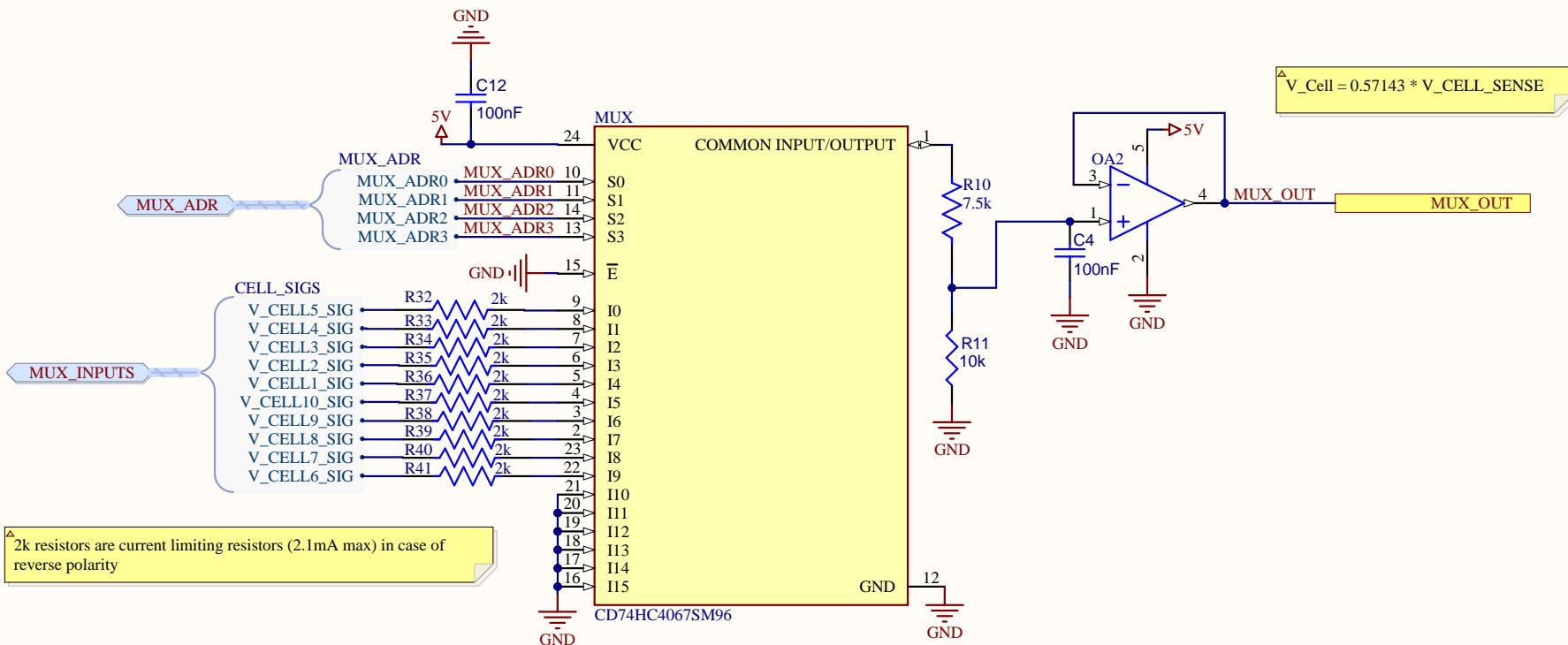
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C

D

D



Title

Size Number

A

Revision

Date: 1-04-2026

Sheet of

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Drawn By:

