

Ch16 Timer PWM Quiz ANS

1. Which register is used to divide the CPU clock frequency to generate a slower Timer Clock frequency?

- A. Auto-Reload Register (ARR)
- B. Capture Compare Register (CCR)
- C. Prescaler Register (PSC)
- D. Control Register (CR1)

ANS: C (Prescaler Register)

2. If the CPU Clock is 16 MHz and PSC is set to 15999, what is the Timer Clock frequency (fCK_CNT)?

- A. 16 MHz
- B. 1 MHz
- C. 1 kHz
- D. 100 Hz

ANS: C ($16,000,000 / (15999 + 1) = 1,000 \text{ Hz} = 1 \text{ kHz}$)

3. In Up-counting Mode, what happens when the Counter reaches the value in the Auto-Reload Register (ARR)?

- A. It stops counting immediately.
- B. It resets to 0 and generates an Update Event (UEV).
- C. It reverses direction and starts counting down.
- D. It waits for a software reset trigger.

ANS: B (Resets to 0 and generates UEV)

4. The formula for the Timer Period in Up-counting mode is:

- A. (ARR + 1) * Clock Period
- B. ARR * Clock Period
- C. (PSC + 1) * ARR
- D. 2 * ARR * Clock Period

ANS: A

5. In Center-aligned Counting Mode, the counter counts:

- A. Up from 0 to ARR, then resets to 0.
- B. Down from ARR to 0, then resets to ARR.
- C. Up from 0 to ARR, then Down from ARR to 0.
- D. Randomly between 0 and ARR.

ANS: C

6. Which PWM Mode behaves as "Low True" (Active Low) in Up-counting mode?

- A. PWM Mode 1
- B. PWM Mode 2
- C. Center-aligned Mode
- D. Capture Mode

ANS: A (Mode 1 is Low True/Active when CNT < CCR)

7. In PWM Mode 1 (Up-counting), if CNT < CCR, the output is:

- A. Active (High)
- B. Inactive (Low)
- C. Toggled
- D. Undefined

ANS: A

8. To increase the Duty Cycle in PWM Mode 1, you should:

- A. Decrease the CCR value.
- B. Increase the CCR value.
- C. Set ARR to 0.
- D. Increase the Prescaler (PSC).

ANS: B (Higher CCR means the "Active" condition CNT < CCR lasts longer)

9. How is the Duty Cycle calculated for PWM Mode 1?

- A. Duty Cycle = $1 - (CCR / (ARR + 1))$
- B. Duty Cycle = $CCR / (ARR + 1)$
- C. Duty Cycle = $(ARR + 1) / CCR$
- D. Duty Cycle = PSC / ARR

ANS: B

10. A timer runs from a 72 MHz clock. PSC = 71 and ARR = 999. In PWM Mode 1, CCR = 250. What is the duty cycle?

- A. 10%
- B. 25%
- C. 50%
- D. 75%

ANS: B (Duty = $CCR / (ARR + 1) = 250 / 1000 = 25\%$)