Ch9 64-bit Data Processing Quiz ANS

Q1. In 64-bit addition using two 32-bit registers per operand, which instruction pair is used to correctly propagate the carry from the lower word to the upper word?
A. ADD and ADD
B. ADDS and ADC
C. ADD and ADC
D. ADCS and ADD

ANS: B

Q2. In the example of 64-bit addition, which registers store the final 64-bit result?
A. r1:r0
B. r3:r2
C. r5:r4
D. r7:r6

ANS: C

Q3. For 64-bit subtraction, which instruction accounts for the borrow between the lower and upper 32-bit words?
A. SUB
B. SUBS
C. SBC
D. ADC

ANS: C

Q4. In ARM subtraction, how is a borrow represented in terms of the Carry flag?
A. Carry = 1 indicates borrow
B. Carry = 0 indicates borrow
C. Carry is unaffected
D. Borrow is stored in the N flag

ANS: B

Q5. Which instruction is used to test the sign bit of the lower 32-bit word during 64-bit sign extension?
A. CMP
B. AND
C. TST
D. TEQ

ANS: C

Q6. During 64-bit sign extension, what value is loaded into the upper word if the sign bit of the lower word is 1?
A. 0x00000000
B. 0x80000000
C. 0xFFFFFFFF
D. Unchanged

ANS: C

Q7. In the 64-bit multiplication example, which instruction computes the initial 64-bit product of the two lower 32-bit operands?
A. MUL
B. MLA
C. SMULL
D. UMULL

ANS: D