

L8-Memory System II Paging

1. In an OS that uses paging to manage its virtual memory, which part of the virtual address is used to index the page?

- A) frame number
- B) page offset
- C) page number
- D) frame offset

ANS:

2. If the size of virtual address is m bits, the page size is 2^n Bytes. How many bits are in the virtual address for the page number and the page offset, respectively?

- A) n , m
- B) m , n
- C) $m-n$, n
- D) $m-n$, m

ANS:

3. Which of the following statements are TRUE for paging?

- A) TLB reduces the number of memory accesses for paging.
- B) Paging may incur external fragmentation.
- C) Multi-level paging reduces the size of page table.

ANS:

4. Assume that we run a 64-bit OS on a device with limited physical memory, with a small page of 2KB.

1. How many bits are needed in the virtual address to represent the page offset?

ANS:

2. Given that the size of a page table entry is 4 bytes, How many page entries can be stored in a page?

ANS:

3. We use only 38 bits out of 64 bits for paging (i.e., a 38-bit virtual address). How many pages can be indexed by a 38-bit address space?

ANS:

4. 3-level paging is implemented in this system to reduce the page table size. The three page directories have the same size. How many bits are used for each level of the page directory?

ANS:

5. Which of the following statement is true about page replacement policy?

- A) A multi-level page table is used to reduce performance overhead.
- B) LRU always performs better than FIFO in terms of the number of page faults for all workloads.
- C) For a given page access sequence, increasing the number of page frames always reduces page faults for all replacement policies.
- D) Upon the first access of a page, two memory references are made.

ANS:

6. Which of the following statements are true?

- A) If the dirty bit of a page is set, it means the page has been modified and is different from the one on disk.
- B) Demand paging loads required pages in advance.
- C) Even using swapping, the virtual address size must be smaller than the physical address size.

ANS:

7. Given the following:

Address space size: 16 KB

Physical memory size: 64 KB

Page size: 256 bytes

7.1 How many bits are needed for the page offset in the virtual address?

ANS:

7.2 Given the following page table, what is the corresponding physical address for the virtual address 0x0bbc?

Page number VPN (Decimal)	Frame number PPN (hexadecimal)
0	0x00000051
1	0x0000006f
2	0x000000a5
3	0x0000003c
4	0x000000ea
5	0x000000c9
6	0x00000010
7	0x00000027
8	0x000000b4
9	0x00000064
10	0x0000001f
11	0x0000009a

ANS:

7.3 Assuming that the page table entries above have been loaded into the TLB. How many TLB misses will occur when the process accesses the following 14 virtual addresses?

0x04db
0x07ad
0x03ef
0x06b8
0x0Ad7
0x0985
0x0D17
0x0B62
0x0264
0x007d
0x05fb

0x0876
0x012f
0x0C15

ANS:

7.4 If TLB lookup time = 1 cycle, Memory access time = 100 cycles

Assuming there is no cache. What is Effective Access Time with TLB for the above address sequences?

Reminder:

$$EAT = \text{Hit Time} * \text{Hit Rate} + \text{Miss Time} * \text{Miss Rate}$$

$$= (m + \sigma) \eta + (2m + \sigma)(1 - \eta) = 2m + \sigma - m \eta$$

ANS:

8. Multi-level cache. Consider a two-level cache L1 and L2 with the following timing parameters:

L1 Hit Time: 1 cycle, L1 Miss Rate: 10%

L2 Hit Time: 10 cycles, L2 Miss Rate: 1%

Main Memory access time: 100 cycles.

a) What is the global miss rate?

b) Calculate the Average Memory Access Time (AMAT).