Heterogeneous Systems Architectures

Lab project

Design and implementation of an image processing heterogeneous digital system

V1.0 – 10th Nov 2023

Revision history

Date	Notes	
Nov 10th, 2023	First release V1.0	jca@fe.up.pt

1. Objectives

The objective of the project is to design a heterogeneous hardware-software system for the ZedBoard development platform, which implements an image processing application given as a C program. The system should be optimized for performance, constrained to the logic resources available in the Zynq device of the target platform.

The work is divided into four main tasks, corresponding to 4 accomplishment goals:

i) Analyze the source software application and study the potential of acceleration when implementing selected tasks as custom hardware accelerators.

ii) For the selected application tasks, design the hardware processing system using High-Level Synthesis and explore adequately the solution design space to optimize the tradeoff between performance and logic complexity.

iii) Build a hardware-software system integrating the custom hardware blocks built in ii) with the ARM9 processing system of the Zynq device; the objective at this stage is to assemble a first functional HW/SW system, before optimizing the data transfer mechanisms between the software and the hardware domains.

iv) Optimize the data transfer processes between the software application and the custom hardware accelerator (using DMA transfers, data streaming interfaces or AXI4 data burst transactions…).

Details on the application are presented in section 3.

2. Grading

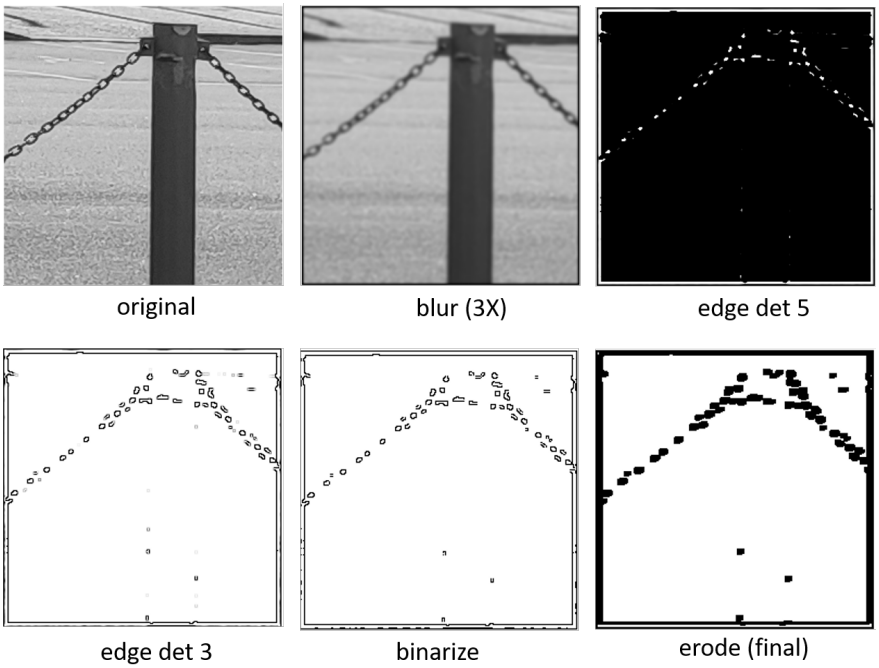
The final grading will be based on the level of realization of the 4 goals listed above, with the following relative weights. Each task will be evaluated between 0 (poor) to 5 (excellent).

task		weight
i)	Application analysis	20%
ii)	HLS design synthesis	30%
iii)	System integration and implementation	30%
iv)	System optimization	20%

3. The C application

The target application implements a sequence of image processing tasks on a 8-bit per pixel gray-scale image, to extract a set of features collected to an output binary image (1 bit per pixel). The input image is read from a text file created by a Matlab/Octave script. The size of the image to process can be configured in the software application and Matlab scripts.

The sequence of images below illustrates the intermediate results of the sequence of the image processing tasks: (i) the original image is blurred; (ii) a 5x5 convolution followed by a 3x3 convolution perform an edge detection filter, (iii) the image is binarized with a fixed threshold (128) and (iv) an erode function is applied to enlarge the regions detected with the previous filters.



The application is implemented in program **aship.c**. The program reads a text file with the input image and writes the output image to a text file. The input text file can be created from a bitmap image by running the Matlab script **im2text.m** and the output text file containing the output image can be converted again to a bitmap image with the script **text2im.m**.

Alternatively, the C code can use the include file **datain.h** also created by the Matlab script **im2text.m** to embed the input image in the C source code (comment out the directive **#define LOAD_FROM_FILE** to disable the file access and use the image included in the code). This will be needed when running this application in the Zynq platform because there is no support for file handling.

Compile the program with the command **gcc aship.c –o aship** or just running **make**. The set of files provided already contain a 512x512 pixel test image selected from the picture **FEUPin.jpg**. In the Matlab script **im2text.m** you can select the pixel position of the top-left corner of the 512x512 window and in this script and the application the image size may also be changed.

Run the program with: **aship datain.txt dataout.txt** and then run the Matlab script **text2im.m** to display the output image and create a JPG file.

The archive provided for this project is organized in 4 folders:

./doc	documentation files (includes this guide and the Vitis HLS UG1399-2020)
./aship	C source files of the image processing application (compile with *make*)
./data	image file and text files created/used by the Matlab/Octave scripts
./Matlab	Matlab/Octave scripts to convert between bitmap images and text files used by the application

4. The project

As said before, the objective if this project is to build a hardware/software heterogeneous system to optimize the performance of the C application, adding a custom accelerator to the Zynq processing

system. The custom IP blocks that implement the custom accelerator will be designed using the XILINX Vitis HLS high-level synthesis design flow.

The HLS optimization should consider various strategies to explore adequately the solution design space: code reorganization (eg. splitting/merging functions), choosing appropriate data types, loop optimization, interface design and partitioning arrays, either temporary arrays or the arrays used as interface.