Guilherme A. Barcelos

MSc in Electrical and Computer Engineering, specializing in FPGA/ASIC design and hardware systems, seeking a role in the semiconductor industry

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Education

Faculty of Engineering, University of Porto – Portugal **2019-2024**

Master's and **Bachelor's** in Electrical and Computer Engineering. Specialization: **Telecommunications**, **Electronics**, and **Computers**. Key Projects: Developed an audio processing **accelerator** in **Verilog** for **Xilinx FPGAs**, verified with **Vivado**; Designed an OpAmp **ASIC** using **Cadence** tools; Implemented a vision **accelerator** using **HLS** on a **Xilinx FPGA** + ARM SoC; Built a custom distance **sensor** for a **signal processing** coursework.

Technical University of Munich – Germany **2023**

Exchange Semester – Focus: **RTL Design**, **Embedded Systems**, and HW/SW Codesign; Courses: **Circuit Design** for Security, HW/SW Codesign, **VHDL** System Design Lab; Project: Designed and implemented a functional clock in **VHDL** on a Zynq7000 FPGA.

Professional Experience

Synogate (Berlin) – Internship & Master Thesis **2024**

Designed an optimized **RTL** Top-K module for **FPGA**-based **AI accelerators**, achieving a **100x** improvement in **resource efficiency** and a significant reduction in **power consumption**. Enhanced the performance of **large language models** (**LLMs**) by optimizing the softmax function with a heap-based **architecture**. Developed using **Gatery** (**C++**) on **Intel FPGA** platforms. Demonstrated and improved proficiency in **hardware design**, **RTL development**, and **FPGA optimization** for **AI applications**.

Deloitte (Porto) – Curricular Internship **2022**

Analyzed the potential for **mmWave** adoption in Portugal through **market** and **technology research**, delivering **strategic insights** on **5G** use cases, industrial applications, and consumer impacts to the Telecom Engineering Center of Excellence (TEE).

Extracurricular Activities

Aerospace and Electronic Systems Society (AESS) – Chairman **2022-2023**

Led the Tarvos Project, prototyping a **model rocket** with **LoRa**-based **communication** and ensuring **system integration** across the project. Transitioned the project into the Porto Space Team, enabling further development.

Porto Space Team – Member **2022-2023**

Defined **system requirements** for a competition **model rocket** and developed base **electronic systems** to **guide new team members**. and **mentored** colleagues on **systems engineering** and subsystem development.

IEEE UP Student Branch – Executive Commitee Secretary **2021-2022**

Recruited new members, **communicated** between teams, university and companies, and **documented** key decisions and meetings.

Debating Society of University of Porto – Member **2021-2022**

Enhanced skills in **argumentation** and **public speaking**. Supported the association with video editing and website management.

Skills

Languages: Portuguese (Native), English (C2), Spanish (A1), Italian (A1), German (A1)
FPGA/ASIC Design: Quartus, Vivado | VHDL, Verilog, HLS | Vivado Simulator, QuestaSim, GTKWave
Embedded Systems: ESPs, Arduino | Microcontroller Programming
Programming/Scripting: Git, C, C++, Python, Bash/Shell, MATLAB, Java
System Administration: Linux, Server Management, Networking
Soft Skills: Team Leadership, Collaboration, Critical Thinking, Adaptability to Multicultural and International Teams, Self-Learning

Prizes

Red Bull Paper Wings – National Champion & World Finalist (2022)

Achieved **national champion** status and represented Portugal in the **world finals** of the Red Bull Paper Wings competition in the Time of Flight category.

Incentive for International Students (2019–2022)

Consistently awarded by the Faculty of Engineering of the University of Porto for having an **outstanding** entry grade and maintaining academic **excellence**. Led to a reduced tuition fee over four consecutive years.