TÉCNICO LISBOA

Circuit Theory and Electronics Fundamentals

T4 Laboratory Report

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Group 61

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1 Introduction

In this laboratory assignment, we analysed, using both a theoretical and simulation analysis, a Sound Amplifier made of Bipolar Junction Transistors. It was made up of two different stages, a Gain stage, with the goal of having the maximum gain possible, and an output stage, whose goal was to lower the impendance. The circuit is presented in **??**.

As mentioned above, we analysed the circuit theoreticaly, combining Operating Point, allowing us to derive important values used in the incremental analysis.

Simultaneously, the circuit is analysed by computational simulation tools, via *Ngspice*, and the results are compared to the theoretical results obtained, in Section 2. The conclusions of this study are outlined in Section 4.

We also used Ngspice to analyse the circuit by computacional tools, and then compared with the results obtained in 2. The results of this comparison are outlined in 4.

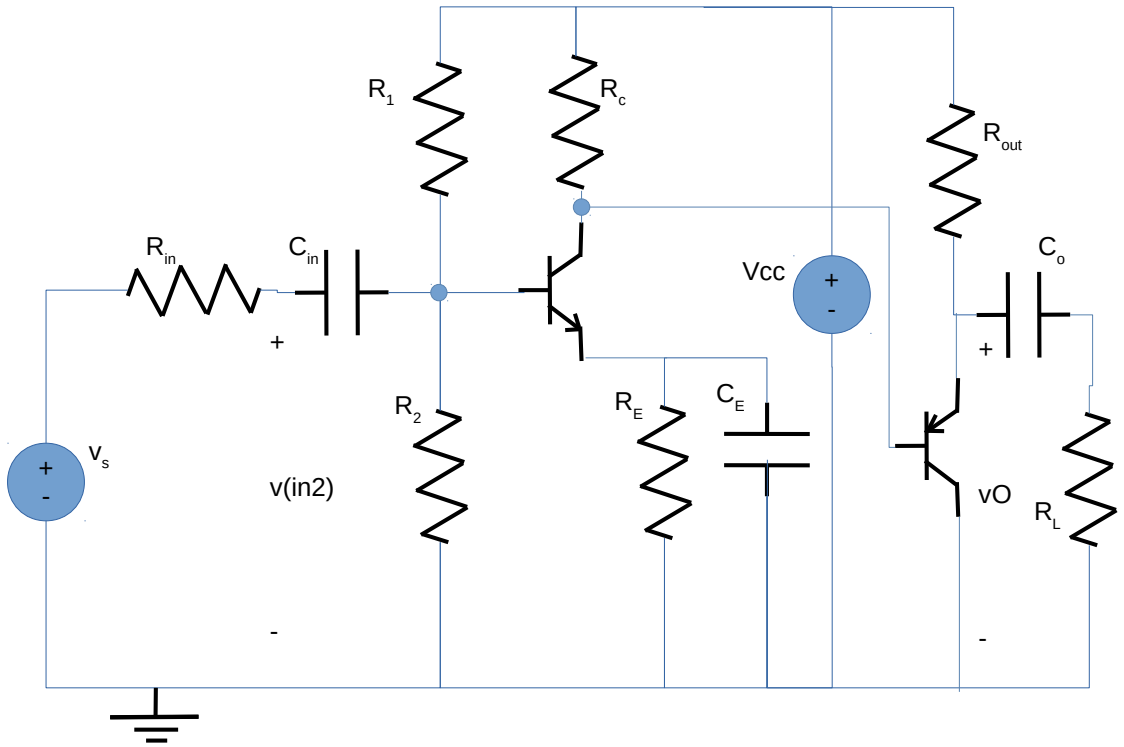


Figure 1: BJT Amplifier

2 Theoretical and Simulation Analysis

We will be dealing with the simulation and theoretical analysis at the same time. Next we present a table of constans that will be used.

Name	Value	Units
R_1	33.7	$k\Omega$ [kOhms]
R_2	3.6	$k\Omega$ [kOhms]
R_C	3.8	$k\Omega$ [kOhms]
R_E	200	Ω [Ohms]
R_{out}	400	Ω [Ohms]
C_{in}	800	μF [μFarads]
C_E	800	μF [μFarads]
C_o	600	μF [μFarads]

Table 1: Constants Values

2.1 Gain Stage

The Gain Stage of the circuit is responsible for insuring a high input voltage so the input signal is not degradated through the circuit. It has ana elevated gain and is the part responsible for signal amplification.

There are 3 types of elements: a NPN BJT, resistors and capacitors.

The first capacitor, C_{in}, is a coupling capacitor, as it acts as a DC Block, so that V_{in} doesn't impose a DC component of 0, that would change the OP of the transistor.

The second capacitor, C_E, acts as a bypass capacitor, for it ensures that for low frequencies all the current flows through R_E, and for high frequencies, it passes through the capacitor.

The output impedance of this stage (Z_{O1}) is high.

2.2 Output Stage

The Gain Stage has a high Z_{O1} soto counter this, we connect a circuit with low output impedance to the first one. This circuit presents similar components but with very distinct results.

Instead of a NPN BJT, we use a PNP BJT, because it has a higher β_F, which lowers the output impedance.

Another capacitor, C_o, is used with a similar goal as the previous coupling capacitor. If we didn't use such component, the gain stage would impose a DC voltage of 0 to the second stage, which would ruin the transistor's OP.

As we'll see, we end up with a lower output impedance in this stage and a higher input impedance (when compared to the output impedance of the gain stage).

When combining both stages, we need to ensure that there is a compatibility between the impedances, the input impedance of the second stage should be much greater than the output impedance of the first one.

2.3 Theoretical Analysis

In the theoretical analysis we will evaluate the four impedances associated with the two stages (Z_{I1}, Z_{O1}, Z_{I2} and Z_{O2}) and the two gains in each stage (A_{V1} and A_{V2}).

2.3.1 Impedances

In the fist stage we can finde the input and output impedances ($\{Z_{I1}$, $Z_{O1}\}$)using KVL and KCL.

$$Z_{I1} = R_B//r_{\pi 1} \tag{1}$$

where $R_B = R_1//R_2$.

We assume $R_E \simeq 0$ (capacitors are short-circuted). The first stage input matches the total input impedance of the circuit.

The first stage output impedance can be obtained by:

$$Z_{O1} = r_o//R_C \tag{2}$$

For the second stage, by analysing the circuit we get:

$$Z_{I2} = \frac{(g_{m2} + g_{\pi 2} + g_{o2} + g_{E2})}{g_{\pi 2}(g_{\pi 2} + g_{o2} + g_{E2})} \tag{3}$$

$$Z_{O2} = \frac{1}{(g_{m2} + g_{\pi 2} + g_{o2} + g_{E2})} \tag{4}$$

And finally, the total output impedance:

$$Z_{OT} = \frac{v_o}{i_o} = \frac{1}{g_{o2} + g_{m2}\frac{r_{\pi 2}}{r_{\pi 2}+Z_{O1}} + g_{E2} + \frac{1}{r_{\pi 2}+Z_{O1}}} \tag{5}$$

The 4 values are presented below,

Impedances	**Ohms (Ω)**
Z_{I1}	1290.209759
Z_{O1}	3411.452239
Z_{I2}	37245.135442
Z_{O2}	1.375831
Z_{OT}	15.566019

Table 2: Theoretical Impedances

Remembering that Z_{O1} needs to be much lower than Z_{I2}, we end up with good results. This is needed so that there is no signal degradation or loss between these stages.

2.3.2 Gain

To calculate the total gain (A_V) we performed a simple multiplication $A_V = A_{V1}A_{V2}$. The real interaction between both stages is negligible, and so we can compute the gain as if it was the total gain of both separate stages.

To acquire a better comparison between theory and simulation, besides this aproach, that considers the gain to be constant through all the frequencies , we also performed the *Time constant method* for the lower cut-off frequency.

We calculate the lower cut-off frequency ($\omega_L = 2\pi f_{CO_L}$) as,

Gain	Value
G_1	-264.565721
G_2	0.991532
G_T	-252.275561
$G_{T_{dB}}$	48.037504

Table 3: Theoretical upper gain bound results

Gain	Value
G_1	-17.126226
G_2	0.991532
G_T	-16.330643
$G_{T_{dB}}$	24.260066

Table 4: Theoretical lower gain bound results

$$\omega_L = 1/R_{eq_i}C_i + 1/R_{eq_e}C_e + 1/R_{eq_o}C_o \implies f_{CO_L} = 2\pi w_L \tag{6}$$

where $R_{eq} \equiv$ equivalent resistor as seen by each capacitor when the others are short-circuits.

We have,

$$R_{eq_{in}} = R_{in} + Z_{I1} \tag{7}$$

$$R_{eq_e} = R_E//(\frac{1}{\frac{1}{R_s||R_B+r_\pi} + \frac{g_m r_\pi}{R_s||R_B+r_\pi}}) \simeq R_E//(\frac{r_\pi + R_s||R_B}{r_\pi}\frac{1}{g_m}) \simeq 1/g_m \tag{8}$$

$$R_{eq_o} = R_L + Z_O \tag{9}$$

The theoretical value of the lower cut-off frequency is presented in the table below.

Name	Value [Hz]
Lower CO freq	28.296662

Table 5: Theoretical Lower Cut-off frequency

2.4 Simulation Analysis

In the Simulation Analysis, we want to get the two impedances associated with the circuit, the two cut-off frequencies, f_{CO_L} and f_{CO_H}, the bandwidth and the total gain, A_V. We also check whether the BJT's are on the Forward Active Region (FAR), by comparing V_{CE} and V_{BE} for the NPN, and, analogously, V_{EC} and V_{EB} for PNP.

Name	Value
V(CE)	3.41818
V(BE)	0.667497
V(CE) greater than V(BE)	Yes

Table 6: NPN voltages and FAR confirmation

Name	Value
V(EC)	4.59871
V(EB)	0.730469
V(EC) greater than V(EB)	Yes

Table 7: PNP voltages and FAR confirmation

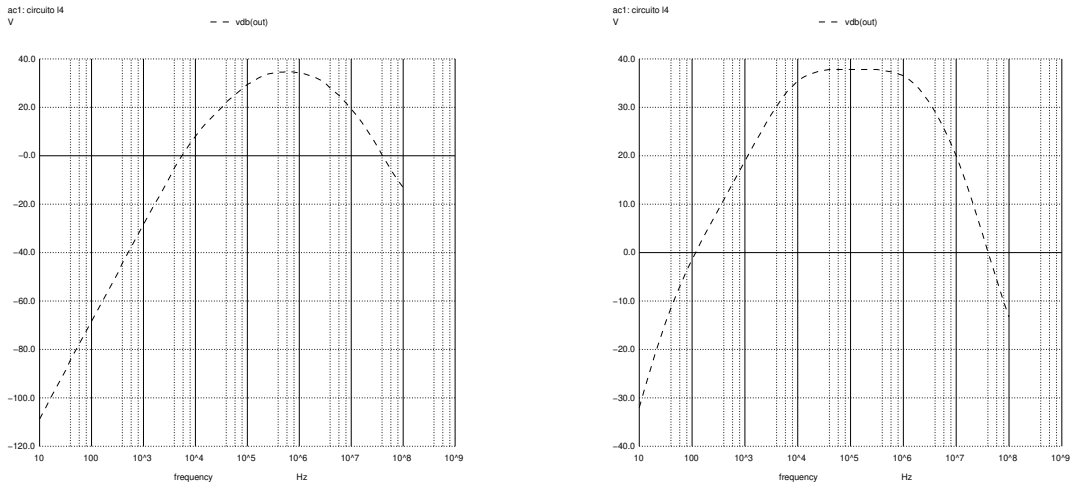
The results are presented in the table below:

Name	Value	Units
Gain (dB)	36.1296	dB
Gain	63.8779	
Lower CO Freq	19.9163	Hz
Higher CO Freq	1.37411E+06	Hz
Bandwidth	1.37409E+06	Hz

Table 8: Simulation results

2.4.1 Coupling Capacitors

To be able to analyse the circuit, we need to understand the Coupling Capacitor's behaviour. In our amplifier we have two coupling capacitors, C_O and C_{in}, but due to the analog nature of the functions, we will focus on the capacitor C_{in}. The two figures of the frequency response analysis are presented below.



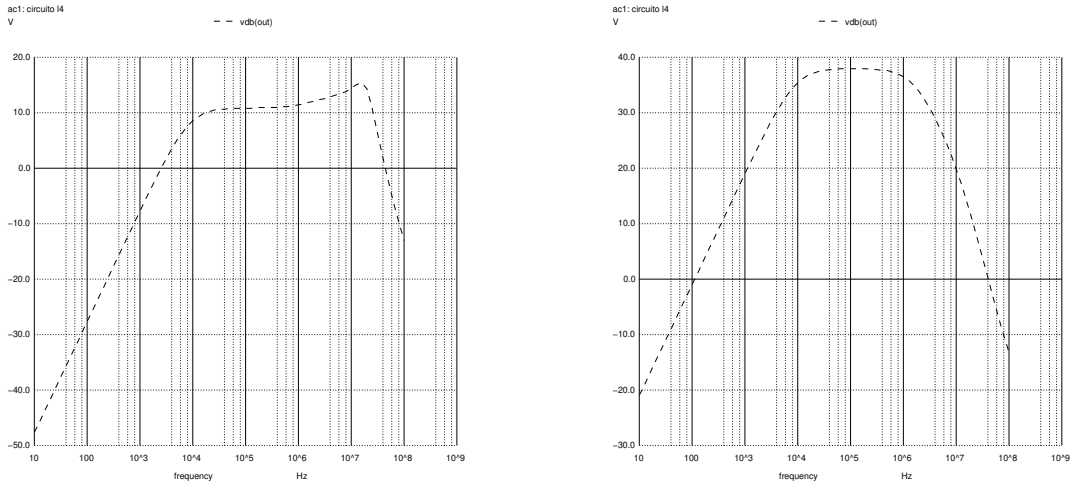
(a) C_i low ($1nF$) (b) C_i high ($1F$)

Figure 2: C_{in} influence

We can see that the increase of the capacitance pushes the cut-off frequency to the left and, without altering the higher cut-off frequency, anticipating it, wich generates a larger bandwidth. As discussed previously, as $\omega \to 0$, $Z(C_{in}) \to \inf$, this is not surprising, so this capacitor prevents the transistor from entering the cut-off regions or the saturation, by blocking the DC component of the Audio In source. This helps the transistor operate at lower frequencies by mantaining the OP of the transistor, as C_{in} increases.

2.4.2 Bypass Capacitor

The two figures of the frequency response analysis, by changing the parameter C_E, are presented below.



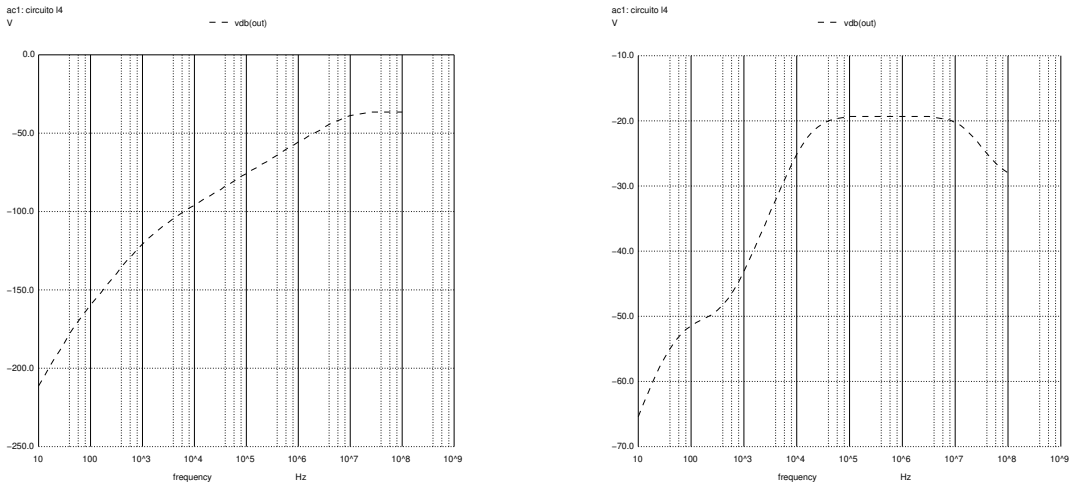
(a) Low C_E effect on Gain ($1nF$) (b) High C_E effect on Gain ($1F$)

Figure 3: C_E influence

Due to the placement of the bypass capacitor in parallel with R_E, this resistor becomes short for high and medium freuqencies. The amplifier's first stage gain being inversely dependent on this resistance leads to the bypass capacitor playing an extremelly importante role in maximizing the gain for high and medium frequencies.

2.4.3 R_C

To conclude, we need to analyse the role of R_C on the total gain of the circuit. We also present assymptotical situations in order to fully understand that behaviour.



(a) Low R_C effect (on the Gain) (10Ω)

(b) High R_C effect on Gain (10$k\Omega$)

Figure 4: R_C influence (on the Gain)

We can see that the gain increases with R_C and also antecipates de passband. This behaviour matches the predictions given by the theoretical analysis on the gain, due to being proporcional to R_C.

To guarantee a high compatibility with speakers and AUDIO IN, we simulate the input and output impedances of the circuit. The goog compatibility is guaranteed with a high input impedance, Z_I, and a low output impedance, Z_O. The results are presented in the tables below.

Name	**Value [Ω]**
Input Imp	-1233.51 + 277.892 j
Absolute Value	1264.42

Table 9: Simulation Input Impedance

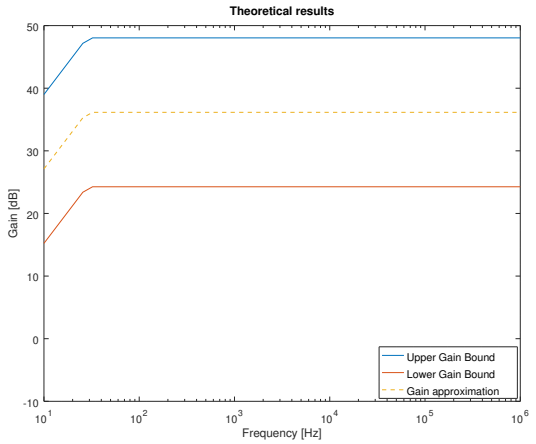
Name	**Value [Ω]**
Output Imp	21.808 + 0.737357 j
Absolute value	21.8204

Table 10: Simulation Output Impedance

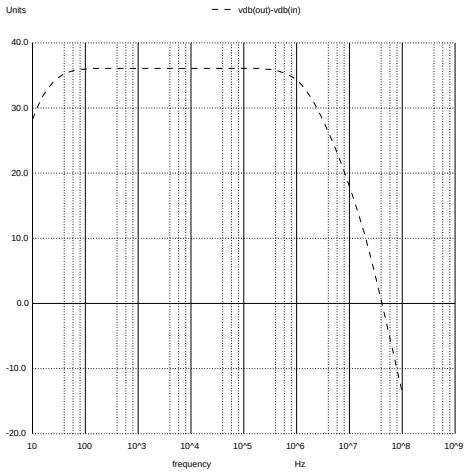
In similarity with the theoretical analysis, the simulation gives off a slightly high output impedance. This is due to the compromises needed fot the merit system.

2.5 Comparison

We are now going to compare theoretical and simulation values.



(a) Theoretical Gain



(b) Simulation Gain

Figure 5: Gain

Above we can see theoretical and simulation graphs of the gain.

In this case, the comparison of the shape can only be done on the left side, since we don't have the theoretical higher cut-off frequency. For this reason, there's no point in plotting the theoretical gain any further than $1MHz$.

The theoretical analysis takes in acount that all capacitors are short-circuted or open-circuted, leading to two different plots one in blue and the other one in orange, respectively. This leaves us with a region of acceptance for the simulation gain, that fits in this region for the interval in study. The yellow plot is the average gain, wich should be a better approximation of the real gain. Considering both graphs we can also comment on their similar shape that confirmes the match of our theoretical aproach. Looking back on the studied values of each the theoretical and the simulation analysis (Z_I and Z_O, A_v and f_{CO_L}), we can confirm that they have the similar orders of magnitude, wich gives us an aproximation within reason.

3 Merit Results

Using the results obtained through the Ngspice simulation (see Section 2.5) and having in mind that we used the data shown in Section 1, we can compute the price and the merit using the *formulae* given in the lab assignment:

The price obtained was 2242.01 and the merit was 1965.72.

We chose to firstly understand what would be produced by each component when its values changed dramatically. So we analysed the circuit *assymptotically* in order to acquire a bigger notion of what would be influenced by each component.

After having a good notion about that, we just made small adjustments get our results as perfect as possible, which made the merit rise. By using this approach, the cost was left as a second thought.

To end, we started decreasing the cost until we found what we thought was a good balance, giving the results presented above.

4 Final Conclusion and General Notes

To conclude this assignement, we can say that simillar to the previous assignment, there is not a major degree of similarity between both analysis, in regards to precision. This was predicteble due to the fact that we are dealing with a non.linear circuit and the model used by *Ngspice* is way more complex than the theoretical model used - the Incremental analysis one, presented on classes, only includes 2 resistors and a dependent current source. Altough these may be differente, the theoretical model gives an overview of the behaviour, so it is very useufl if we dont have the simulation tools available, or to very quickly verify the simulation results obtained.

With all of this present, this laboratory assigment as given us the opportunity ti deepen our knowledge regarding BJTs and how we can implement them to develop circuits with different purposes - in our case, an AUDIO Amplifier, even though the real model amplifiers are far more complex than the circuit implemented, achieving gains of around 115 dB. On the other hand, we were able to use new concepts such as the *Time constant method*, the incremental models, the input and output impedances and the gain (these, eventough already familiar, allowed us to gain flexibility and easiness).

Observing our results, and especially the simulation ones, our main goal was to have a high gain and a large enough bandwidth that would cover at least 20Hz to 20kHz, which are the correspondent values to the human hearing range. We can say that the results observed more than cover the range mentioned before, and would be suitable for a real audio amplifier. Knowing this, one way we could improve our circuit would be to increase the gain even more, which it's not in our power to do.