ECM 245 – Arquitetura e Organização de Computadores

INTEL STRATIX 10

GRUPO

- Enricco D L Amaral 17.00165-0
- Fernanda Veneroso de Almeida 17.00122-9
- Paulo Belo Kaari Fernandes 16.00962-2
- Xiaoying He 17.00670-8
- Karina L. D. Kuroda 17.00709-7

O INTEL STRATIX 10: MODELOS

Intel® Stratix® 10 GX FPGAs

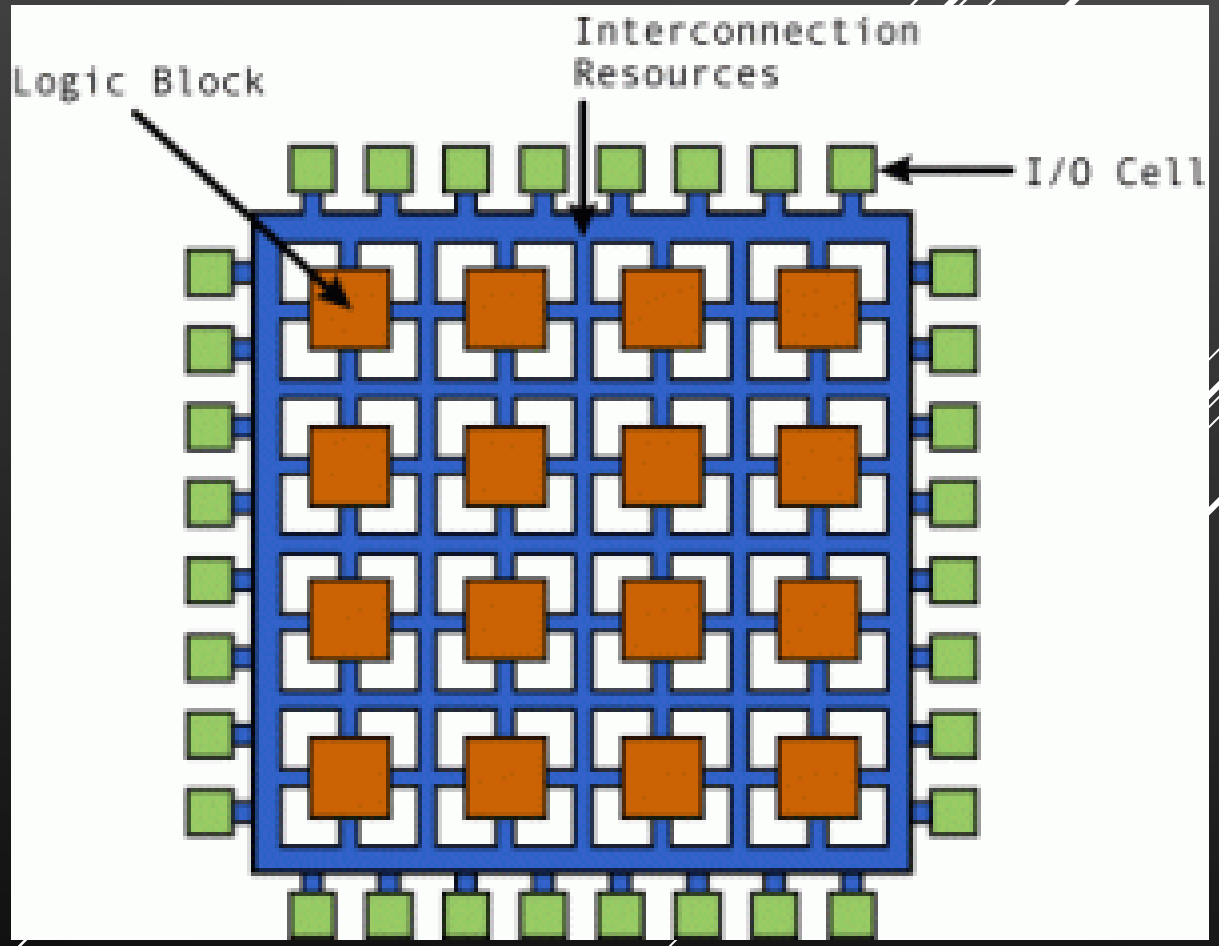
Intel® Stratix® 10 SX SoC FPGAs

Intel® Stratix® 10 TX FPGAs

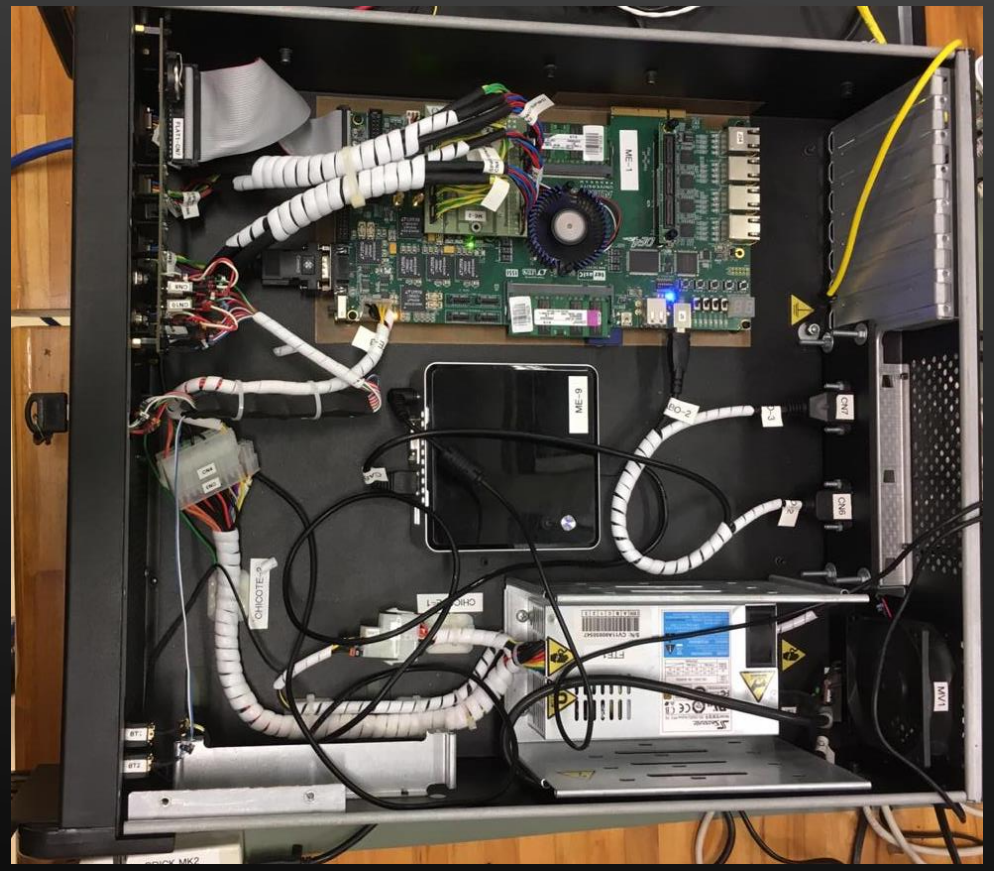
Intel® Stratix® 10 MX FPGAs

O QUE É FPGA?

O FPGA (*Field Programmable Gate Array*) é um CI que pode ser configurado por softwares para implementar circuitos digitais, é composto basicamente por três tipos de componentes: blocos de entrada e saída (IOB), blocos lógicos configuráveis (CLB) e chaves de interconexão (Switch Matrix), agrupando vários elementos lógicos para formar um sistema mais complexo, tal como CPU, controlador de rede.

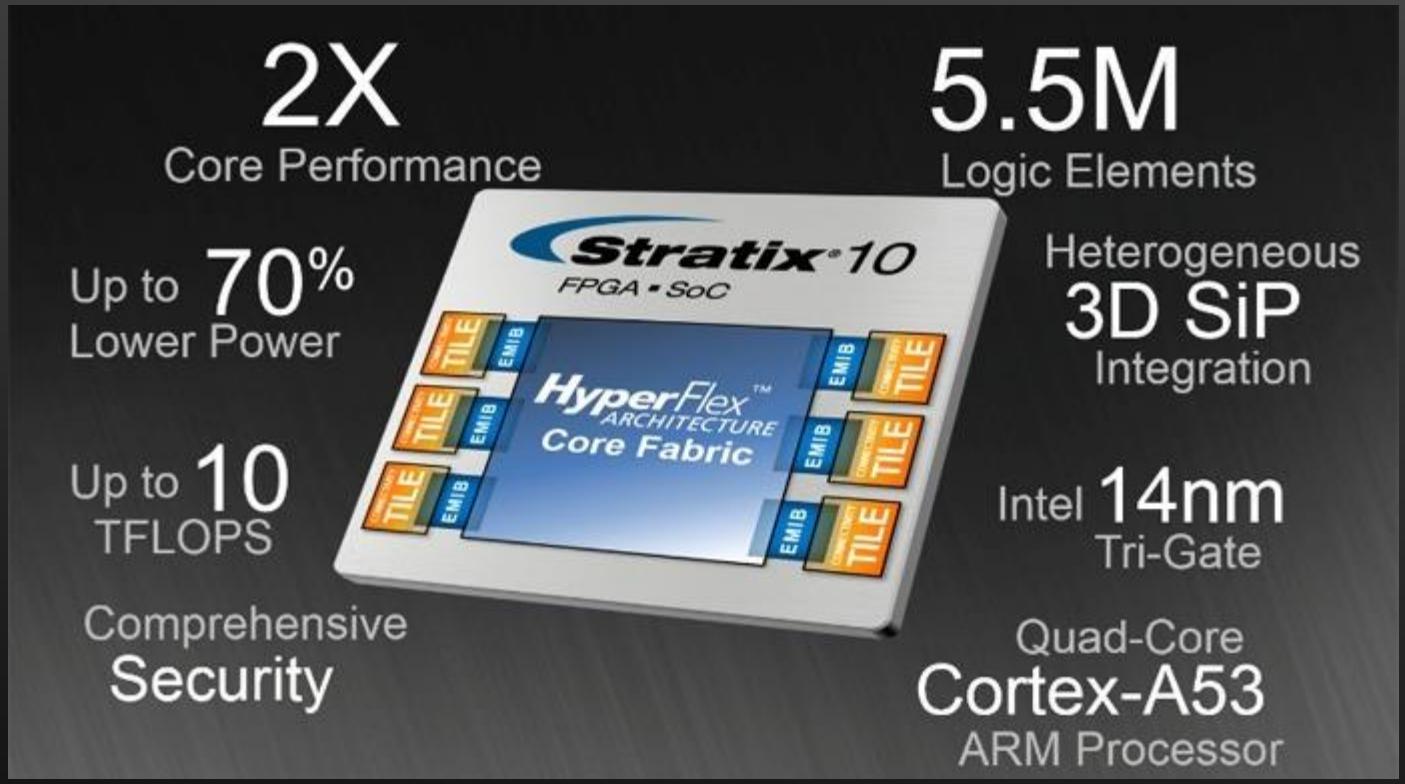


EXEMPLO DE FPGA:



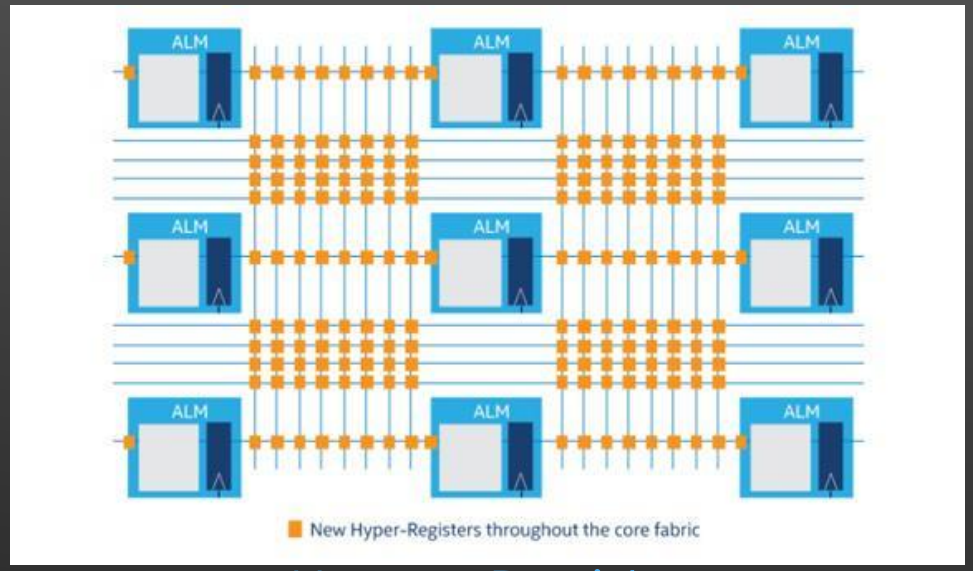
Projeto do Instituto Mauá de Tecnologia de capitação de imagem em satélites

INTEL STRATIX 10 SOC FPGAS

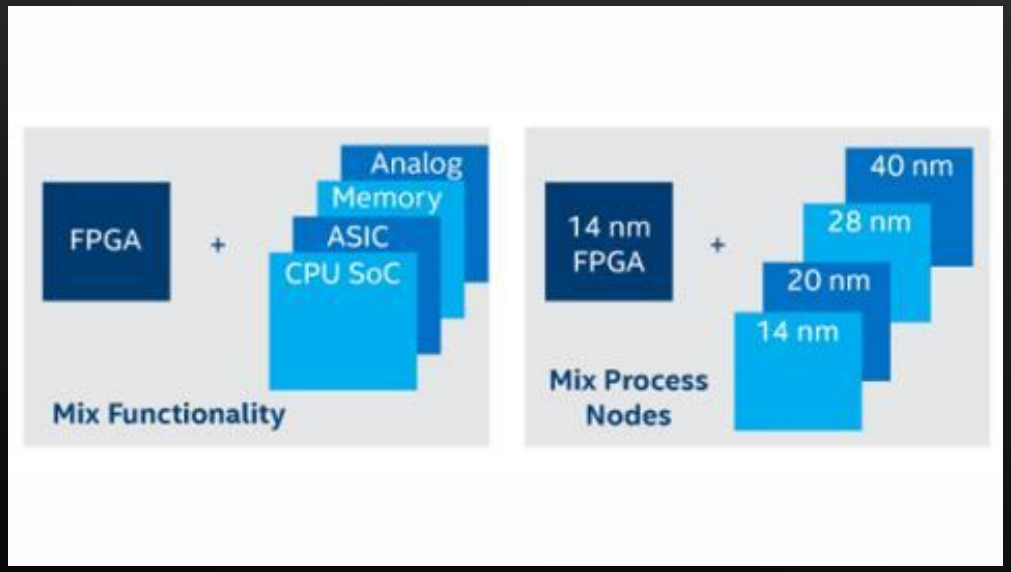


Intel Stratix 10 FPGA-Recursos Principais:

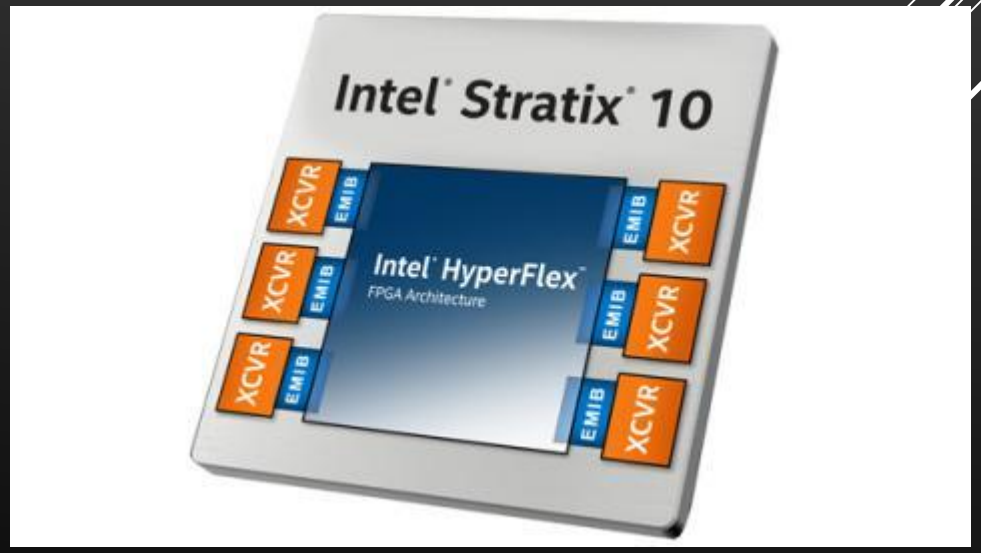
- Hyper-Register
- Transceivers
- 3D Integration
- Secure Device Manager (SDM)
- Digital Signal Processing (DSP)-10TFLOPS
- SEU Mitigation – 14 nm Tril-gate



Hyper - Register



3D System – in - Package



Transceiver

INTEL STRATIX 10 GX FPGA

Recursos

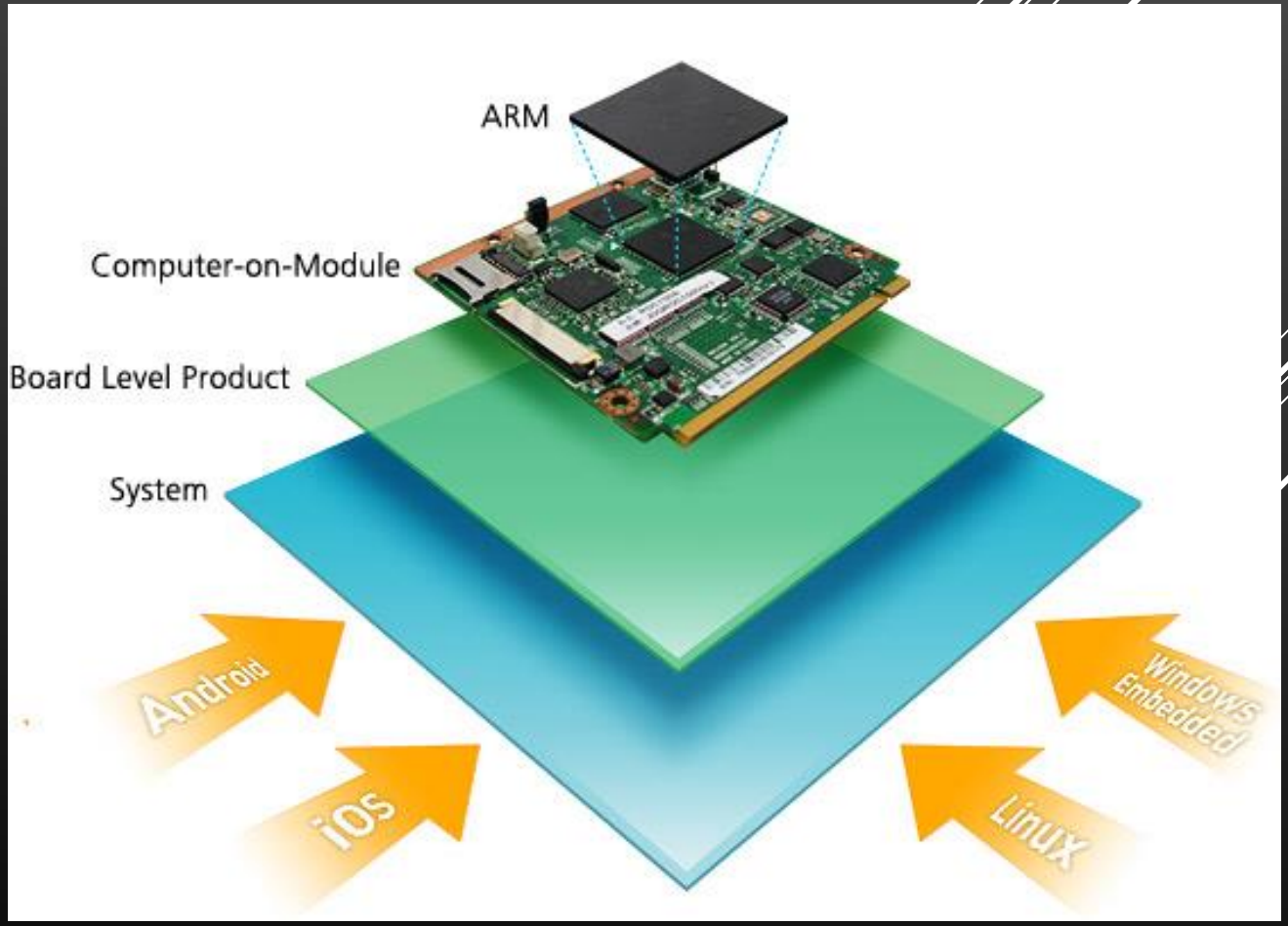
- Logic elements (Les)
- Adaptive logic modules (ALMs)
- ALM registers
- Hyper-Registers from Intel® HyperFlexTM FPGA architecture
- Programmable clock trees synthesizable
- M20K memory blocks
- M20K memory size (Mb)
- M20K memory size (Mb)
- MLAB memory size (Mb)
- Variable-precision digital signal processing (DSP) blocks
- 18 x 19 multipliers
- Peak fixed-point performance (TMACS)2
- Peak floating-point performance (TFLOPS)3

I/O e recursos arquitetônicos

- Secure device manager
- Maximum user I/O pins
- Maximum LVDS pairs 1.6 Gbps (RX or TX)
- Total full duplex transceiver count
- GXT full duplex transceiver count (up to 28.3 Gbps)
- GX full duplex transceiver count (up to 17.4 Gbps)
- PCI Express* (PCIe*) hard intellectual property (IP) blocks (Gen3 x16)
- Memory devices supported

O QUE É SOC?

O SoC (System on a Chip) é um sistema dentro de um chip, se refere a todos os componentes (processador, memória e até placa de vídeo) de um computador, ou qualquer outro sistema eletrônico, em um circuit integrado(chip), assemelha-se de um microcontrolador.



O QUE É SOC?

CPU	MCU	MPU	SOC	MCM
				
Central Processing Unit	Micro Computer Unit	Micro Processing Unit	System On Chip	Multi Chip Module


2X PERFORMANCE
HETEROGENEOUS 3D SiP INTEGRATION
UP TO 70% LOWER POWER
INTEL 14nm TRI-GATE
UP TO 10 TFLOPS
ALTERA
Stratix 10
FPGA • SoC
MOST COMPREHENSIVE SECURITY
5.5M LOGIC ELEMENTS
QUAD-CORE CORTEX-A53 ARM PROCESSOR

O INTEL STRATIX 10 SOC FPGA

- O FPGA Intel Stratix 10 SoC combina um FPGA com um hard processor system (HPS) que é capaz de inicializar aplicativos Bare Metal (instalado diretamente no hardware) ou sistemas operacionais como Linux .
- O INTEL STRATIX 10 Soc FPGA feito principalmente para o processamento de big data e inteligência artificial.

O SOC FPGA

- Com essa mentalidade foi criado a nomenclatura SoC FPGA.
- O Intel Stratix 10 não pode ser considerado um SoC porque é totalmente configurável como um FPGA, e não pode ser considerado um FPGA por ter vários núcleos de processadores como um SoC.

INTEL® STRATIX® 10 SOC FPGAS

- Possui todos os recursos de um FPGA
- Processador: Quad-core ARM* Cortex*–A53 MPCore
- Frequência máxima do processador: 1.5 GHz
- Processor cache and co-processors:
  - • L1 instruction cache (32 KB)
  - • L1 data cache (32 KB) with error correction code (ECC)
  - • Level 2 cache (1 MB) with ECC
  - • Floating-point unit (FPU) single and double precision
  - • ARM NEON media engine
  - • ARM CoreSight* debug and trace technology
  - • System Memory Management Unit (SMMU)
  - • Cache Coherency Unit (CCU)
- Scratch pad RAM : 256 KB
- HPS DDR memory : DDR4, DDR3 (Up to 64 bit with ECC)
- Direct memory access (DMA) controller : 8 channels

INTEL STRATIX 10 TX

Intel Stratix 10 SoC FPGA

+

eSRAM memory blocks

+

eSRAM memory size (Mb)

+

GXE transceiver count - PAM4 (up to 57.8 Gbps) or NRZ (up to 28.9 Gbps)

+

100G Ethernet MAC (no FEC) hard IP blocks

+

100G Ethernet MAC + FEC hard IP blocks

INTEL STRATIX 10 - APLICAÇÕES

- ASIC Prototyping
- Cyber Security
- Data Center Acceleration
- Wireline
- Radar
- OTN/Data Center Interconnect

DATA CENTER ACCELERATION

INTEL STRATIX 10 MX SOC

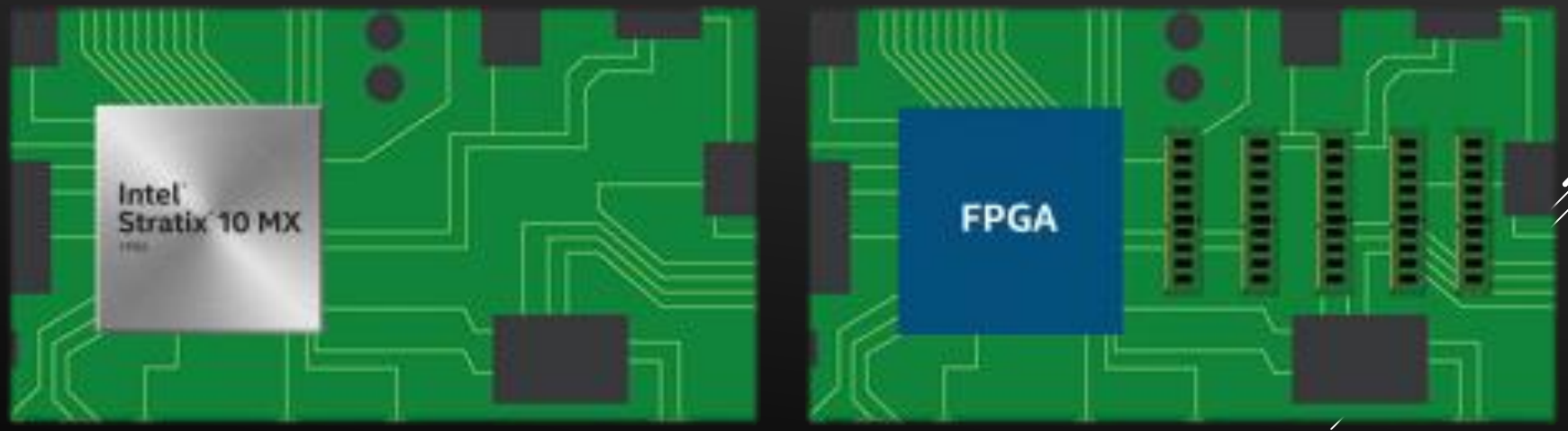
Intel Stratix 10 TX

+

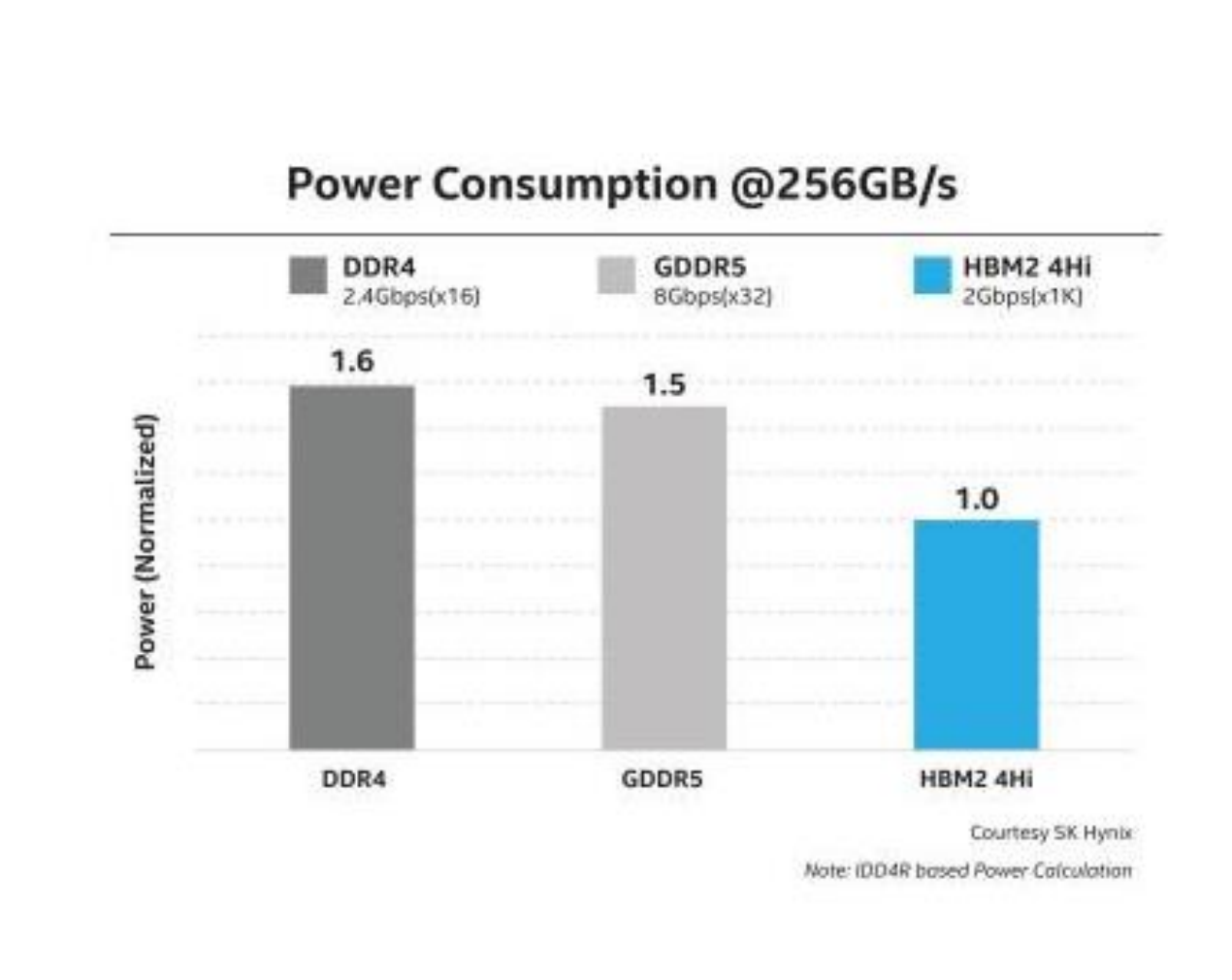
~~Quad-core ARM Cortex-A53 MPCore~~

+

HBM2 high-bandwidth DRAM memory (GBytes)

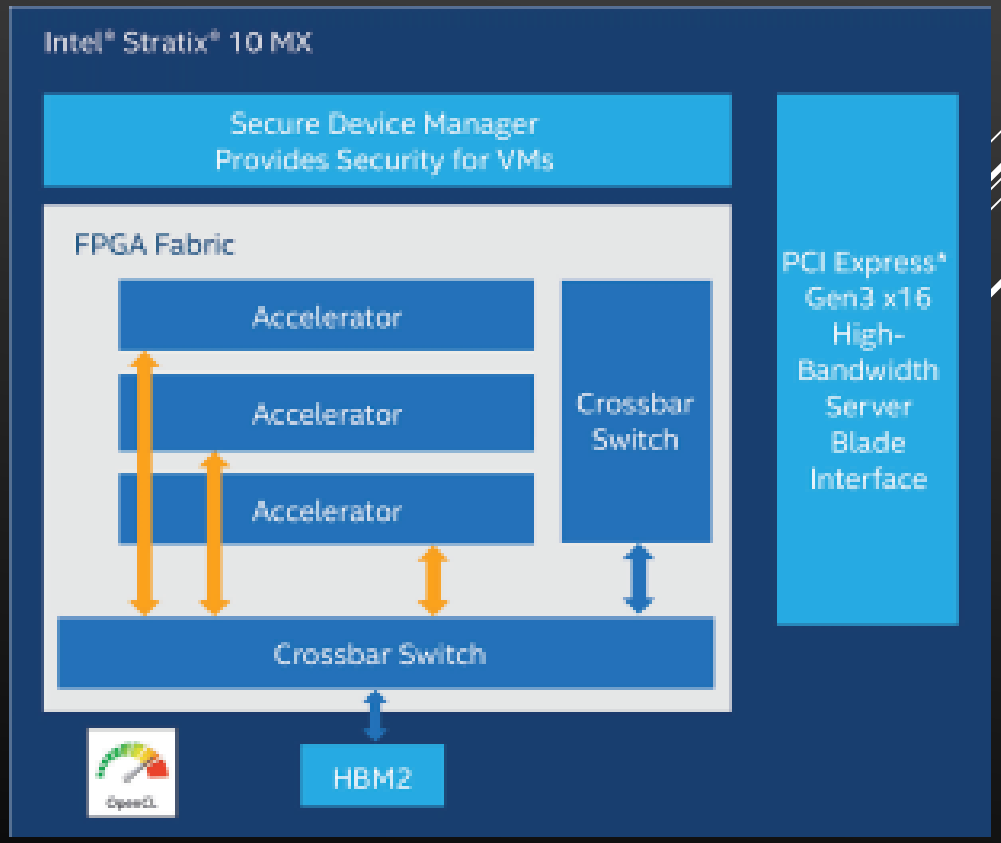


INTEL STRATIX 10 MX SOC



INTEL STRATIX 10 MX - APLICAÇÕES

- Wireline Traffic Manager
- Wireline Deep Packet Inspection
- Computação cognitiva de Data Center
- Transmissão
- Cyber Security Analytics



REFERÊNCIAS

- https://www.intel.com/content/www/us/en/products/programmable/sip/stratix-10-mx.html
- https://www.filipeflop.com/blog/fpga-no-modo-spartan-com-papilio-one/
- https://canaltech.com.br/hardware/O-que-e-um-SoC/
- https://pt.wikipedia.org/wiki/System-on-a-chip
- https://www.intel.com/content/www/us/en/wireline/products/programmable/applications/nfv.html?_ga=2.20309681.820925634.1552935765-1338476956.1552517951
- https://www.intel.com/content/www/us/en/products/programmable/sip/stratix-10-mx/applications.html
- https://www.intel.com/content/www/us/en/programmable/products/boards_and_kits/dev-kits/altera/stratix-10-soc-development-kit.html
- https://www.intel.com.br/content/www/br/pt/products/programmable/fpga/stratix-10.html
- https://www.intel.com.br/content/www/br/pt/products/programmable/soc/stratix-10.html
- https://www.intel.com.br/content/dam/www/programmable/us/en/pdfs/literature/pt/stratix-10-tx-product-table.pdf
- https://www.intel.com.br/content/dam/www/programmable/us/en/pdfs/literature/pt/stratix-10-product-table.pdf