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Design and test of SiC circuit board for MIST satellite

KTH Student Satellite MIST

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Bachelor's Thesis

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Abstract

This paper describes work related to the “Miniature Student Satellite” (MIST) project and the “SiC in Space” project, located at KTH, Stockholm, Sweden. The goal of the MIST project is to launch KTH’s first student satellite into space, carrying multiple scientific experiments where SiC in Space is included.

This thesis contains a compilation of three MIST-related bachelor theses that were carried out at KTH in the spring of 2016, primarily consisting of constructing and testing circuits for power supply and measurements for the SiC in Space part of the satellite.

A printed circuit board has been developed, which accommodates experiment circuits to evaluate the features and functionality of silicon carbide components in a space environment, and power the supply to the SiC in Space and the Piezo LEGS projects. The development includes designing, assembling and testing the PCB according to the MIST team’s demands and requirements.

Emphasis has been laid on electrical safety to ensure that the design can not short circuit the satellite battery, as well as EMC considerations to minimize the EMI between different parts of the satellite. Final testing of the hardware has not been executed due to an ordering error and time shortage, wherefore the planned test protocol has been included for future work.

Keywords

Silicon Carbide, satellite, overcurrent protection, printed circuit board, schematics.

Abstract

Denna kandidatuppsats beskriver arbete relaterat till ”Miniature Student Satellite” (MIST)-, samt SiC in Space-projekten, vid KTH, Stockholm, Sverige. MIST-projektets mål är att skicka KTH:s första studentsatellit till rymden, där SiC in Space är ett av flera medföljande vetenskapliga experiment.

Detta projekt sammanställer tre examensarbeten relaterade till MIST som genomfördes vid KTH under våren 2016, huvudsakligen bestående av att konstruera och testa kretsar för strömförslagning samt mätningar för SiC in Space-delen av satelliten.

Ett kretskort som innehåller experimentkretsar för att utvärdera egenskaper och funktionalitet för komponenter av materialet kiselkarbid i en rymdmiljö, samt strömförslagningskretsar till SiC in Space- och Piezo LEGS-projekten har utvecklats. Utvecklingen omfattar design, montering and testning av kretskortet enligt MIST-gruppens krav.

Tonvikt har lagts på elsäkerhet för att säkerställa att designen inte kan kortsluta satellitens batteri, såväl som EMC för att minimera EMI mellan olika delar av satelliten. Slutgiltig testning av hårdvaran har ej kunnat genomföras på grund av tidsbrist beroende på ett beställningsfel. Därför har det planerade testprotokollet inkluderats för framtida arbete.

Nyckelord

Kiselkarbid, satellit, säkerhetskrets, överströmsskydd, kretskort, kretsschema.

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List of acronyms and abbreviations

AC	Alternating Current
ADC	Analog to Digital Converter
BJT	Bipolar Junction Transistor
DAC	Digital to Analog Converter
DC	Direct Current
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
GPIO	General Purpose Input and Output
HAL	Hardware Abstraction Layer
I/O	Input and/or Output
I²C	Inter Integrated Circuit. A serial communication protocol
ICT	Information and Communication Technology
LEO	Low Earth Orbit, 160 km – 2000 km above ground
MCU	Microcontroller Unit
MIST	MIniature STudent Satellite
N/A	Not applicable
OBC	On Board Computer
PCB	Printed Circuit Board
Si	Silicon
SiC	Silicon Carbide
SWD	Single Wire Debug
VDD	Positive voltage reference for digital use, 3.3V
VDDA	Positive voltage reference for analog use, 3.3V
USART	Universal Synchronous/Asynchronous Receive Transmit

1 Introduction

This chapter provides an overview of the project and describes the background of the thesis, and presents the project purposes and goals.

1.1 Background

The environmental conditions on Venus are extreme compared to earth, with a surface temperature of 460°C , and a pressure of 92 bar[1]. Hence, to travel to Venus and land a spacecraft on the planet, the materials of the components used would have to be carefully considered, and they would need to withstand substantial amounts of radiation as well. Transistors are commonly made of silicon, and one option for increasing the robustness and durability of the transistor is to use the material silicon carbide[2] (SiC).

To evaluate how SiC would perform in a space environment, tests have been performed on earth. The goal of the *SiC in Space* experiment is to further evaluate this material by examining the SiC properties and performance in a space environment, which can be achieved with the project MIST[3] (Miniature Student Satellite).

MIST is a project carried out by students at KTH, where the goal is to launch a satellite into low earth orbit and perform several experiments, including *SiC in Space*. The performance of a SiC transistor, as well as a standard silicon transistor, will be measured in orbit around earth and evaluated for comparison.

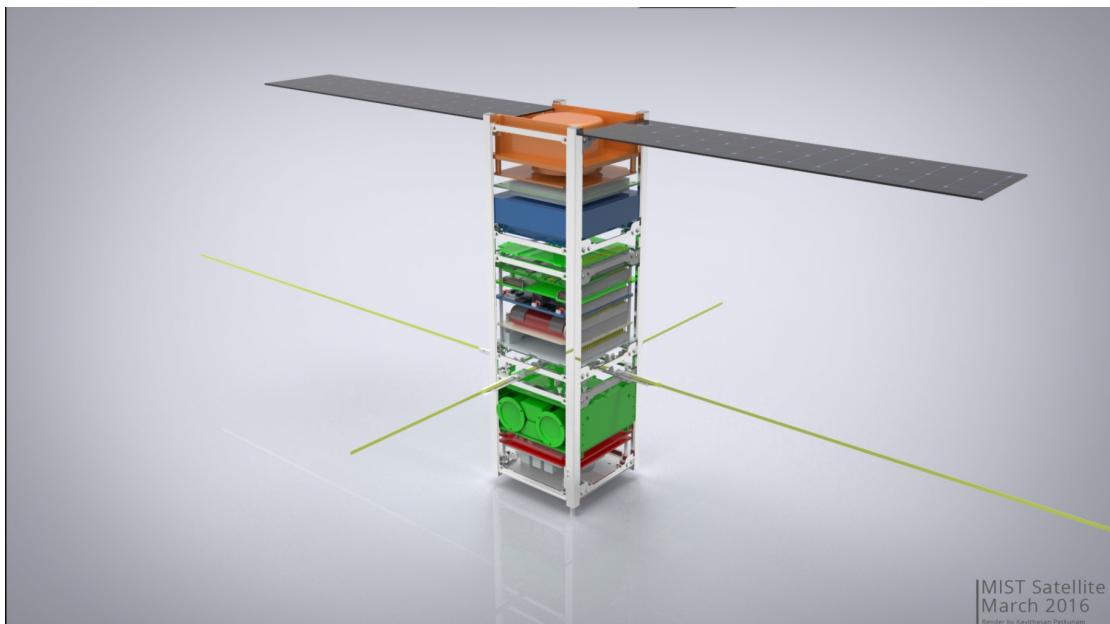


Figure 1: MIST Satellite[4]

This thesis will cover the work of combining previously made works with the *SiC in Space* experiment by designing a PCB that will accommodate the power supplies, measurement circuits and the MCU required for conducting the required experiments, as well as the assembly and testing of the final product. Furthermore, the designed PCB will also contain the power supply for the Piezo LEGS experiment.

The SiC experiment measurement circuits were designed and tested by Matthias Ericsson and Johan Silverudd. The power supplies for the SiC experiment and the Piezo LEGS experiment were both designed and tested by Simon Johansson. To control the SiC experiments and to record the data, an appropriate MCU was selected and tested by Hannes Paulsson and Mikael André. This MCU is also used to turn the experiments on and off at command, as well as to control the power supply for the Piezo LEGS experiment.

The final design also includes a battery bus power switch to handle overcurrent on the MIST battery bus[5], as well as to ensure that no experiment can short circuit the satellite battery. In the PCB design, careful considerations will be made in regards to EMC to limit the PCB emissions of electromagnetic fields that could interfere with, or damage other parts on the satellite.

The time frame for this project is 10 weeks, and the final design of the PCB is expected to be in a finished state. The software for the MCU is not expected to be finished, leaving that work for future students to finish.

1.2 Problem definition

The following questions need to be considered and answered to design and develop the SiC PCB:

1. What are the most important PCB design aspects to accommodate all the required circuits on a 90 x 96 mm PCB?
2. In case of a short circuit from one of the experiments, will the battery bus always be protected?
3. If the battery switch is turned off, will the experiments be turned off automatically, to preserve battery life?
4. What are the most important PCB design aspects to best meet the system requirements, as well as the EMC requirements?
5. What are the advantages of using a four-layer PCB design, as opposed to a two-layer design?

1.3 Purpose

The purpose of this thesis is to evaluate and compile, as well as elaborate upon, the previous work that has been carried out regarding the SiC experiments. This is done by answering the questions in the problem definition.

The purpose of the project is to ensure that the SiC experiments can be carried out on behalf of KTH, as well as to provide power supply to both the SiC PCB and the Piezo LEGS PCB in a safe manner.

Overall, all work is to be carefully documented to provide accurate and necessary information for the MIST team. This thesis will also be used as a reference for future work when finalizing the MCU software.

1.4 Goal

The goal of this project is to deliver a functional PCB to the MIST team that meets the system requirements, as well as software to test the PCB functionality. The project can be divided into the following parts:

1. Compilation, finishing and improving upon previous schematics.
2. Implementation of a battery bus power switch to provide overcurrent protection for the battery in case of experiment failure.
3. Final PCB design, based on the final schematic.
4. Test of the final PCB to ensure desired functionality.
5. Documentation of all work and specifications.
6. To provide guidelines for the future final software development.

Due to the time frame of this project, and due to the fact that the final communication protocol between the OBC and the MCU is not yet finished, the software can not be completed. This thesis will however provide sufficient documentation and guidelines for this future software development.

1.5 Methodology

The foundation of this thesis is the qualitative literature study, in which the previous theses which this work is built upon, is studied and evaluated. This work needs verification to ensure desired functionality, which is done by theoretical study as well as computer simulations and measurements. Guidelines regarding PCB design and reducing electromagnetic interference (EMI) is also to be studied.

Since this project is a work in progress consisting of several teams working individually, the specifications and requirements are constantly being updated to meet many different demands and desires. Because of this, an agile approach is taken to the thesis work, to grant flexibility and allowing changes continuously if conditions are changed. Therefore, work has been carried out iteratively, making sure that every iteration could be changed according to possible changes using a modular design.

1.6 Delimitations

Measurements of EMI would be desirable to evaluate the PCB EMC, but due to equipment limitations, measurements will not be possible at this time. Due to the time constraint of the project this work will be hardware-oriented, and the MCU software will need to be finished at a later point. Another reason for this is that the communication protocol between the OBC and the MCU is not finished as of yet.

1.7 Outline

Chapter 2 presents the MIST project background and provides a description over the previously carried out work from 2016, as well as the risks and challenges of the thesis work.

Chapter 3 presents the scientific methods used during the thesis work.

Chapter 4 presents an overview over the satellite battery and its power distribution.

Chapter 5 presents the relevant EMC theory needed to corroborate the made design choices.

Chapter 6 presents the improvements made over last year's work in order to compile it, as well as necessary implementations to fulfill new hardware requirements.

Chapter 7 presents the final PCB layout and arguments behind made design choices.

Chapter 8 presents a description over the development of the test software needed to evaluate the PCB functionality and performance.

Chapter 9 presents the thesis work results.

Chapter 10 presents conclusions and reflections over made thesis work.

Chapter 11 presents discussion about ethics, sustainability and what benefits can be made from this thesis work, as well as environmental considerations.

Chapter 12 presents the future work needed to be made in order to complete the testing of the SiC PCB.

2 Project background

This chapter provides basic background information about the MIST project and information about the different experiments that will be conducted on the satellite. This chapter also contains the development and testing of the SiC circuit board as well as an overview of the hardware and software system requirements.

2.1 MIST

The project covered in this thesis is a part of the larger project carried out at KTH called MIST - Miniature Student Satellite. This section will give a brief introduction to the project and the experiment that will be conducted on the satellite.

2.1.1 What is MIST?

The MIST project was initiated by the KTH Space Center and is carried out by student belonging to different sections at KTH, working on it as a bachelor or master thesis project lasting one semester, and then handing it over to a new team of students to continue the work in the following semester until the satellite is ready for launch[6]. Apart from the students, MIST is managed by Dr. Sven Grahn, a KTH engineering physics graduate (1969) and veteran of Swedish space activities. He is assisted by Ms Agnes Gärdebäck, a KTH engineering physics student, who functions as a teaching assistant in the project. She also supervises the work of some of the sub-teams (management, structure) into which the students are organized. Mr. Grahn supervises the sub-teams for the ground station and for functional testing.

Other sub-team supervisors are:

Dr. David Broman, associate professor, KTH Software and Computer Systems (on-board computer software).

Dr. Gunnar Tibert, KTH associate professor of mechanics (attitude control and mechanical test).

Mr. Theodor-Adrian Stana, electronics engineer from KTH's astro particle physics group (electrical).

Mr. Andreas Berggren, a recent graduate from KTH and an employee of Surrey Satellite Technology Ltd (thermal control).

2.1.2 The satellite

The satellite is based on the CubeSat model, a commonly used structure for experimental satellites. Since the first CubeSat was launched in 2003, hundreds of CubeSats have been successfully launched, and their popularity is still growing. In 2017, 569 CubeSat launches were announced[7].

The MIST satellite will host eight different functional and scientific experiments. Every experiment has its own requirements regarding temperature, radiation, power, and other aspects. This results in a highly complex set of requirements that is needed to be satisfied to the highest degree possible[4].

The satellite is divided into three stacks:

Top stack

The top stack is on the topmost part of the satellite, which holds three experiments; Cube prop, SEUD and MoreBac, placed one below the other.

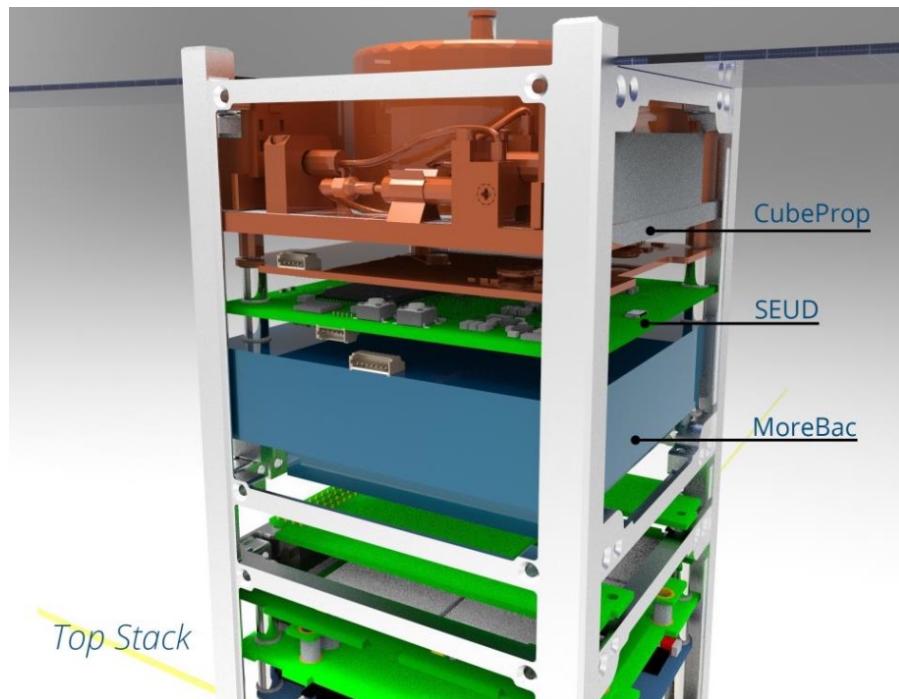


Figure 2: Top stack of the satellite[4]

Middle stack

The middle stack contains all the satellite subsystems; the IGIS, TRXVU, OBC, Power Board, Battery, iMTQ, HDRM, and the antenna.

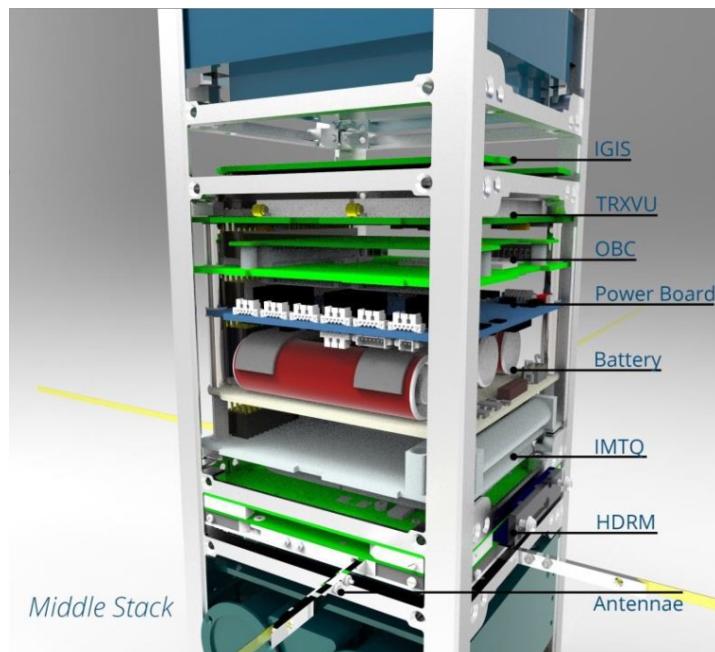


Figure 3: Middle stack of the satellite[4]

Bottom stack

The bottom stack contains the experiments RATEX-J, SiC, Piezo LEGS and Cubes.

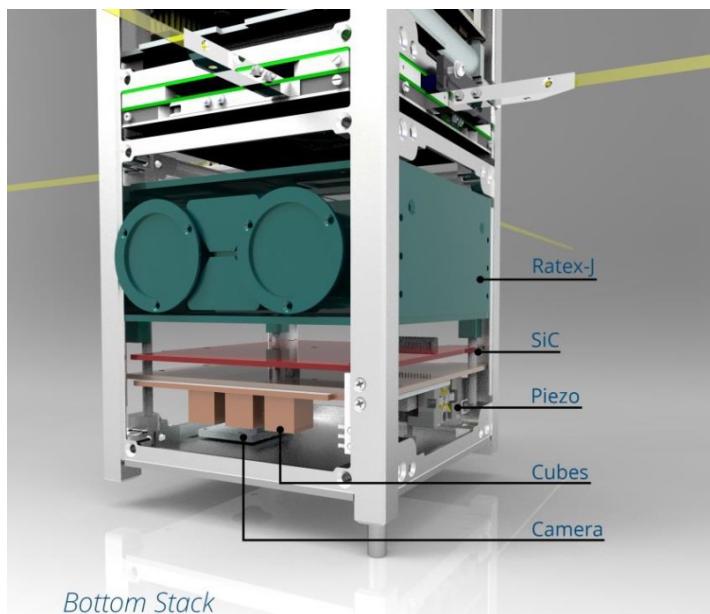


Figure 4: Bottom stack of the satellite[4]

2.2 Working on Venus

Researchers on KTH are working on the project *Working on Venus*, to develop electronics fit for a space mission to collect data on the planet Venus. The purpose of the project is to research the planet's climate, which may in turn explain earth's climate, being a neighbouring planet. In the mid-1970s, Soviet attempts were made to collect data on Venus, lasting only a few hours because of electrical failure due to the heat.

2.3 SiC in Space

There are several challenges when sending probes to Venus, where one of the biggest ones is the extreme environment. Venus has an average temperature of 460°C and an atmosphere consisting of 96,5% carbon dioxide. Hence, the probes that are to be sent to Venus would need semiconductors that are highly heat resistant, which is why SiC is subject to research.

Previous studies have shown that SiC BJTS:s remain operational at high temperatures, and the purpose of *SiC in Space* is to test and verify that these will also work in a space environment, which could potentially aid the progress of sending probes to Venus in the future[8].

2.4 Piezo LEGS

There is an increasing interest from different space institutes and companies to use PiezoMotor[4] motors in space applications. In general, the motors are expected to work well in harsh environment but in some cases the life time need to be considered.

The absence of air subjects the motors to more friction, resulting in more wear, which has been confirmed in high vacuum tests in earth. Moreover, it is of interest to confirm that the motors work well in a high radiation environment. The purpose of the test is to follow the motors function over time to see the possible change of performance and to measure distance the motor can operate in total.

Due to satellite space limitation, the 48V power supply needed for the Piezo LEGS experiment was suggested to be fit on the SiC PCB, which is placed directly above the Piezo PCB, and had more free space for additional circuits.

2.5 Previous work

This part describes the previous work that has been carried out regarding the *SiC in Space* experiments, as well as the respective results and conclusions. Further elaboration and improvements upon this previous work can be found in chapter 6.

2.5.1 Design of microcontroller circuit for SiC experiment

The task of designing an MCU circuit for the SiC experiments was carried out by Hannes Paulson and Mikael André[9].

The purpose of this thesis was to evaluate and choose a microcontroller suitable for the task of doing experimental measurements in space. The purpose of the microcontroller itself was divided into three main tasks.

1. Provide the test circuit with reliable and stable voltage levels during the test phase, to allow the test to be conducted under different circumstances.
2. To read the analogue signals from the test circuit and store them as readable values.
3. Send the stored values to the satellite OBC, for transfer of the stored data to earth for further analysis.

When selecting the microcontroller, it was important to meet the requirements regarding the space environment, the required interfaces for the experiment, and the power consumption constraints set by the satellite as, the only power source comes from its solar panels.

The SiC project owner required an ADC with at least ten channels and at least 10-bit resolution to provide sufficient precision for the intended experiments, as well as at least one DAC. Due to the limited space on the PCB, the MCU footprint size and the number of I/O was to be kept to a minimum. This resulted in the selection of the STM32L053C6 MCU from ST Microelectronics, which met all of the demands and requirements.

2.5.2 Design of measurement circuits for SiC experiment

The task of designing the measurement circuits for the SiC experiment was carried out by Matthias Ericsson and Johan Silverudd[10]. The purpose of the thesis is to describe how the characteristics of a transistor can be measured using analog circuitry and how the environment in low earth orbit affects the DC current gain of a silicon carbide BJT, and particularly how the temperature changes the DC current gain.

2.5.3 Design of power supplies for Piezo LEGS and SiC experiment

The task of designing power supplies for the Piezo LEGS and SiC experiments were carried out by Simon Johansson[11].

The purpose of this thesis is to describe the design of two DC-DC converters that can operate in a space environment, while maintaining a high level of safety as to not short-circuit the satellite battery. The requirements for the DC-DC converters were to supply the Piezo motor with 48 V and 15 mA, and the SiC experiments with 10 V and 10 mA.

2.6 SiC PCB system requirements

- The physical dimensions of the PCB are to follow the PC/104 standard, 90x96 mm with a cut-out to accommodate cables.
- All components must be surface-mounted, and no electrolytic capacitors may be used.
- The PCB must be designed with EMC considerations in mind.
- The MCU must communicate with the on board computer using the I²C protocol.
- The PCB must include a battery bus power switch to protect the satellite battery from a short circuit.
- All work, including source code, schematics and other documentation must be available for future work.

2.7 Project risks and challenges

The following risks with this project were identified:

- Previous work not meeting the new system requirements and demands, or incorrect hardware implementations.
- Unfinished specifications and system requirements from the MIST team.
- Time shortage, resulting in a failure to deliver a functional and thoroughly tested PCB.

When working in a large-scale project spanning over several years involving many different people and teams, it is important to calculate risks that may impede work progress. New demands or circumstances that alter the system requirements and specifications are likely to emerge over time, which has to be taken in account for.

As preventive work to minimize these risks, much time will be spent initially to verify the different designs and confirming compatibility. The PCB will be designed as quickly as possible, while retaining a high level of care for the final product. Overall, keeping an agile and modular approach as well as design strategy is important, to easily implement possible changes.

2.8 Summary

The MIST project is a KTH student-managed attempt to launch a satellite into space, containing several different experiments, including the *SiC in Space* experiment. The *SiC in Space* experiment's goal is to research the material Silicon Carbide, which can be used in electrical components in extreme environments, for example on Venus. This thesis is based upon three thesis works from 2016 related to *SiC in Space*, and the goal is to compile and improve upon this work to produce the final *SiC in Space* PCB included in the MIST satellite.

3 Methodology

This chapter presents the project methodology, as well as a description of the workflow. All work begun with an idea or hypothesis being conceived, then verified successfully or otherwise discarded after computer simulation, and finally implemented in the architectural design.

3.1 Literature study

The initial part of the project consisted of reading and understanding the previous theses that this project is based upon, and gathering necessary information about the satellite and all the required technical specifications. Therefore, research was done to fully understand the previous challenges and problem definitions, as well as how these were solved respectively. Technical specifications and requirements were studied carefully, to certify that all previous work was carried out in accordance with the MIST system design file.

PCB design guidelines and EMC theory was also studied, to provide a sensible design approach, most notably regarding important aspects for reducing EMI.

After compiling all the previous work, a meeting was held with Agnes Gärdebäck to make certain what system requirements and/or conditions of the project had changed, if any. Regular consultation meetings were also held with academic advisor Bengt Molin continuously during the project. One meeting was attended together with all the MIST electrical teams as well as the teams responsible for the OBC.

3.2 Agile and modular development

To provide means of handling the fact that conditions could, and would change throughout the project, as well as to minimize the project risks, all work was carried out iteratively in an agile manner. A first draft of the complete schematic was finalized early in the development, and was then constantly updated with the ambition to not include features that could not be subsequently modified, by dividing the system architecture into logical blocks. This approach allowed flexibility while providing a comprehensive overview of the system as it was fully realized in each work iteration.

The same modular approach was taken when designing the PCB layout, with the division of circuits into subcircuits creating logical interchangeable blocks, assuring compatibility, should any conditions change.

3.3 Simulations

All of the included circuits were carefully simulated using the computer software LTSpice XVII, and tested in the previous works, but since new demands and conditions emerged further simulations of the previously designed circuits needed to be conducted to ensure proper performance and functionality of all included circuits according to the system requirements. A simulation of the battery bus switch circuit was also required.

This approach was taken to provide a theoretical foundation to the project, before empirical verification was possible, to provide credibility.

3.4 Assembly and testing

After receiving the PCB from the manufacturer and assembling the components, test code for the MCU needed to be developed to provide means of testing and verifying the PCB functionality and performance.

3.5 Documentation

In order for the SiC PCB to be useful for the MIST team, its use needed to be carefully documented. This included the functionality of the different circuits, as well as the MCU pin use and configuration. Documentation was also imperative to provide a future software team with an accurate system description, since the final MCU software is still to be developed. The constant documentation also provided an intuitive way of reflecting upon the work continuously throughout the project.

4 Satellite battery and power distribution

The satellite has solar panels mounted on the surface as a primary source of power, which are used to charge the batteries and supply the systems. When the satellite enters eclipse, the charged batteries becomes the only source of power, which results in a varying output voltage, ranging from 12-14 V[4].

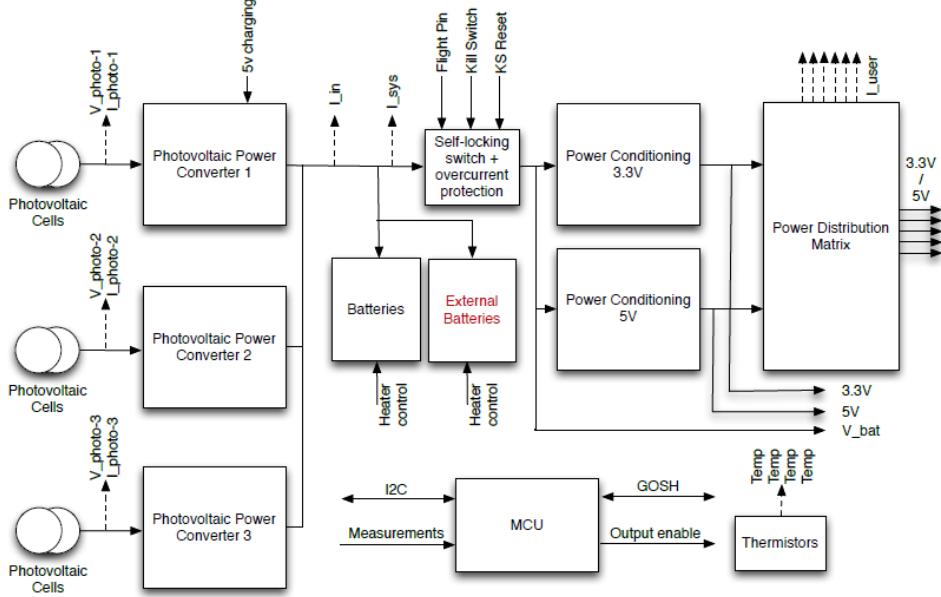


Figure 5: Satellite battery and power distribution[4]

The charging cycles are then stabilized with power converters, and the voltages are converted to 3.3V and 5V respectively for distribution through a power matrix. The outputs are controlled by a microcontroller, and are latch-protected

The power distribution matrix has a limited number of distribution lines for the two different voltages and when this project was initiated, it was yet to be decided if the SiC experiment PCB would be provided with 3.3V or 5V. Eventually, the SiC experiment PCB was assigned a 5V power supply line.

Accessing the satellite battery voltage directly in need of a greater voltage than 5V was decided to be acceptable by the MIST team only if a battery bus protection circuit implemented. Since the SiC experiments requires a voltage of 10V and the Piezo LEGS experiment requires 48V, this was a necessary consideration for the SiC PCB. The suggested solution and its results is elaborated upon in section 6.5.

5 EMC theory

5.1 EMC definition

Electromagnetic interference (EMI) is an increasing form of serious environmental pollution with a wide range of effects, varying from minor broadcast reception crackles to electrical or electronic malfunctions, to corruption of safety-critical control systems, with potentially fatal outcome[12, p. 1].

The absence of effects due to EMI on the other hand, is known as electromagnetic compatibility (EMC). In the International Electrotechnical Vocabulary[13], EMC is defined as:

The ability of a device, equipment or system to function satisfactory in its electromagnetical environment without introducing intolerable electromagnetic disturbance to anything in that environment

This not only applies between different equipment and devices, but also within close environments, i.e. parts within the same system. The goal when designing electromagnetically compatible hardware then, is immunity to such disturbances as well as limiting electromagnetic emission.

5.2 Intra-system EMC

When several electrical or electronic systems are closely packed together, as is the case in a satellite, EMC can be particularly problematic[12, p. 7]. Special precautions may be needed for maintained compatibility, since sensitive parts and systems are closely positioned. Accurate knowledge of the characteristics of any emitters and their potential victims, as well as the installation circumstances are required to do this effectively. The SiC PCB was designed with EMC considerations in mind, with is further elaborated upon in section 7.4.

5.3 Malfunction scope

Modern control systems are often operated by a processor, and rely on a bus-linked architecture where software controls the multiplexing of several signals onto a single hardware bus. Since only a low energy is needed to induce a change of state, such an arrangement may be affected by interference. Furthermore, it is impossible to predict the effects of such an interference, depending on the control process.

According to *EMC for product designers* by Tim Williams, control systems can be expected to be interfered by the following phenomena[12, p. 9]:

- Supply voltage interruptions, dips, surges and fluctuations
- Fast transient overvoltages (spikes and surges) on supply, signal and control lines
- Radio frequency fields, both pulsed (radar) and continuous, coupled directly into the equipment or onto its connected cables
- Electrostatic discharge from a charged object or person
- Low frequency magnetic or electric fields

Often, faulty software may cause malfunction confused with those due to EMI. System crashes, faulty data and erroneous calculations can be identical with the symptoms caused by EMI, which can be difficult to diagnose and characterize.

5.4 Inductance

Every wire or PCB trace has an inductance which increases with the length, and decreases with the width of the conductor. This inductance makes the voltage drop when current is flowing, which creates radiation that propagates, in power routing. Hence in a PCB design, it is desirable to keep the inductance as low as possible[14]. Measures taken to mitigate inductance is presented in section 7.4.

5.5 Current loops and antennas

Every signal that is sent from an MCU to any other chip is a current pulse which after travelling to the receiving unit returns to the MCU ground pin through the other unit's ground pin.

Since the current always needs to return to its source, a loop is inherently created. This also applies to any noise voltage and its associated current, which always propagate via the path of lowest impedance, again, back to its source. Keeping this in mind, it is possible to reduce noise by controlling the shape and impedance of the return path.

In the simplest instance, a trace loop can be modelled as a small loop antenna, which radiates energy directly from the PCB[12, p. 235]. A small loop is defined as a loop whose dimensions are smaller than $\frac{1}{4}$ wavelength at the present frequency. As the dimensions of the loop approaches $\frac{1}{4}$ wavelength, the currents appear out of phase at a distance, at different points on the loop. A dipole is also an antenna, where an increased dipole length equals increased radiation, once again, until the antenna reaches a length of $\frac{1}{4}$ wavelength[14].

Hence, it is necessary to keep loop areas as small as possible in order to minimize emission. For reference, with a loop area of 10 cm^2 , a current of 10 mA and a frequency of 50 MHz , an electric field with a strength of about $42 \text{ dB}\mu\text{V/m}$ would be created[12, p. 235], which is 12 dB over the EN Class B limit[15]. Furthermore, not only is such an antenna prone to emit radiation, a good antenna always functions as a good receiver as well.

6 Improvements and implementations

This chapter describes the improvements over the previous design and schematics that was provided, emanating from suggested future work. For full schematics, see Appendix A.

6.1 Design update and elaboration

Several new requirements and demands from the MIST team emerged, changing the conditions for the SiC PCB compared to the previously made work in 2016:

- To protect the satellite main battery, a battery bus power switch circuit needed to be implemented, in case of a short circuit on either of the experiment circuits. This circuit would also include inrush current protection.
- To preserve battery life, a hardware implementation was needed to ensure that all experiments would be turned off automatically in case of a battery switch suspension.
- The 5V power line for the Piezo LEGS MCU needed to be managed and controlled by the SiC MCU using a switch.
- An I²C buffer circuit needed to be implemented to reduce the capacitive load on the I²C bus.
- A transistor switch needed to be implemented, to provide means for the SiC MCU to control the 5V power supply line to the Piezo PCB, which is further discussed in section 6.4.

6.2 Design improvements

The following measures has been taken to accommodate the new system requirements and the suggested changes, with insights gained from previous work:

- A four-layer PCB design was implemented to create a solid ground plane and simplify trace routing. The full description of the advantages of a four-layer design is covered in section 7.3.
- The Piezo LEGS team requested an output capacitor with at least 4.7 µF capacitance on the DC-DC boost circuit, whose effects is discussed in section 6.3.
- The MIST team decided that the SiC PCB will be provided with 5V, resulting in the requirement of a 3.3V step down regulator to provide the correct MCU voltage.
- The 3.3V regulator LM1117 that was used by Paulsson and André in the previous design had a large quiescent current which failed to meet the system requirements, and was replaced by the regulator LT1129[16] for greater power efficiency as suggested by Paulsson and André.
- Any components and interfaces used by Paulsson and André that are not necessary for the final PCB design was removed, including a reset button and the USART interface.
- There was a design error made regarding the operational amplifier OpUbe[10] in the schematics provided by Silverudd and Ericson, which was taken into consideration and corrected. In the schematic, a chip containing two operational amplifiers is used, but in the previous design, two separate chips were used, resulting in the operational amplifiers not being connected to power.

- Several component patterns were updated and refined to better agree with the manufacturer datasheets.
- The DC-DC boost circuit designed by Johansson for providing the Piezo LEGS experiment with power was implemented and added to the PCB.
- The DC-DC converter LT8570-1 used in the 48V DC-DC boost circuit needed means of cooling, since there is no air in space to remove produced heat. The manufacturer datasheet suggested drilling five vias[17] to the PCB ground plane to transfer heat which was implemented in the design.
- The output capacitors and resistors used in Johansson's design were rated for a maximum voltage of 50V, which was discussed in the future work section in this thesis. These components have been replaced by components with a 75V or 100V rating to provide a greater safety margin.

6.3 48 V DC-DC boost circuit simulation results

The functionality of the DC-DC boost circuit has been simulated, tested and verified by Simon Johansson[11], but since the Piezo team required a $4.7 \mu\text{F}$ output capacitor of as opposed to the $0.22 \mu\text{F}$ capacitor used in the original design, and the effects of this change needed to be simulated.

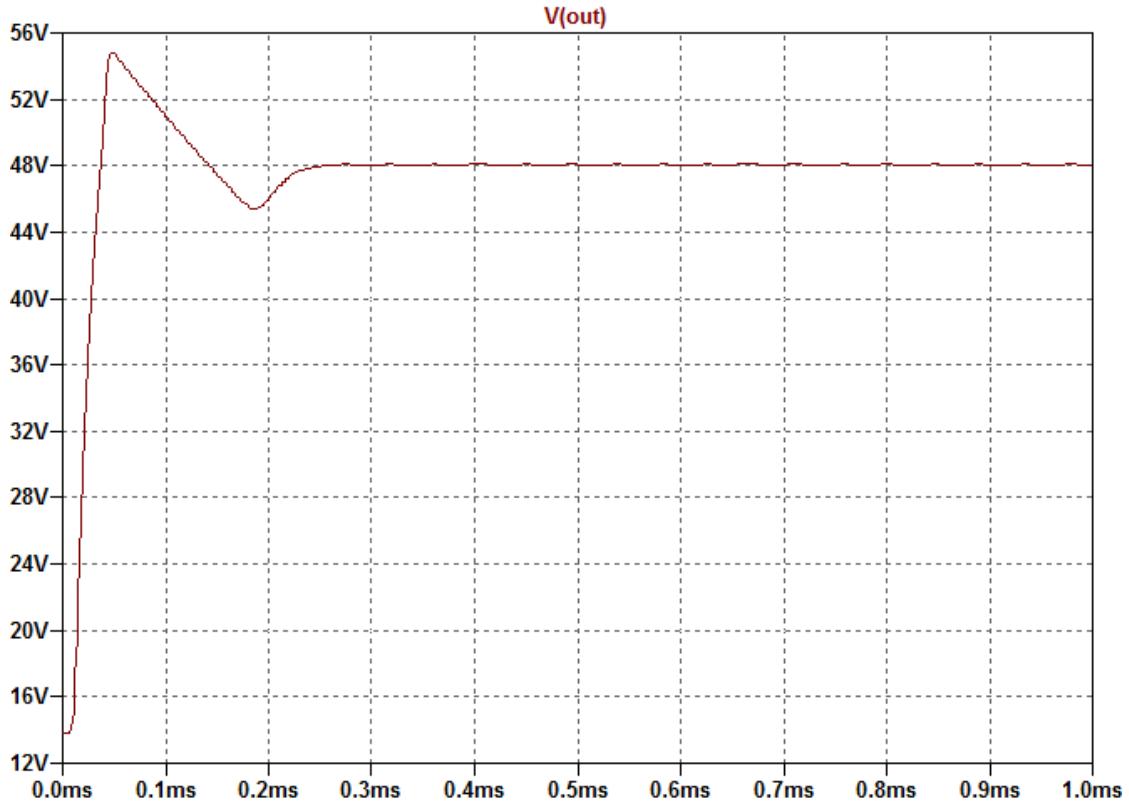


Figure 6: Voltage rise time and overshoot using a $0.22 \mu\text{F}$ output capacitor

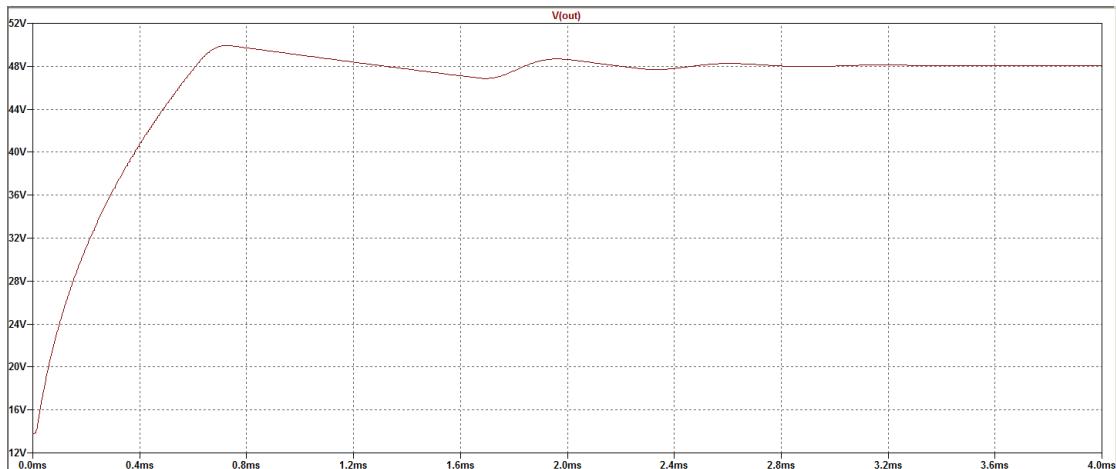


Figure 7: Voltage rise time and overshoot using a $4.7 \mu\text{F}$ output capacitor

The immediate effects of replacing the output capacitor from $0.22 \mu\text{F}$ to $4.7 \mu\text{F}$ is that while the output voltage rise time increases, the voltage overshoot decreases, as well as the voltage ripple. This is to be expected, as the larger capacitance of the output capacitor helps to stabilize the output voltage at the expense of speed, since it would take longer time to charge a bigger capacitor.

6.4 Transistor switch design

The 5V power line to the Piezo experiment MCU is to be controlled by the SiC MCU, which was solved using a PMOS transistor switch.

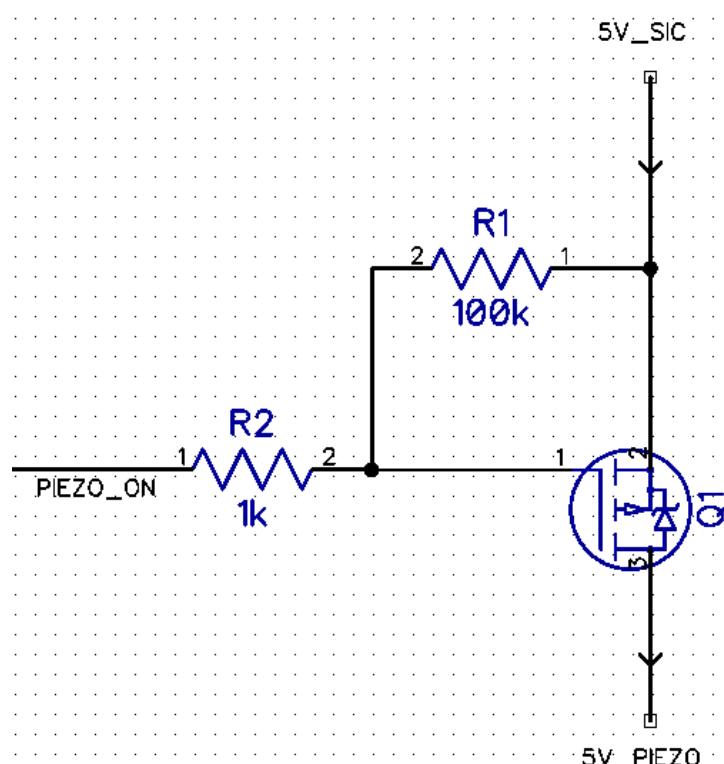


Figure 8: Transistor switch for the 5V_PIEZO line

The PIEZO_ON signal is controlled by an open drain configured MCU pin, which when driven low activates the PMOS transistor, allowing current to flow from the 5V_SiC line to the 5V_PIEZO line, powering the Piezo MCU.

6.5 Battery protection circuit

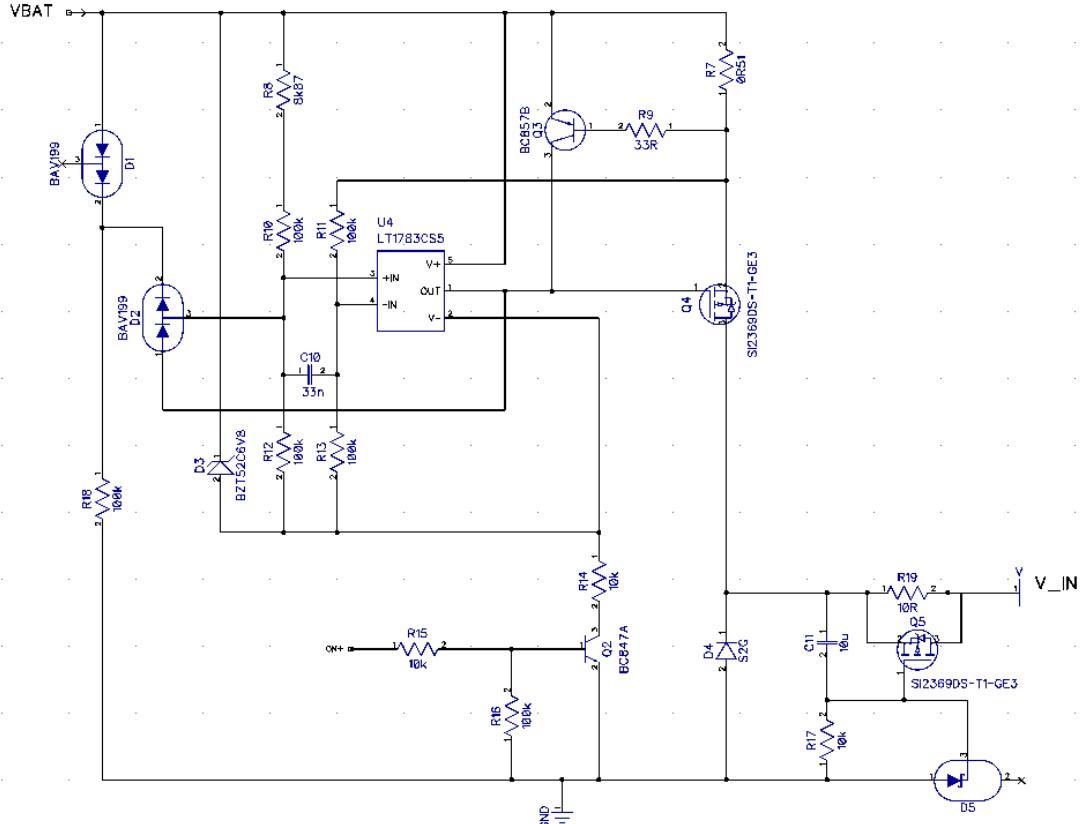


Figure 9: Battery bus switch schematic design

To protect the battery bus, a switch design needed to be implemented. The selected circuit has been used in several Swedish satellite projects[5], where the most recent one, Odin, is still operational after 16 years in space. When the transistor Q2 receives a logic ON command (+3.3V) from the MCU, the negative rail of the amplifier U1 is pulled down below the BATT+ rail, via the Zener diode D3 and the resistor R14.

The capacitor C10 initially biases the resistor bridge consisting of the resistors R8, R10, R12, R7, R11 and R13. This bias voltage between the inputs of the OP-amp forces the amplifier output low and switches on the power transistor Q4.

Thus, as long as there is no excessive load generating a too large voltage drop across the resistor R7, the non-inverting input of the amplifier remains lower than the inverting input, keeping the output low. With this configuration, the time of current limit before fusing is 2 ms (determined by C10), the fuse level is 1 A (determined by R8), and the current limit is 1.3 A (determined by R7).

Due to supply issues, the diode D4, S2GA-13-F was replaced by the similar diode S2G, and its effects were simulated. In Figure 9: **Battery bus switch schematic design**, the voltage VBAT denotes the raw battery voltage and V_IN denotes the circuit output voltage, i.e. the input voltage for the 10V linear converter and the 48V DC-DC boost circuit.

6.5.1 Simulation results

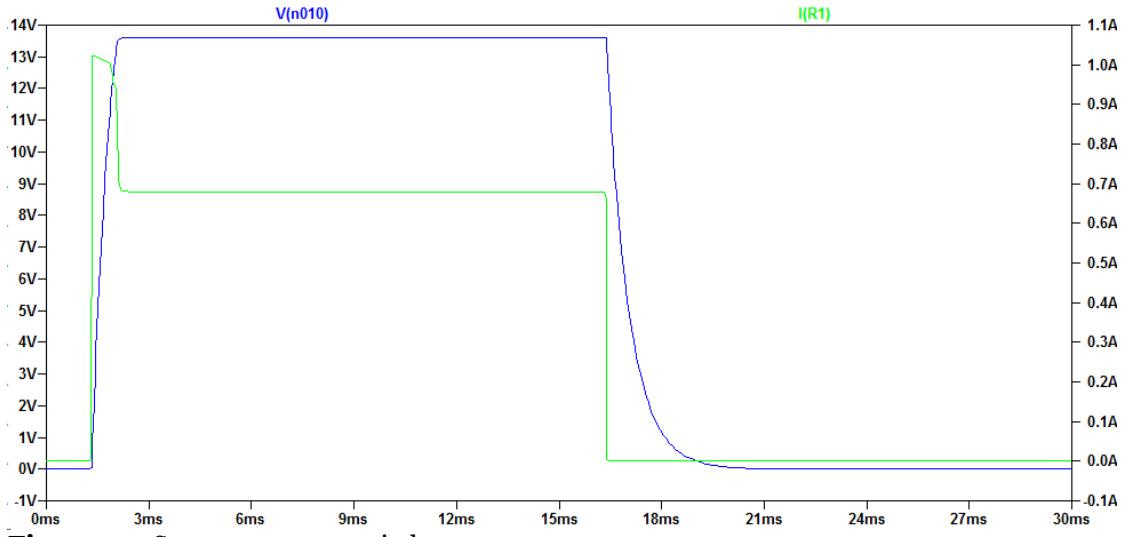


Figure 10: Surge current at switch-on

In case of a large capacitive load causing a surge current, the voltage drop across resistor R7 will switch on the transistor Q3, which in turn will force the gate of the transistor Q4 positive, thus reducing the output voltage until the current is acceptable. Figure 10 shows a simulation of this circuit with the load $20 \Omega // 33 \mu\text{F}$.

- The green line shows the output current, where the surge current is limited to 1 A, and the steady state current is 0.7 A.
- The blue line shows the output voltage with slow rise and fall during the charge/discharge of the capacitor.

If this situation or a short-circuit would happen, the current limiting will remain only until the capacitor C10 gets recharged, and the power output will be switched off.

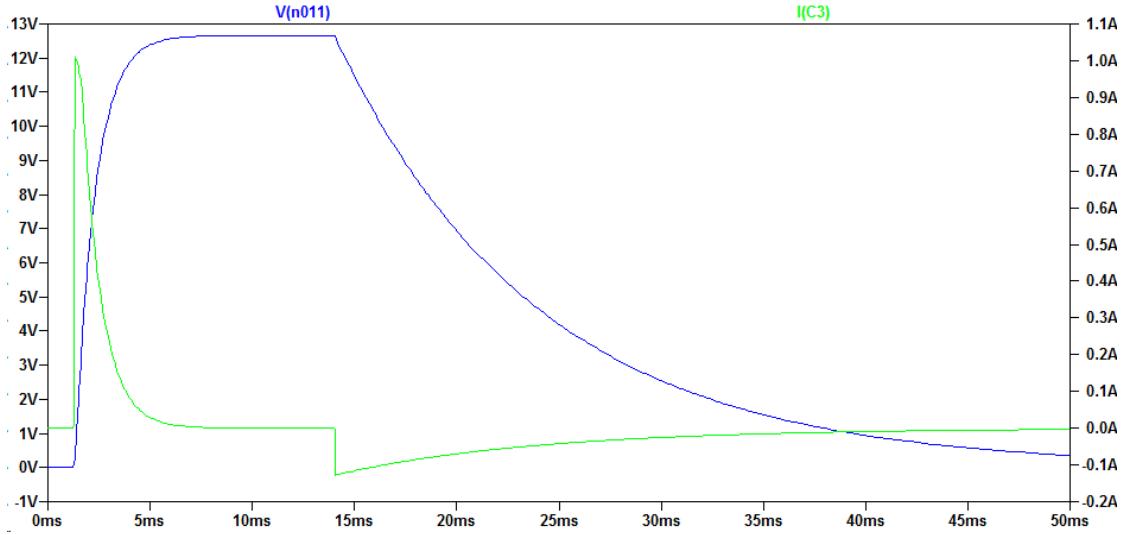


Figure 11: Inrush current limiting

The battery bus switch also includes a circuit to prevent an excessive inrush current to experiments is prevented. The simulation results shown in Figure 11 uses the load $100 \Omega // 100 \mu\text{F}$ to represent the equipment load.

- A peak current, represented by the green curve, of 1 A is delivered, and when the charging of the capacitor is almost finished, the resistor R19 is shorted by the transistor Q5.
- The voltage rise over the capacitive load is represented by the blue curve. The switch is turned off at 13 ms and the voltage drops with the RC constant of the load.

6.5.2 Automatic experiment shutdown hardware control

One of the newly emerged MIST hardware requirements was that if the 5V battery switch is turned off, all experiment circuits must be turned off automatically as a hardware implementation, ensuring that no experiments would continue to draw battery power.

The +ON logic command of the battery bus power switch is controlled via the PB12 pin on the SiC MCU connected to the base of the NPN transistor, effectively shutting down the battery power connection to the SiC PCB when this trace is connected to GND. Hence, if the 5V switch is turned off, the MCU loses power and the transistor base is pulled to GND.

This in turn functions as a hardware switch for the SiC and Piezo experiments, since the shutdown pins on the 10V linear converter and the 48V boost converter are active low, controlled by the SiC MCU pins PB10 and PB11 respectively. If the MCU fails to deliver a 3.3V signal to these pins, both voltage regulators will shut down immediately. This ensures experiment shutdown in case of a 5V switch-off, in accordance with the MIST team requirements.

6.6 I²C buffer circuit

To reduce the capacitive load on the I²C bus, a buffer circuit is required on each experiment PCB.

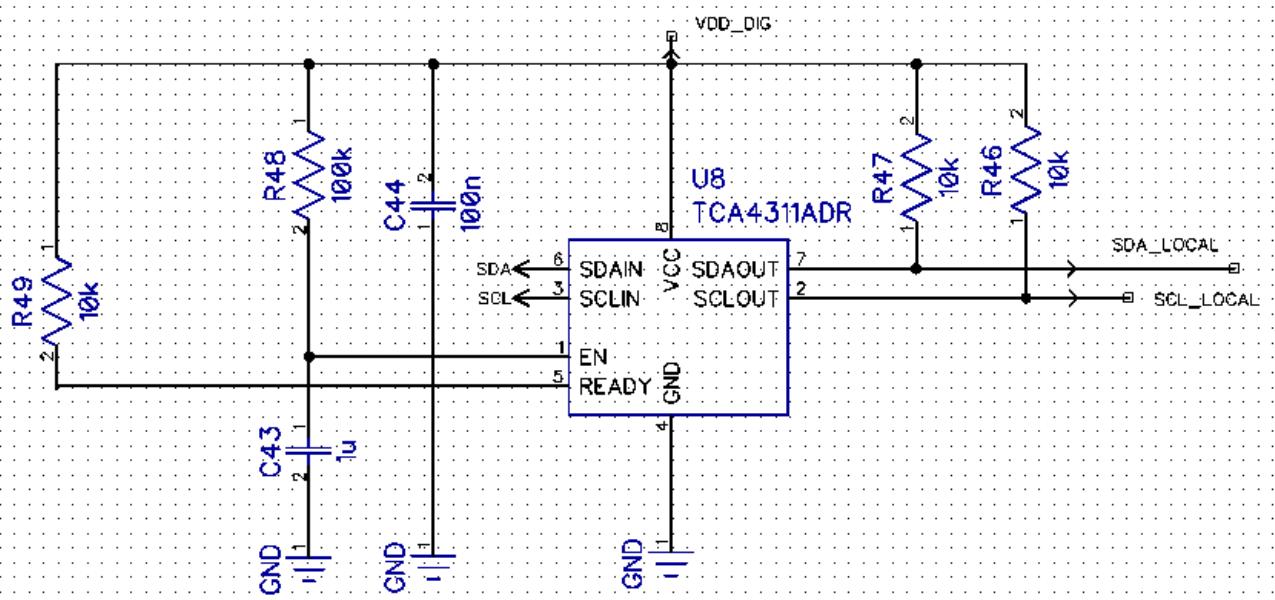


Figure 12: I²C buffer circuit schematic

When the SiC 3.3V power is active the enable pin on the I²C buffer circuit is driven high, bypassing the circuit, enabling I²C communication. In contrast, when this voltage is low, the circuit will not encumber the I²C bus. Since all units on this bus has open-drain outputs, pull up-resistors are needed to drive the outputs high.

7 PCB Layout

This chapter describes the hardware implementations and discussions of the final design of the PCB and its respective circuits. All schematic capture and PCB design were made using the software DipTrace[18].

7.1 Interface

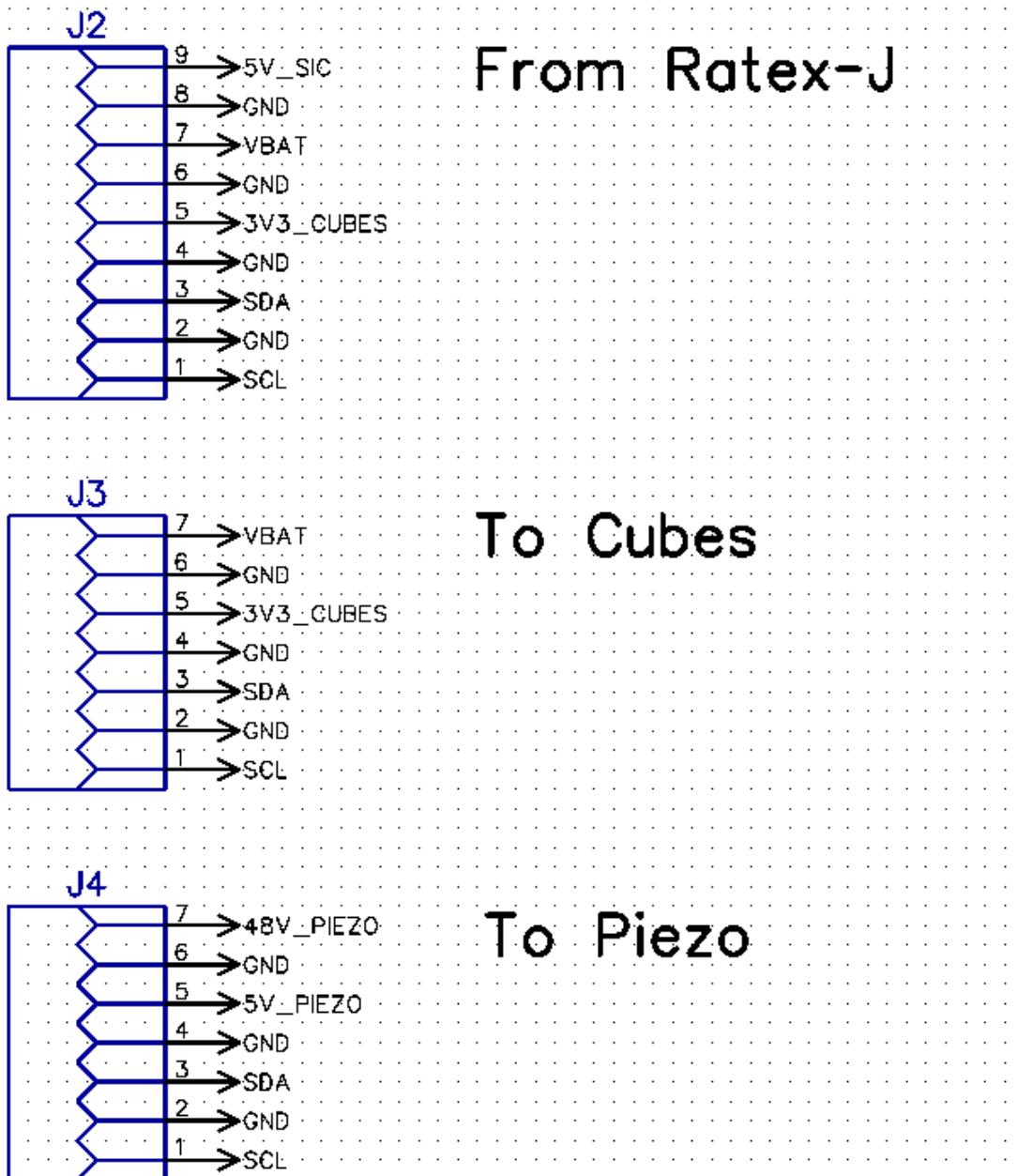


Figure 13: PCB I/O connectors with respective pin configuration

The SiC PCB is equipped with three I/O connectors in accordance to the MIST harness design[19]: The input connector J2, wired from the Ratex-J PCB, the output connector J3, wired to the Cubes PCB, and the output connector J4, wired to the Piezo PCB.

7.1.1 J2: Input connector from Ratex-J

This connector features the 5V input voltage needed to power the SiC MCU, the 12-14V raw battery voltage, the 3.3V input voltage needed for the Cubes PCB, the SDA and SCL data lines for I²C communication, as well as four GND pins.

7.1.2 J3: Output connector to Cubes

This connector features the 3.3V voltage needed for the Cubes MCU, the 12-14V raw battery voltage, the SDA and SCL data lines for I²C communication, as well as three GND pins.

7.1.3 J4: Output connector to Piezo

This connector features the 48V voltage needed for the Piezo LEGS experiment via the 48V DC-DC boost circuit, the 5V voltage needed for the Piezo MCU via the transistor switch, the SDA and SCL data lines for I²C communication, as well as three GND pins.

7.2 Circuit partitioning and final PCB layout

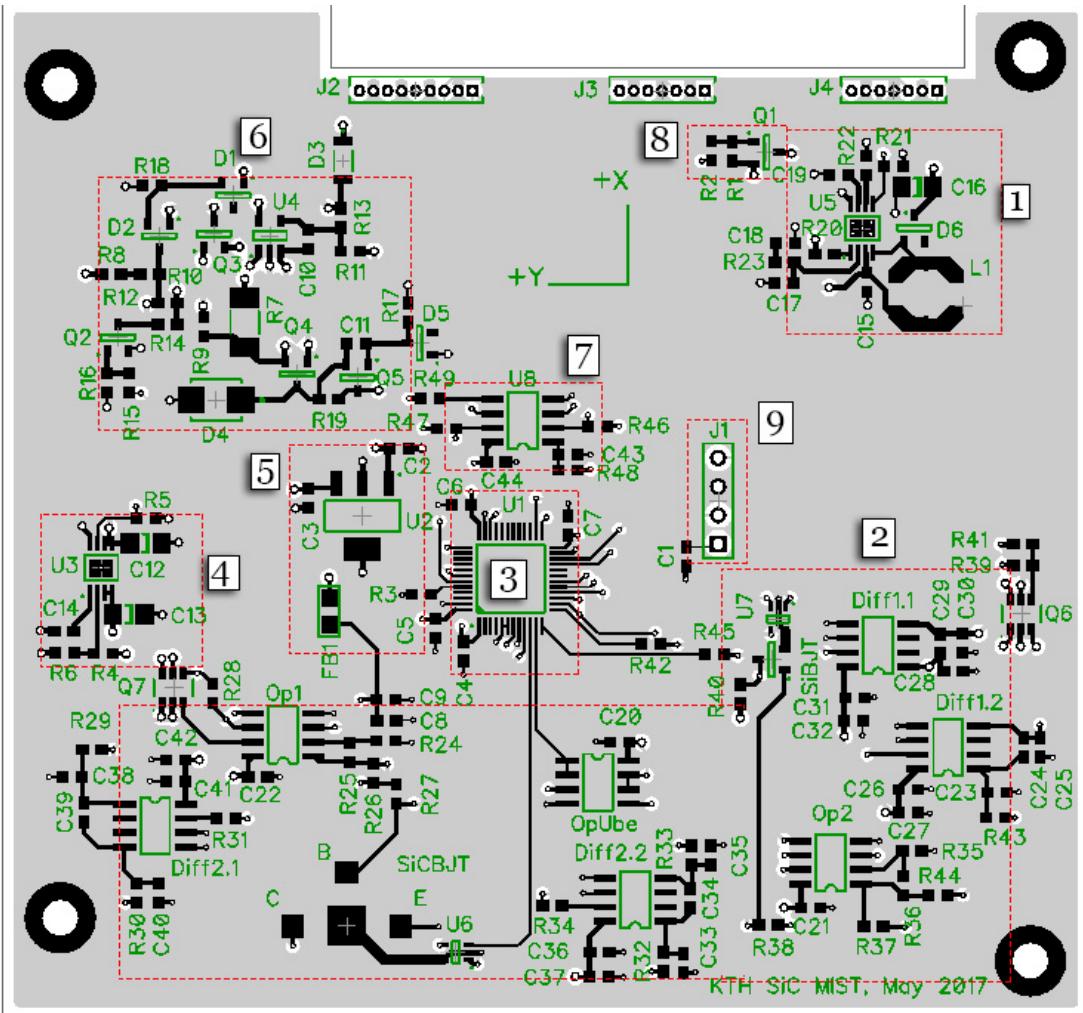


Figure 14: Final PCB design

The circuits of the PCB design have been partitioned as:

1. 48V DC-DC converter
2. Experiment measurements circuits
3. SiC MCU
4. 10V linear converter
5. 3.3V voltage regulator
6. Battery bus power switch
7. I²C buffer circuit
8. 5V transistor switch
9. SWD interface for MCU flash programmer

7.3 PCB layer stack-up and design considerations

7.3.1 PCB layer stack-up

In the most simplistic PCB design, as in the final prototype board used in the previous work which this report is built upon, two layers are used, whereas the SiC PCB uses four layers:

1. Top signal layer
2. Ground layer
3. Voltage layer
4. Bottom signal layer

7.3.2 PCB design considerations

- Using a four-layer stack-up, trace routing and component placement is facilitated due to having two signal layers available.
- Due to board space limitations, only SMD components has been used, almost exclusively in the package size 0603, which is the equivalent of 0.6 mm x 0.3 mm. Ceramic capacitors are used as opposed to electrolytic capacitors, since the latter are not allowed to be used in vacuum (space) by the MIST team due to containing fluids.
- Active components in a circuit should always be equipped with decoupling capacitors to shunt AC signals[20] that may be present in a DC signal to ground. The power rails on each such active components have been decoupled with one 100 nF capacitor in parallel with one 10 μ F capacitor to shunt high frequency noise. These are placed as close as possible to the voltage pins.
- The analog 3.3V voltage has been filtered using a ferrite bead, in accordance with the Design checklist proposed by Williams[12, p. 441].
- The 3.3V voltage regulator has been placed as close as possible to the MCU in accordance to the *PCB Design Guidelines For Reduced EMI* by Texas Instruments[14, p. 12].
- As a rule of common practice, all PCB traces uses 45° angles for every corner.

7.3.3 Grounding philosophy

A separate, intact ground plane has been used, which has several benefits in order to reduce EMI:

- The inductance decreases as the area increases; hence a large copper pour lowers the inductance and impedance as the ground plane is used as the signal return path.
- The ground plane has a screening effect, reducing EMI from the SiC PCB to the experiments stacked below. This also helps to reduce the incoming EMI from below.
- The four mounting holes on the PCB has been connected to ground, in accordance to a requirement from the MIST team.

7.3.4 Voltage planes division

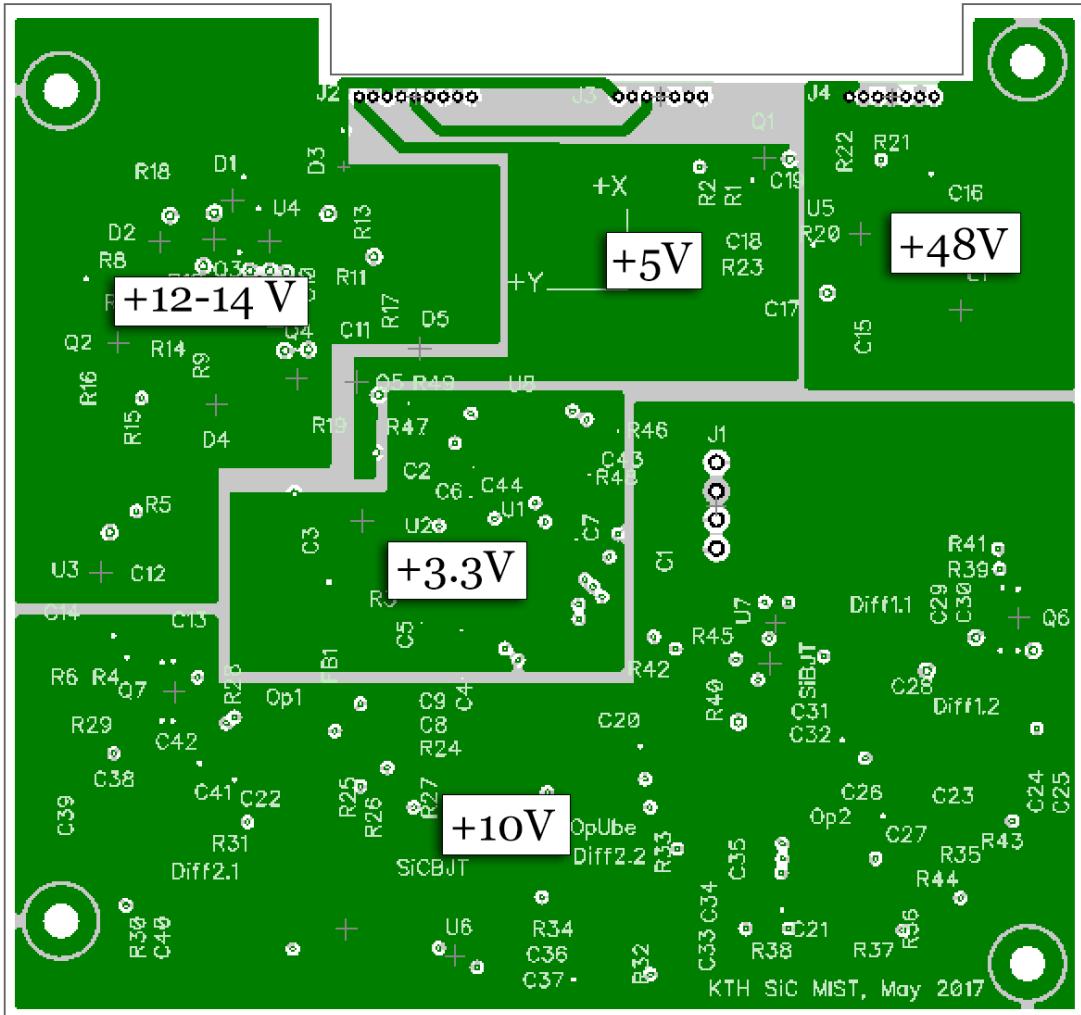


Figure 15: Voltage plane division

- Using a voltage plane can drastically reduce the inductance and impedance to the components due to the reduced power wiring[20].
- The second most top layer has been divided into five voltage planes, carrying 12-14V, 5V, 48V, 3.3V and 10V respectively according to figure Figure 15: **Voltage plane division**. This design allows for easy power routing using vias directly. Since the voltage layer and the ground layer are closely stacked together with an isolating layer in between, a capacitance is created, to increase voltage stability[21].
- The MIST team required that the PCB traces for the output power lines should be sized for 1A output current, which is why their width were chosen to 1 mm. Since there is no air in space to dissipate heat generated from the flowing current, the trace width needs to be selected with a margin. This width was calculated using the Advanced Circuits 4PCB trace width online calculator[22]. According to the PCB design tutorial rev. A, a 10 mil trace (0.254 mm) is otherwise considered an appropriate width for a current of 1A in air to secure a 10 °C temperature rise[20].
- Power planes and traces has been routed on the same layer, according to the EMC design guidelines from the web authority LearnEMC[23].

7.4 EMC considerations

The following measures have been taken in order to reduce EMI and increase the electromagnetic compatibility of the SiC PCB.

- The 48V DC-DC boost circuit is the only present circuit operating at a high frequency (1.5 MHz), and in order to reduce interference with the MCU and the analog measuring circuits, it has been isolated as far away as possible while still retaining as short distance as possible to its output connector on J4 in order to reduce trace inductance. Since the voltage plane supplying 48V, situated below this circuit, is connected directly to pin 7 on J4 as opposed to through a trace, inductance is mitigated.
- Analog and digital circuits should preferably be separated according to Williams' design guidelines[12, p. 441], and the only digital circuit present is the MCU. The MCU was placed in the center of the PCB, close to the analog measuring circuits. Keeping the 48V DC-DC boost circuit isolated was considered a bigger issue, which is why the MCU is found closer to the analog measuring circuits due to space limitation, as a compromise.
- No traces are routed below the MCU in order to avoid crosstalk between adjacent traces.
- All traces are kept as short as possible to reduce inductance, and therefore the EMI, most notably for the power traces. This also applies to the power trace widths, which have been selected as 1 mm wide for the same reason.
- Voltage and ground connections are made using vias, allowing for fewer and shorter traces which in turn reduces the EMI, and saves space.
- Only SMD components have been used to reduce EMI[14].
- All vias have been given a larger dimension of 0.25-0.5 mm as opposed to the minimum recommended via diameter of 0.2 mm, as to reduce inductance and therefore EMI.

7.4.1 DC-DC boost circuit hot loop

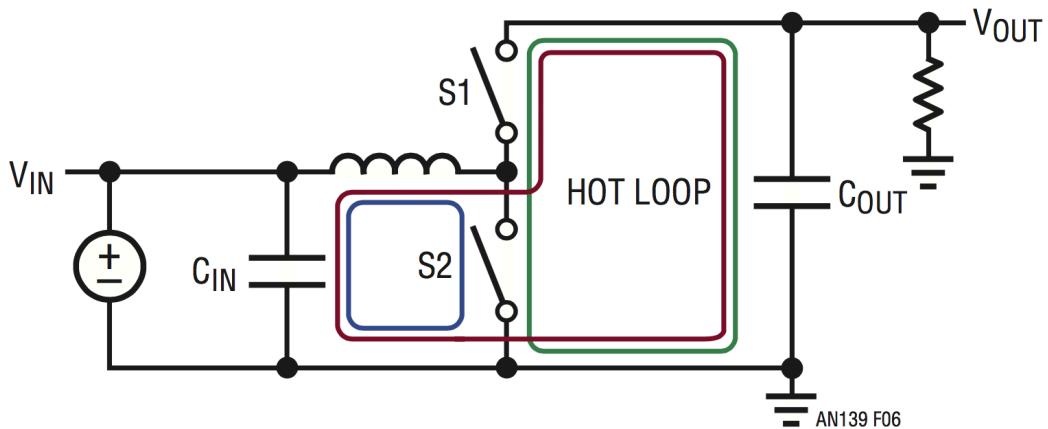


Figure 16: Hot loop[24].

In accordance to the LT8570 application note[24], the hot loop areas present in the 48V DC-DC boost circuit has been designed as small as possible in order to reduce EMI, which was previously examined by Simon Johansson.

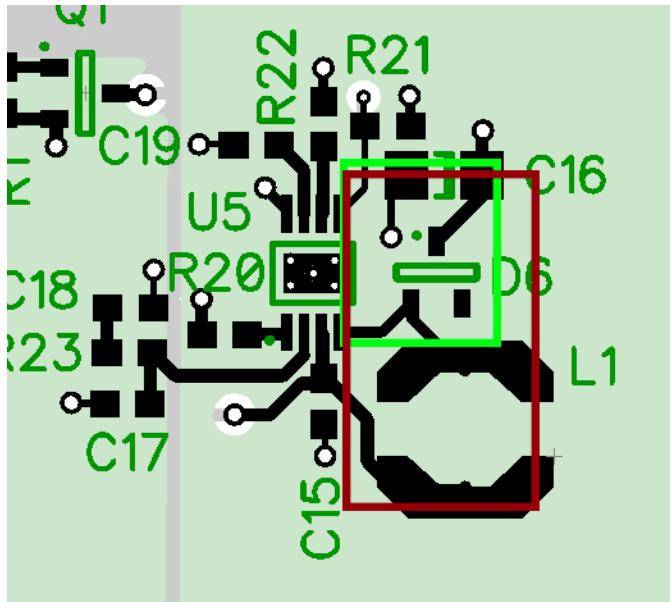


Figure 17: PCB hot loops

Figure 17: **PCB hot loops** shows the corresponding hot loop areas on the SiC PCB design.

7.5 PCB Assembly

The components on the PCB were populated using a grounded ESD mat and an anti-static wrist wrap in order to protect sensitive components from static electricity, which may otherwise posterior damage active components. Solder paste was applied to the PCB which was preheated on a hot plate, and the tin was then heated with a hot air gun until melted, securely attaching the components. Visual inspection to ensure good connectivity was done using a stereo microscope.

7.6 PCB Testing and fatal ordering mistake

The SiC PCB was ordered at, and manufactured by *Seeed Studio Fusion PCB Manufacturing*[25]. When the PCB had been populated, testing immediately showed that it did not work as intended and troubleshooting took place.

In a four-layer PCB design, there exists three possible variations of via holes: through-hole, blind and buried vias. The through-hole type is drilled through all layers of the board, the blind via is drilled from the top layer to the third or fourth layer only, and the buried via is drilled between layer two and three, making the hole buried between layers.

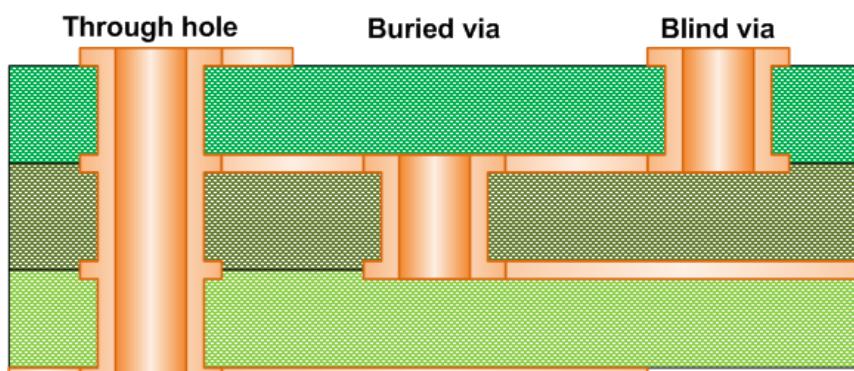


Figure 18: Via styles

The final PCB design present in this report and at the time of ordering, contained multiple blind vias, which is a common design practice. Nevertheless, the PCB ordering routine requires the user to specify whether the design contains blind and/or buried vias, since this requires a more refined drilling technique. Due to a misunderstanding, this option was not checked, and the conclusion was that this was the reason for the PCB malfunction.

Because of this, none of the blind vias were drilled, disconnecting numerous components and connectors, leaving the PCB non-functional. An updated design using only through-hole vias was made swiftly, and a new PCB order was made. Due to time constraints, however, the testing of this corrected PCB design will not be covered in this thesis work. Had there been more time, the new PCB would have been assembled and tested. Furthermore, the completion of the PCB design was delayed due to several important specifications and requirements not being decided by the MIST team at the time being.

The risk of a PCB malfunction was taken into consideration early in the thesis work since it would be difficult or even impossible to make multiple PCB orders time-wise, and while it would have been highly desirable to include the testing and confirmation of the intended functionality of the final SiC PCB design to confirm validity, this thesis will instead include the intended testing routines and protocol as well as a detailed section intended for future work.

8 Test software

To test the hardware, two test applications were developed: test application 1 to simulate the OBC and test application 2, to perform the different commands on the SiC MCU that are sent from application 1. A test application was developed by Hannes Paulsson and Mikael André in the semester of 2016 but due to several new hardware and software requirements on the hardware, the software needed to be further developed.

Test application 2 is flashed directly to the MCU on the SiC PCB and the communication between the two applications is handled by the I²C protocol. A description of the performed tests can be found in Appendix C.

8.1 Software initialization

Both test applications were initialized by the software tool STM32CubeMX, which generates the initialization code. This development tool allows the user to choose configuration parameters such as the function of each GPIO pin and the CPU clock speed.

The generated code can then be modified during the software development if circumstances change or new features need adding. Most of the code generated by STM32CubeMX, as well much of the code used during the development phase of this project, is based on a Hardware Abstraction Layer (HAL) library provided by the microcontroller manufacturer ST-Microelectronics. The HAL-library is used to simplify the hardware part of the code, that is, all the code written intended to use or manipulate the MCU or any peripherals.

This development software tool was chosen because the developers of the two test applications have previous experiences with this particular software.

8.1.1 Software delimitations

Both applications were written for test purposes only, to make it possible to test the hardware functions on the SiC PCB. Test application 1 only sends commands and retrieve data from test application 2 via I²C. There is no watchdog implemented, meaning if something goes wrong with the communications, the application will flush the buffer which contains the command and continue through the list of commands. Test application 1 will not receive any acknowledgements from test application 2.

The communication protocol and data packet specifications are not yet finalized by the MIST team; hence this would need to be correctly implemented in the final version of the software.

8.1.2 I²C addressing

Each I²C slave device has a 7-bit address that needs to be unique on the bus. Some devices have fixed I²C address while others have few address lines which determine lower bits of the I²C address. This makes it easy to have all I²C devices on the bus with unique I²C addresses.

Communication starts with a byte, where a 7-bit address followed by a data direction bit. If bit 0 in the address byte is set to 1 then the master device will read from the slave device, or if this bit is 0, the master device will write to the slave device.

Master devices need no addresses since it generates the clock (via SCL) and addresses individual I²C slave devices[26].

8.2 Test application 1 – OBC simulation

The main purpose of this test application is to simulate the OBC, that will send commands to the MCU on the SiC PCB as well as to retrieve data from the experiment that is performed on the board. This chapter gives an overview for how this application works.

The development board that was used was the STM32F3-Discovery development card. Based on the STM32F303VCT6 MCU, it includes an ST-LINK/V2 or ST-LINK/V2-B embedded debug tool, USB connection, LEDs and push-buttons[27].

To simplify the measuring on the developed PCB, the blue user push- on the STM32f3-discovery card was used to make it possible to test one function at a time. GPIO pins PB6 and PB7 are used for SCL and SDA respectively, for the I²C communication.

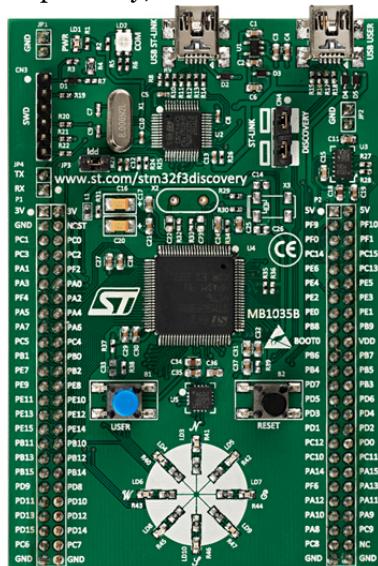


Figure 19: STM32F3 Discovery board[27]

8.2.1 Main program

The main program starts when the User button is pushed, and then sends commands to the SiC MCU in the following order each time this button is pushed:

1. “SHDNLinera” – this command shuts down the 10V linear converter.
 2. “SHDNSwitch” – this command shuts down the 48V DC-DC converter.
 3. “SHDNPoerPiezo5V” – this command shuts down the power to the Piezo legs MCU.
 4. “SHDNBatteryPower” – this command shuts down the battery power switch, which will also shut down the power to the SiC and Piezo experiments.
 5. “StartExperiment” – this command starts collecting data from the SiC experiments which is further explained according to the test protocol in Appendix C.

The results from the experiments are stored in a struct specified as “experiment_package” for which contains the following values:

- uint16_t temperature
 - float vrb
 - float vrc
 - float ube

To follow the executed command by to test application 1, the variable “aTxBuffer” can be added to the live watch.

8.3 Test application 2 – SiC measurement software

Test application 2 is run on the SiC MCU and includes tests to collect data from the experiments and to execute the desired commands from the OCB, including shutdown control for the voltage regulators as well as controlling the 5V supply line to the Piezo LEGS MCU.

The development board STM32Lo-Discovery was used. The STM32Lo53 Discovery kit is part of the STMLo series microcontrollers. The board is based on an STM32Lo53C8T6 MCU, and it includes an ST-LINK/V2-1 embedded debug tool interface, linear touch sensor, touch keys, LEDs, pushbuttons and a USB Mini-B connector [28]. GPIO pins PB6 and PB7 are used for SCL and SDA respectively, for the I²C communication.



Figure 20: STM32Lo-Discovery board[28]

8.3.1 Main program

The main program consists of three functions:

- Flush_Buffer()
 - Receive_message()
 - Check_OBC_message()

To follow the executed command by to test application 2, the variable “aRxBuffer” can be added to the live watch.

8.3.2 SHDN Command

The MIST group has specified that the following circuits need to be switched on/off by command from the OBC:

- Battery bus power switch
- 48V DC-DC converter
- 10V linear converter
- 5V switch to Power Piezo Legs MCU

The regulators in the 48V DC-DC converter[17] and the 10V linear converter[29] have a SHDN pin that is active low, meaning that the circuits will be turned off if these pins are not connected to +3.3V.

8.3.3 SetDac

To perform any of the experiment a Digital to Analogue Converter is required. The function setdac(double Voltage) sets the desired output voltage by the formula:

$$V_{dac} = \frac{(2^{12} - 1) * Voltage}{Vdd} = \frac{4095 * Voltage}{3.3}$$

For example: $\text{setdac}(3.1) \Rightarrow \frac{4095 * 3.1}{3.3} = 3847 = 0xF07$

The calculated value V_{dac} is then used as a parameter for the function HAL_DAC_SetValue.

8.3.4 Convert_temperature

The temperature sensors used to measure the temperature of the SiC and Si transistors is the LMT85, which is an analog temperature sensor with class-AB output, developed by Texas Instruments. The LMT85/LMT85-Q1 are precision CMOS integrated circuit temperature sensors with an analog output voltage that is linearly and inversely proportional to temperature. It has accuracy specified in the operating range of -50°C to 150°C[30].

Although the LMT85/LMT85-Q1 is almost linear, its response has a slight umbrella parabolic shape. This shape is calculated using the formula:

$$\text{Temperature} = \frac{8.194 - \sqrt{(-8.194)^2 + 4 * 0.00262 * (1324 - V_{temp})}}{2 * (-0.00262)} + 30$$

The function Convert_temperature converts the output voltage from the temperature sensors to the temperature in °C with this formula before the collected data from the experiment are sent back to test application 1.

8.3.5 StartExperiments

When test application 1 sends the command “StartExperiments”, test application 2 will start the function StartExperiments which will perform 4 readings. There will be 4 different Voltage settings which is executed by the DAC and is executed in the specific order:

1. 3.1V
2. 2.1V
3. 1.1V
4. 0.5V

Before and after each voltage setting the DAC is set to 0V and then a delay of 2ms is executed before next reading takes place. So, to be more specific of how the DAC will set the voltage the DAC will execute the following setting:

1. 0V
2. 3.1V
3. 0V
4. 2.1V
5. 0V
6. 1.1V
7. 0V
8. 0.5V

The readings are all copied in to the struct “experiment_package” named experiments which is an array with 8 slots, and is then transferred to test application 1.

9 Results

Due to not yet having access to the final PCB, little testing could be made. Only the test applications were tried and tested, using last year's PCB prototype, to the extent it was possible considering the hardware incompatibility between the new and the old designs.

Test application 1 and 2 worked as intended without any errors or failure and most notably, proved a working I²C communication which was yet to be confirmed by the previous work from 2016.

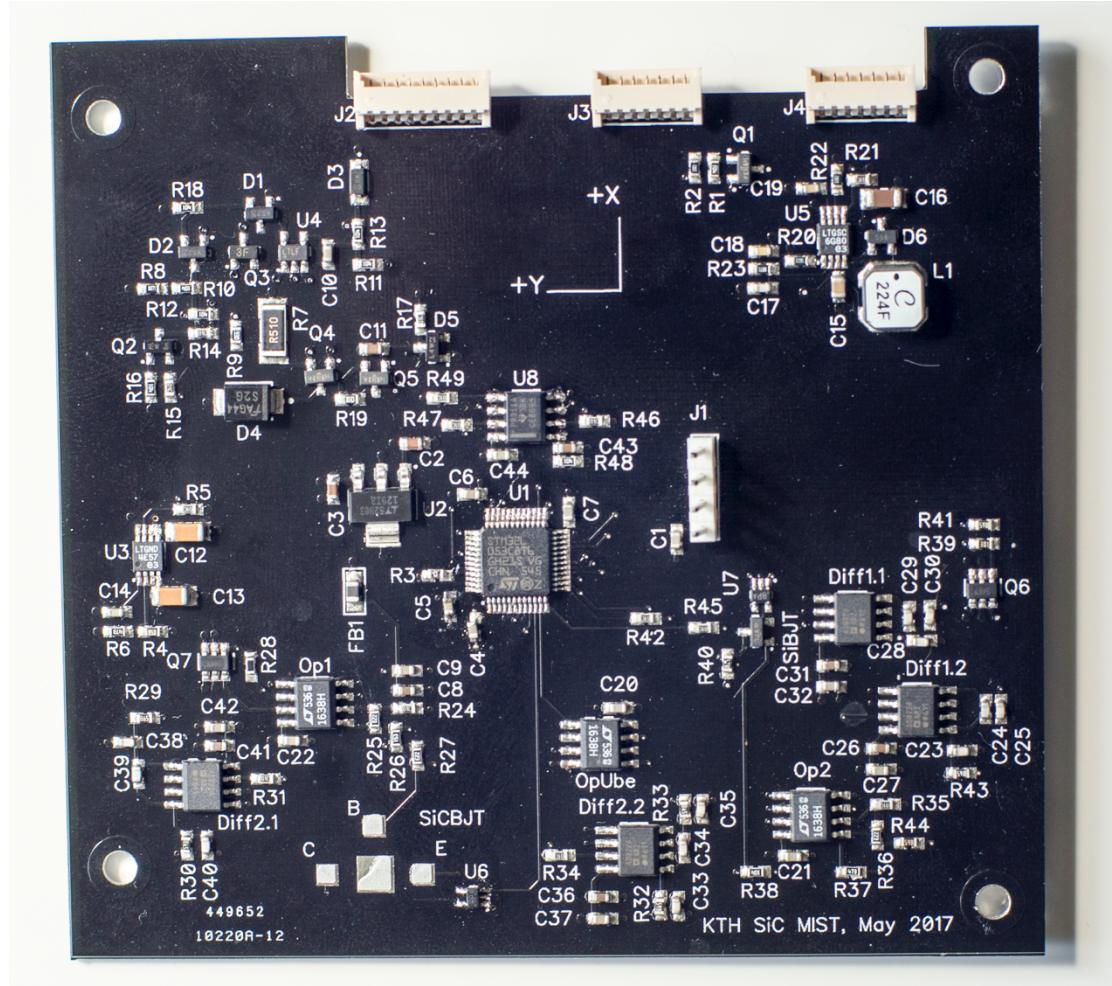


Figure 21: Finished populated SiC PCB

9.1 Test protocol

The following software and hardware tests were executed using the test applications or by manually measuring:

Circuit	Test description	MCU pin	Header/pin	Desired output	Result
MCU (U1)	I ² C communication – send command from OBC to MCU	PB6 PB7	J3 - pin 11	Working	Working
MCU (U1)	I ² C communication – receive data from MCU to OCB	PB6 PB7	J3 - pin 11	Working	Working
10V linear converter	Test to confirm that the 10V linear converter can be switched off from the OBC.	PB10	R4, pin 2 GND	The 10V linear converter delivers 0V at OFF and 10V at ON	Working
N/A	Test to confirm the 3.3V voltage to Cubes	N/A	J2, pin 5 J3, pin 5	The measured output voltage is 3.3V	Working
N/A	Test to confirm the VBAT voltage to Cubes	N/A	J2, pin 7 J3, pin 7	The measured output voltage is equal to the input voltage (12-14V)	Working

Note that all of the above performed tests will need to be performed anew on the final PCB.
For a full list of all required tests, see Appendix C.

10 Conclusions

This section will contain a theoretical discussion regarding the PCB design rather than conclusions in regard to testing and verifying the PCB functionality. The original problem definition for this thesis was:

1. What are the most important PCB design aspects to accommodate all the required circuits on a 90 x 96 mm PCB?
2. In case of a short circuit from one of the experiments, will the battery bus always be protected?
3. If the battery switch is turned off, will the experiments be turned off automatically as well, to preserve battery life?
4. What are the most important PCB design aspects to best meet the system requirements, as well as the EMC requirements?
5. What are the advantages of using a four-layer PCB design, as opposed to a two-layer design?

Theoretically, questions 2 and 3 in the problem definition have been answered and solved, albeit only through means of simulation. To provide validity, experiments and measurements need to be made. Questions 1, 4 and 5 have been answered in sections 10.1-10.4.

The project goals for this thesis were:

1. Compilation, finishing and improving upon previous schematics.
2. Implementation of a battery bus power switch to provide overcurrent protection for the battery in case of experiment failure.
3. Final PCB design, based on the final schematic.
4. ~~Test of the final PCB to ensure desired functionality.~~
5. Documentation of all work and specifications.
6. To provide guidelines for the future final software development.

Goals 1-3 have been met, as described in section 10.2. Goal 4 has not been met, as described in section 10.6. Goal 5 has been made by the completion of this degree work. Goal 6 has been met, through the inclusion of section 12.2 in this report.

10.1 Design feasibility

Using a four-layer design with separate ground and voltage planes proved to be of great benefit regarding simplifying trace routing and overall component placement. This in turn made it possible to put greater care into the circuit partitioning, where both aspects help to mitigate EMI due to reduced inductance and impedance. Furthermore, the ground and voltage planes should help to improve voltage stability due to the capacitance between the two closely stacked planes.

10.2 Design improvements and implementations

The SiC PCB design successfully houses all necessary circuits from last year's theses work which this thesis is based upon, and also takes every new MIST-team hardware requirement into consideration. This includes:

- Adding of the 48V DC-DC boost circuit to the PCB design.
- Adding a 4.7 μF output capacitor to the DC-DC boost circuit.
- Replacing the output capacitors and resistors in the 48V DC-DC boost circuit to components with a higher maximum voltage rating of 75V to 100V to provide adequate safety margin.
- Adding of drilled vias to the LT8570-1 ground plate used in the 48V DC-DC boost circuit to provide cooling through heat dissipation, by manufacturer recommendation.
- Adding a 3.3V step down regulator to provide the correct MCU voltage, based on recommendation from Paulsson and André to meet the system requirements.
- Removing of components and interfaces used by Paulsson and André that are not necessary for the final PCB design.
- Various corrections to the supplied schematics and designs from last year's theses.
- Adding of an I²C buffer circuit.
- Adding of a transistor switch to provide means for the SiC MCU to control the 5V power supply line to the Piezo PCB.
- Adding of a battery bus power switch to protect the satellite battery in case of a short circuit on either of the experiment circuits, as well as inrush current protection.
- The hardware implementation of an experiments shutdown in case of a battery switch suspension to preserve satellite battery life.

10.3 EMC considerations

The circuit that is most likely to emit radiation is the 48V DC-DC boost converter, and it has been isolated from all other circuits. The voltage plane supplying 48V, situated below this circuit, is connected directly to pin 7 on J4 as opposed to through a trace, thus inductance is mitigated.

Using a separate ground plane to provide a low-impedance signal current return path reduces loop areas and in turn, the EMI. The copper ground plane also helps with shielding from incoming and outgoing radiation.

Measuring the resulting EMI radiated from the PCB, as well as its susceptibility to incoming EMI would be desirable, but is outside the scope of this thesis work.

10.4 Via styles

Using only through-hole vias as opposed to blind vias in the four-layer PCB-design proved to be a more sensible approach, as to avoid ordering inconvenience. The manufacturing costs for this type of vias are then also considerably reduced.

10.5 Test software

Two test applications were developed, based upon the software created by Johansson and André during last year's thesis work. Application 1 is used to simulate the satellite OBC, to send commands to the SiC MCU, and to collect data from the experiments. Application 2 is run on the SiC MCU, to collect data from the experiments and to execute the desired commands from the OCB, including shutdown control for the voltage regulators as well as controlling the 5V supply line to the Piezo LEGS MCU.

This software could only be partially tested due to not having access to a working specimen of the SiC PCB, however what tests could be made using last year's hardware worked as intended.

10.6 Drawbacks

Working in a large-scale project including numerous people has the benefits of collaboration and the exchange of experiences and knowledge. To the individual working in the project, this potentially means having less control and conforming to management decisions. For different equitable reasons, this meant that the ordering of the final PCB was delayed. During the eventual ordering process an error was made resulting in a non-functional product, and due to time-shortage, there was not enough time to order, populate and test a new product.

The probability of a PCB malfunction was constantly taken into consideration in the thesis as a project risk and considering the time scope, the effects were beyond control. This document contains a description of all the tests that were to be performed on the final PCB to ensure functionality.

11 Ethics, sustainability and benefit

Since this is the first time KTH launches a satellite, in a larger perspective, KTH will ultimately gain knowledge and experience for possible future launches. Hence the SiC PCB, being part of the satellite, will assist in this matter. Furthermore, knowledge has been gained regarding four-layer PCB design specifically, and some pitfalls that may arise.

The *SiC in Space* experiment could potentially provide research valuable for the future of space exploration, if SiC demonstrates the desired qualities. KTH could also gain knowledge on how to design power supplies suitable for use in space, including battery safety and power management.

The MIST project may produce space debris containing toxic materials, which should be subject to future research in order to minimize environmental effects. The amount of debris in the LEO is to be minimized by incinerating the satellite after conducting the experiments. During soldering, only lead-free solder was used due to environmental considerations.

The final non-functional PCB will not be discarded, but instead put to use by the MIST team who will use it in a 3D mockup of the satellite.

12 Future work

12.1 Software and hardware tests

The following additional tests need to be performed on the final PCB in future work to ensure PCB functionality:

- SWD interface – MCU flashing
- Battery bus current draw limitation
- Battery bus short-circuit simulation
- Shutdown – 48V DC-DC converter
- Shutdown – battery bus switch
- Shutdown – 5V transistor switch for Piezo LEGS MCU
- Voltage readings for the Si/SiC-transistors
- Temperature readings for the Si/SiC-transistors

All measurements are implemented in the finished test applications, as well as the shutdown control. MCU flashing can be made using the STM32Lo-Discovery board with ST-link, using the Keil MDK software.

For additional technical details and requirements regarding the test protocol, see Appendix C.

12.1.1 Battery bus current draw limitation and short-circuit simulation

To test the battery bus current draw limitation, a sensible approach would be to simulate a short circuit. This can be achieved by connecting a $1\ \Omega$ resistor across pin 3 on transistor Q5 and GND, i.e. the output voltage from the battery bus power switch circuit (V_{IN}) and measuring the resulting current draw through, and the voltage across the resistor.

The results should be similar to the simulated results in section 6.5.1, showing that the current draw is never greater than 1 A. It would be necessary to use a resistor with at least 1W power rating, since the power dissipation should be equal to 1W, provided a current of 1 A and a voltage of 1V.

12.1.2 Automatic circuit shutdown control

To ensure that no experiments draw power from the satellite battery if the 5V battery switch is turned off, the voltage can be measured across pin 7 on J4 and GND for the 48V DC-DC boost circuit, and across pin 2 of resistor R4 and GND for the 10V linear converter. As soon as the 5V voltage is turned off, the 48V and 10V voltages should reach 0V for a positive result.

12.1.3 Power supply specifications

The requirements for the DC-DC converters are to supply the Piezo motor with 48V and 15 mA, and the SiC experiments with 10V and 10 mA. To ensure that the specifications for the 48V converter are met, a $3.2\ k\Omega$ resistor could be mounted across pin 7 on J4, and GND. With this load, the measured current draw should be equal to the required 15 mA. Using an oscilloscope, the output voltage ripple could also be evaluated, to ensure DC stability. The power dissipation in the resistor would be equal to 0.72 W using this configuration, hence its power rating should be at least 1 W or greater.

To ensure that the specifications for the 10V converter are met, a $1\ k\Omega$ resistor could be mounted across pin 2 of resistor R4 and GND. With this load, the measured current draw should be equal to the required 10 mA.

12.1.4 Vibration tests

When eventually launching the satellite, it may be subjected to a high level of vibrations. The SiC PCB would need vibration testing to simulate these conditions to ensure component placement.

12.1.5 SWD header

After assembly and the subsequent MCU flash programming, the SWD header is to be removed to save space.

12.1.6 Diode D6

The diode D6 used in Johansson's design of the 48V DC-DC boost converter is the ZHCS506[31] small signal Schottky diode, which has a forward-voltage drop rating of 630 mV. LT8570-1 boost converter datasheet specifies the recommendation of a low forward-voltage drop Schottky diode such as the Diodes Inc. PD3S140[32], which has a forward-voltage drop of 550 mV. A change of this component may improve the circuit performance, and would need to be evaluated in future work.

12.2 Software completion

At the time of this thesis work, the satellite communication protocol, as well as the I²C data package specification is yet to be decided. Eventually, when these details emerge, the SiC MCU software will need to be completed with these implemented specifications in order to send and receive messages via the I²C bus to the OBC.

As a suggestion, this could be a future thesis work suitable for one person since the test software developed for this thesis work is well advanced and would need few additions to be considered completed. Testing would also have to be made to certify that the OBC commands are executed correctly by the SiC MCU.

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Appendix A – PCB schematics

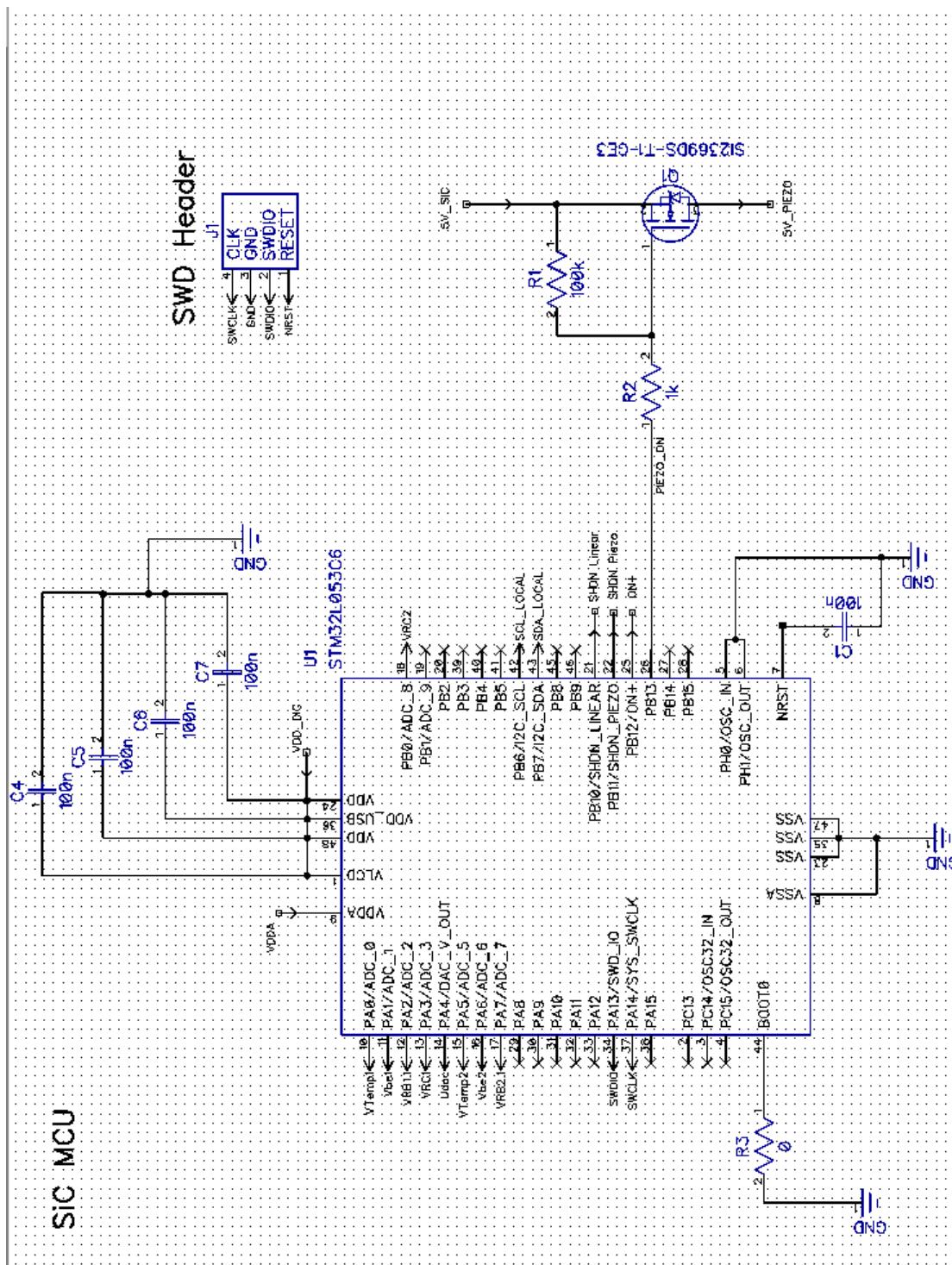


Figure 22: MCU/SWD header/transistor switch schematic

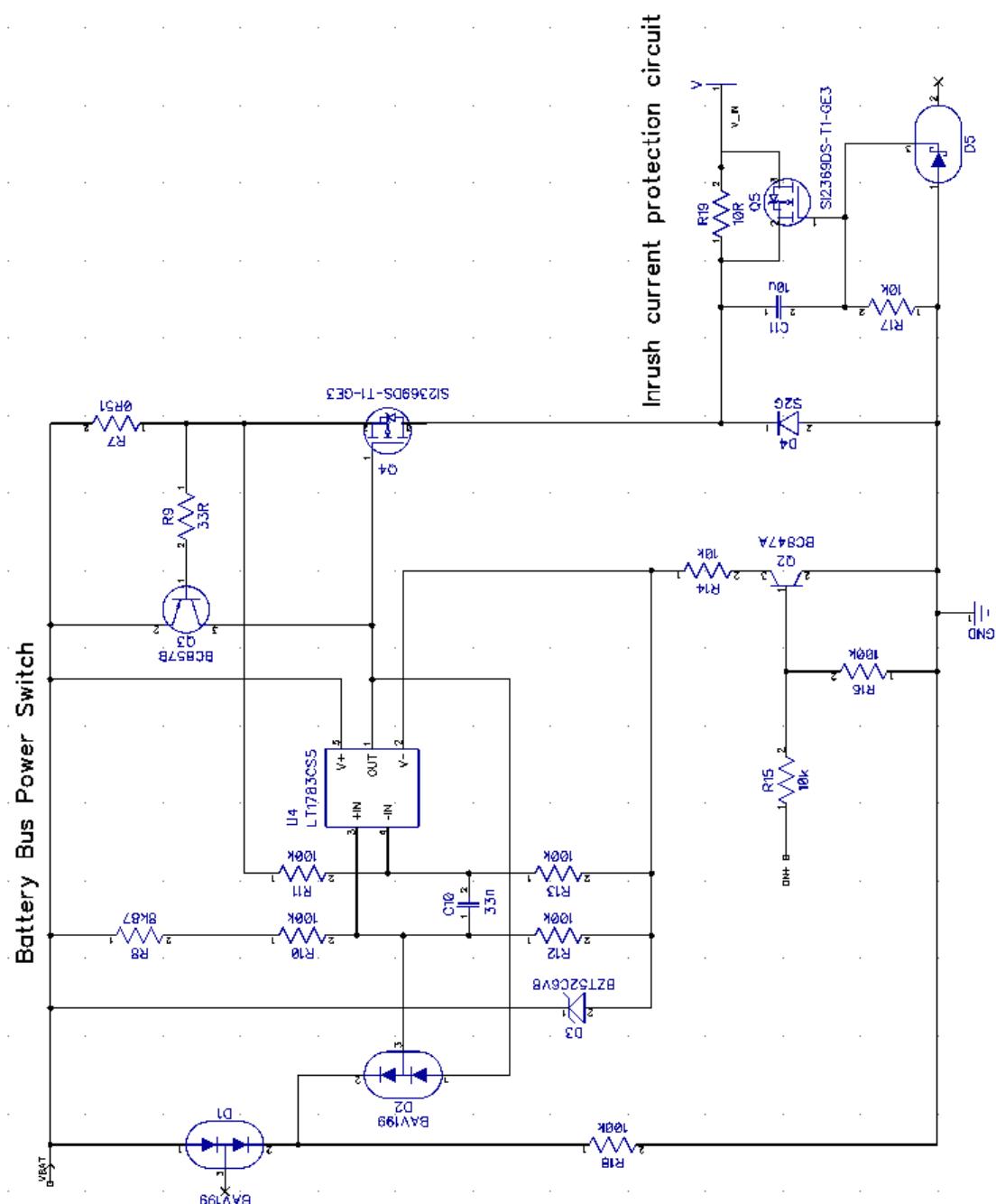
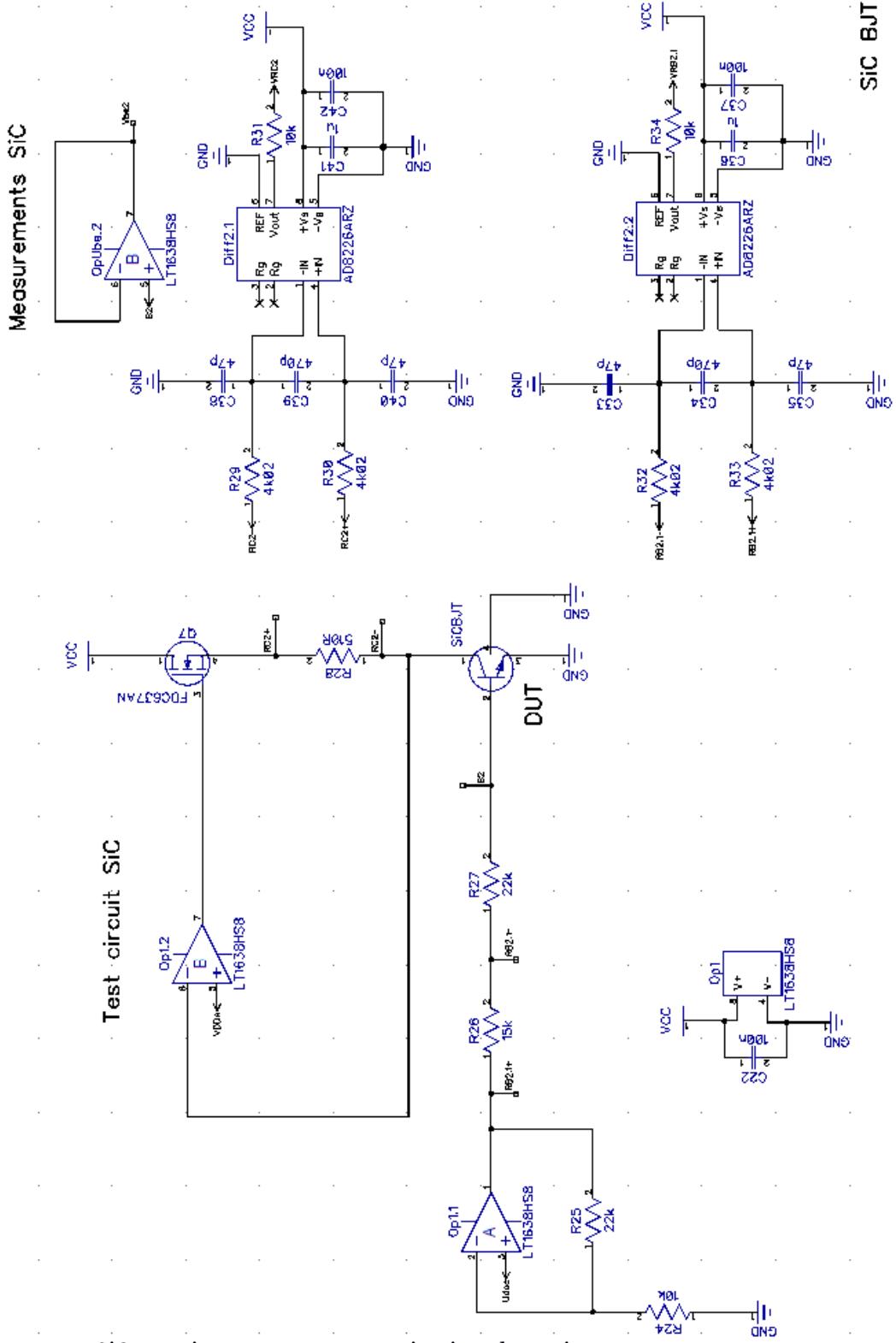


Figure 23: Battery bus power switch with inrush current protection schematic



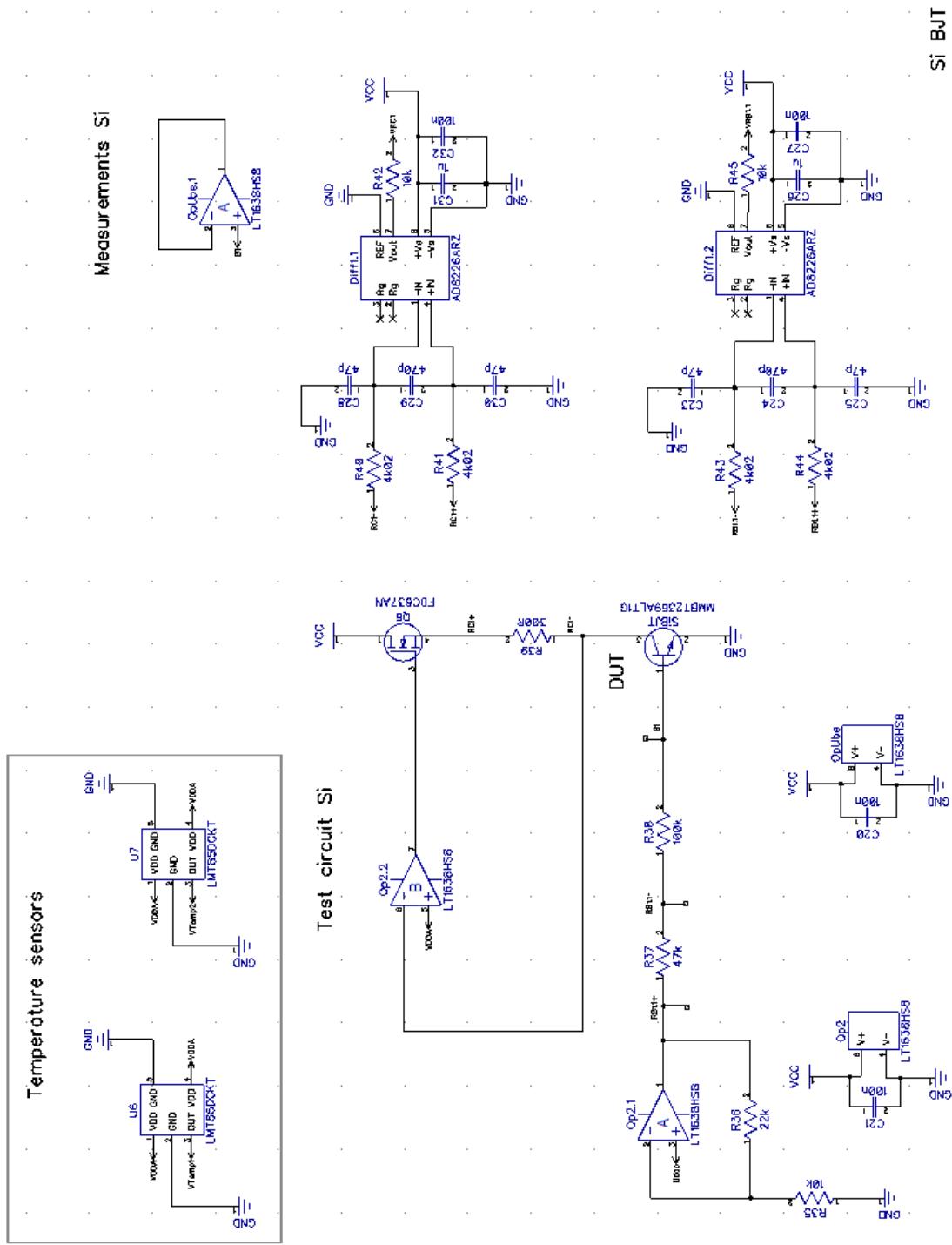


Figure 25: Si experiment measurement circuits schematics

10V Linear converter

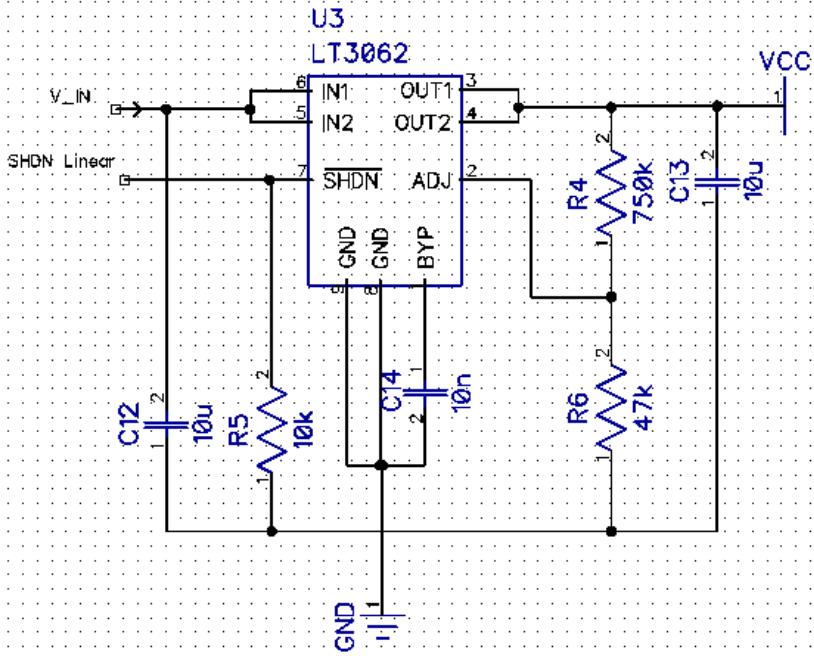


Figure 26: 10V linear converter schematic

48V Piezo LEGS DC-DC Boost converter

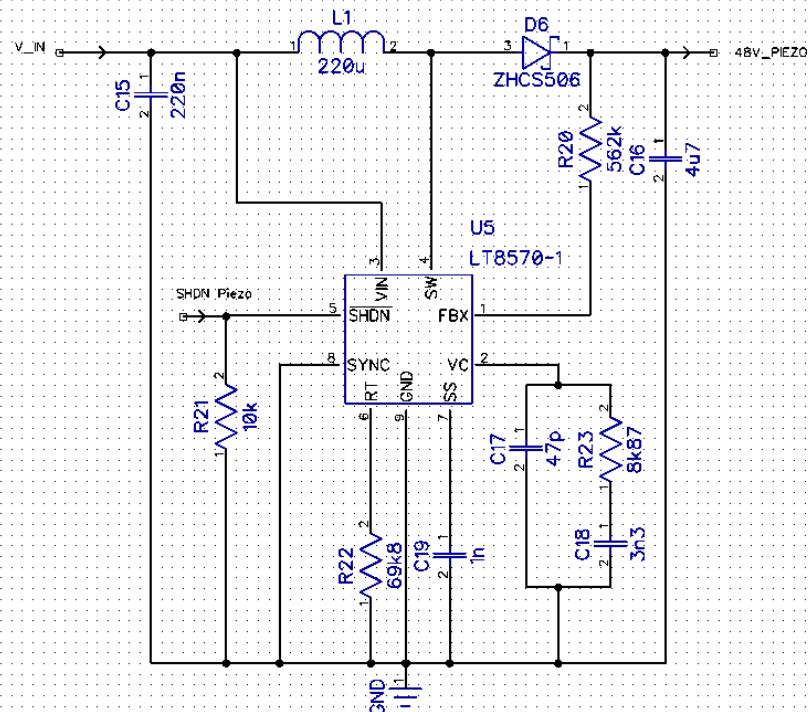


Figure 27: 48V Piezo LEGS DC-DC boost converter schematic

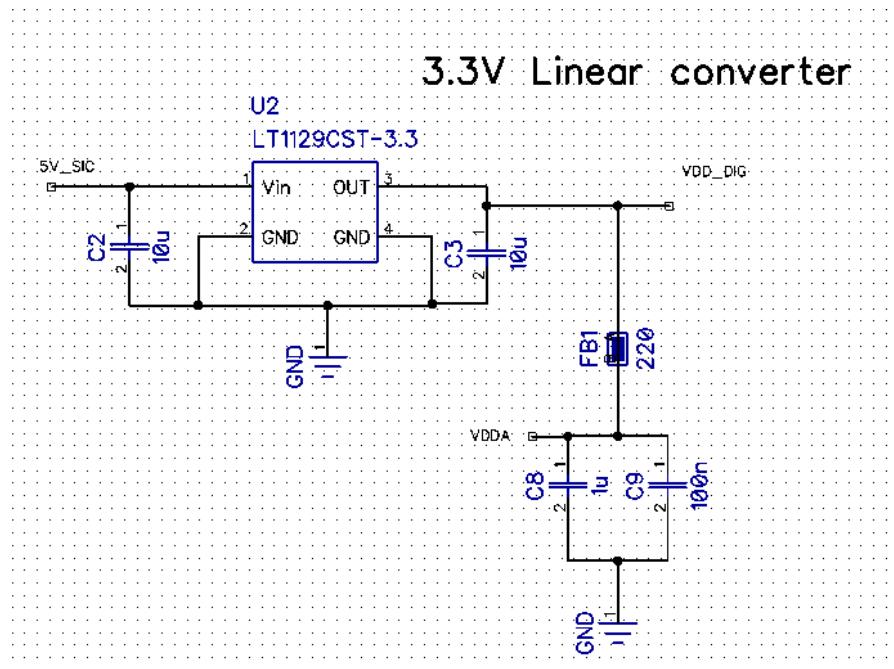


Figure 28: 3.3V MCU linear converter schematic

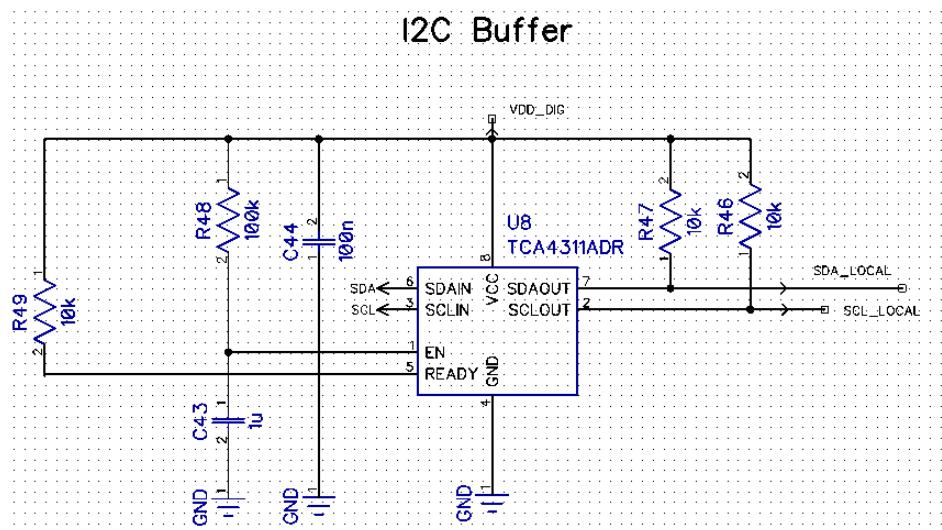


Figure 29: I²C buffer schematic

Appendix B – Bill of materials

RefDes	Value	Name	RefDes	Value	Name
C1	100n	CAP_0603	C24	470p	CAP_0603
C2	10u	CAP_0603	C25	47p	CAP_0603
C3	10u	CAP_0603	C26	1u	CAP_0603
C4	100n	CAP_0603	C27	100n	CAP_0603
C5	100n	CAP_0603	C28	47p	CAP_0603
C6	100n	CAP_0603	C29	470p	CAP_0603
C7	100n	CAP_0603	C30	47p	CAP_0603
C8	1u	CAP_0603	C31	1u	CAP_0603
C9	100n	CAP_0603	C32	100n	CAP_0603
C10	33n	CAP_0603	C33	47p	CAP_0603
C11	10u	CAP_0603	C34	470p	CAP_0603
C12	10u	CAP_1206	C35	47p	CAP_0603
C13	10u	CAP_1206	C36	1u	CAP_0603
C14	10n	CAP_0603	C37	100n	CAP_0603
C15	220n*	CAP_0603	C38	47p	CAP_0603
C16	4u7*	CAP_1206	C39	470p	CAP_0603
C17	47p*	CAP_0603	C40	47p	CAP_0603
C18	3n3*	CAP_0603	C41	1u	CAP_0603
C19	1n*	CAP_0603	C42	100n	CAP_0603
C20	100n	CAP_0603	C43	1u	CAP_0603
C21	100n	CAP_0603	C44	100n	CAP_0603
C22	100n	CAP_0603			
C23	47p	CAP_0603			
D1		BAV199	J3		53048-0710
D2		BAV199	J4		53048-0710
D3		BZT52C6V8	L1	220u	LPS6235
D4		S2G	Op1		LT1638HS8
D5		BAT54	Op2		LT1638HS8
D6		ZHCS506	OpUbe		LT1638HS8
Diff1.1		AD8226ARZ	Q1		SI2369DS-T1-GE3
Diff1.2		AD8226ARZ	Q2		BC847A
Diff2.1		AD8226ARZ	Q3		BC857B
Diff2.2		AD8226ARZ	Q4		SI2369DS-T1-GE3
FB1	220	FB_0805	Q5		SI2369DS-T1-GE3
J1		SWD_HEADER	Q6		FDC637AN
J2		53048-0910	Q7		FDC637AN
R1	100k	RES_0603	R24	10k	RES_0603
R2	1k	RES_0603	R25	22k	RES_0603
R3	0R	RES_0603	R26	15k	RES_0603

R4	750k	RES_0603	R27	22k	RES_0603
R5	10k	RES_0603	R28	510R	RES_0603
R6	47k	RES_0603	R29	4k02	RES_0603
R7	0R51	RES_2010	R30	4k02	RES_0603
R8	8k87	RES_0603	R31	10k	RES_0603
R9	33R	RES_0603	R32	4k02	RES_0603
R10	100k	RES_0603	R33	4k02	RES_0603
R11	100k	RES_0603	R34	10k	RES_0603
R12	100k	RES_0603	R35	10k	RES_0603
R13	100k	RES_0603	R36	22k	RES_0603
R14	10k	RES_0603	R37	47k	RES_0603
R15	10k	RES_0603	R38	100k	RES_0603
R16	100k	RES_0603	R39	300R	RES_0603
R17	10k	RES_0603	R40	4k02	RES_0603
R18	100k	RES_0603	R41	4k02	RES_0603
R19	10R	RES_0603	R42	10k	RES_0603
R20	562k*	RES_0603	R43	4k02	RES_0603
R21	10k	RES_0603	R44	4k02	RES_0603
R22	69k8*	RES_0603	R45	10k	RES_0603
R23	8k87*	RES_0603	R46	10k	RES_0603
			R47	10k	RES_0603
			R48	100k	RES_0603
			R49	10k	RES_0603

***75V or 100V
rated component**

SiBJT	MMBT2369ALT1G
SiCBJT	SiC-transistor
U1	STM32L053C6
U2	LT1129CST-3.3
U3	LT3062
U4	LT1783CS5
U5	LT8570-1
U6	LMT85DCKT
U7	LMT85DCKT
U8	TCA4311ADR

Appendix C – SiC PCB test protocol

Circuit	Test description	MCU pin	Header/pin	Desired output	Result
MCU (U1)	Test to confirm that the MCU can be flash programmed	PA13 PA14	J1	Successful flashing	
MCU (U1)	I ² C communication – send command from OBC to MCU	PB6 PB7	J3 - pin 1,3	Working	
MCU (U1)	I ² C communication – receive data from MCU to OCB	PB6 PB7	J3 - pin 1,3	Working	
48V DC-DC converter	Test to confirm that the DC-DC boost converter can be switched off from the OBC	PB11	J4, pin 7 GND	The 48V DC-DC boost converter circuit delivers 0V at OFF and 48V at ON	
48V DC-DC converter	Test to confirm the DC / DC boost converter specifications	N/A	J4, pin 7 GND	The measured output voltage and current is 48V/15 mA	
10V linear converter	Test to confirm the 10V linear converter specifications	N/A	R4, pin 2 GND	The measured output voltage and current is 10V/10 mA	
10V linear converter	Test to confirm that the 10V linear converter can be switched off from the OBC.	PB10	R4, pin 2 GND	The 10V linear converter delivers 0V at OFF and 10V at ON	
Battery bus power switch	Test to confirm that the Battery bus power switch can be switched off from the OBC.	PB12	Q5, pin 3 GND	The measured voltages is OV at OFF and 12-14V at ON	
Battery bus power switch	Short circuit simulation using 1 Ω resistor.	N/A	Q5, pin 3 GND	Current draw < 1 A and output voltage < 1 V.	
SiC BJT/U6	Test to measure the SiC BJT temperature	PAo	N/A	SiC BJT temperature (°C)	
Si BJT/U7	Test to measure the Si BJT temperature	PA5	N/A	Si BJT temperature (°C)	

Si BJT	Test to measure the voltage across the base and emitter of the Si BJT @3.1V	PA1/Vbe1	N/A	The measured voltage is ~0.75V	
Si BJT	Test to measure the voltage across the base of the Si BJT @3.1V	PA2/Vrb1.1	N/A	The measured voltage is ~2.41V	
Si BJT	Test to measure the voltage across the collector of the Si BJT @3.1V	PA3/Vrc1	N/A	The measured voltage is ~1.72V	
Si BJT	Test to measure the voltage across the base and emitter of the Si BJT @2.1V	PA1/Vbe1	N/A	The measured voltage is ~0.74V	
Si BJT	Test to measure the voltage across the base of the Si BJT @2.1V	PA2/Vrb1.1	N/A	The measured voltage is ~1.92V	
Si BJT	Test to measure the voltage across the collector of the Si BJT @2.1V	PA3/Vrc1	N/A	The measured voltage is ~1.14V	
Si BJT	Test to measure the voltage across the base and emitter of the Si BJT @1.1V	PA1/Vbe1	N/A	The measured voltage is ~0.72	
Si BJT	Test to measure the voltage across the base of the Si BJT @1.1V	PA2/Vrb1.1	N/A	The measured voltage is ~0.90V	
Si BJT	Test to measure the voltage across the collector of the Si BJT @1.1V	PA3/Vrc1	N/A	The measured voltage is ~0.54V	
Si BJT	Test to measure the voltage across the base and emitter of the Si BJT @0.5V	PA1/Vbe1	N/A	The measured voltage is ~0.69V	
Si BJT	Test to measure the voltage across the base of the Si BJT @0.5V	PA2/Vrb1.1	N/A	The measured voltage is ~0.28V	
Si BJT	Test to measure the voltage across the collector of the Si BJT @0.5V	PA3/Vrc1	N/A	The measured voltage is ~0.17V	

SiC BJT	Test to measure the voltage across the base and emitter of the SiC BJT	PA6/Vbe2	N/A	The measured voltage is ~2.5-3.0V	
SiC BJT	Test to measure the voltage across the base of the SiC BJT	PA7/Vrb2.1	N/A	N/A	
SiC BJT	Test to measure the voltage across the collector of the SiC BJT	PBo/Vrc2	N/A	N/A	
Piezo transistor switch (Q1)	Test to confirm that the Piezo MCU voltage can be controlled by the OBC	PB13	J4, pin 5 GND	The measured voltage should be 0V at OFF and 5V at ON	
3.3V MCU voltage regulator (U2)	Test to measure that the 3.3V regulator output voltage is 3.3V.	N/A	U2, pin 3 GND	The measured output voltage is 3.3V	
N/A	Test to confirm the 3.3V voltage to Cubes	N/A	J2, pin 5 J3, pin 5	The measured output voltage is 3.3V	
N/A	Test to confirm the VBAT voltage to Cubes	N/A	J2, pin 7 J3, pin 7	The measured output voltage is equal to the input voltage (12-14V)	

Appendix D – Source code and design files

All source code is licensed under MIT license.

<https://opensource.org/licenses/MIT>

Test application 1 and 2 source code is available on GitHub:

https://github.com/drdevilo8o/SiC_Test?files=1

To run Test application 1, use Keil MDK

<http://www.keil.com/>

To run Test application 2, use IAR Embedded Workbench

<https://www.iar.com/iar-embedded-workbench/>

DipTrace files for PCB schematics and layout, as well as the Gerber-files used for ordering the final PCB are available on GitHub:

<https://github.com/drdevilo8o/SiC/tree/master/Diptrace>

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