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Lógica Digital

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- Objetivos
  - Estudar os circuitos digitais presentes nos computadores
- Conteúdos
  - Funções Lógicas
  - Portas Lógicas
  - Circuitos Integrados
  - Álgebra de Boole (Booleana)
  - Circuitos Digitais
  - Circuitos Básicos

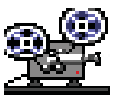
Sistema Digital

É uma combinação de dispositivos projetados para manipular informação lógica ou quantidades físicas que são representadas no formato digital, ou seja, as quantidades podem assumir apenas valores discretos.

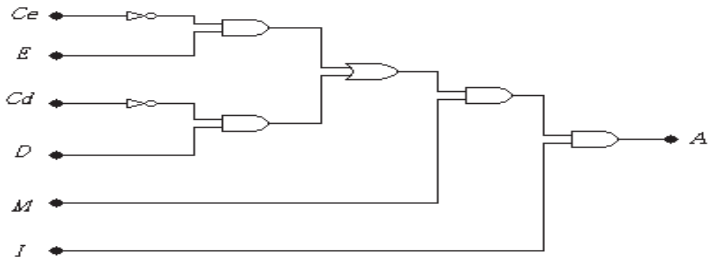
Tocci & Widmer
Sistemas Digitais

Portas Lógicas

Assista o vídeo sobre Portas Lógicas
(link: https://youtu.be/ckOBTc1XJik).



Circuito Combinacional



Portas Lógicas

Inversora

A	X = A`
0	1
1	0

AND

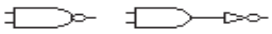
A	B	X = (A.B)
0	0	0
0	1	0
1	0	0
1	1	1

OR

A	B	X = (A+B)
0	0	0
0	1	1
1	0	1
1	1	1

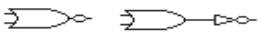
Portas Lógicas (cont.)

NAND



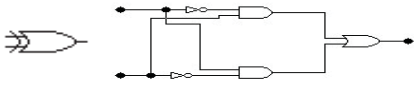
A	B	X = (A.B)`
0	0	1
0	1	1
1	0	1
1	1	0

NOR



A	B	X = (A+B`)`
0	0	1
0	1	0
1	0	0
1	1	0

XOR

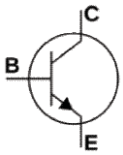


A	B	X = (A⊕ B)
0	0	0
0	1	1
1	0	1
1	1	0

Transistor (*Transference Resistor*)

Coletor

Base



Emissor

Base = 1 → circuito fechado

Base = 0 → circuito aberto

Transistor (em corte)

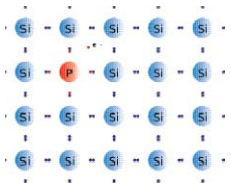
Semicondutores

Semicondutor

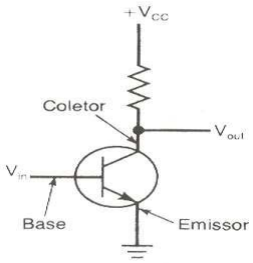
- Si
- Ge
- GaAs

Dopagem

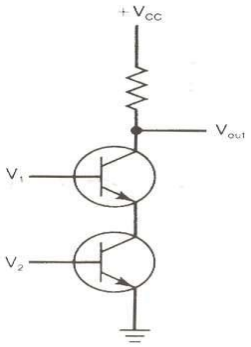
- Tipo N
- Tipo P



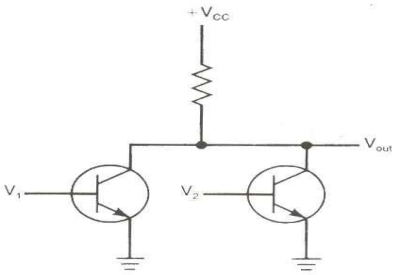
Circuito Elétrico das Portas Lógicas



Inversora

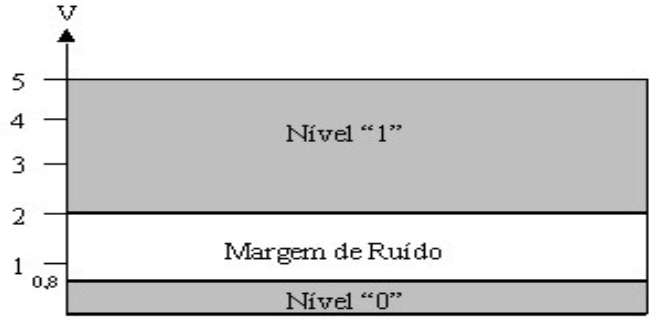


NAND

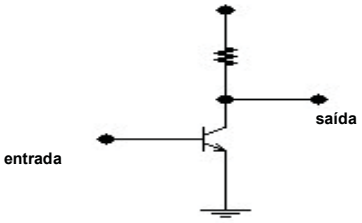


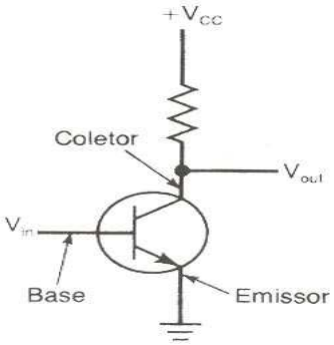
NOR

Níveis Lógicos

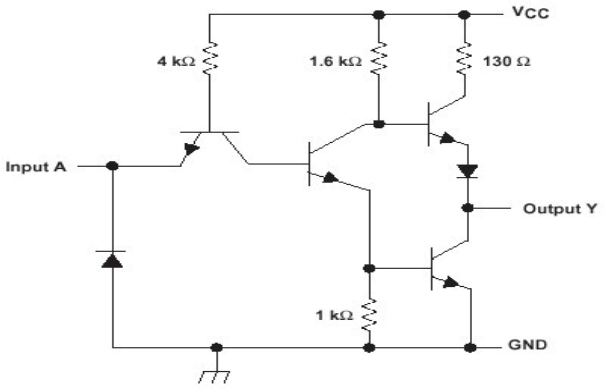


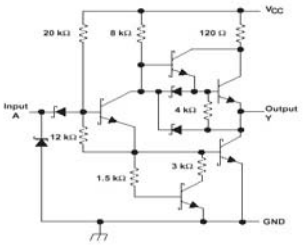
Porta Inversora

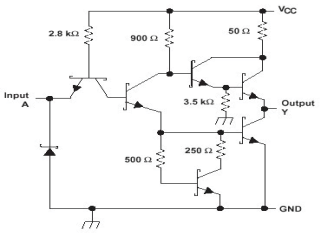




Porta Inversora (7404)





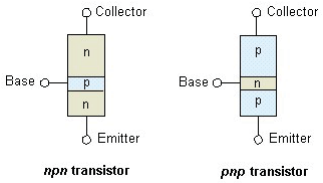


Tecnologia de Famílias Lógicas

- **Bipolar** → TTL (*Transistor-Transistor Logic*)
- **MOS** → CMOS (*Complementary Metal-Oxide Semiconductor*)

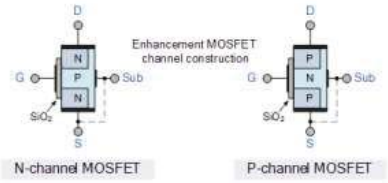
Tipos de Transistores

Bipolar



npn transistor *pnp* transistor

MOSFET



N-channel MOSFET P-channel MOSFET

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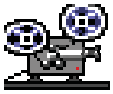
Circuitos Integrados

Assista o vídeo sobre Circuitos Integrados
(link: https://youtu.be/ti9VVBHljWU).



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SN5486, SN54LS86A, SN54S86
SN7486, SN74LS86A, SN74S86
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

SDLS124 – DECEMBER 1972 – REVISED MARCH 1988

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S86 . . . . . −55°C to 125°C
SN74S86 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54S86			SN74S86			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−1	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54S86			SN74S86			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA			0.5			0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V			50			50	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V			−2			−2	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−40		−100	−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2		50	75		50	75	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2: I_{CC} is measured with the inputs grounded and the outputs open.

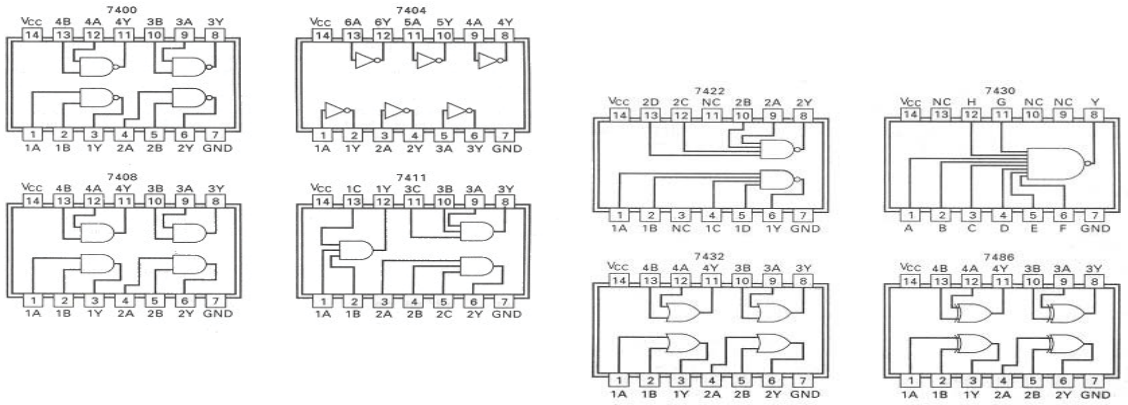
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	Other input low		7	10.5	ns
t_{PHL}					6.5	10	
t_{PLH}	A or B	Y	Other input high	C_L = 15 pF, R_L = 280 Ω, See Note 3	7	10.5	ns
t_{PHL}					6.5	10	

¶t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS

Circuito Integrado (*Layout*)



Circuitos Integrados (CI)

- SSI (*Small Scale Integration*): até 10 portas
- MSI (*Medium Scale Integration*): 10 a 100 portas
- LSI (*Large Scale Integration*): 100 a 100.000 portas
- VLSI (*Very Large Scale Integration*): > 100.000 portas

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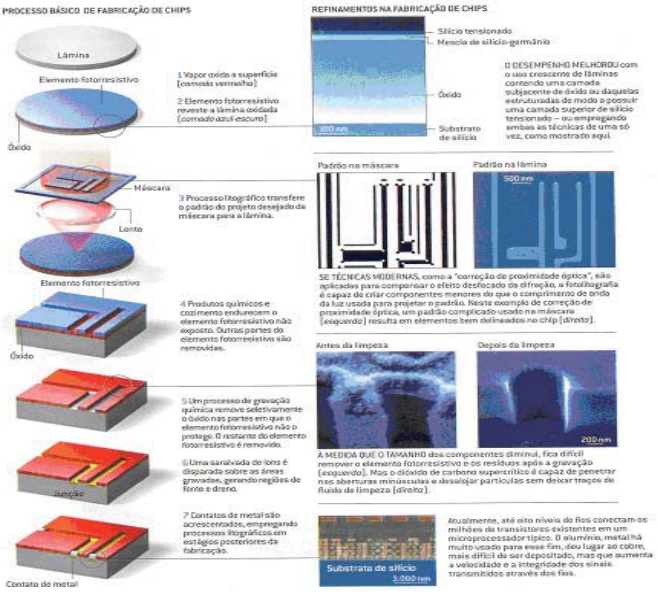
O VELHO E O NOVO NA FABRICAÇÃO DE SEMICONDUTORES

UMA LÂMINA CIRCULAR de silício, do tamanho aproximado de um prato comum, é o ponto de partida para o processo de fabricação de chips em etapas, que esculpe os transistores e suas interconexões. Algumas das manipulações apresentadas abaixo são repetidas diversas vezes durante a produção para construir estruturas complexas, camada por camada.



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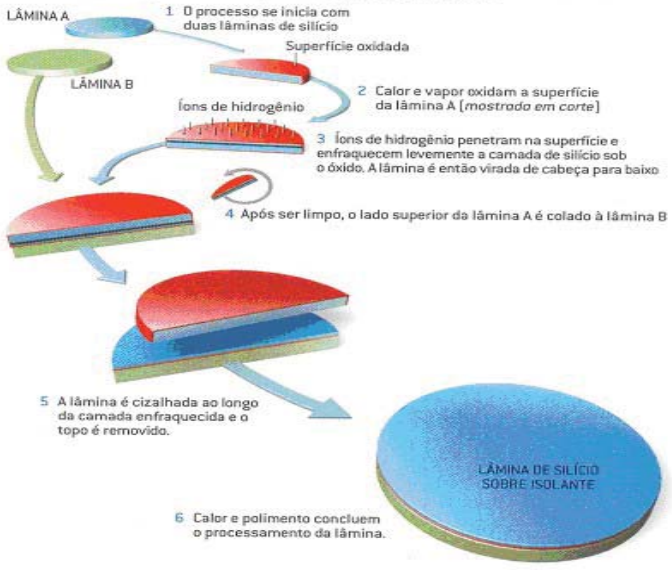
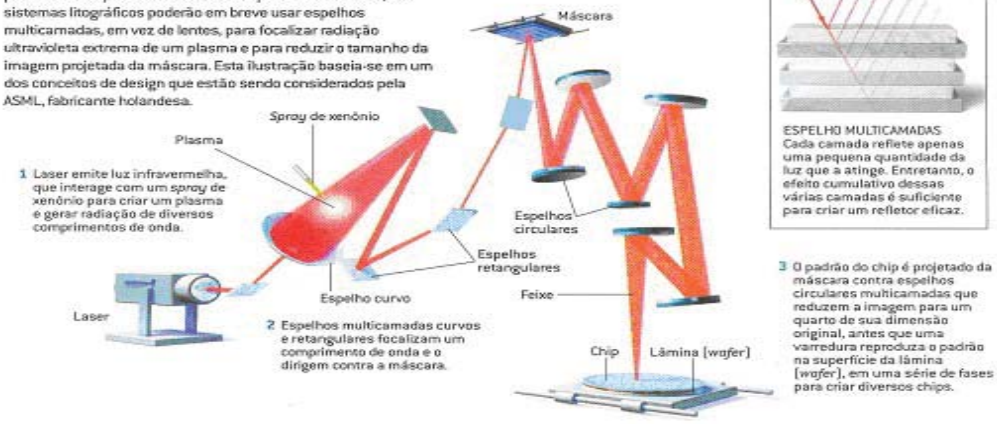
FATIANDO UM NANOCHIP

A TECNOLOGIA DE SILÍCIO SOBRE ISOLANTE, que ajudou a melhorar consideravelmente o desempenho dos chips, ficou mais barata e mais fácil de ser adotada graças a uma técnica chamada Smart-Cut, desenvolvida pela Soitec, empresa francesa.

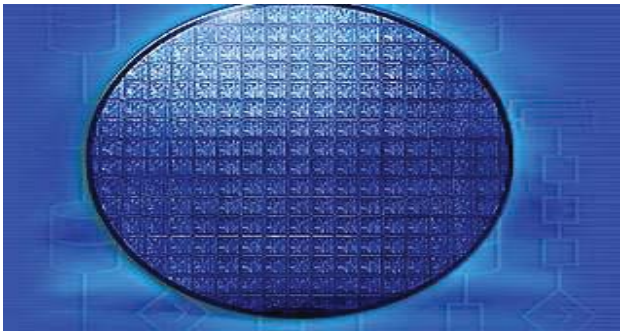


LITOGRAFIA ULTRAVIOLETA EXTREMA

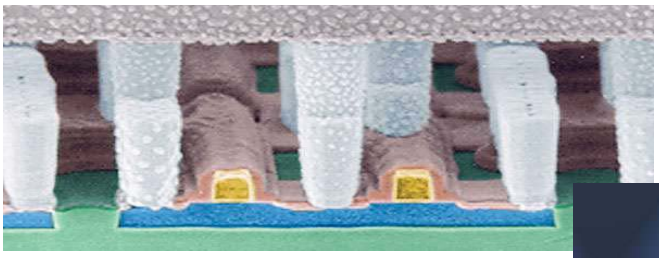
LENTES que são usadas em sistemas litográficos convencionais absorveriam a luz ultravioleta extrema necessária para formar o padrão de componentes menores do que 50 nm. Por isso, os sistemas litográficos poderão em breve usar espelhos multicamadas, em vez de lentes, para focalizar radiação ultravioleta extrema de um plasma e para reduzir o tamanho da imagem projetada da máscara. Esta ilustração baseia-se em um dos conceitos de design que estão sendo considerados pela ASML, fabricante holandesa.

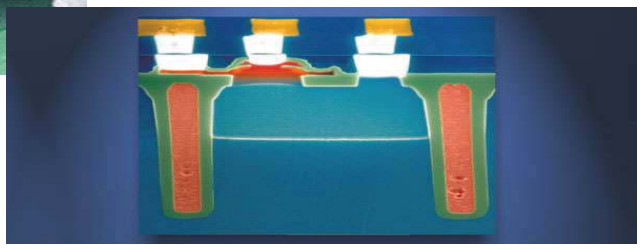


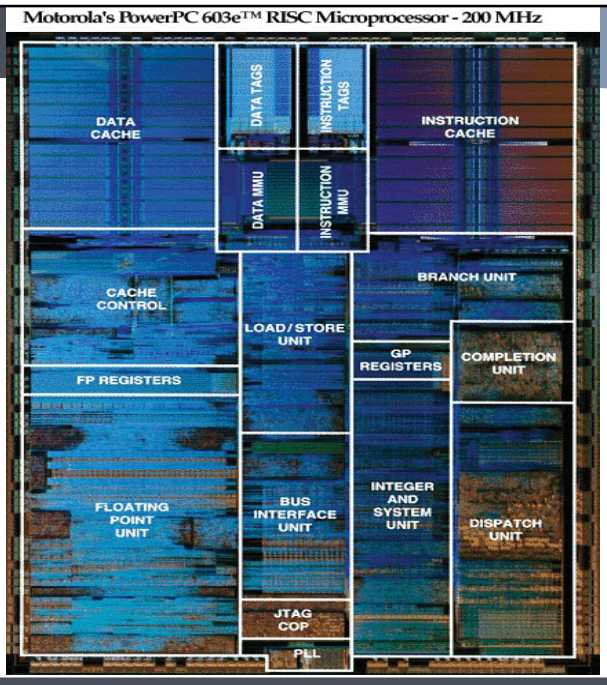
Wafer



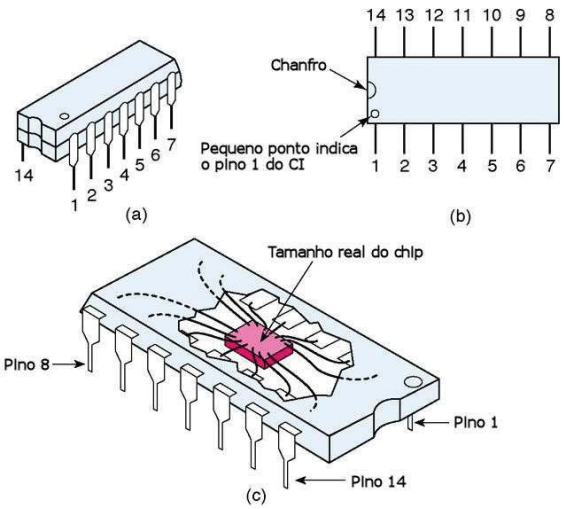
Chip em Corte

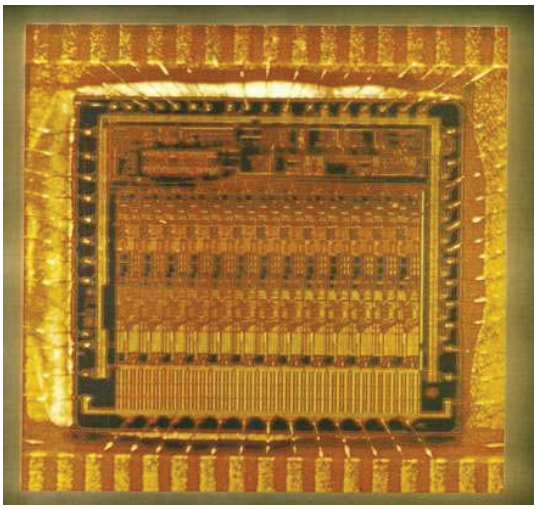






Encapsulamento





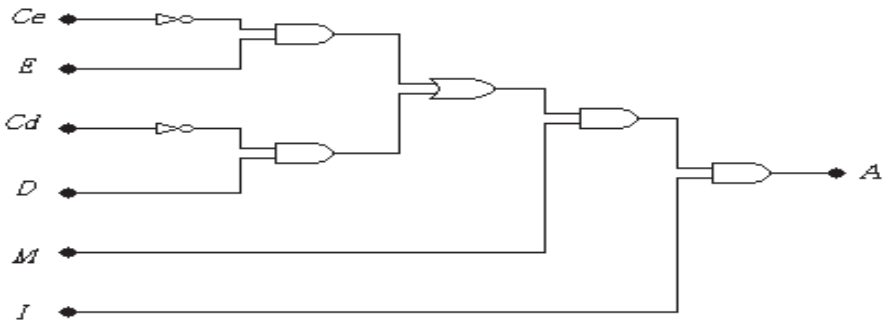
Funções Lógicas

Sistema de alarme de cinto de segurança:

- •Sensores para gerar entradas (sensor=1) se estiver ativado.
- •Existe um sensor que indica se a marcha (M) está engatada
- •É posicionado um sensor sob cada banco frontal (D e E)que será ativado quando alguém ocupa este banco
- •Outro tipo de sensor é instalado em cada banco para determinar se o cinto (Cd e Ce) está fechado
- •Deve-se acionar a buzina quando a ignição (I) é ligada e a marcha está engatada e contanto que qualquer banco frontal esteja ocupado e o cinto correspondente não esteja fechado.

$$A = I.M.\left(\left(D.\overline{Cd}\right)+\left(E.\overline{Ce}\right)\right)$$

Função Lógica
Circuito



Circuito Eletrônico (como desenhar)

Assista o vídeo sobre Álgebra Booleana
(link: https://youtu.be/N0QtxqZid48).

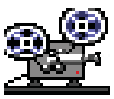
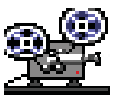


Tabela Verdade

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

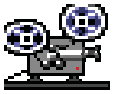
Equação Lógica

Assista o vídeo sobre Equação Lógica
(link: https://youtu.be/Y-r-JLRo6zQ).



Álgebra Booleana

Assista o vídeo sobre Álgebra Booleana (link: https://youtu.be/gLMgEG1VuvU).



Álgebra Booleana

Propriedade	Equação	
Idempotência ou Equipotência	$x + x = x$ $x.x = x$	(1) (1`)
Identidade	$x + 1 = 1$ $x.0 = 0$ $x + 0 = x$ $x.1 = x$	(2) (2`) (3) (3`)
Comutatividade	$x + y = y + x$ $x.y = y.x$	(4) (4`)
Associatividade	$(x + y) + z = x + (y + z)$ $(x.y).z = x.(y.z)$	(5) (5`)
Complementação	$x + \overline{x} = 1$ $x.\overline{x} = 0$	(6) (6`)
Distributividade	$x.(y + z) = (x.y) + (x.z)$ $x + (y.z) = (x + y).(x + z)$	(7) (7`)
Teoremas de De Morgan	$\overline{(x + y)} = \overline{x}.\overline{y}$ $\overline{(x.y)} = \overline{x} + \overline{y}$	(8) (8`)

Simplificação Algébrica

$$
\begin{aligned}
f(x, y) &= x + xy \\
&= x.1 + xy && (3`) \\
&= x(1 + y) && (7) \\
&= x.1 && (2) \\
&= x && (3`)
\end{aligned}
$$

Mapa de Karnaugh

A	B	C	S
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

Extraia somente as variáveis que não se alteram

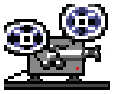
C \ AB	00	01	11	10
0	0	0	0	1
1	1	1	0	1

$\sum m(1,2,4,6)$
=A'B'C + A'BC + AB'C' + AB'C'
=A'C + AC + AB' + AB' → a + a = a
=A'C + AB'

S = A'C + AB'

Mapa de Karnaugh

Assista o vídeo sobre Mapa de Karnaugh
(link: https://youtu.be/y9QrmQ6aWW4).

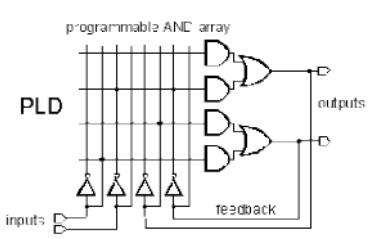


Método Quine-McCluskey

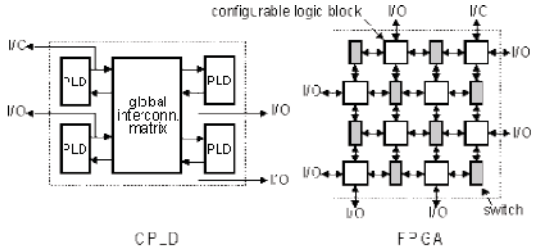
O **Algoritmo de Quine–McCluskey** (ou **método dos implicantes primos**) é um método utilizado para minimização de funções booleanas desenvolvido por W.V. Quine e Edward J. McCluskey em 1956.

Dispositivos Reconfiguráveis

PLDs (*Programmable Logic Device*)
CPLDs (*Complex* PLD)
FPGAs (*Field-Programmable Gate Array*)

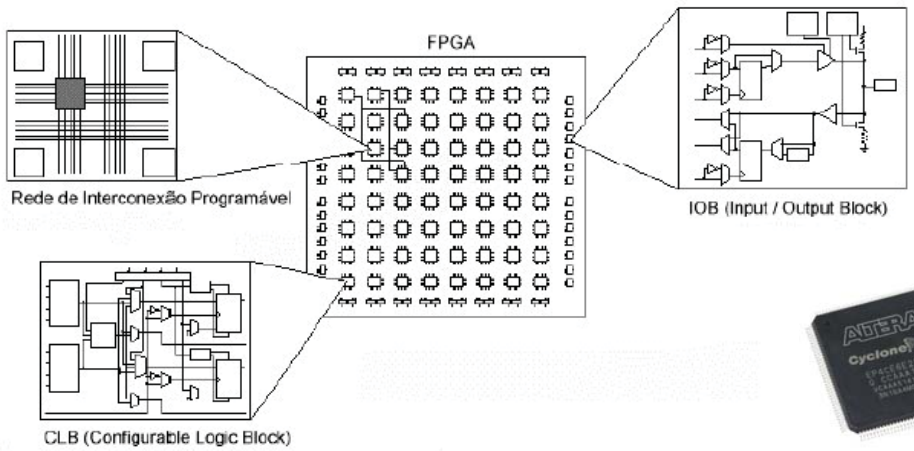


PLD Architecture



CPLD and FPGA Architectures

Arquitetura Interna



VHDL – VHSIC *Hardware Description Language*

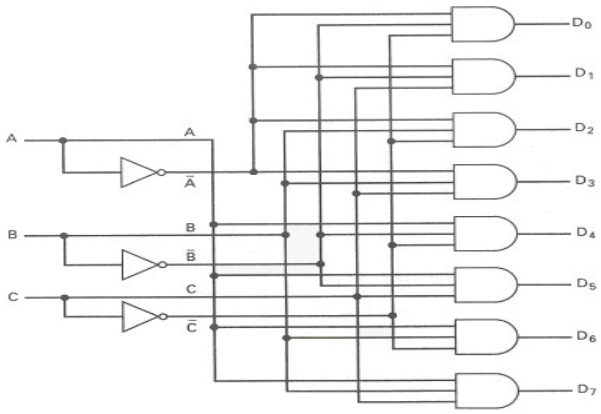
```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity signed_adder is
  port
  (
    aclr : in  std_logic;
    clk  : in  std_logic;
    a    : in  std_logic_vector;
    b    : in  std_logic_vector;
    q    : out std_logic_vector
  );
end signed_adder;

architecture signed_adder_arch of signed_adder is
  signal q_s : signed(a'high+1 downto 0); -- extra bit wide

begin -- architecture
  assert(a'length >= b'length)
    report "Port A must be the longer vector if different sizes!"
    severity failure;
  q <= std_logic_vector(q_s);

  adding_proc:
  process (aclr, clk)
    begin
      if (aclr = '1') then
        q_s <= (others => '0');
      elsif rising_edge(clk) then
        q_s <= ('0'&signed(a)) + ('0'&signed(b));
      end if; -- clk'd
    end process;

end signed_adder_arch;
```

VHSIC – ***Very High Speed Integrated Circuit***

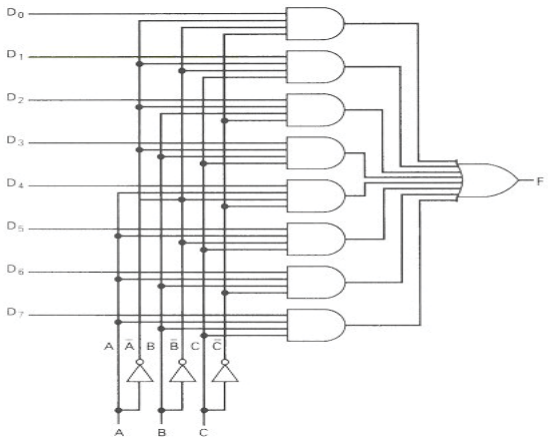
Professor
Edson Pedro FERLIN
professorferlin.blogspot.com

Exemplos de Circuitos Básicos

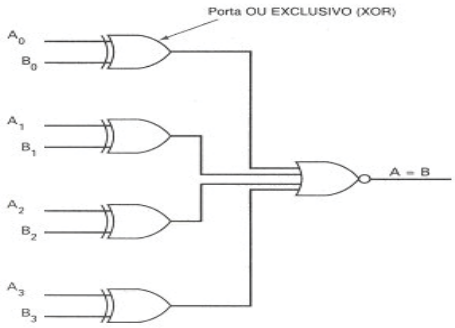
Decodificador



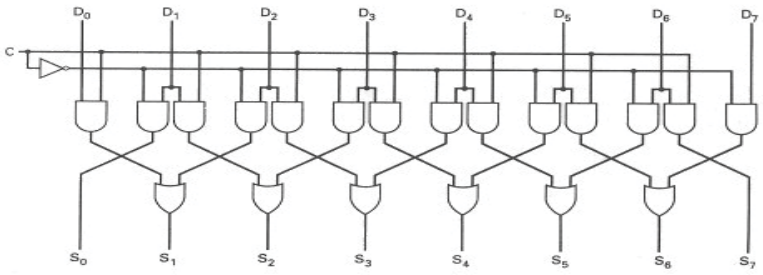
Multiplexador



Comparador



Deslocador

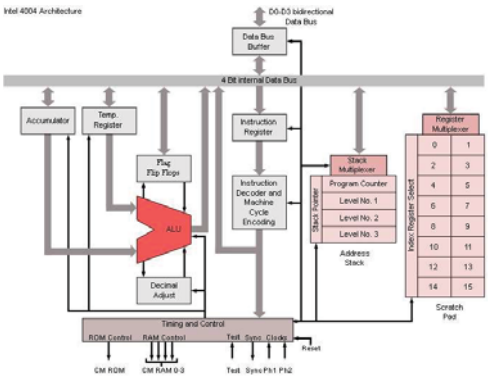


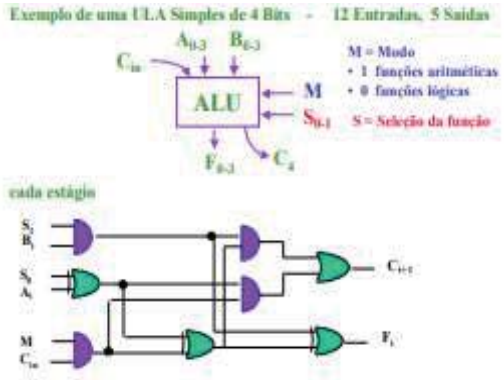
Aritmética Binária

	Soma	Resto
0 + 0	0	0
0 + 1	1	0
1 + 0	1	0
1 + 1	0	1

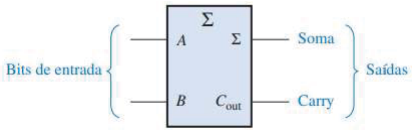
- Adição
- Subtração
- Multiplicação
- Divisão

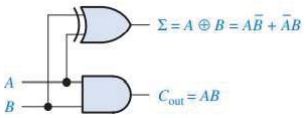
ULAs - CPUs





Meio Somador (*Half Adder*)

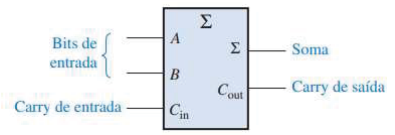


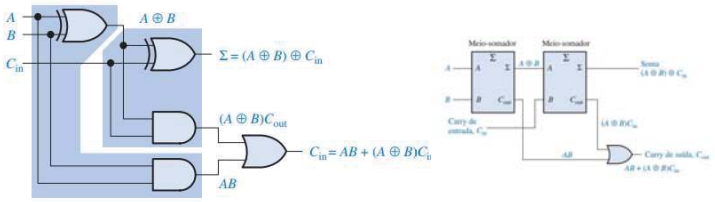


A	B	C_{out}	Σ
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Σ = soma
C_{out} = carry de saída
A e B = variáveis de entrada (operandos)

Somador Completo (*Full Adder*)

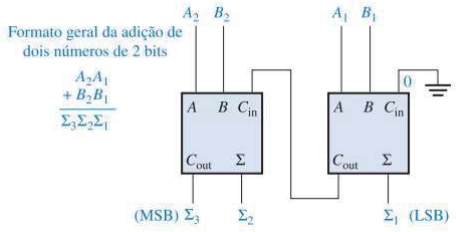




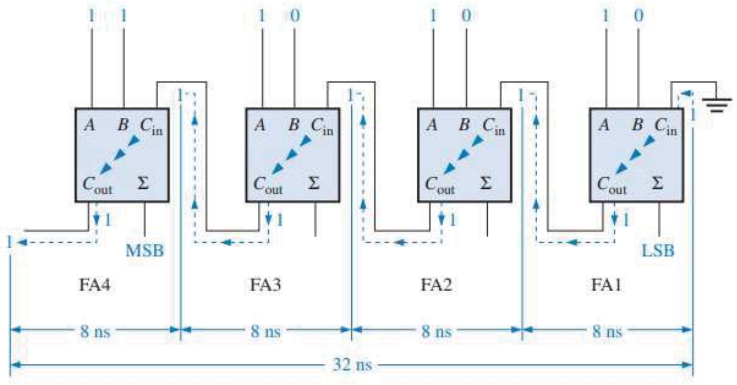
A	B	C_{in}	C_{out}	Σ
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

C_{in} = carry de entrada, algumas vezes indicado como *CI*
C_{out} = carry de saída, algumas vezes indicado como *CO*
Σ = soma
A e B = variáveis de entrada (operandos)

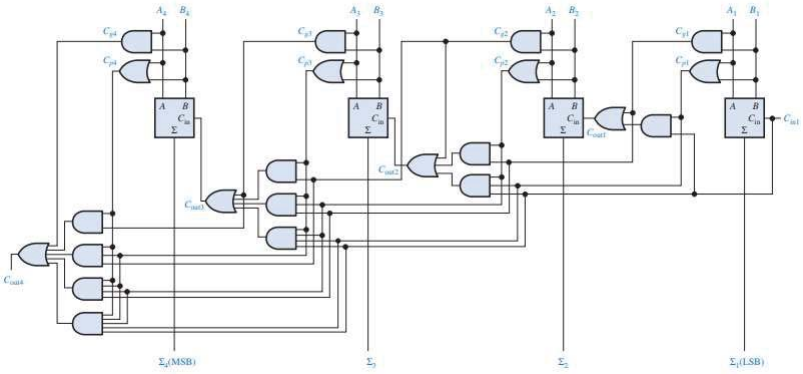
Somadores Binários Paralelos



Somador com *Carry* ondulante



Somador com *Carry* antecipado



Somador-completo 1:

$$C_{out1} = G_{p1} + C_{p1}C_{in1}$$

Somador-completo 2:

$$C_{in2} = C_{out1}$$
$$C_{out2} = G_{p2} + C_{p2}C_{in2} = G_{p2} + C_{p2}C_{out1} = G_{p2} + C_{p2}(G_{p1} + C_{p1}C_{in1})$$
$$= G_{p2} + C_{p2}G_{p1} + C_{p2}C_{p1}C_{in1}$$

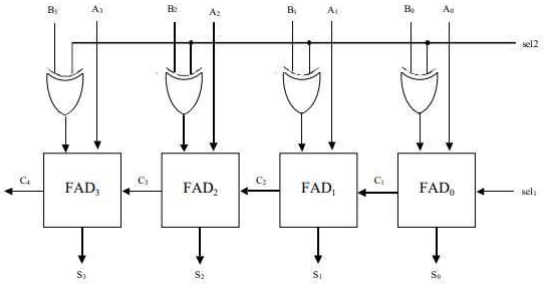
Somador-completo 3:

$$C_{in3} = C_{out2}$$
$$C_{out3} = G_{p3} + C_{p3}C_{in3} = G_{p3} + C_{p3}C_{out2} = G_{p3} + C_{p3}(G_{p2} + C_{p2}G_{p1} + C_{p2}C_{p1}C_{in1})$$
$$= G_{p3} + C_{p3}G_{p2} + C_{p3}C_{p2}G_{p1} + C_{p3}C_{p2}C_{p1}C_{in1}$$

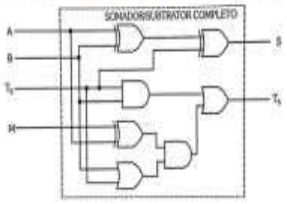
Somador-completo 4:

$$C_{in4} = C_{out3}$$
$$C_{out4} = G_{p4} + C_{p4}C_{in4} = G_{p4} + C_{p4}C_{out3}$$
$$= G_{p4} + C_{p4}(G_{p3} + C_{p3}G_{p2} + C_{p3}C_{p2}G_{p1} + C_{p3}C_{p2}C_{p1}C_{in1})$$
$$= G_{p4} + C_{p4}G_{p3} + C_{p4}C_{p3}G_{p2} + C_{p4}C_{p3}C_{p2}G_{p1} + C_{p4}C_{p3}C_{p2}C_{p1}C_{in1}$$

Somador/Subtrator completo

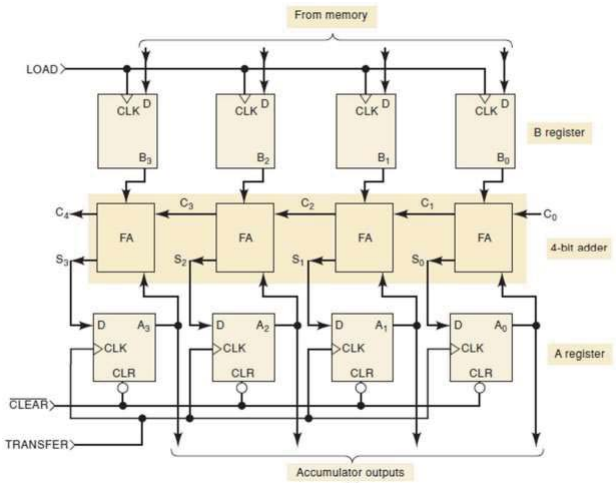


Circuito do Somador/Subtrator Completo:

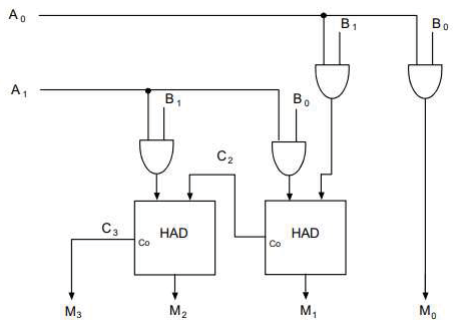


sel_2	sel_1	operação	descrição
0	0	S = A + B + 0	adiciona A e B (S = A + B)
0	1	S = A + B + 1	adiciona A e B incrementado (S = A + B + 1)
1	0	$S = A + \overline{B} + 0$	subtrai B decrementado de A (S = A – B - 1)
1	1	$S = A + \overline{B} + 1$	subtrai B de A (S = A - B)

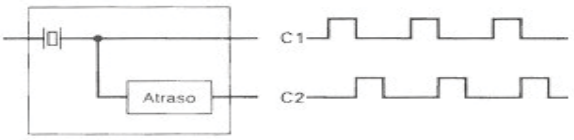
Somador Completo com Registradores



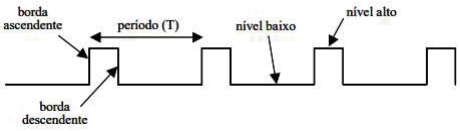
Multiplicador Binário

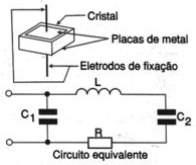


Clock

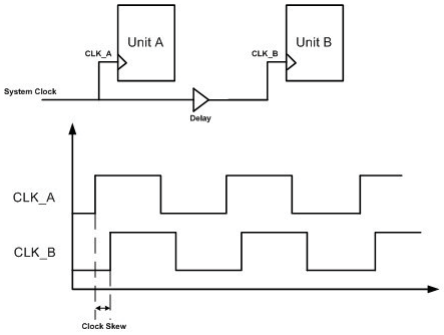


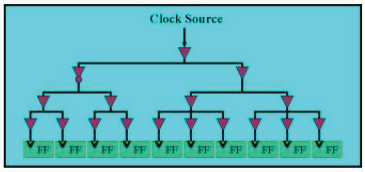
$$f = \frac{1}{T}$$





Distribuição do *Clock*



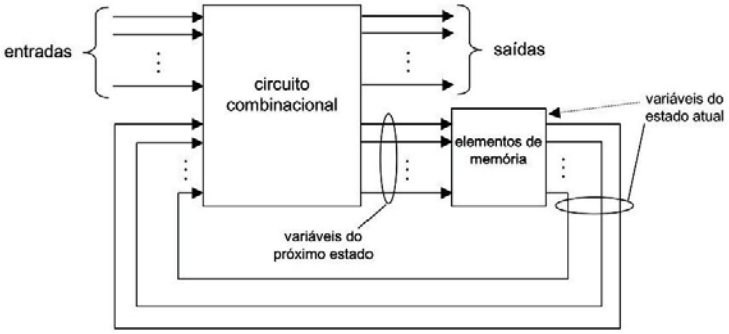


Circuitos Sequenciais

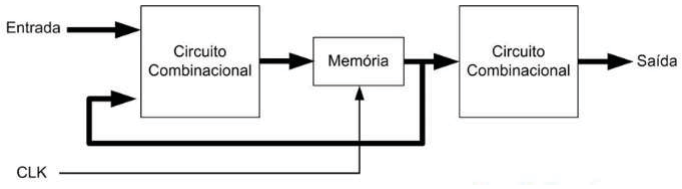
Máquina de Estados Finitos
(FSM – Finite State Machine)

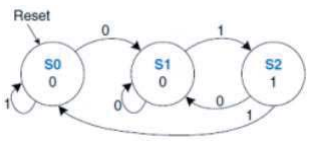
•Mealy → Transições (estados + entradas)

•Moore → Estados

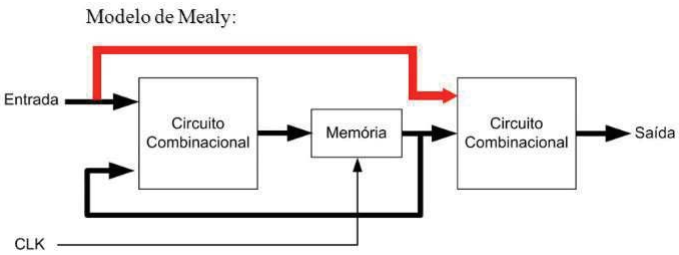


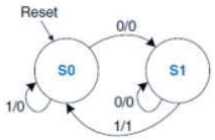
Máquina de Moore



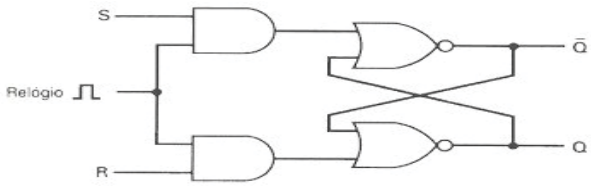


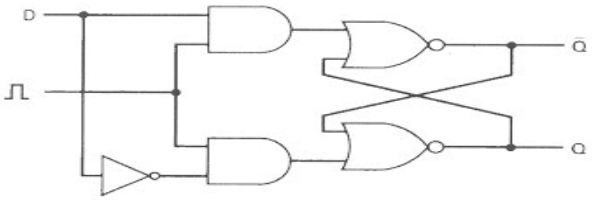
Máquina de Mealy



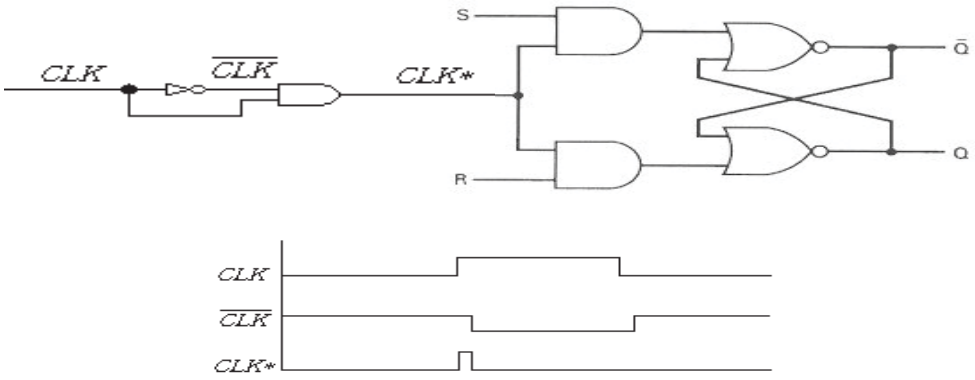


Latch

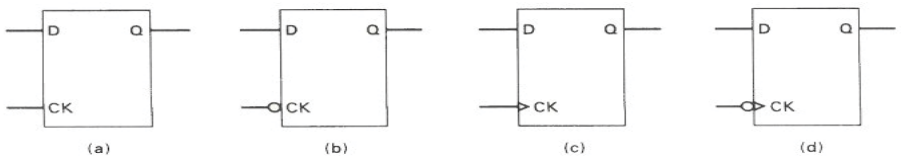




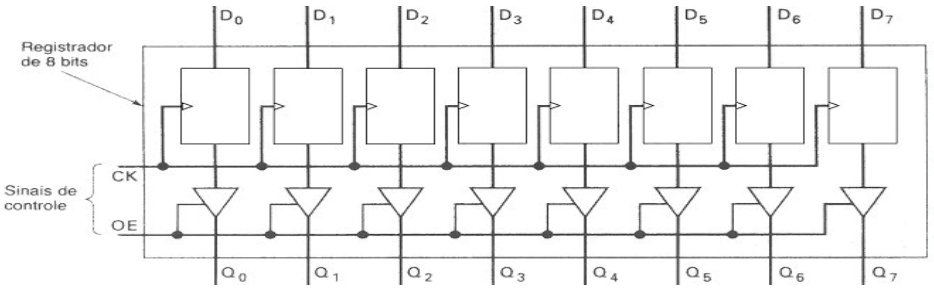
Flip - Flop



Flip – Flop ou Latch



Registrador



Atividade

- Resolver os exercícios.