Proceedings of the 2nd International IEEE EMBS
Conference on Neural Engineering
Arlington, Virginia · March 16 - 19, 2005

A Conductance-Based Silicon Neuron with Dynamically Tunable Model Parameters

S. Saïghi, J. Tomas, Y. Bornat, S. Renaud
IXL Laboratory, UMR 5818 CNRS / ENSEIRB / University Bordeaux 1
351, cours de la Libération
33405 Talence Cedex, France

***Abstract* — This paper presents an analog neuromimetic ASIC. It integrates Hodgkin-Huxley (HH) model types, computed in real-time and in analog continuous mode. We developed a library of sub-circuits calculating the elementary mathematical functions encountered in the HH models. Those sub-circuits are organized to form the model set of equations, in which all numerical parameters are dynamically tunable via a mixed analog-digital interface. Neural activity examples are presented to validate the library elements and illustrate the diversity of models simulated by a single ASIC.**

***Keywords* — aVLSI circuits – Neuromimetic devices – Hodgkin-Huxley – Silicon neuron.**

I. Introduction

Since the first silicon neuron from M. Mahowald and R. Douglas [1], research groups have developed and used analog neuromimetic integrated circuits to address fundamental neurosciences questions.

Such devices emulate and therefore allow a detailed analysis of activity patterns of single neurons or small networks. When based on biophysical models, the circuits provide a precise temporal replica of the neurons electrical activity.

In this paper, we consider devices where the models are computed in analog mode and in real-time. The variations of the signal are then continuously computed, while their dynamics strictly fits the biological neurons ones. The applications of such circuits have been notably detailed and discussed in [2], [3] and [4].

Two approaches can be identified when designing those custom circuits: in the first one, an integrated circuit (IC) is fabricated to fit a specific model card (set of parameters), and will be used to study a single class of neurons. In that case, more silicon neurons can be integrated on a single chip, and applications generally address network and synaptic modulation questions [5]. For the second approach, the IC receives inputs to set the chosen model card. It is then used as a simulation tool where the user can access and tune the models parameters, building its proprietary neuron and network adapted to its application.

The IC presented here has been designed according to the second approach. It is specified to accept a wide range of model parameters, which correspond to realistic neurons diversity. We will show that it can precisely emulate different types of neurons, characterized by specific activity patterns. When describing the design process, we will also explain how, by choosing a modular structure for the circuit, we built a library of electronic sub-cirucits.

II. The Class of Model

We chose to work with a conductance-based class of models, derived from the Hodgkin-Huxley model [6]. The numerical parameters of such models directly represent biophysical characteristics of the modeled neuron, and different complexity levels can be considered by adding conductances or internal dependences (see examples in paragraph V). Those models are close to biological reality, which helps for the design of experiments using the silicon neurons. Reciprocally, we can rely for the IC tests on a rich collection of well-experienced models in the neuroscience community.

A. The Hodgkin-Huxley formalism

The electrical activity of a neuron is the consequence of the ionic species diffusion through its membrane. This activity is characterized by a membrane potential, which is the voltage difference between the outside and the inside of the cell. Ions flow through the cell membrane through ion-specific channels, generating specific ionic currents. A reverse (resting) potential is associated to each ionic species, according to the difference between the intracellular and extracellular concentrations. The fraction of opened ion-specific channels determines the global conductance of the membrane for that ion. This fraction results from the interaction between time and voltage dependent activation and inactivation processes.

The Hodgkin-Huxley formalism provides a set of equations and an electrical equivalent circuit (Fig. 1) that describe these conductance phenomena.

The current flowing across the membrane is integrated on the membrane capacitance, following the equation (1).

$$C_{mem}\frac{dV_{mem}}{dt} = -\sum_i I_{ion} + I_S \qquad (1)$$

where V_{mem} is the membrane potential, C_{mem} the membrane capacitance and I_s an eventual stimulation or synaptic current.

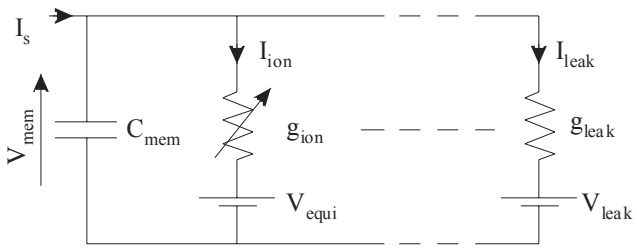

Fig. 1: Neuron electrical equivalent circuit

I_{ion} is the current passing through one channel type, and is given by (2), in which g_{max} is the maximal conductance value, m and h respectively represent activation and inactivation terms, which are the dynamic functions describing the permeability of membrane channels to this ion. V_{equi} is the ion-specific reverse potential and p, q are integers.

$$I_{ion} = g_{max} m^p h^q (V_{mem} - V_{equi}) \quad (2)$$

According to kinetic function (3), m converges to its associated steady-state value m_∞, which is a sigmoïdal function of V_{mem} (4). The time constant for the convergence is τ_m. In (4) V_{offset} is the activation sigmoïd offset and V_{slope} the activation sigmoïd slope. Inactivation h follows identical equations except that the sign of $(V_{mem} - V_{offset})$ is reversed.

$$\tau_m \frac{dm}{dt} = m_\infty - m \quad (3)$$

$$m_\infty = \frac{1}{1 + \exp\left(\frac{-(V_{mem} - V_{offset})}{V_{slope}}\right)} \quad (4)$$

The maximal conductance may also depend on an internal variable, such as an ionic concentration. Internal dependence functions were integrated in the circuit but will not be further presented in this paper.

B. Library of mathematical functions

The repetition of mathematical operations within each ionic channel is an advantage for systematic developments of neuromimetic circuits if the circuitry allows each mathematical function to receive tunable parameters.

The specifications of the mathematical functions were set in collaboration with a neurophysiology research laboratory that has been exploiting our silicon neurons since ten years. The constraints that result from those specifications for the integrated circuits design are strong ones if we compare for example the range of the V_{equi} parameters [-150mV; 150mV] with the minimal and maximum values of the V_{mem} variable [-120mV; 50mV].

C. Ionic current generators implemented

We retained for our design five channel types: leakage, sodium, potassium, calcium and calcium-dependent potassium. Each channel is built following the modular principle described previously and ionic current generators can then be represented as block diagrams (Fig. 2).

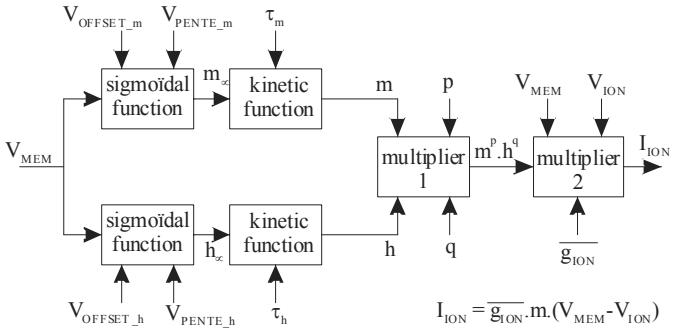

Fig. 2: Block diagram of the ionic current generator.

III. CHIP DESIGN

The principle of developing a library of mathematical functions for custom analog design was already validated in a previous IC. However, this circuit emulated a specific type of neuron with fixed set of parameters and was dedicated to the study of plasticity in pyramidal cells networks [7].

We wish now to develop a library of tunable functions. Those functions are assembled in an analog computation core built as a set of ionic current generators. Digital functions are added to manage the core topology as well as analog memory cells to store the parameters.

A. Analog computation core

5 ionic current generators are integrated in the core (Na, K, Ca, K(Ca) and Leak), 8 synapses [8] for network applications and one stimulation input (Fig. 3).

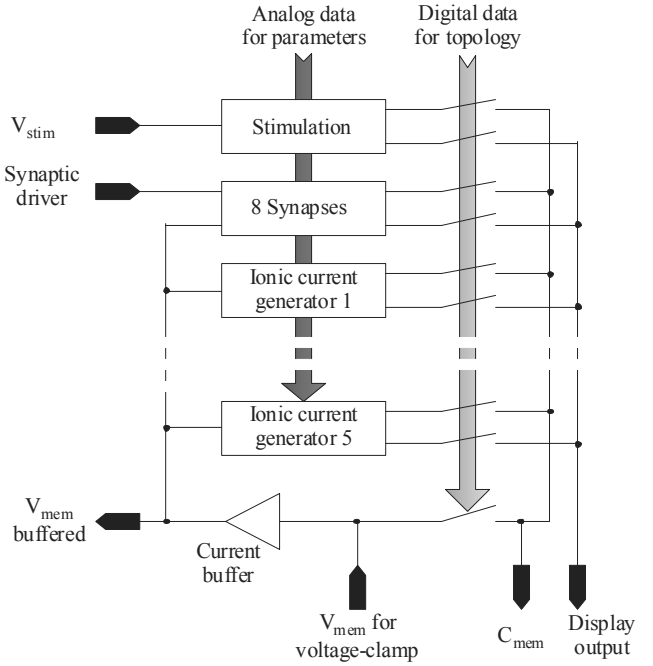

Fig. 3: Analog computation core

All functions have two outputs: the first one can be connected to the external capacitor C_{mem} that represents the membrane capacitor; the second one is a display output used

to observe each ionic or synaptic current. A current buffer authorizes through a third output the display of electrical membrane activity with a scope probe. The switch between the current buffer and the external capacitor can be closed for neuronal electrical activity simulation or open for voltage-clamp experiments to identify individual channels parameters.

B. Core Topology and storage parameters

To minimize the chip area, only two analog computation cores were implanted in the IC first prototype (Fig. 4).

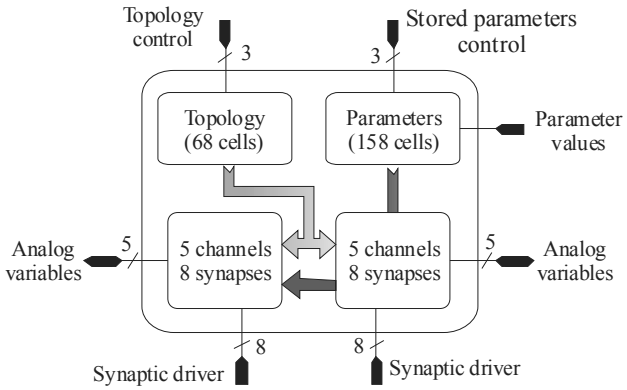

Fig. 4: Chip block diagram

To build the neuron or network model, the user has to define which ionic or synaptic current generators are connected via the switches to the external capacitor C_{mem}; each switch in Fig. 4 is controlled by a digital signal, stored in the topology memory. The two cores require a topology memory size of 68 bits. To program the topology memory, we use a 3 wires serial bus (Clock, Reset and Data).

Dynamic analog memories, based on integrated capacitors, were designed to store the 158 analog model parameters that are necessary for the 2 analog cores. The memory cells array needs only one external ADC, which sequentially refreshes the analog parameter values. This technique allows the dynamic modification of one or more parameters. One modification necessitates three refreshing cycles (< 5 ms). To program the parameter memories we use another 3 wires serial bus (Clock, Reset and Data) and an analog bus (Parameters values). Both analog and digital buses are controlled via a custom PCI interface (driver and board). The user sets the topology and the parameters values using a dedicated set of instructions in C language.

C. Simulation running

The simulation starts with a set of initialization parameters. Topology is first programmed then the values of the model card parameters are sent to the analog memory cells. The initialization process takes less than 10 ms. The system is then ready to simulate continuously and in real-time the neuron electrical activity. The largest advantage of that device is the dynamical reprogramming of one or more parameter values while the simulation is still running.

IV. Silicon Integration

The prototype ASIC was designed in full-custom mode with a BiCMOS SiGe 0.35µm technology process from *austria**micro**systems* (AMS) under Cadence environment. Figure 5 is a microphotograph of the ASIC called "Pamina". The ionic current generators have been designed in current mode [9], which means that the internal variables are physically represented by currents. Topology and analog memory cells can also be identified on the figure.

"Pamina" contains around 19000 MOS transistors, 2000 bipolar ones and 1200 passive elements; its area is 4170 x 3480 μm^2. Ionic and synaptic current generators and analog memory cells are designed in full-custom mode whereas digital cells are from the *austria**micro**systems's* library. 71% of the 22 000 components are resulting from a full-custom design procedure. Optimized analog layout procedures, like common-centroïd and dummy devices, have been used to implement critical structures and harden it to technological process mismatch and variations [10].

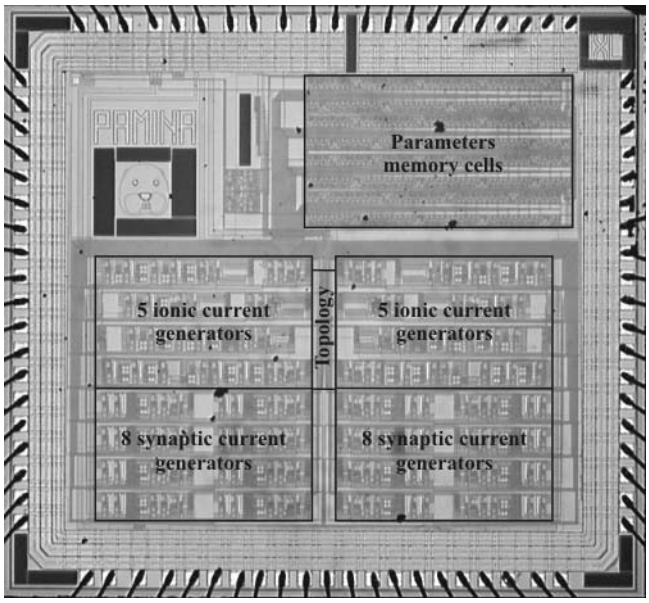

Fig. 5: Microphotograph of the chip "Pamina"

V. Results

A. Calcium plateau

The first result presented here is a 4 conductance neuron electrical activity (Sodium, Potassium, Leak and Calcium) [6]. All currents expressions follow equation (2).

The 4 scope screen captures on Fig. 6 represent the neuron electrical activity with an increasing conductance value for the calcium channel (g_{Ca_max}). This maximum conductance value increases from A) to D). On each screen, from top to bottom, the stimulation current, the calcium current and the neuron electrical activity are plotted. Before the stimulation, the artificial neuron is silent. When the stimulation current is applied, the neuron starts oscillations and the calcium current

increases, which rises of the oscillations frequency. When the stimulation pulse ends, we can observe several patterns depending on the maximal conductance value of calcium channel. In A) g_{Ca_max} is the smallest; the neuron electrical activity stops at the end of the stimulation. In B), C) and D) the oscillations are maintained during a period increasing with g_{Ca_max}.

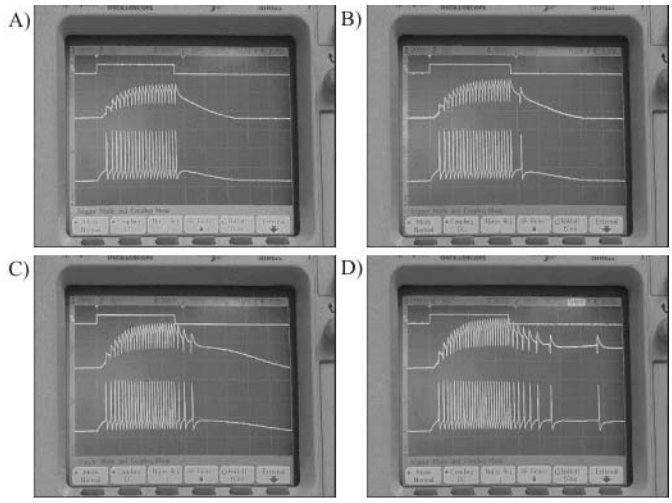

Fig. 6: The 4 conductances neuron electrical activity evolves when the g_{Ca_max} parameter is modified.

B. Inhibitory and excitatory neurons

We then tested the models currently used to represent the two main neuronal types present in the neocortex, so called "regular spiking" and "fast spiking" neurons [11]. The model defined for the inhibitory fast spiking neuron is a 3 conductances one: sodium, potassium and leak. The model of the excitatory regular spiking includes 4 conductances: sodium, potassium, leak and modulator. The modulator current generates the adaptation phenomenon present in the discharge pattern; its represents the calcium and potassium calcium dependent currents effect. We use the same chip as in paragraph V – A and simply changed the model card.

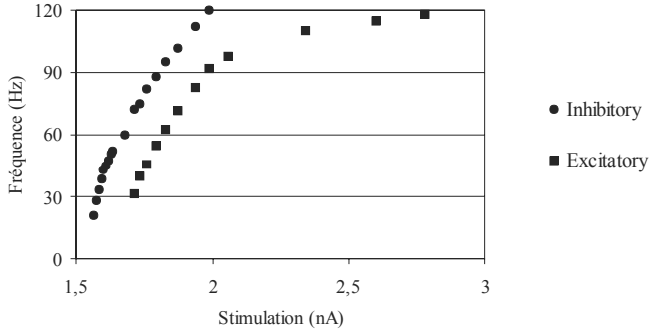

Fig. 7: f(I) responses for a 3 conductances inhibitory neuron and a 4 conductances excitatory neuron.

Figure 7 displays the oscillation frequency vs. stimulation current: f(I) curves. Those characteristics present a good overview of the neurons activity range. The results presented here are in the range of the biological neurons ones [11] and the hardware models can be used to study the plasticity of small neural networks of pyramidal cells.

VI. Conclusion

We presented in this paper an analog neuromimetic integrated circuit. The device acts as a simulator where the model parameters are dynamically tunable in a wide range and specified by the user via an software interface. The mixed analog-digital ASIC was designed using a custom library of electronic cells: each cell computes a mathematical function necessary for the conductance-based models. Programmability is obtained by the integration of analog memory cells and of digital functions.

The results illustrate the precision and the diversity of the models emulated by the same ASIC. A single ionic current generator can be calcium or modulator type.

The main advantage of our library is that it can be directly re-used for a semi-automatic design of ICs. The next generations of ASICs will address two goals: include more ionic channels to study complex models at the single neuron level; or compute a set of neurons with a fixed model card for a network approach.

Acknowledgment

The authors thank Pr. G. Le Masson (INSERM E 358 – France) for his help on model specifications. This work was supported by E.U. Grant SENSEMAKER (IST-2001-34712).

References

[1] M. Mahowald and R. Douglas, "A silicon neuron", Nature, vol. 345, pp 515-518, 1991.

[2] G. Le Masson, S. Renaud-Le Masson, D. Debay and T. Bal, "Feedback inhibition controls spike transfer in hybrid thalamic circuits », Nature, vol. 417, pp. 854-858, 2002.

[3] M. F Simoni, G. S. Cymbalyuk, M. E. Sorensen, R. L. Calabrese and S. P. DeWeerth, 'A multiconductance Silicon Neuron with Biologically Matched Dynamics", *IEEE Trans. Bio. Eng.*, vol. 51, NO 2, pp. 342-354, 2004.

[4] G. Indiveri, "A Neuromorphic VLSI Device for Implementing 2-D Selective Attention Systems", *IEEE Trans. Neural Network*, vol. 12, NO 6, pp 1455-1463, 2001.

[5] L. Alvado et al., "Hardware computation of conductance-based neuron models", *Neurocomputing*, vol. 58-60, pp. 109-115, 2004.

[6] C. Koch, *Biophysics of Computation*, New York, Oxford University Press, 1999, pp. 212-231.

[7] L. Alvado, "Artificial Silicon Neurons: Towards the Networks", PhD Thesis, University Bordeaux 1, NO 2674, 2003.

[8] A. Destexhe, Z.F. Mainen, T.J. Sejnowski, "An Efficient Method for Computing Synaptic Conductances Based on a Kinetic Model of Receptor Binding", *Neural Computation*, vol. 6, pp. 14-18, 1994.

[9] C. Toumazou, F. G. Lidgey, D. G. Haigh, *Analogue IC Design: the current mode approach*, Peter Peregrinus Ltd, London, 1990.

[10] A.Hastings, *The art of analog layout*, Prentice Hall, 2001.

[11] D. A. McCormick, Z. Wang, J. Huguenard, "Neurotransmitter Control of Neocortical Neuronal Activity and Excitability", Cerebral Cortex, vol. 3, pp. 387-398, 1993.