Exercise E4: Design of a transimpedance amplifier based on a nullor+resistor structure

Use LTSpice simulation file E4_AC.asc and E4_Tran.asc.

Last update: 21 Dec 2021 (clarifications in text, redistribution of points)

A photodiode detects light coming from an optical fibre. We want to measure the resulting current generated by the photodiode with an amplifier having a low-ohmic input impedance and a high bandwidth to support high data rates. We will first design a simple nullor-resistor combination that has the ideally desired behaviour. Later we will implement the nullor as a MOS amplifier and look at the accuracy that can be achieved.

E4a: Draw a nullor-resistor combination that has zero input impedance and an I-V conversion determined by the resistor (5 points) and show with network equations that the circuit has the desired properties (5 points).

We will now use the Trans Impedance Amplifier ("TIA") shown in the upper left corner of figure 1. This amplifier converts the current generated by the photo diode (current source i_{in}) to a voltage via R_f. Now, a problem may occur when we want to connect different types of measurement systems. Some of these systems have a high ohmic input impedance, where the capacitance plays the most important role (e.g. an 1Mohm/10pF oscilloscope), whereas others have a broadband 50 Ohm input (sometimes with a large series capacitor to block DC voltages). We want to enable measurements with both types of loads, using a single circuit. We will now examine the suitability of Op-amp implementations of figures a) and b) for this purpose.

Important data:

- Photo-diode current (i_{in}): 100nA .. 100µA
- Photo-diode capacitance: 10pF
- Required equivalent noise input current < 2pA/$\sqrt{Hz}$ (derived elsewhere from photo diode noise specifications)
- Bias the transistor in strong inversion and saturation at a V_{GS} of a few hundred milli-Volts above the threshold voltage. Choose W/L ratios in the range 1/10 to 1000
- Load: R_L=50 ohm with big capacitor in series, or capacitance C_L=10 pF
- Bandwidth: as high as possible

Note: in this project we will target a linear and accurate current to voltage response. This may be overkill, especially when receiving digital signals for which it may be acceptable to let the amplifier clip. Still, we target linear signal processing here.

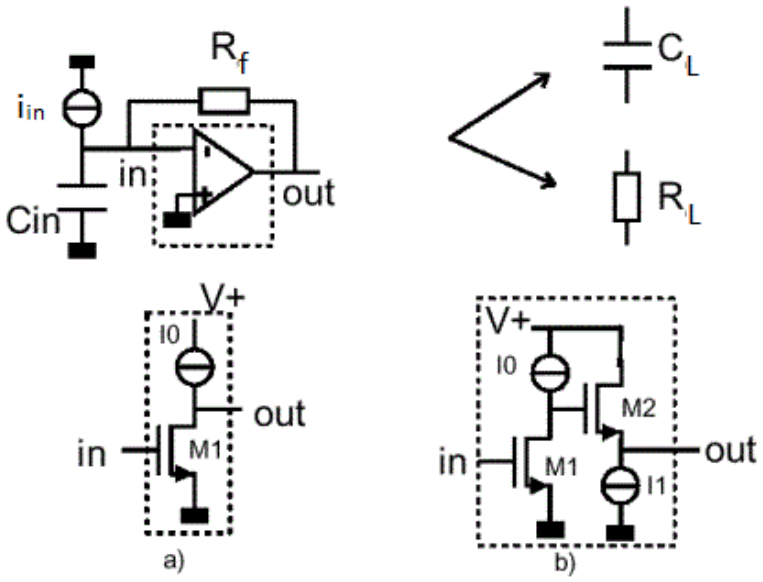

Figure 1 Transimpedance amplifier with feedback resistor R_f designed to drive both a capacitive load C_L and a resistive load R_L. a) Single stage amplifier; b) 2-stage amplifier alternative.

E4b: Show that the requirement on the noise performance leads to requirement on the minimum value of resistor R_f in the order of 10Kohm due to the noise of the resistor (10 points).

For accuracy reasons, we want to set the value of the I-V conversion to within 2% accuracy (compared with the ideal nullor circuit). Because we have accurate 10Kohm resistors with good temperature stability, we want to use this resistor as R_f. However, apart from this resistor, the limited gain of the amplifier may also affect loop-gain and hence I-V transfer accuracy. Also the load impedance may affect the loop-gain. To analyse these aspects, draw an equivalent small signal circuit modelling MOSFET V-I conversion but also channel length modulation. Do this for both the resistive and capacitive load and calculate the closed loop transfer function for both cases. The goal is to find the (low-frequency) I-V transfer to compare it to the desired one of E4a.

E4c: Relate load impedance to accuracy (5 points). Show by hand calculations that the circuit in figure 1a can drive a load capacitor C_L of 10pF with the required (low frequency) accuracy (5 points), but NOT the load resistor R_L of 50 ohm (5 points). Show this also by simulations using file E4_AC.asc (5 points).

E4d: Derive equations that demonstrate whether it makes sense to use a cascode stage instead of M1 in Figure 1a, or whether it is better to cascade by adding a second stage as done in figure 1b (2x5 points). Explain how both a cascode and cascade can improve performance (5 points), but there is a clear difference between driving R_L and C_L. Highlight key differences and draw a clear conclusion (5 points).

From here on, either do exercises E4e) and E4f) for the circuit in figure 1b) or do these exercises for your own circuit, if you feel you have a better idea (see *) bonus below).

E4e: Design and analyse an amplifier that can drive both R_L and C_L with the required accuracy (10 points). Motivate how you choose the values of W/L for the transistors and the current sources (5 points) As is the case in most design problems, there are multiple possible solutions. Simulate the resulting circuit and show that it fits to your expectations (5 points).

To keep the circuit stable and give it a decent closed-loop step-response for sudden variations in the incoming light, we want to try to achieve a 60 degrees phase-margin. To limit the required chip area, we would like to keep the capacitance as small as possible but certainly below 2pF. To analyse the phase margin, you can estimate pole-positions to find out whether the desired phase-margin can be achieved. To simplify analysis it is sufficient to consider only 3 capacitors: C_i and C_L and a third capacitor of max. 2 pF connected between the input of M2 and ground (or in another way if you use another circuit). Model MOSFETs with their transconductance (g_m), but for M1 also model output resistance to model a finite loop-gain. When needed to evaluate the open loop behaviour, cut the loop between the output of the amplifier and R_f (at this node a large difference in impedance exists, minimizing loading effects (see the lecture slides)).

E4f: Estimate the phase margin by hand calculations and predict the theoretical closed loop behaviour on that basis (10 points). Then simulate the closed loop behaviour for some different values of the crucial capacitor(s) using simulation file E4_Tran.asc. Explain how the results fit to your predictions based on calculations (5 points) and try to propose a design that satisfy the requirements (5 points).

*) Optional bonus (up to 10 points): If you have ideas to do better than circuit b), propose a schematic and simulate it, demonstrating good performance. Demonstrate both accuracy (exercise e) and step-response (exercise f)

General note: analogue circuits can always be improved further by smart design, i.e. optimization may take forever. Advice: playing around with analogue circuits may be fun, but you can also waste a lot of time with that (as with challenging puzzles or computer games). Try to take a pragmatic view and finish this course as soon as possible, certainly before starting the Wireless Transceiver Electronics design project).