

E0: MOST Large/small signal modelling (10% weight)

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Instructions

Use LTSpice and simulation file E0_DCandOP.asc. Unless otherwise stated use transistor data from table 2.1 of Razavi's book and assume $W=50\mu\text{m}$ and $L=0.5\mu\text{m}$ and assume $V_{DD}=3\text{V}$. These parameters are available in LTSpice from library `...lib\cmp\standard.mos` as model `nmos_ve2_level1` and `pmos_ve2_level1`. Note that this level1 model is a very simple quadratic model often used for hand calculation. However, even such a simple model can be valuable to find a first guess for component values and acquire insight in design trade-offs (e.g. increasing R_{drain} in a CS-stage improves the gain, but reduces the bandwidth). This model has only a few parameters. You can view and change them in file `...lib\cmp\standard.mos` to study parameter dependencies (don't forget to return to the standard parameters after experiments!).

As the level1 model in LTSpice is very similar to a quadratic hand calculation model, you can check your calculations by simulations. This is useful, as an error is easily made during hand calculations. Note that a difference between hand calculations and simulations of e.g. 10-20% is often acceptable, as the main goal is not accurate analysis, but first order insight in the design trade-offs. Keep this in mind during the exercises, and feel free to make simplifying assumptions to simplify formulas, but always motivate your modelling choices.

Keep your models simple and answer to-the-point: max. 1 page/question a, b, ..!

Let's start with the first exercise. Load circuit E0_DCandOP.asc in LTSPICE. Its aim is the basic understanding of the transistor large signal model and its relation to small signal behaviour.

Simulate $I_D(V_{GS})$ for a 50/0.5 NMOS biased in strong inversion at such a drain voltage that the MOS is biased in saturation, while $V_{SB}=0\text{V}$. By looking at the derivative of I_D with respect to V_{GS} verify that the MOS behaves as a quadratic Voltage Controlled Current Source. (Note: the mathematical operations 'derivative' is 'd()', see help "waveform arithmetic" or file LTspice_Waveform_Arithmetic.pdf; choose a suitable step size to obtain a smooth curve).

E0a) Demonstrate by a simulation that the MOS behaves quadratically and determine μC_{ox} (15 points) and V_{TH} (10 points) in this region from the simulation results.

Let's now try to understand how the simulation results are controlled by simulation parameters in the component library. In this case we use SPICE level 1.

E0b) Calculate μC_{ox} (10 points) and V_{TH} (5 points) from the SPICE level 1 parameter values, using the following information: $\mu=U_0$ [cm²/Vs]; $C_{ox} = \epsilon_{\text{SiO}_2}/t_{ox}=3.45\text{E-}11[\text{F/m}]/\text{TOX}[\text{m}]$. Comment on how your results compare to the previous answer of

E0a (10 points).

Notes: U_0 and TOX are SPICE level1 MOS model parameters given in table 2.1 in Razavi; note that despite of its name, C_{ox} is NOT a simple capacitance, but a capacitance per unit area!!

Let's now have a look at the small signal modeling.

E0c) Using the model equations and the data above, estimate the transconductance (g_m , 5 points), output conductance (g_o , 5 points) and gate-source capacitance (C_{gs} , 5 points) of a 50/0.5 NMOS transistor biased at $V_{GS}=1\text{V}$, $V_{DS}=1\text{V}$ and $V_{SB}=0\text{V}$. How do these results relate to the .OP analysis results obtained from LTSpice (5 points)? And how to the .TF simulation (10 points)?

Note: Only activate the .op analysis. After running a simulation, a window with bias voltages and currents pops up. Click "View" --> "SPICE Error Log" to find a list of small signal parameters for the transistors, including operating point and small signal capacitances and (trans)conductances. Then only activate .TF and try to explain the results.

Finally look at the PMOS transistor and adapt the LTSPICE schematic to bias it in strong inversion and triode. Simulate $I_D(V_{DS})$ for a 50/0.5 PMOS in strong inversion at such a drain voltage that the MOS is biased in the linear region (triode region), while $V_{SB}=0\text{V}$.

E0d) Using the formulas find a value for the resistance r_{ds} (15 points) for small V_{DS} and check it with simulations (10 points). How well do they fit to each other?