E1: Large/small signal modelling- CG Amplifier (10% weight)

Last update: 21 Dec 2021 (text clarified)

Use LTSpice file E1_DC_OP_AC.asc. Unless otherwise stated use W/L=50/0.5 transistors and data from table 2.1 of Razavi's book and assume VDD=3V.

Keep your models simple and answer to-the-point: max 1 page/question a, b, ..!

Suppose we aim to design an amplifier for a 75 ohm coax video system featuring:

- A resistive input impedance of 75 ohm (equal to the characteristic impedance of the cable to avoid reflections)
- Voltage Amplification >4
- Signals amplitudes <100mV
- Bandwidth 50MHz-900MHz (VHF en UHF TV bands and internet cable modem bands)

Used the LTSPICE circuit shown below driven by a signal current Iin, while biasing the transistor by Vbias and Ibias, resulting in a DC-bias voltage V(in) when Iin=0.
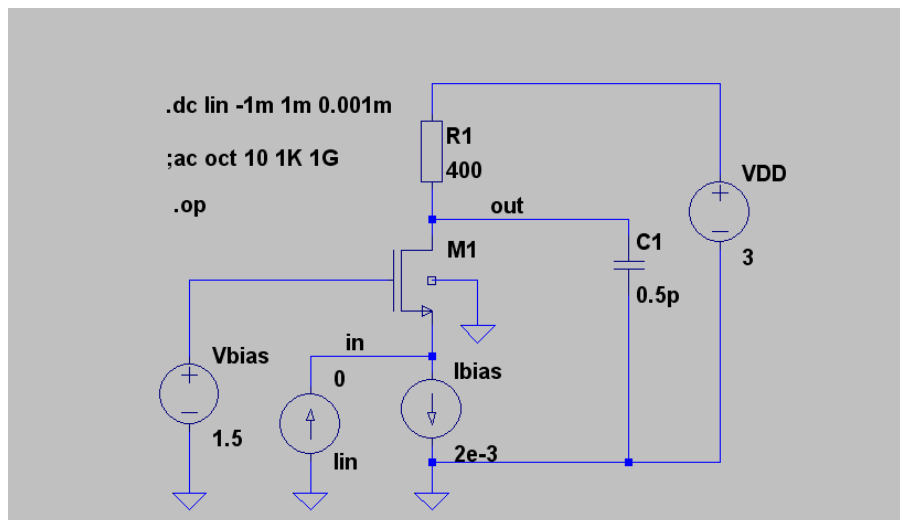
If Iin is changed, V(in) will also change and we will see a large signal non-linear response, which can however for small signals be approximated by a Taylor series. Using large signal equation and approximating them by a Taylor series we can also find the output voltage V(out). This is what we will pursue first. However, alternatively, we can also use a small signal equivalent circuit model, which is often easier to do, while it also can model capacitive and inductive parasitics, so that we can use such a model for frequency dependent analysis. We will use both methods and we should expect that the results are similar in some respects.

Let's now start with DC large signal equations and the Taylor series method. Although the

circuit is driven by current sources, it may be easier to analyse it as if it were driven by a voltage, as a MOSFET is a voltage controlled current source.

E1a) Sketch the large signal DC input characteristic Iin(V(in)) (10 points) and the transfer characteristic V(out)=f(V(in)) (5 points), using expressions derived via a simple quadratic MOS model (assume lambda=0). Pay special attention to the expected MOSFET operating regions (weak/strong inversion, triode/ saturation; (10 points)).

To check whether your prediction is correct we will now do simulations, but we first need some component values before we can do this.

E1b) Use the expression derived under E1a) to find an expression for the small signal input impedance (5 points). Based on this expression choose a combination of Vbias, W and Ibias that renders 75 ohm input impedance (5 points). Show by a DC simulation using simulation file E1_DC_OP_AC.asc that your design matches to 75 ohm for small signals (5 points) and also check it by an AC simulation (5 points). Finally increase the voltage range for the DC-analysis to the point where the source of the NMOS goes more than 0.6V negative and explain what happens (5 points).

Lets now move to small signal equivalent circuits and analyze frequency dependent behavior.

E1c) Using a simple small signal equivalent model, find expressions estimating:
- The frequency dependent small signal input impedance (5 points)
- The frequency dependent small signal output impedance (5 points)
- The frequency dependent voltage amplification (5 points)
- Then do AC simulations for the above mentioned 3 properties (5 points).
- Substitute numerical values in your expressions and show that you find a fair estimate of AC simulation results (5 points).

Notes: Please write the equations in a standard form clearly indicating the poles. For simplicity, only model a pole at the input and one at the output, both related to a total capacitor to ground (most of the MOSFET parasitic capacitances can now be considered as a part of these two capacitors, although not all; hence don't expect a perfect match between model and simulation). Assume that a current source is driving the input (as defined in the LTSpice file) and a load impedance C1 of 0.5pF is always present (modelling the input capacitance of the next circuit, e.g. a mixer, next amplifier or A/D converter). Study chapter 3 of Razavi if you encounter any problems. Also always double-check the operating point information (see also exercise E0c).

E1d) What is the highest achievable small-signal gain if you cannot accept more than 3dB roll-off in the transfer function at 900MHz? First find the -3dB bandwidth (5 points), then the relation with small-signal gain (10 points) and its maximum (5 points); finally simulate gain and bandwidth and draw conclusions (5 points)

Hint: in a first order system, the -3dB bandwidth is the pole-frequency; this circuit can be modelled with 2 poles; please indicate which of the two poles dominates in your circuit.