Exercise E3: Current mirrors, noise and mismatch (30% weight)

Last update: 22 Dec 2021: (text clarified)

Use LTSpice simulation file E3_DC_AC_Noise.asc.
Keep your models simple and answer to-the-point: max 1 page/question a, b, ..!
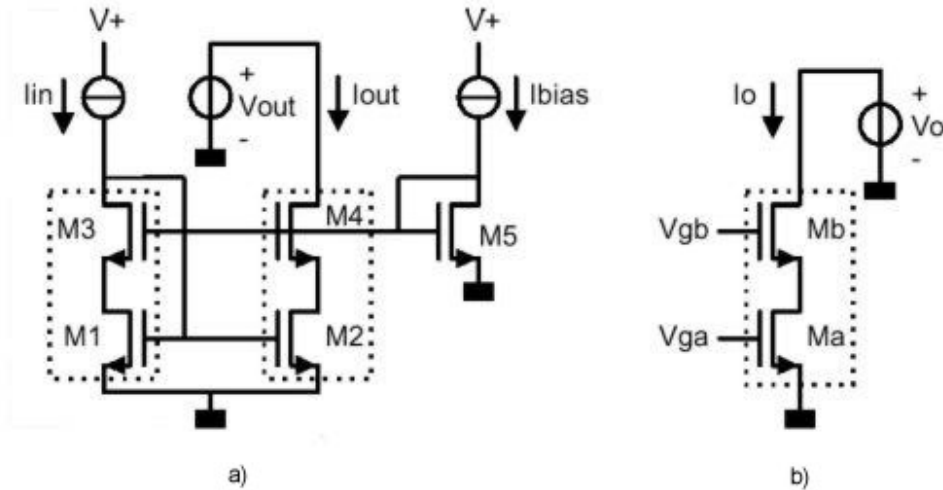

Figure 1: a) current mirror consisting of two equal voltage-controlled current sources (marked in the drawing) and a bias circuit consisting of M5 and a current source Ibias; b) The voltage controlled current source sub-circuit used in the mirror of a).

The current mirror in figure 1a consists of two equal voltage controlled current sources (like the one in figure 1b) and a bias circuit consisting of transistor M_5 and the current source I_{bias}. By choosing the bias-circuit correctly, the mirror can give an output current I_{out} equal to the input current I_{in} over a very wide voltage range of V_{out}.

All transistors are modelled as follows (you can neglect the body effect):

$$I_D = \frac{K}{2}(V_{GS} - V_{TH})^2 (1 + \lambda \cdot V_{DS})$$

with

$$K = \mu \cdot c_{ox} \cdot \frac{W}{L}$$

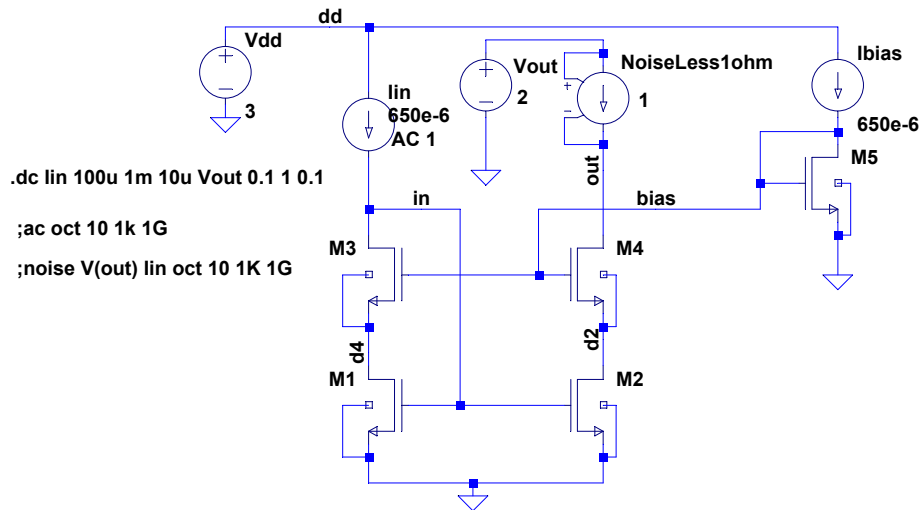Note: depending on what you want to calculate and how accurate, it may be acceptable to put λ to zero.

Figure 2: current mirror consisting of two equal voltage-controlled current sources (marked in the drawing Assume that M1=M2=M3=M4 and W1/L1 = 50μm/0.5μm

Use the circuit in Figure 2 for the following three questions (you can assume that the NoiseLess1ohm is small enough to hardly affect circuit behaviour):

Note: The output current of a current mirror should not be sensitive to what happens at its output, e.g. a change in V_{out}. In practice, there will be a dependence e.g. because transistors enter the triode region instead of the saturation region. By design, one can try to maximise the output voltage range for which good current mirror operation occurs.

E3a) Find the value of W/L for transistor M_5 for which the voltage range for V(out) is maximised. Assume the maximum value of the input current $I_{in,maximum}=I_{bias}=650$ μA. Neglect the influence of short-channel effects. Check the limit of the V_{out} range via DC simulation (DC-sweep of V_{out} and plot I_{out}/I_{in}) (15 points).

E3b) Draw a PMOS current mirror version of the mirror you designed with NMOS transistors and give all corresponding MOSFETs the same W/L as for the NMOS case (5 points). Repeat the simulation you did for the NMOS mirror, changing polarities in such a way that the PMOS mirror works intended normally. Plot a similar plot than for a) and comment on the differences that you may observe (or not) (15 points).

E3c) Show for the voltage-controlled current source of figure 1b that current I_o is more sensitive to variations in voltage V_{ga} than for variations in V_{gb}. Use a small signal transistor model with only transconductance and output resistance to show this. Then use the result to calculate the input impedance of the mirror in a very simple way. Verify the value by simulating the AC input impedance V_{in}/I_{in} (15 points)

Now we want to evaluate the noise of the output current of the mirror. As LTSPICE can only simulate voltage noise, a noiseless 1 ohm resistor was added as I-V converter (this is small enough to hardly affect DC biasing and current transfer).

We model the noise as an extra current source between drain and source, and assume that the "Noise Excess Factor" is equal to 2/3 for the MOST transistors (that means that the noise is equal to that given by a resistor of value $1/g_m$):

$$\overline{i_d^2} = 8/3 \cdot k \cdot T \cdot g_m \cdot \Delta f$$

E3d) Re-using the small-signal circuit from b) with the noise sources added, show that the noise contribution of the cascode transistor M_b is insignificant compared to that of main current-defining transistor M_a (15 points)

E3e) Calculate the noise current density of the output current I_{out}, assuming that currents I_{in} and I_{bias} are noise-free, but mind that M1, M3 and M5 are still noisy (hint: you can use the conclusion of b) to simplify the analysis). Verify the result by noise simulation using file E3_noise.asc. Which transistors contribute most to the noise? (15 points)

Finally, we will evaluate current copying accuracy due to the limited component matching of the transistors in the current mirror. Suppose that we can accept an error of 1% in the mirror currents due to transistor mismatch. Assume also that only transistors M_1 and M_2 contribute to the error. Use the following mismatch data for a transistor pair:

$$\sigma_K = \frac{A_K}{\sqrt{WL}} \qquad \sigma_{V_{TH}} = \frac{A_{V_{TH}}}{\sqrt{WL}}$$

and: $A_K / K = 2 \% \ \mu m$; $A_{VTH} = 5 \ mV \ \mu m$

f) Does the mirror designed above meet the 1% current mismatch criterion? If not, propose how you would change the circuit to meet the requirement. Anyway explain how you would improve accuracy if a factor X improvement in current mismatch would be needed. Note: assume that "3σ-design" is required to achieve sufficient yield in production. Motivate your answer quantitatively using equations (25 points).