Exercise E2: Differential amplifier (25% weight)

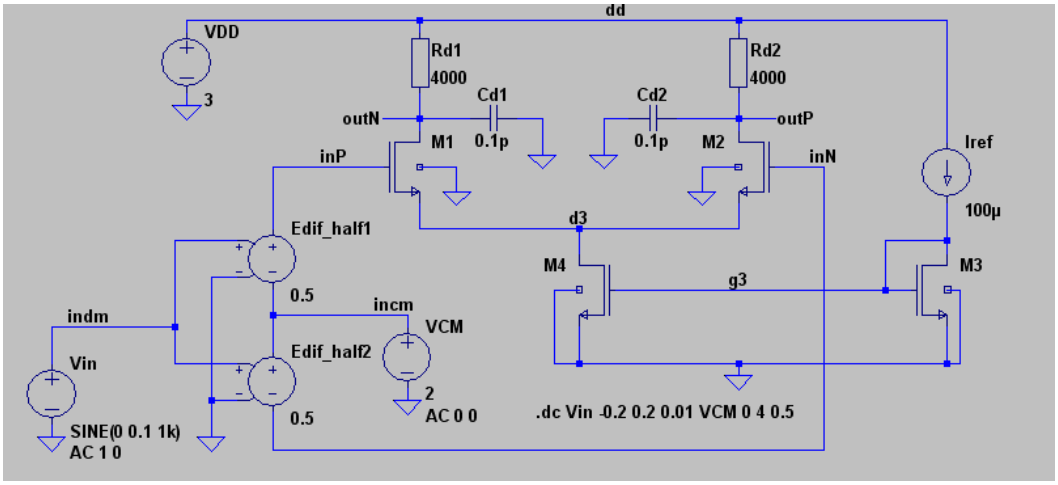
Last update: 22 Dec 2021 (text clarified)

Use LTSpice and simulation file E2_DC_AC_TRAN.asc.

Keep your models simple and answer to-the-point: max 1 page/question a, b, ..!

Differential pairs are commonly used in OPAMPs, but also in many other circuits like wideband amplifiers, variable gain amplifiers, comparators, V-I converters, high-speed current mode logic, line-drivers and line-receivers for USB, etc. In this exercise, we will examine some key properties of the differential pair, and see how we can adapt them by designing for the right combination of W/L values, resistance values, bias voltages and bias currents. The key properties involved are transconductance, bandwidth, linearity, common-mode range and common-mode rejection.

Note: design problems usually have multiple possible solutions: you can e.g. get high gain with a high transconductance and low resistance or the other way around.



E2a) Using the first order MOS model, estimate the common mode voltage range (V_{CM}) for which the differential amplifier operates properly, with all transistors operating in strong inversion and saturation (15 points). Note that the body effect also plays a role. Verify your expectations by .op analysis using file E2_DC_AC_TRAN.asc (5 points).

E2b) Calculate the low-frequency voltage-gain A_v of the differential amplifier as a function of bias current I_{ref}, resistance R_d, and W/L values (10 points). Choose values such that A_v=3x and that all transistors operate in strong inversion and saturation (5 points). Verify your design via a DC simulation (5 points).

The differential amplifier can only amplify signals linearly with a limited input voltage swing, because of the nonlinear I(V) curve of the differential pair. One of the ways to characterize such nonlinearity is by considering the "slope variation" or “small signal gain variation” as function of the input voltage (in Taylor series terms: plotting dy/dx versus x). Ideally this slope should not change for a perfectly linear circuit, and the variations that does occur gives useful information about nonlinearity. The shape of the curve for instance tells us which nonlinear term dominates (2^{nd} or 3^{rd} order nonlinearity) and the magnitude of the changes in slope defines the amount of harmonic distortion. A convenient way to obtain this information is to evaluate the DC-transfer (.DC analysis) and then take the derivative.

Suppose now that we define the linear input range of the differential pair in terms of slope variation, where we allow for 10% variation.

E2c) Derive now an expression and value for the linear input range of the differential pair (10 points). Verify the value by simulation (DC simulation setup can be used, taking the derivative of Iout(Vin)) (5 points). Question: how can you distinguish between even order harmonics distortion (e.g. HD2, HD4, etc) and odd order distortion (HD3, HD5, etc) from the shape of the differential gain curve (5 points)?

E2d) Calculate the bandwidth of the amplifier for pure balanced differential mode excitation (5 points). Verify it by AC simulation and comment on the results (5 points). Question: How can we improve the bandwidth and still achieve the same low-frequency gain without changing the capacitive load (5 points)? Proof that you are right via an AC simulation (5 points).

E2e) Examine the common mode rejection of the circuit via AC simulation (5 points), but now with a COMMON mode voltage excitation, while still monitoring the differential output (for this purpose put the AC value of source V_{in} to 0Volt (off), and the AC value of source V_{CM} to 1Volt). Examine what happens if R_{d1} and R_{d2} are not equal (5 points). Also add a capacitance to the common source node of M_1/M_2. Explain the results qualitatively (5 points) and give a design advice to maximise common mode rejection (5 points).