

## Features

- Low-voltage and Standard-voltage Operation
  - 2.7 ( $V_{CC} = 2.7V$  to  $5.5V$ )
- Internally Organized 16,384 x 8 and 32,768 x 8
- Two-wire Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- 400 kHz Compatibility
- Write Protect Pin for Hardware and Software Data Protection
- 64-byte Page Write Mode (Partial Page Writes Allowed)
- Self-timed Write Cycle (5 ms Max)
- High Reliability
  - Data Retention: 40 Years
- Lead-free/Halogen-free Devices Available
- 8-lead JEDEC SOIC and 8-lead TSSOP

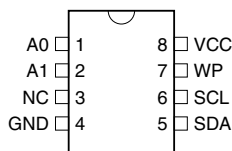
## Description

The AT24C128/256 provides 131,072/262,144 bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 16,384/32,768 words of 8 bits each. The device's cascadable feature allows up to 4 devices to share a common Two-wire bus. The device is optimized for use in many automotive applications where low power and low voltage operation are essential. The AT24C128 is available in space-saving 8-lead JEDEC SOIC and 8-lead TSSOP packages. The AT24C256 is available in a space-saving 8-lead JEDEC SOIC package. In addition, the entire family is available in 2.7V (2.7V to 5.5V) version.

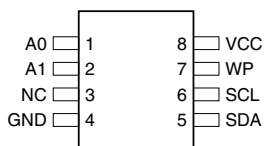
**Table 1.** Pin Configuration

Pin Name	Function
A0 - A1	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
NC	No Connect
GND	Ground

8-lead TSSOP



8-lead SOIC



## Two-wire Automotive Temperature Serial EEPROMs

128K (16,384 x 8)

256K (32,768 x 8)

## AT24C128 AT24C256

**Not Recommended  
for New Design.  
Replaced by  
AT24C128C/256C  
Automotive.**

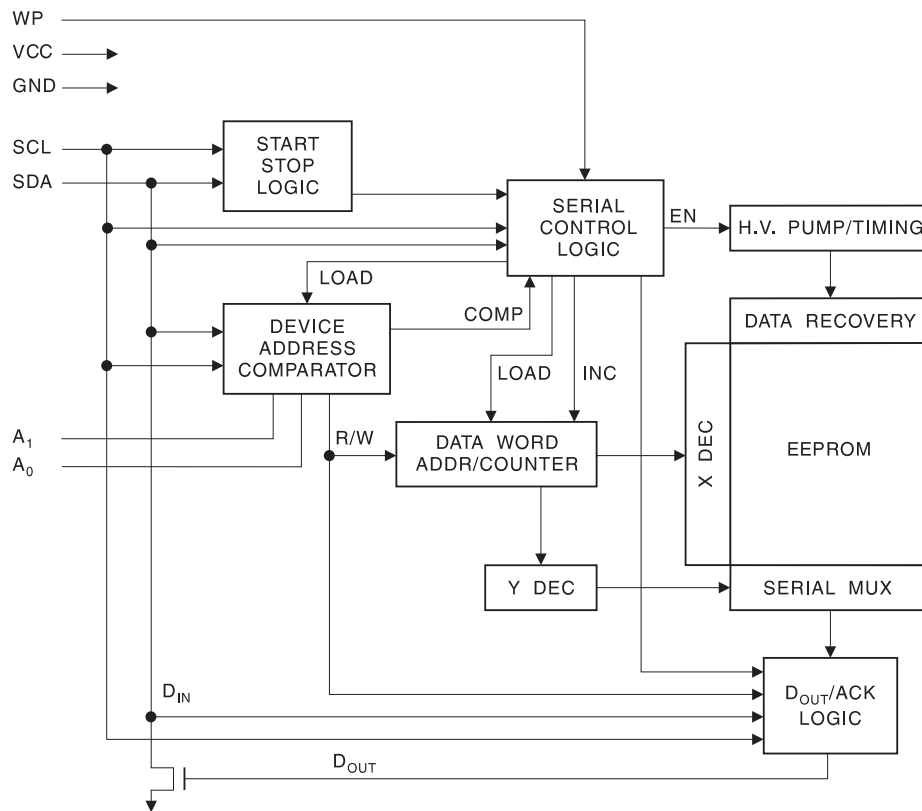


## Absolute Maximum Ratings\*

Operating Temperature .....	-55°C to +125°C
Storage Temperature.....	-65°C to +150°C
Voltage on Any Pin with Respect to Ground .....	-1.0V to +7.0V
Maximum Operating Voltage .....	6.25V
DC Output Current.....	5.0 mA

**\*NOTICE:** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Figure 1.** Block Diagram



## Pin Description

**SERIAL CLOCK (SCL):** The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

**SERIAL DATA (SDA):** The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open collector devices.

**DEVICE/ADDRESSES (A1, A0):** The A1 and A0 pins are device address inputs that are hardwired or left not connected for hardware compatibility with other AT24CXX devices. When the pins are hardwired, as many as four 128K/256K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section). If the pins are left floating, the A1 and A0 pins will be internally pulled down to GND if the capacitive coupling to the circuit board  $V_{CC}$  plane is  $<3$  pF. If coupling is  $>3$  pF, Atmel recommends connecting the address pins to GND.

**WRITE PROTECT (WP):** The write protect input, when connected to GND, allows normal write operations. When WP is connected high to  $V_{CC}$ , all write operations to the memory are inhibited. If the pin is left floating, the WP pin will be internally pulled down to GND if the capacitive coupling to the circuit board  $V_{CC}$  plane is  $<3$  pF. If coupling is  $>3$  pF, Atmel recommends connecting the pin to GND.

## Memory Organization

**AT24C128/256, 128K/256K SERIAL EEPROM:** The 128K/256K is internally organized as 256/512 pages of 64-bytes each. Random word addressing requires a 14/15-bit data word address.

**Table 2.** Pin Capacitance<sup>(1)</sup>

Applicable over recommended operating range from  $T_A = 25^\circ\text{C}$ ,  $f = 1.0\text{ MHz}$ ,  $V_{CC} = +2.7\text{V}$  to  $+5.5\text{V}$

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O} = 0\text{V}$
$C_{IN}$	Input Capacitance ( $A_0$ , $A_1$ , SCL)	6	pF	$V_{IN} = 0\text{V}$

Note: 1. This parameter is characterized and is not 100% tested.

**Table 3.** DC Characteristics

Applicable over recommended operating range from:  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{CC} = +2.7\text{V}$  to  $+5.5\text{V}$

(unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units	Symbol
$V_{CC3}$	Supply Voltage		2.7		5.5	V	$V_{CC3}$
$I_{CC}$	Supply Current $V_{CC} = 5.0\text{V}$	READ at 100 kHz		0.4	1.0	mA	$I_{CC}$
$I_{CC}$	Supply Current $V_{CC} = 5.0\text{V}$	WRITE at 100 kHz		2.0	3.0	mA	$I_{CC}$
$I_{SB3}$	Standby Current $V_{CC} = 2.7\text{V}$	$V_{IN} = V_{CC}$ or $V_{SS}$		1.6	4.0	$\mu\text{A}$	$I_{SB3}$
$I_{SB4}$	Standby Current $V_{CC} = 5.0\text{V}$	$V_{IN} = V_{CC}$ or $V_{SS}$		8.0	18.0	$\mu\text{A}$	$I_{SB4}$
$I_{LI}$	Input Leakage Current	$V_{IN} = V_{CC}$ or $V_{SS}$		0.10	3.0	$\mu\text{A}$	$I_{LI}$
$I_{LO}$	Output Leakage Current	$V_{OUT} = V_{CC}$ or $V_{SS}$		0.05	3.0	$\mu\text{A}$	$I_{LO}$
$V_{IL}$	Input Low Level <sup>(1)</sup>		-0.6		$V_{CC} \times 0.3$	V	$V_{IL}$
$V_{IH}$	Input High Level <sup>(1)</sup>		$V_{CC} \times 0.7$		$V_{CC} + 0.5$	V	$V_{IH}$
$V_{OL2}$	Output Low Level $V_{CC} = 3.0\text{V}$	$I_{OL} = 2.1\text{ mA}$			0.4	V	$V_{OL2}$
$V_{OL1}$	Output Low Level $V_{CC} = 1.8\text{V}$	$I_{OL} = 0.15\text{ mA}$			0.2	V	$V_{OL1}$

Note: 1.  $V_{IL}$  min and  $V_{IH}$  max are reference only and are not tested.

**Table 4. AC Characteristics**

Applicable over recommended operating range from  $T_A = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ,  $V_{CC} = +2.7\text{V}$  to  $+5.5\text{V}$ ,  $CL = 1$  TTL Gate and  $100\text{ pF}$  (unless otherwise noted)

Symbol	Parameter	AT24C128/256		Units
		Min	Max	
$f_{\text{SCL}}$	Clock Frequency, SCL		400	kHz
$t_{\text{LOW}}$	Clock Pulse Width Low	1.2		$\mu\text{s}$
$t_{\text{HIGH}}$	Clock Pulse Width High	0.6		$\mu\text{s}$
$t_{\text{AA}}$	Clock Low to Data Out Valid	0.1	0.9	$\mu\text{s}$
$t_{\text{BUF}}$	Time the bus must be free before a new transmission can start <sup>(1)</sup>	1.2		$\mu\text{s}$
$t_{\text{HD,STA}}$	Start Hold Time	0.6		$\mu\text{s}$
$t_{\text{SU,STA}}$	Start Set-up Time	0.6		$\mu\text{s}$
$t_{\text{HD,DAT}}$	Data In Hold Time	0		$\mu\text{s}$
$t_{\text{SU,DAT}}$	Data In Set-up Time	100		ns
$t_{\text{R}}$	Inputs Rise Time <sup>(1)</sup>		300	ns
$t_{\text{F}}$	Inputs Fall Time <sup>(1)</sup>		300	ns
$t_{\text{SU,STO}}$	Stop Set-up Time	0.6		$\mu\text{s}$
$t_{\text{DH}}$	Data Out Hold Time	50		ns
$t_{\text{WR}}$	Write Cycle Time		5	ms
Endurance <sup>(1)</sup>	3.3V, $25^{\circ}\text{C}$ , Page Mode	1M		Write Cycles

Note: 1. This parameter is ensured by characterization only.

## Device Operation

**CLOCK and DATA TRANSITIONS:** The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see Figure 4 on page 7). Data changes during SCL high periods will indicate a start or stop condition as defined below.

**START CONDITION:** A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see Figure 5 on page 8).

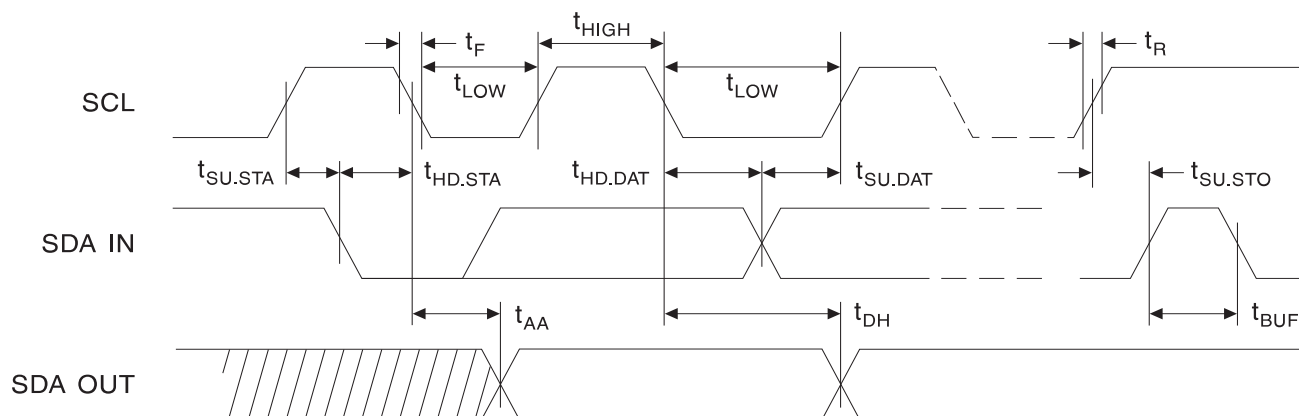
**STOP CONDITION:** A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (see Figure 5 on page 8).

**ACKNOWLEDGE:** All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero during the ninth clock cycle to acknowledge that it has received each word.

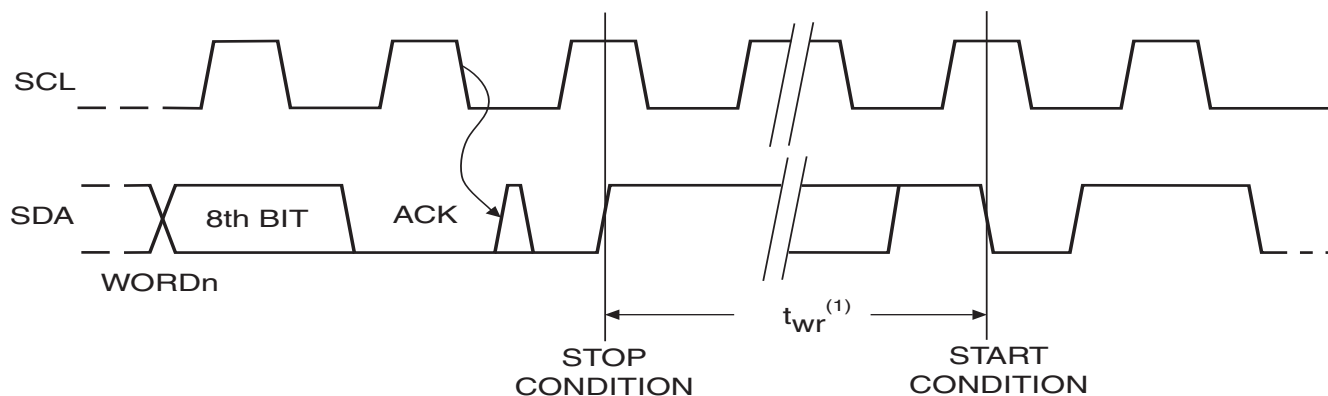
**STANDBY MODE:** The AT24C128/256 features a low power standby mode which is enabled: a) upon power-up and b) after the receipt of the STOP bit and the completion of any internal operations.

**MEMORY RESET:** After an interruption in protocol, power loss or system reset, any two-wire part can be reset by following these steps: (a) Clock up to 9 cycles, (b) look for SDA high in each cycle while SCL is high and then (c) create a start condition as SDA is high.

**Figure 2.** Bus Timing (SCL: Serial Clock, SDA: Serial Data I/O)

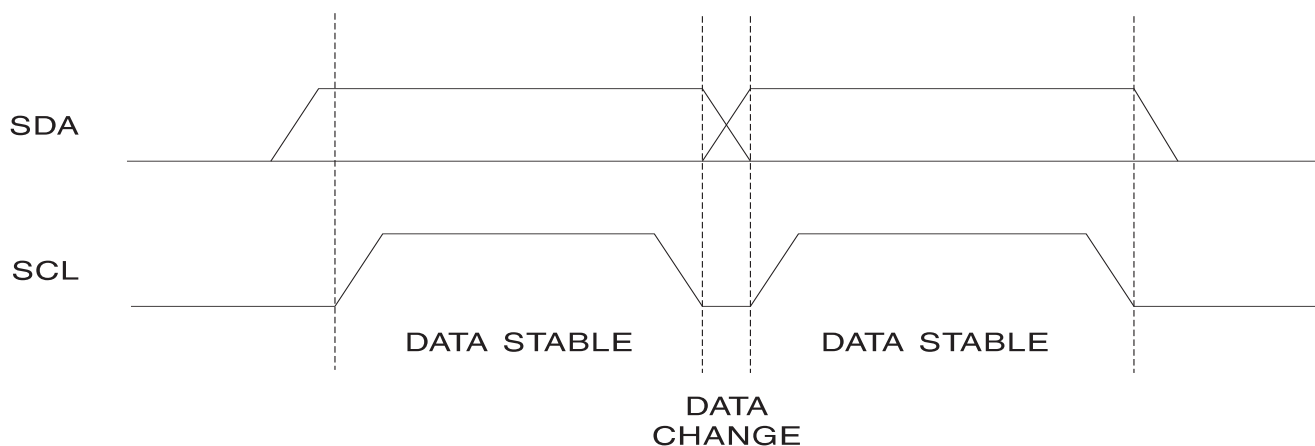


**Figure 3.** Write Cycle Timing (SCL: Serial Clock, SDA: Serial Data I/O)

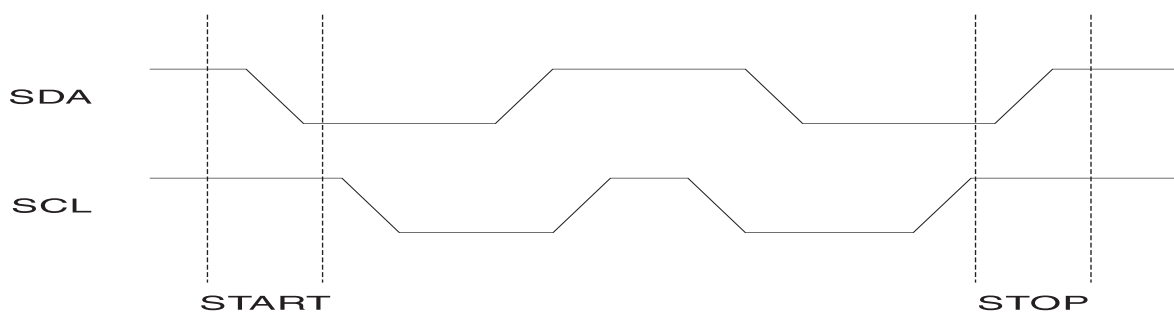


Note: 1. The write cycle time  $t_{wr}$  is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

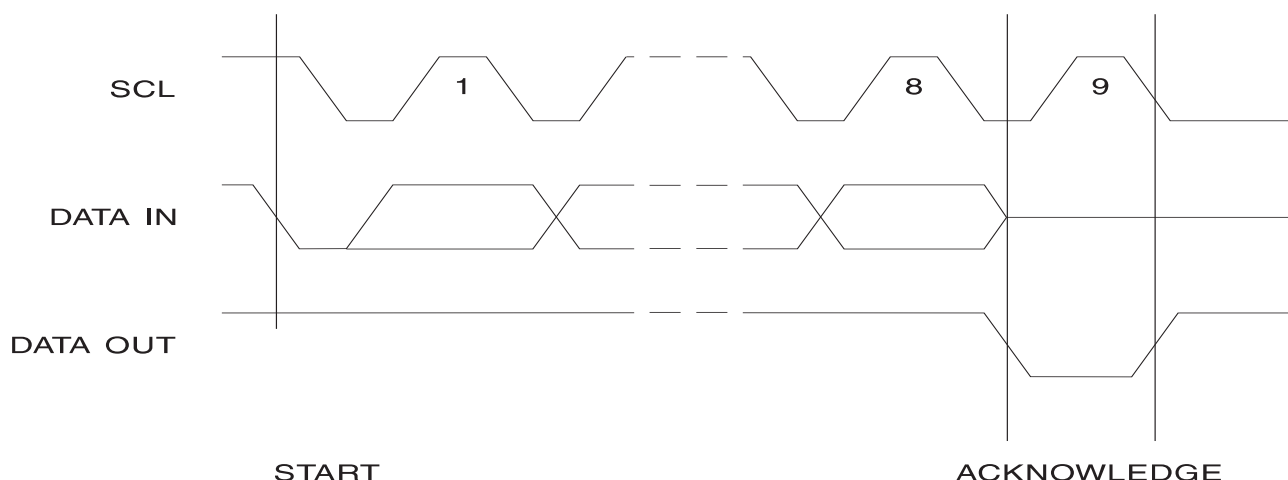
**Figure 4.** Data Validity



**Figure 5. Start and Stop Definition**



**Figure 6. Output Acknowledge**



## Device Addressing

The 128K/256K EEPROM requires an 8-bit device address word following a start condition to enable the chip for a read or write operation (see Figure 7 on page 10). The device address word consists of a mandatory one, zero sequence for the first five most significant bits as shown. This is common to all two-wire EEPROM devices.

The 128K/256K uses the two device address bits A1, A0 to allow as many as four devices on the same bus. These bits must compare to their corresponding hardwired input pins. The A1 and A0 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are allowed to float.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a zero. If a compare is not made, the device will return to a standby state.

**DATA SECURITY:** The AT24C128/256 has a hardware data protection scheme that allows the user to write protect the whole memory when the WP pin is at  $V_{CC}$ .



## Write Operations

**BYTE WRITE:** A write operation requires two 8-bit data word addresses following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero. The addressing device, such as a microcontroller, then must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally-timed write cycle,  $t_{WR}$ , to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see Figure 8 on page 10).

**PAGE WRITE:** The 128K/256K EEPROM is capable of 64-byte page writes.

A page write is initiated the same way as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 63 more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (see Figure 9 on page 11).

The data word address lower 6 bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 64 data words are transmitted to the EEPROM, the data word address will “roll over” and previous data will be overwritten. The address “roll over” during write is from the last byte of the current page to the first byte of the same page.

**ACKNOWLEDGE POLLING:** Once the internally-timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero, allowing the read or write sequence to continue.

## Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations: current address read, random address read and sequential read.

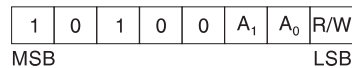
**CURRENT ADDRESS READ:** The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address “roll over” during read is from the last byte of the last memory page, to the first byte of the first page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following stop condition (see Figure 10 on page 11).

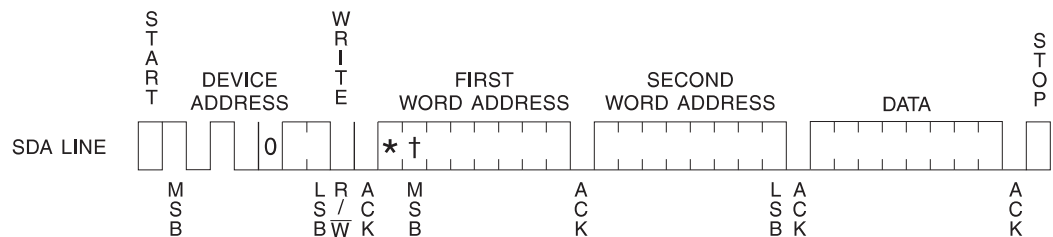
**RANDOM READ:** A random read requires a “dummy” byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition (see Figure 11 on page 11).

**SEQUENTIAL READ:** Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will “roll over” and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition (see Figure 12 on page 11).

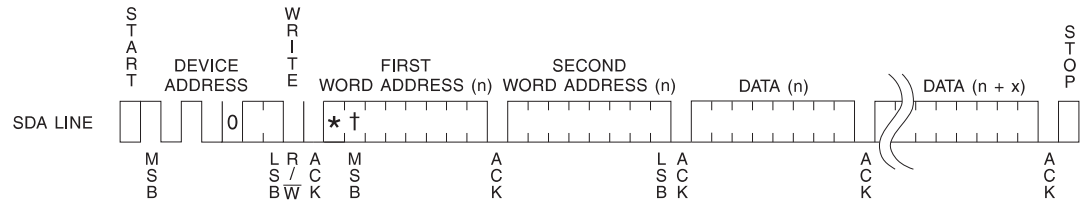
**Figure 7. Device Address**



**Figure 8. Byte Write**

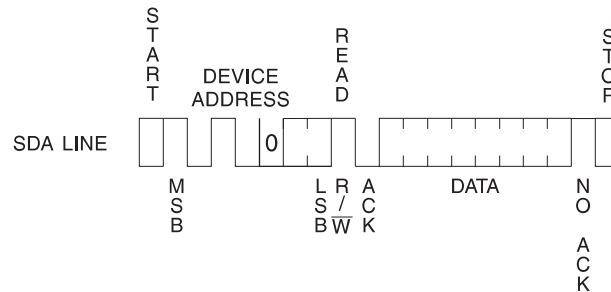


**Figure 9. Page Write**

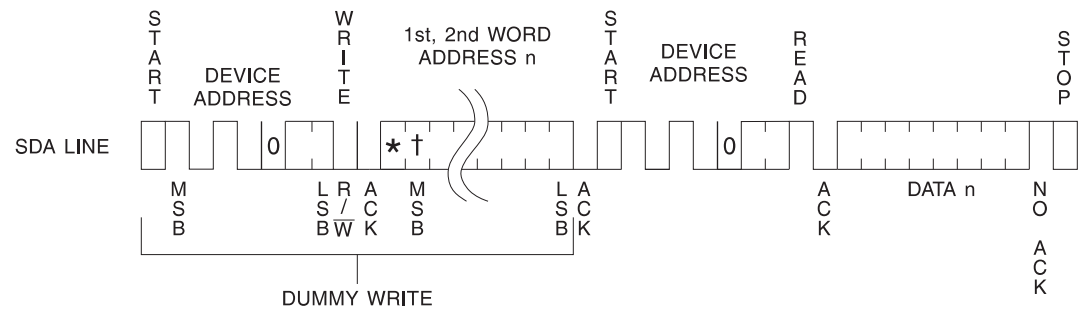


Notes: (\* = DON'T CARE bit)  
(† = DON'T CARE bit for the 128K)

**Figure 10. Current Address Read**

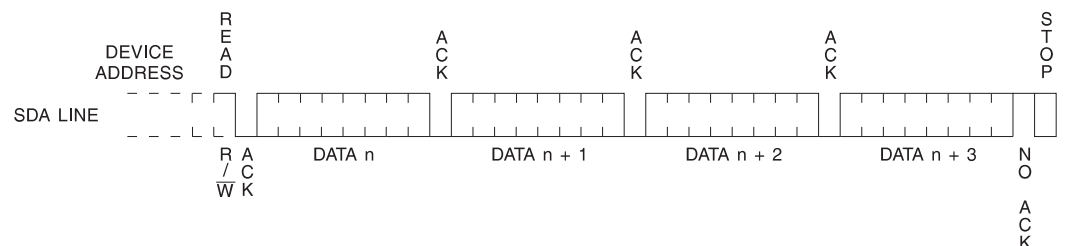


**Figure 11. Random Read**



Notes: (\* = DON'T CARE bit)  
(† = DON'T CARE bit for the 128K)

**Figure 12. Sequential Read**





## AT24C128 Ordering Information

Ordering Code	Package	Operation Range
AT24C128-10TQ-2.7 AT24C128N-10SQ-2.7	8A2 8S1	Lead-free/Halogen-free/ Automotive Temperature (–40°C to 125°C)

Package Type	
<b>8S1</b>	8-lead, 0.150" Wide, Plastic Gull Wing Small Outline Package (JEDEC SOIC)
<b>8A2</b>	8-lead, 4.4 mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)
Options	
<b>–2.7</b>	Low-voltage (2.7V to 5.5V)

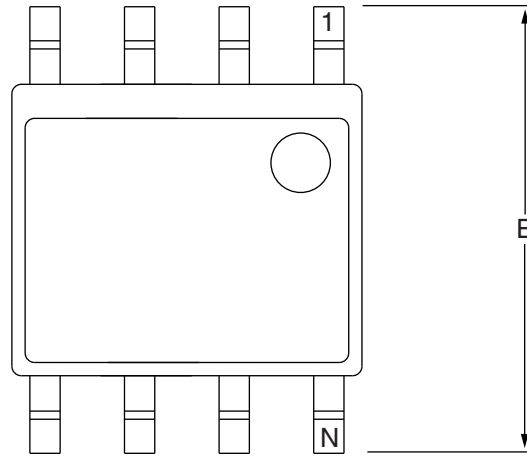
## AT24C256 Ordering Information

Ordering Code	Package	Operation Range
AT24C256N-10SQ-2.7	8S1	Lead-free/Halogen-free/ Automotive Temperature (–40°C to 125°C)

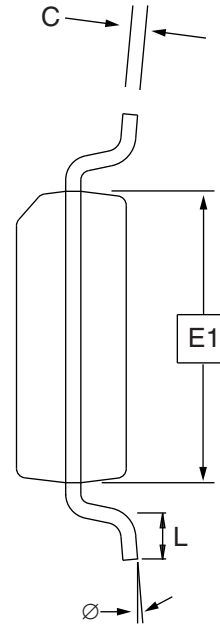
Package Type	
<b>8S1</b>	8-lead, 0.150" Wide, Plastic Gull Wing Small Outline Package (JEDEC SOIC)
<b>8A2</b>	8-lead, 4.4 mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)
Options	
<b>–2.7</b>	Low-voltage (2.7V to 5.5V)

## Packaging Information

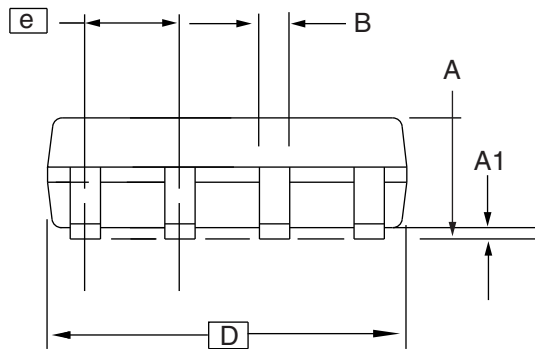
### 8S1 – JEDEC SOIC



Top View



End View



Side View

**COMMON DIMENSIONS**  
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.00	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
Ø	0°	–	8°	

Note: These drawings are for general information only. Refer to JEDEC Drawing MS-012, Variation AA for proper dimensions, tolerances, datums, etc.

10/7/03



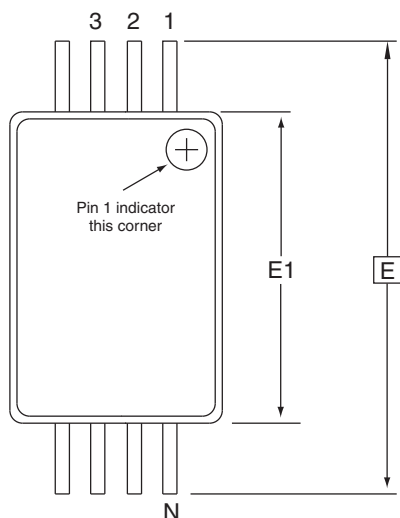
1150 E. Cheyenne Mtn. Blvd.  
Colorado Springs, CO 80906

**TITLE**  
**8S1**, 8-lead (0.150" Wide Body), Plastic Gull Wing  
Small Outline (JEDEC SOIC)

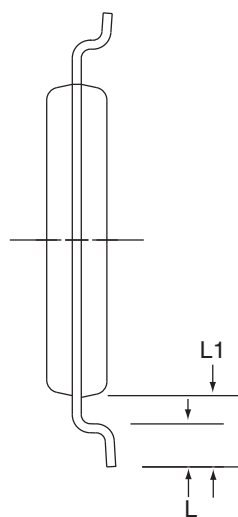
**DRAWING NO.**  
8S1

**REV.**  
B

# 8A2 – TSSOP



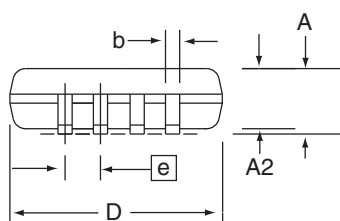
Top View



End View

## COMMON DIMENSIONS (Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
D	2.90	3.00	3.10	2, 5
E	6.40 BSC			
E1	4.30	4.40	4.50	3, 5
A	–	–	1.20	
A2	0.80	1.00	1.05	
b	0.19	–	0.30	4
e	0.65 BSC			
L	0.45	0.60	0.75	
L1	1.00 REF			



Side View

- Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
  2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006 in) per side.
  3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010 in) per side.
  4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07 mm.
  5. Dimension D and E1 to be determined at Datum Plane H.

5/30/02



2325 Orchard Parkway  
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### TITLE

**8A2**, 8-lead, 4.4 mm Body, Plastic  
Thin Shrink Small Outline Package (TSSOP)

### DRAWING NO.

8A2

### REV.

B

## Revision History

Doc. Rev.	Date	Comments
5121B	8/2012	Not recommended for new design. Replaced by AT24C128C/256C Automotive.
5121B	1/2007	Implemented revision history Removed PDIP package offering Remove PB'd parts





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### Literature Requests

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