

Random Number G

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I. ABSTRACT

This report presents the design and implementation of a random number generator using two D flip-flops and a seven-segment display. The random number generator utilizes the XOR operation between the Q1 and Q2 outputs of the first D flip-flop to generate random bits. The generated random bits are then displayed on a seven-segment display using logic gates and decoder ICs.

II. INTRODUCTION

The random number generator using two D flip-flops and a seven-segment display is a hardware project that generates random numbers and displays them on a seven-segment display. This report provides an overview of the project, the components used, the design implementation, and the functionality of the system.

III. COMPONENTS

The following components are used in the random number generator system:

- Two SN74LS74N D Flip-Flops: These flip-flops are used to store and manipulate the random number bits.
- SN74LS86N XOR Gate: This gate is used to perform the XOR operation between the Q1 and Q2 outputs of the first flip-flop.
- NE555P Timer IC: This IC is used to provide clock pulses for the flip-flops.
- SN74LS47 Seven-Segment Decoder/Driver: This IC is used to decode the random number bits and drive the seven-segment display.

IV. DESIGN AND IMPLEMENTATION

The random number generator system is implemented as follows:

A. Random Bit Generation

- Connect the D1 input of the first flip-flop (SN74LS74N) to the XOR gate output (SN74LS86N).
- Connect the Q1 and Q2 outputs of both flip-flops to their respective D inputs.
- Connect the output of the XOR gate to the D1 input of the first flip-flop.

B. Clock Signal Generation

- Connect the NE555P Timer IC in astable mode to generate clock pulses.
- Connect the output of the NE555P to the clock inputs of both flip-flops.

C. Seven-Segment Display

- Connect the Q1 and Q2 outputs of the second flip-flop to the inputs of the SN74LS47 Seven-Segment Decoder/Driver.
- Connect the outputs of the decoder to the seven-segment display segments.

V. FUNCTIONALITY

The random number generator system operates as follows:

- Upon applying power, the NE555P Timer IC generates clock pulses.
- The clock pulses drive the flip-flops, causing them to toggle and generate random bit sequences.
- The XOR gate combines the Q1 and Q2 outputs of the first flip-flop to generate random bits.
- The random bits are decoded by the SN74LS47 Seven-Segment Decoder/Driver and displayed on the seven-segment display.
- The display continuously updates with new random numbers as the flip-flops generate them.

VI. CONCLUSION

The random number generator using two D flip-flops and a seven-segment display provides a simple and visually appealing way to generate random numbers. The combination of flip-flops, XOR gate, and decoder ICs allows for the generation and display of random numbers on a seven-segment display. This project demonstrates the application of digital logic and ICs in creating a random number generation system.

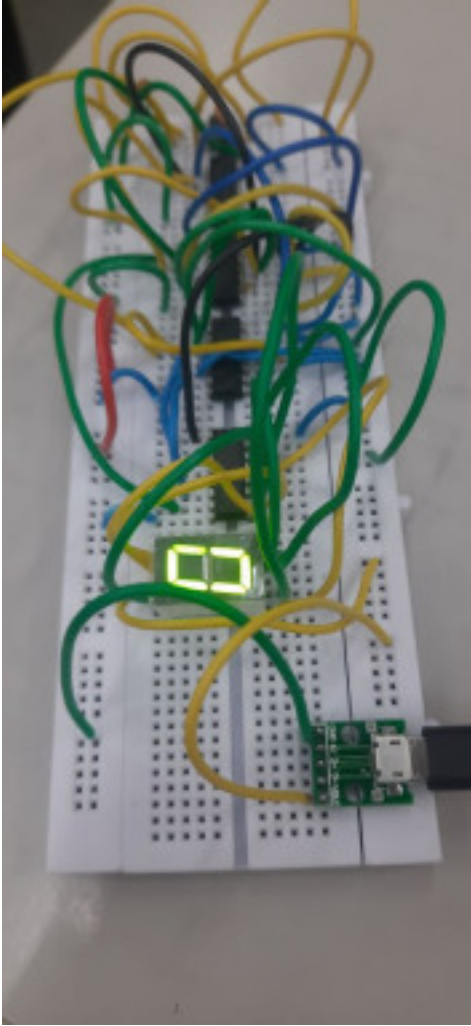


Fig. 1. Circuit diagram of the random number generator.