浙江大学 2018－2019 学年夏学期

《高级操作系统》课程期末考试试卷

课程号：_____，开课学院：计算机学院_____

考试试卷：√A 卷、B 卷（请在选定项上打√）

考试形式：闭、开√卷（请在选定项上打√），允许带__任何资料__入场

考试日期：2019 年 06 月 26 日，考试时间：120 分钟

诚信考试，沉着应考，杜绝违纪。

考生姓名：_____学号：_____所属院系：_____

总 分	
评卷人	

Instructions: each question has exactly one correct answer. Please fill in your answers in the table below. GRADING IS BASED ON THE TABLE, NOT what you write on the questions.

1	2	3	4	5	6	7	8	9	10
C	**B**	**B**	**B**	**C**	**B**	**A**	**B**	**B**	**C**
11	12	13	14	15	16	17	18	19	20
B	**D**	**A**	**B**	**C**	**A**	**C**	**D**	**B**	**B**
21	22	23	24	25	26	27	28	29	30
B	**A**	**B**	**A**	**A**	**B**	**A**	**A**	**B**	**D**
31	32	33	34	35	36	37	38	39	40
A	**B**	**D**	**B**	**A**	**A**	**B**	**C**	**B**	**C**
41	42	43	44	45	46	47	48	49	50
F	**B**	**C**	**D**	**B**	**B**	**A**	**C**	**B**	**D**

1. What is Moore’s Law?

A. Number of CPU cores on the processor chip doubles every 18 to 24 months

B. Processor chip clock frequency doubles every 18 to 24 months

C. Number of transistors on the processor chip doubles every 18 to 24 months

D. Size of in-chip cache doubles every 18 to 24 months

ANS: _____

C

2. What is the use of the Memory Management Unit (MMU)?

A. To support virtual memory by mapping from physical memory addresses to virtual memory addresses

B. To support virtual memory by mapping from virtual memory addresses to physical memory addresses

C. To support memory allocation operations (malloc() in C or new() in C++)

D. All of the above

E. None of the above

ANS: _____

B

3. Cache coherence protocols are used to:

A. lock cache lines so they are not pushed out to memory

B. keep data consistent across multiple private caches on a multicore processor

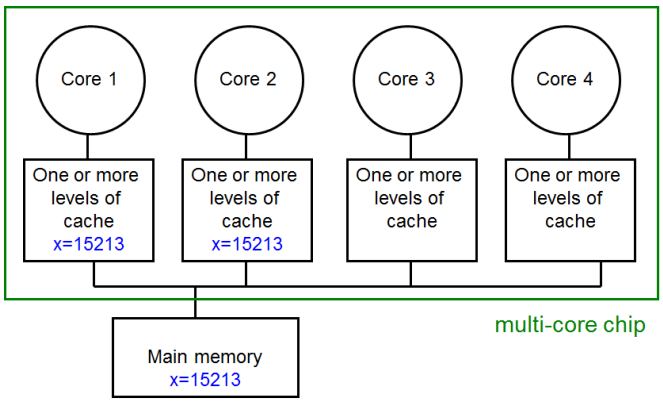
C. implement virtual memory on a multicore processor using the Memory Management Unit (MMU)

D. perform cache partitioning to give each application its own private cache space and avoid cache contention on a multicore processor.

ANS: _____

B

4. In the following multicore processor with *invalidation-based* cache coherence protocol, if Core 3 executes the write operation “x=83”, what happens to value of the x variable in Core 1 and Core 2’s local caches?



A. They stay the same (x=15213)

B. They are both invalidated

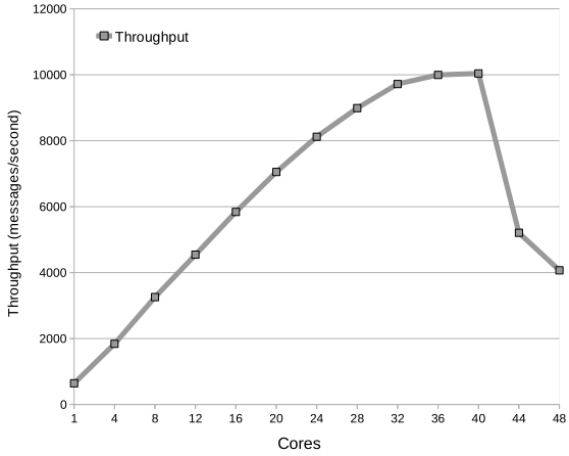
C. They are both updated to the new value （x=83）

D. In Core 1, x stays the same (x=15213); in Core 2, x=83

E. In Core 2, x stays the same (x=15213); in Core 1, x=83

ANS: _____
B

5. In [Boyd-Wickizer10] “An Analysis of Linux Scalability to Many Cores”, what caused the scalability collapse when the number of CPU cores exceeds 40?



A. Synchronization overhead due to shared data protected by spinlocks

B. Increased cache coherence traffic on the interconnect

C. All of the above

D. None of the above

ANS: _____
C

6. In [Boyd-Wickizer10] “An Analysis of Linux Scalability to Many Cores”, what is the general approach to improving scalability with a large number of cores?

A. Rewrite the applications to have better parallelism

B. Reduce access to global shared data by adding per-core non-shared data structures in the OS

C. Adding more cores to improve performance

D. All of the above

E. None of the above

ANS: _____
B

7. The computation model of GPU (Graphics Processing Unit) is:

A. SIMT (Single instruction, multiple threads)

B. MIMD (Multiple instructions, multiple data)

C. SISD (Single instruction, single data)

D. MISD (Multiple instruction, single data)

ANS: _____
A

8. The computation model of a NUMA multicore CPU is:

A. SIMT (Single instruction, multiple threads)

B. MIMD (Multiple instructions, multiple data)

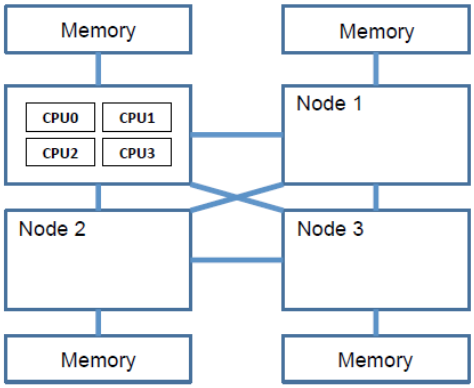
C. SISD (Single instruction, single data)

D. MISD (Multiple instruction, single data)

ANS: _____

B

9. Is the following architecture NUMA (Non-Uniform Memory Access) or UMA (Uniform Memory Access)?



A. UMA

B. NUMA

C. Both

D. Neither

ANS: _____

B

10. Which of the following is NOT a NUMA (Non-Uniform Memory Access) architecture?

A. The 48-core AMD machine used in [Boyd-Wickizer10] “An Analysis of Linux Scalability to Many Cores”

B. The 16-core AMD Opteron system used in [Blagodurov11] “A Case for NUMA-aware Contention Management on Multicore Systems”

C. The dual-core ARM processor used in smart phones

ANS: _____

C

11. In [Clements13] “The Scalable Commutativity Rule: Designing Scalable Software for Multicore Processors.”, what does it mean that a software system is “scalable”?

A. System performance stays constant with increasing number of cores on a multicore processor.

B. System performance increases linearly with increasing number of cores on a multicore processor.

C. System performance deteriorates with increasing number of cores on a multicore processor.

D. System performance is independent of the underlying hardware platform.

ANS: _____

B

12. In [Gaud14] “Large Pages May Be Harmful on NUMA Systems”, large pages are harmful to system performance for what reasons?

A. Hot pages accessed by multiple nodes concentrated in the physical memory of one node

B. Page-level false sharing

C. NUMA (Non-Uniform Memory Access) architecture

D. All of the above

E. None of the above

ANS: _____

D

13. A GPU typically has larger register file size than L1 or L2 cache size.

A. True

B. False

ANS: _____

A

14. Which of the following figure depicts the typical floorplan of a GPU?

A. The left one

B. The right one

C. Neither figure

D. I don’t know, and I don’t care

ANS: _____

B

15. Consider a CUDA program with 3 thread blocks, indexed 0, 1, 2, each including 256 threads. The thread with thread index 700 belong to which thread block?

A. Thread block 0

B. Thread block 1

C. Thread block 2

D. Can be any one of the thread blocks, depending on runtime scheduler.

ANS: _____

C

16. The CUDA function declaration *__global__ void KernelFunc()* means that

A. It is executed on the GPU (device), callable from the CPU (host)

B. It is executed on the GPU (device), callable from the GPU (device)

C. It is executed on the CPU (host), callable from the CPU (host)

D. It is executed on the CPU (host), callable from the GPU (device)

ANS: _____

A

17. Consider a vector addition program, where 2 integer vectors a and b are added element-wise, and assigned to integer vector c:

#define N 10

int a[N], b[N], c[N]

Suppose each integer is 32 bits (4 Bytes). What is the total amount of data transferred between CPU and GPU?

A. 40 Bytes

B. 80 Bytes

C. 120 Bytes

D. 160 Bytes

ANS: _____

C

18. Which of the following is NOT one of the popular programming languages for GPU?

A. CUDA

B. OpenCL

C. OpenGL

D. C#

E. DirectX

ANS: _____

D

19. In [Bhatotia12] “Shredder: GPU-Accelerated Incremental Storage and Computation”, how did the authors address the communication bottleneck of PCIe bus between CPU and GPU?

A. Adopting the integrated GPU architecture to eliminate the PCIe bus

B. Adopting the asynchronous execution model that overlaps CPU-GPU memory transfer phase and GPU computation phase

C. Using OpenCL instead of CUDA to write GPU programs

D. All of the above

ANS: _____

B

20. In [Go17] “APUNet: Revitalizing GPU as Packet Processing Accelerator”, the authors addressed

A. Discrete GPU architecture

B. Integrated GPU architecture

C. All of the above

D. None of the above

ANS: _____

B

21. In [Rossbach11] “PTask: Operating System Abstractions To Manage GPUs as Compute Devices”, what is the problem with the following CUDA program?

```
matrix gemm(A, B) {
matrix res = new matrix();
copyToDevice(A);
copyToDevice(B);
invokeGPU(gemm_kernel, A, B, res);
copyFromDevice(res);
return res;
}
matrix modularSlowAxBxC(A, B, C) {
matrix AxB = gemm(A, B);
matrix AxBxC = gemm(AxB, C);
return AxBxC;
}
```

A. This program is not modular from a software engineering perspective, hence not easily reused.

B. The program is not efficient, since intermediate result (A × B) is copied back from GPU to CPU and back to GPU unnecessarily.

C. The program is not efficient, since there are not enough threads to fully utilize the GPU

D. The program is too large to fit in the GPU on-chip cache.

ANS: _____

B

22. In [Rossbach11] “PTask: Operating System Abstractions To Manage GPUs as Compute Devices”, what is the problem with the following CUDA program?

```
matrix gemm(A, B) {
matrix res = new matrix();
copyToDevice(A);
copyToDevice(B);
invokeGPU(gemm_kernel, A, B, res);
copyFromDevice(res);
return res;
}
matrix nonmodularFastAxBxC(A, B, C) {
matrix intermed = new matrix();
matrix res = new matrix();
copyToDevice(A);
copyToDevice(B);
copyToDevice(C);
invokeGPU(gemm_kernel, A, B, intermed);
invokeGPU(gemm_kernel, intermed, C, res);
copyFromDevice(res);
return res;
}
```

A. This program is not modular from a software engineering perspective, hence not easily reused.

B. The program is not efficient, since intermediate result (A × B) is copied back from GPU to CPU and back to GPU unnecessarily.

C. The program is not efficient, since there are not enough threads to fully utilize the GPU

D. The program is too large to fit in the GPU on-chip cache.

ANS: _____

A

23. What is the purpose of the “datablock” data structure in PTask[Rossbach11]?

A. To act as a communication buffer for PCIe data transfers between GPU and GPU

B. To track buffer validity per memory space on CPU and GPU to avoid unnecessary copies.

C. To give the GPU more cache space and improve its performance

D. To give the CPU more cache space and improve its performance

ANS: _____

B

24. The main purpose of TimeGraph ([Kato11]) is to:

A. Improve real-time predictability of GPUs in multitasking environments

B. Design the next generation GPU architecture for NVidia

C. Design a high-performance simulator for GPGPU computing

D. Design a high-performance compiler for CUDA programs

E. Design a high-level high-productivity programming language for GPUs.

ANS: _____

A

25. True or false: in TimeGraph ([Kato11]), the Posterior Enforcement (PE) Policy may cause some GPU task to have negative execution budget.

A. True

B. False

ANS: _____

A

26. In TimeGraph ([Kato11]), which policy requires runtime online prediction of a GPU program’s execution time?.

A. Posterior Enforcement (PE) Policy

B. Apriori Enforcement (AE) Policy

C. High Throughput (HT) Policy

D. Predictable Response Time (PRT) Policy

ANS: _____

B

27. The purpose of Data Swapping in GDev ([Kato12] “Gdev: First-Class GPU Resource

Management in the Operating System”) is to:

A. Swap memory pages between CPU(host) memory and GPU(device) memory to give more memory space to GPU tasks
B. Swap memory pages between CPU memory and GPU memory to give more memory space to CPU tasks
C. Swap data between CPU memory and hard disk to give more memory space to CPU tasks
D. Swap data between GPU memory hard disk to to give more memory space to GPU tasks

ANS: _____

A

28. Which of the following describes the Scalable Commutativity Rule in [Clements13] “The Scalable Commutativity Rule: Designing Scalable Software for Multicore Processors.”?

A. If interface operations commute, then they can be implemented in a way that scales
B. If interface operations commute, then their implementation must be scalable.
C. If interface operations commute, then their implementation must be not scalable.
D. If interface operations commute, then their implementation must be deadlock-free.
E. If interface operations commute, then their implementation must be livelock-free..

ANS: _____

A

29. In [Kim14] “GPUnet: Networking Abstractions for GPU Programs”, the authors implemented the TCP/IP stack on GPU

A. True
B. False

ANS: _____

B

30. In [Kim14] “GPUnet: Networking Abstractions for GPU Programs”, the dataflow of a GPU-accelerated server with GPUnet is

A. NIC (Network Interface Card) → CPU memory → GPU memory
B. NIC → GPU memory → CPU memory
C. NIC → CPU memory
D. NIC → GPU memory

ANS: _____

D

31. The dataflow of a traditional GPU-accelerated server (without GPUnet) is:

A. NIC (Network Interface Card) → CPU memory → GPU memory

B. NIC → GPU memory → CPU memory

C. NIC → CPU memory

D. NIC → GPU memory

ANS: _____

A

32. In [Silberstein14] “Operating System Services for High Throughput Processors”, GPUfs is designed to

A. Allow CPU to issue commands to open/read/write files on the persistent storage system attached to the GPU

B. Allow GPU to issue commands to open/read/write files on the persistent storage system attached to the CPU

C. Allow GPU to issue commands to open/read/write files on the persistent storage system attached to the GPU

D. All of the above

E. None of the above

ANS: _____

B

33. In [Silberstein14] “Operating System Services for High Throughput Processors”, the authors advocate viewing GPU as

A. Co-processor to CPU

B. Slave processor to CPU

C. Master processor that controls the CPU

D. Peer-processor to CPU

ANS: _____

D

34. In [Silberstein14] “Operating System Services for High Throughput Processors”, what is the reason for adopting a weak data consistency model, i.e., an updated file needs to be closed or fsync’ed on GPU before the CPU can see the updates?

A. To provide a more programmer-friendly API

B. To reduce CPU-GPU communication and synchronization overhead

C. To reduce the effect of weak memory consistency models

D. All of the above

E. None of the above

ANS: _____

B

35. In [Silberstein14] “Operating System Services for High Throughput Processors”, the RPC queue is located in

A. The CPU memory

B. The GPU memory

C. The persistent storage

D. The GPUfs distributed buffer cache

ANS: _____

A

36. In [Kato11] “TimeGraph: GPU Scheduling for Real-Time Multi-Tasking Environments”, the authors implemented their algorithms in an open-source GPU driver

A. True

C. False

ANS: _____

A

37. In [Gupta11] “Pegasus: Coordinated Scheduling for Virtualized Accelerator-based Systems”, the authors implemented their algorithms in an open-source GPU driver

A. True

B. False

ANS: _____

B

38. In [Gupta11] “Pegasus: Coordinated Scheduling for Virtualized Accelerator-based Systems”, the accelerator (GPU) ready queues are located in

A. Each VM

B. The XEN hypervisor

C. XEN Dom0

D. None of the above

ANS: _____

C

39. In [Gupta11] “Pegasus: Coordinated Scheduling for Virtualized Accelerator-based Systems”, the CPU ready queues are located in

A. Each VM

B. The XEN hypervisor

C. XEN Dom0

D. None of the above

ANS: _____

B

40. In [Gupta11] “Pegasus: Coordinated Scheduling for Virtualized Accelerator-based Systems”, each aVPU (accelerator VCPU) executes on

A. CPU

B. GPU

C. Both CPU and GPU

D. Neither CPU nor GPU

ANS: _____

C

41. In [Gupta11] “Pegasus: Coordinated Scheduling for Virtualized Accelerator-based Systems”, which scheduling policy has the best performance?

A. AccCredit (AccC)

B. XenCredit (XC)

C. SLA feedback based (SLAF)

D. Augmented Credit based (AugC)

E. Coscheduled (CoSched)

F. None of the above, since it depends on different system goals and different application characteristics

ANS: _____

F

42. In [Yoon12] “AppScope: Application Energy Metering Framework for Android Smartphone Using Kernel Activity Monitoring”, what machine learning technique is used for building the device power model?

A. Classification

B. Linear Regression

C. Nonlinear Regression

D. Clustering

E. Dimentionality reduction

ANS: _____

B

43. In [Yoon12] “AppScope: Application Energy Metering Framework for Android Smartphone Using Kernel Activity Monitoring”, what mechanisms are used to collect hardware component

usage statistics?

A. Linux kprobes

B. Android Binder IPC

C. All of the above

D. None of the above

ANS: _____

C

44. In [Yoon12] "AppScope: Application Energy Metering Framework for Android Smartphone Using Kernel Activity Monitoring", which of the following components are not supported by AppScope?

A. CPU

B. 3G network interface

C. WiFi network interface

D. GPU

E. LCD display

F. GPS

ANS: _____

D

45. For Differential Privacy: A summary statistic function $A()$ gives ϵ-differential privacy if for all pairs of datasets S, S' differing in only one element, and all choices of the test set Q: $\Pr(A(S) \in Q) \leq (1+\epsilon)\Pr(A(S') \in Q)$, larger value of ϵ implies

A. Stronger privacy protection

B. Weaker privacy protection

C. I don't know, and I don't care

ANS: _____

B

46. For Differential Privacy: adding more noise to the summary statistic function $A()$ will lead to

A. Larger value of ϵ

B. Smaller value of ϵ

C. It does not affect value of ϵ

ANS: _____

B

47. In [Roy10] "Airavat: Security and Privacy for MapReduce", the authors assume

A. untrusted mapper + trusted reducer

B. untrusted mapper + untrusted reducer

C. trusted mapper + untrusted reducer

D. trusted mapper + trusted reducer

ANS: _____

A

48. In [Roy10] "Airavat: Security and Privacy for MapReduce", what prevents a malicious mapper from directly sending Peter's private data over the network to a third party?

A. User authentication mechanism in SELinux

B. Differential Privacy mechanism

C. Mandatory access control mechanism in SELinux

D. All of the above

ANS: _____

C

49. In [Roy10] "Airavat: Security and Privacy for MapReduce", the Differential Privacy mechanism is implemented in

A. The mapper

B. The reducer

C. SELinux kernel

D. None of the above

ANS: _____

B

50. In [Roy10] "Airavat: Security and Privacy for MapReduce", what happens if a malicious mapper outputs value, say 100,000, outside the specified range [0, M], say [0,100]?

A. This will never happen, since the range [0, 100] is a safe bound obtained offline

B. The output value of 100,000 is sent to the reducer as is

C. The output value is replaced by a value inside [0, 100], and the user of Map-Reduce is notified

D. The output value is replaced by a value inside [0, 100], and the user of Map-Reduce is not notified

E. The system throws an exception

ANS: _____

D