CME 2003
Digital Logic

SYNCHRONOUS COUNTER DESIGN

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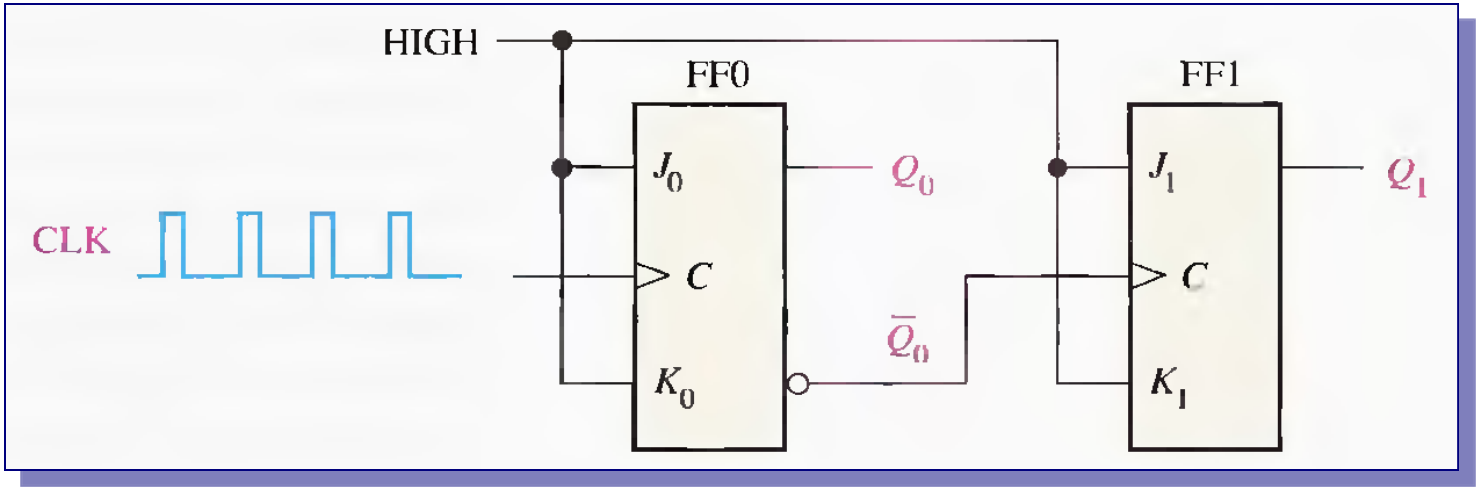
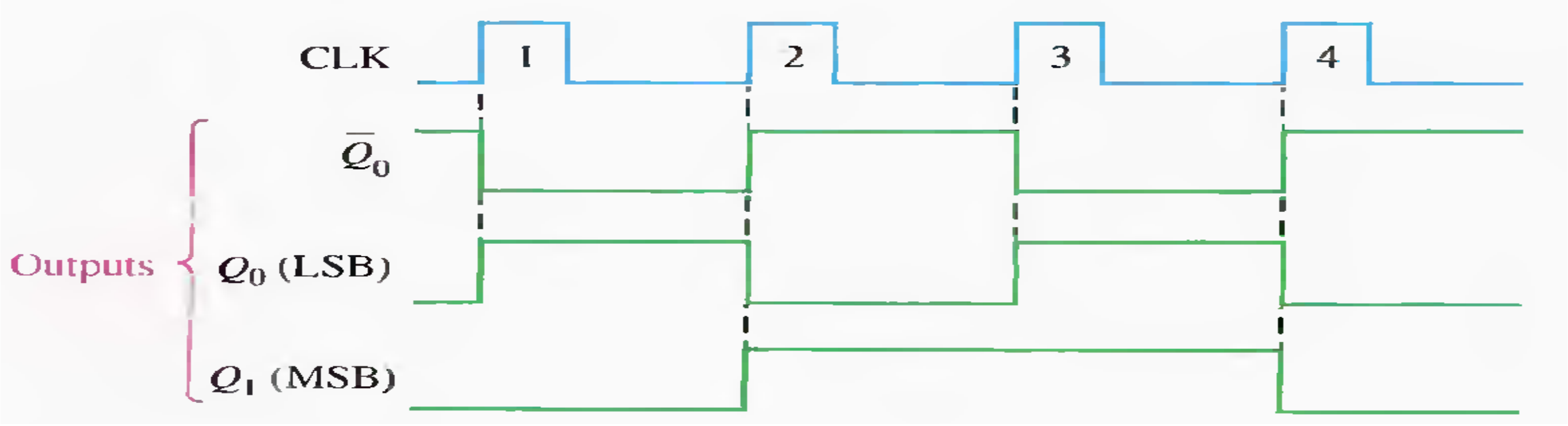
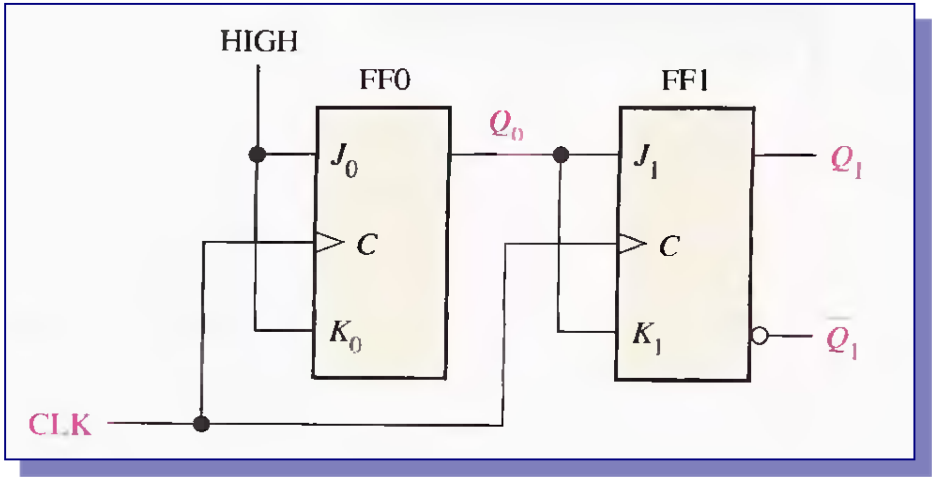
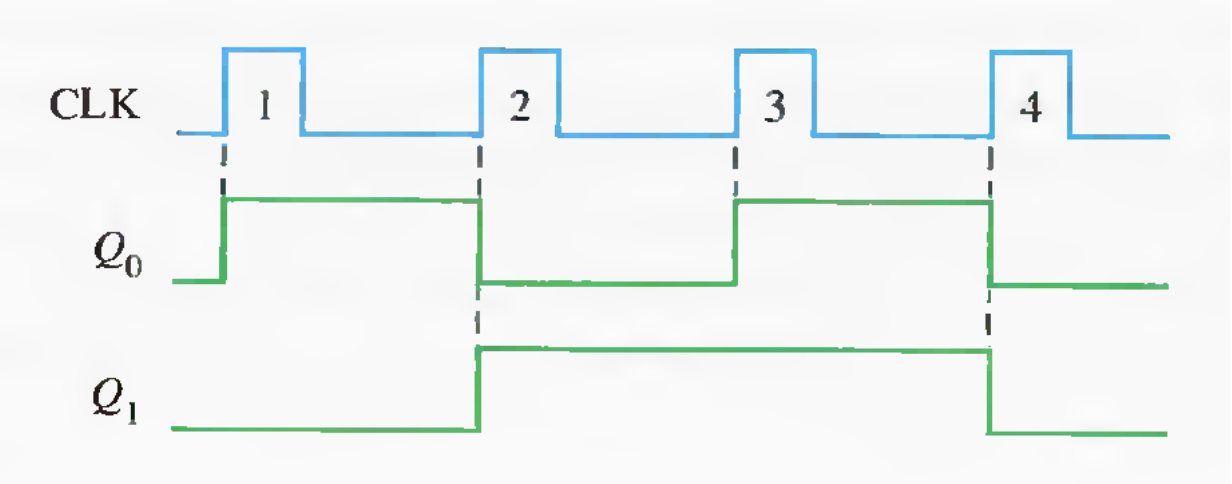
2-Bit Asynchronous Binary Counter



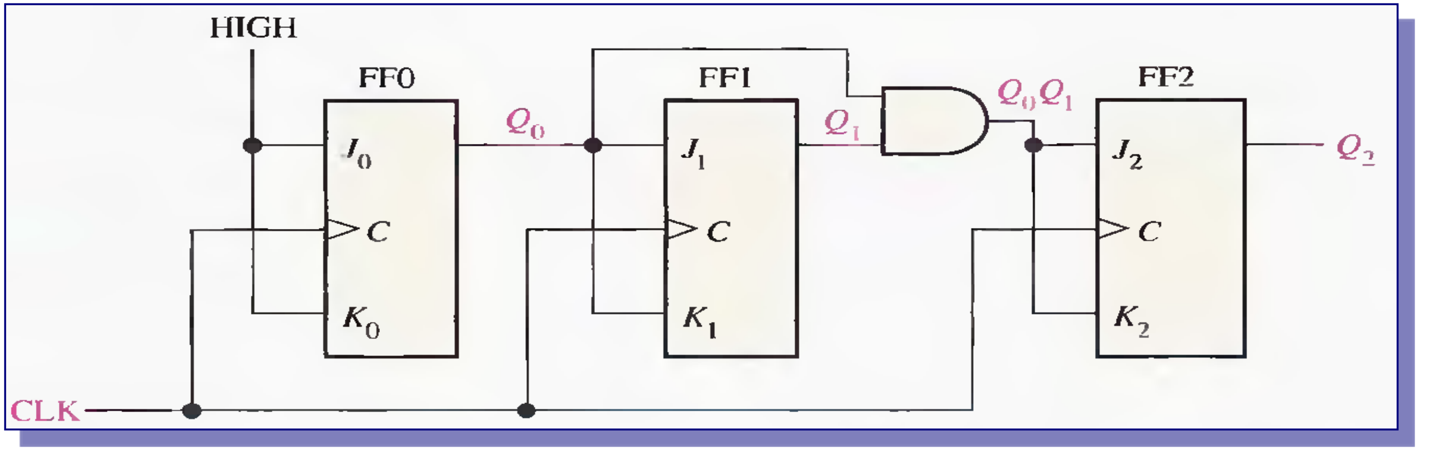


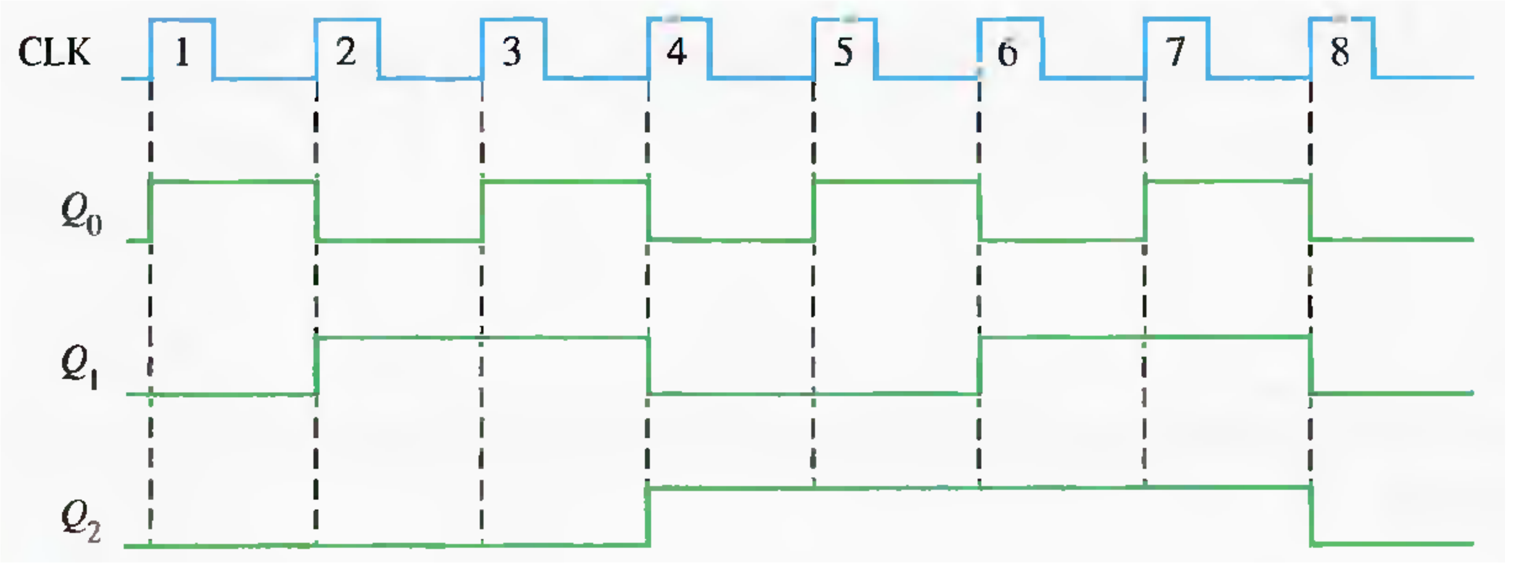
2-Bit Synchronous Binary Counter



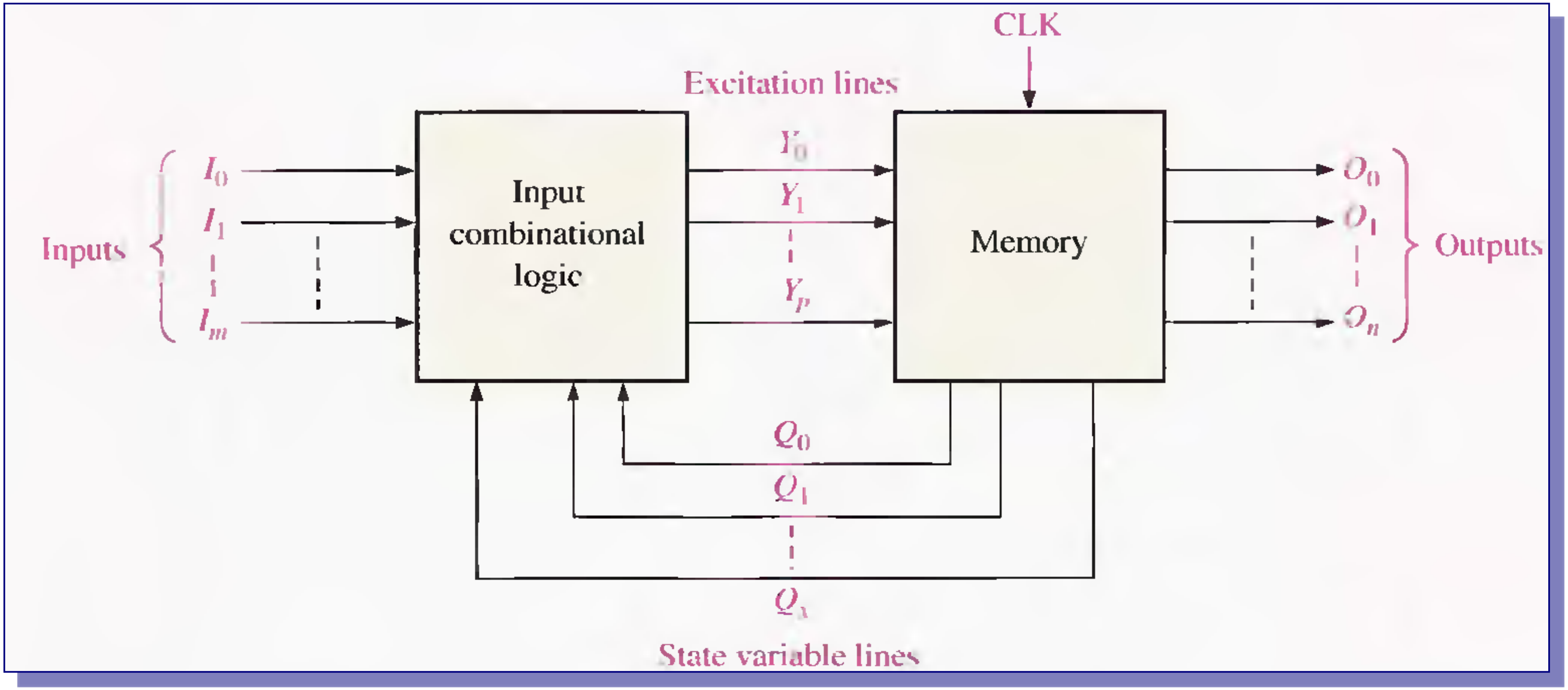


3-Bit Synchronous Binary Counter



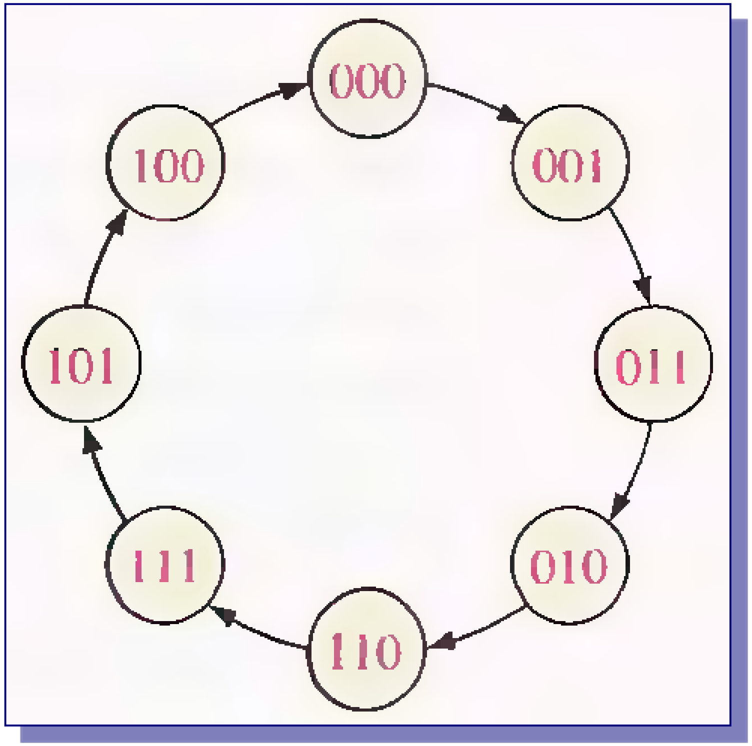


Design of Synchronous Counters



Step 1: State Diagram

- A *state diagram* shows the progression of states through which the counter advances when it is clocked.
- *Example:* State diagram for a 3-bit Gray code counter.



Step 2: Next-State Table

- a *next-state table* lists each state of the counter (present state) along with the corresponding next state.
- the *next state* is the state that the counter goes to from its present State upon application of a clock pulse

Next State Table for 3-bit Gray Code

PRESENT STATE			NEXT STATE		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
0	0	0	0	0	1
0	0	1	0	1	1
0	1	1	0	1	0
0	1	0	1	1	0
1	1	0	1	1	1
1	1	1	1	0	1
1	0	1	1	0	0
1	0	0	0	0	0

Step 3: Flip-Flop Transition Table

- All possible output transitions are listed by showing the Q output of the flip-flop going from present states to next states.
- Q_N is the present state of the flip-flop (before d clock pulse) and Q_{N+1} is the next state (after a clock pulse).
- For each output transition. the J and K inputs that will cause the transition to occur are listed.
- An X indicates a "don't care" (the input can be either a 1 or a 0).

Transition table for a J-K flip-flop

OUTPUT TRANSITIONS			FLIP-FLOP INPUTS	
Q_N		Q_{N+1}	J	K
0	$\longrightarrow$	0	0	X
0	$\longrightarrow$	1	1	X
1	$\longrightarrow$	0	X	1
1	$\longrightarrow$	1	X	0

Q_N: present state

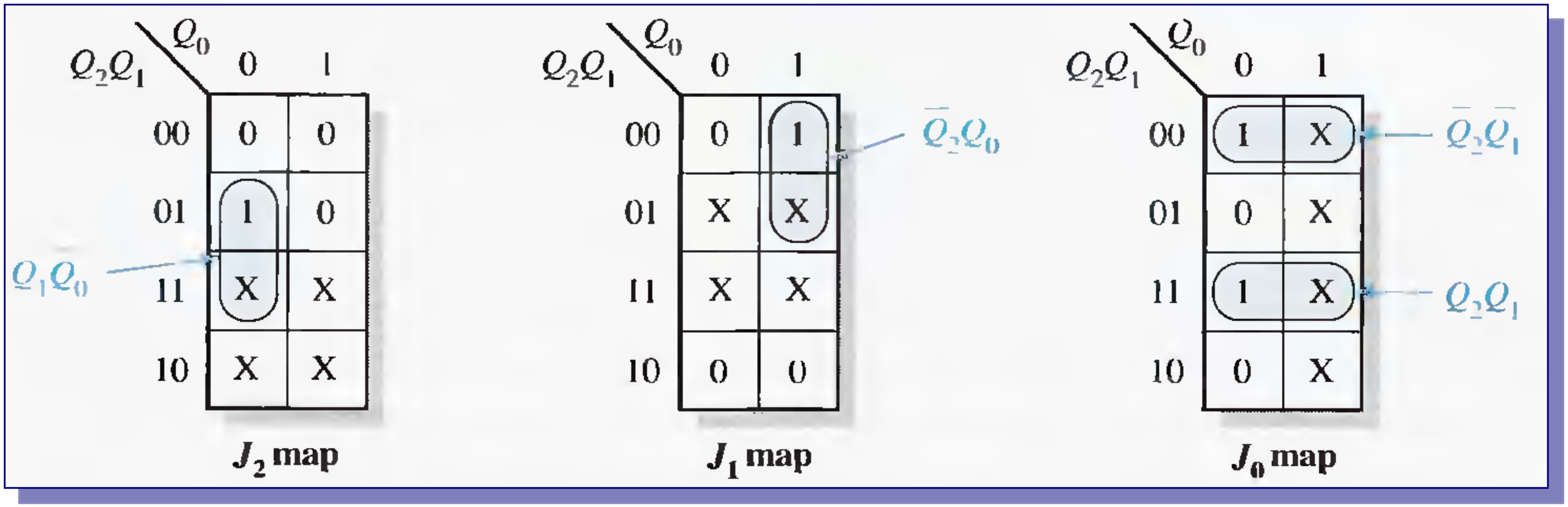
Q_{N+1}: next state

X: "don't care"

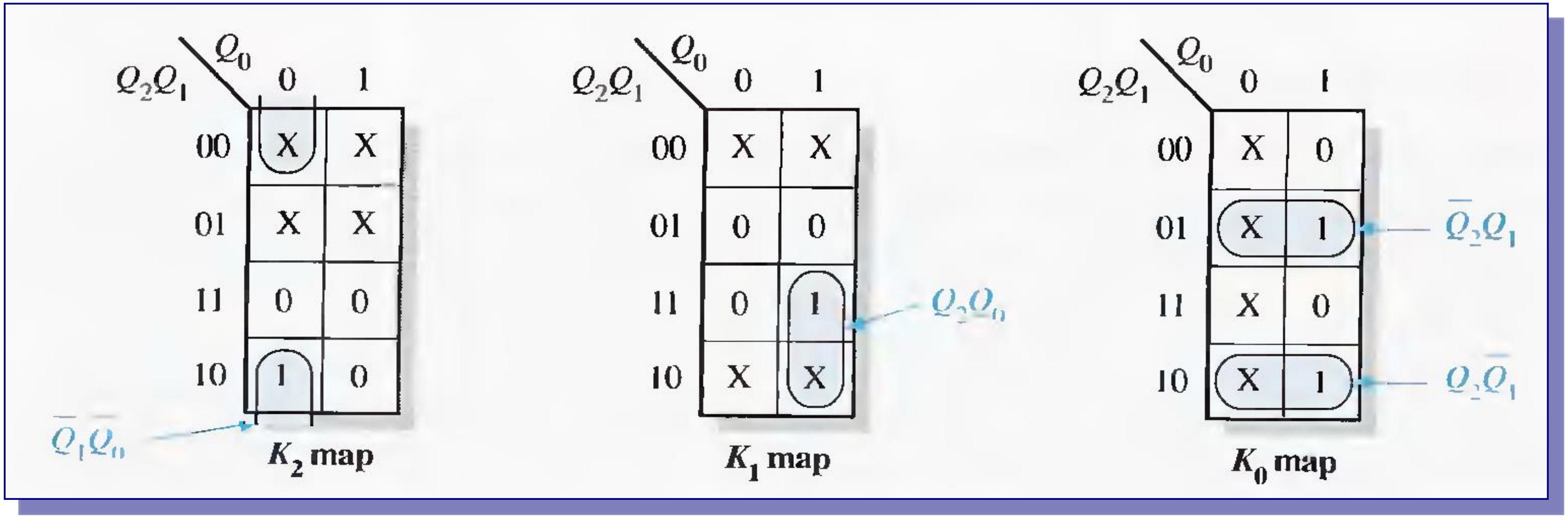
Step 4: Karnaugh Maps

- Karnaugh maps can be used to determine the logic required for the J and K inputs of each flip-flop in the counter.
- There is a Karnaugh map for the J input and a Kamaugh map for the K input of each flip-flop.
- each cell in a Kamaugh map represents one of the present states in the counter sequence.

Karnaugh maps for present-state J input



Karnaugh maps for present-state K input



Step 5: Logic Expressions for Flip-Flop Inputs

- the following expressions for the J and K inputs of each flip-flop obtained from the Karnaugh maps

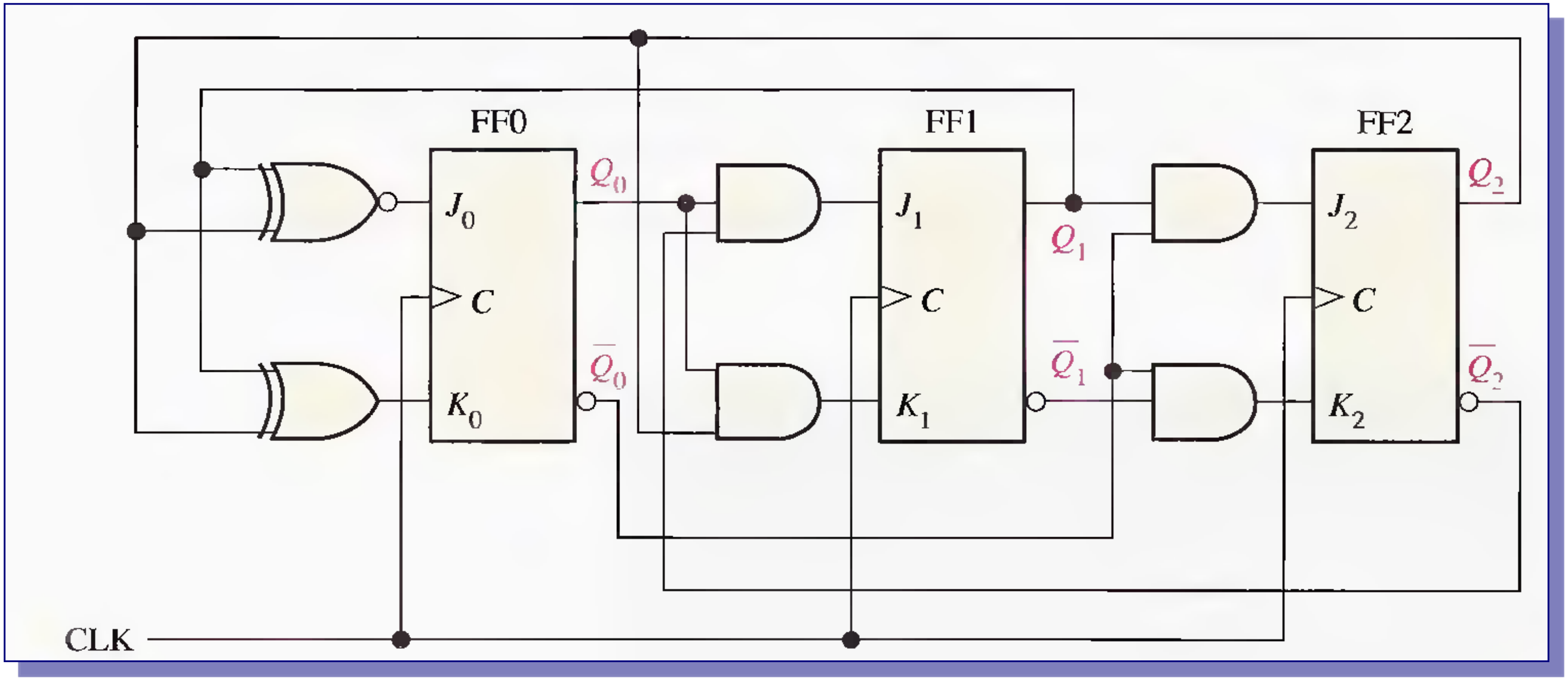
$$J_0 = Q_2 Q_1 + \overline{Q}_2 \overline{Q}_1 = \overline{Q_2 \oplus Q_1}$$

$$K_0 = Q_2 \overline{Q}_1 + \overline{Q}_2 Q_1 = Q_2 \oplus Q_1$$

$$J_1 = \overline{Q}_2 Q_0 \qquad J_2 = Q_1 \overline{Q}_0$$

$$K_1 = Q_2 Q_0 \qquad K_2 = \overline{Q}_1 \overline{Q}_0$$

Step 6: Counter Implementation



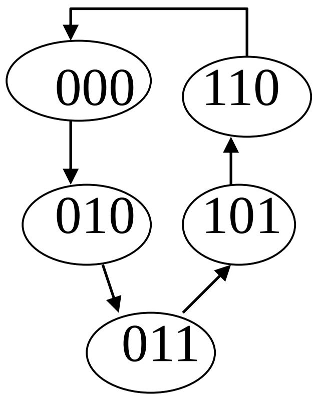
A summary of steps used in the design of a synchronous counter.

1. Specify the counter sequence and draw a state diagram.
2. Derive a next-state table from the state diagram.
3. Develop a transition table showing the flip-flop inputs required for each transition. The transition table is always the same for a given type of flip-flop.
4. Transfer the J and K states from the transition table to Karnaugh maps. There is a Karnaugh map for each input of each flip-flop.
5. Group the Karnaugh map cells to generate and derive the logic expression for each flip-flop input.
6. implement the expressions with combinational logic. and combine with the flip- flops to create the counter.

EXAMPLE

Synchronous Counter Implementation Using J-K FFs

State Transition Diagram



State Transition Table

Present State C	B	A	Next State C^+	B^+	A^+
0	0	0	0	1	0
0	0	1	x	x	x
0	1	0	0	1	1
0	1	1	1	0	1
1	0	0	x	x	x
1	0	1	1	1	0
1	1	0	0	0	0
1	1	1	x	x	x

State Transition Table and Remapped Next-State Functions

Present State C	B	A	Next State C^+	B^+	A^+	Remapped Next State JC	KC	JB	KB	JA	KA
0	0	0	0	1	0	0	x	1	x	0	x
0	0	1	x	x	x	x	x	x	x	x	x
0	1	0	0	1	1	0	x	x	0	1	x
0	1	1	1	0	1	1	x	x	1	x	0
1	0	0	x	x	x	x	x	x	x	x	x
1	0	1	1	1	0	x	0	1	x	x	1
1	1	0	0	0	0	x	1	x	1	0	x
1	1	1	x	x	x	x	x	x	x	x	x

J-K Flip-Flop Excitation Table

Q	Q^+	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

$$Q^+ = J\overline{Q} + \overline{K}Q$$

Next State Functions

$$J_C = A \qquad K_C = \overline{A}$$

$$J_B = 1 \qquad K_B = A + C$$

$$J_A = B\overline{C} \qquad K_A = C$$

Remapped K-Maps for J-K Implementation.

J_C

A \ CB	00	01	11	10
0	0	0	x	x
1	x	1	x	x

K_C

A \ CB	00	01	11	10
0	x	x	1	x
1	x	x	x	0

J_B

A \ CB	00	01	11	10
0	1	x	x	x
1	x	x	x	1

K_B

A \ CB	00	01	11	10
0	x	0	1	x
1	x	1	x	x

J_A

A \ CB	00	01	11	10
0	0	1	0	x
1	x	x	x	x

K_A

A \ CB	00	01	11	10
0	x	x	x	x
1	x	0	x	1

J-K Flip-Flop Implementation of 3 Bit Counter