CME2003 Logic Design
Experiment 4

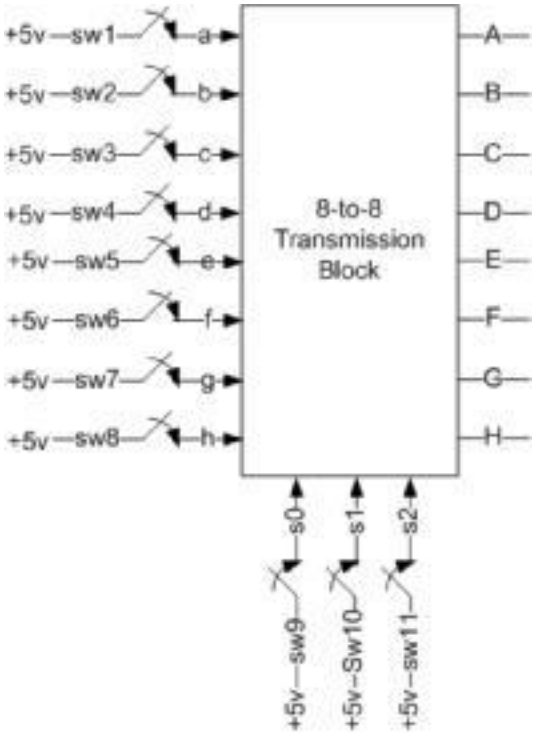
1.The following function is given. Implement it using a 3x8 multiplexer.

$$F(A,B,C,D) = \sum(1,3,4,7,12,13)$$

$$d(A,B,C,D) = \sum(0,2,5,6,8,11)$$

2. Design **8-bit parallel input, serial output transmission circuit**. The block diagram of circuit is shown below. 8-bit *abcdefgh* input will be set by switches connected to 5V in one position and to ground in other position. 8-to-8 Transmission Block consists of a MUX and a DEMUX. *ABCDEFGH* output of the Transmission Block will be as follows according to $S_2S_1S_0$ connected to switches:

S_2	S_1	S_0	A	B	C	D	E	F	G	H
0	0	0	**a**	1	1	1	1	1	1	1
0	0	1	1	**b**	1	1	1	1	1	1
0	1	0	1	1	**c**	1	1	1	1	1
0	1	1	1	1	1	**d**	1	1	1	1
1	0	0	1	1	1	1	**e**	1	1	1
1	0	1	1	1	1	1	1	**f**	1	1
1	1	0	1	1	1	1	1	1	**g**	1
1	1	1	1	1	1	1	1	1	1	**h**



Preliminary Work

Draw truth tables and logic diagrams of the designs.
Construct and test the designed circuits in MaxPlus II. Bring the logic diagrams and waveforms.
Come with your PreLab report and data sheets of the ICs you used in your designs.
Prepare the PreLab report **individually**.

Equipments

- 74LS138 (DeMultiplexer), 74LS151 (Multiplexer), and other necessary ICs such as OR, AND
- Breadboard
- Connection cables