CME2003 Logic Design
Experiment 2

Preliminary Work

1. Examine function F and
   a. Draw the truth table and Karnaugh map of function F
   b. Use Altera Max+Plus II software to implement logic design of F.
   c. Simulate your circuit and verify that it works correctly using the waveform.

$$F(w, x, y, z) = \sum(0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)$$

2. Design **full adder** circuit using primitive logic gates.
   - Give the truth table and Karnaugh map of the design.
   - Use Altera Max+Plus II software to implement your design.
   - Simulate your circuit and verify that it works correctly using the waveform.

3. Prepare preliminary work report
   The PreLab report should include truth tables, logic diagrams, Karnaugh maps, waveforms and all other preliminary works.

The preliminary work and report are expected from each student **individually**. Bring datasheets of the ICs you need in your design.

Equipments

- AND (IC 7408), OR (IC 7432), NOT (IC 7414), XOR (IC 7486)
- Breadboard
- Connection cables
- Any other equipments necessary for the experiment

Lab Work

1. Simplify the Boolean function F and implement it by using integrated circuits(IC).
2. Implement full adder circuit by using ICs.