Review Questions 3

Combinational Logic and Functions

1 – Use NAND gates, NOR gates or combinations of both to implement the following logic expressions:

(a) X = A'B + CD + (A + B)'[ACD + (BE)']

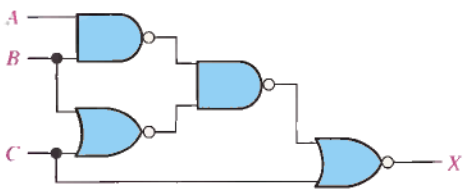
(b) X = ABC'D' + DE'F + (AF)'

(c) X = A'[B + C'(D + E)]

2 - Implement a logic circuit for the following truth table.

A	B	C	X (Output)
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	1	1
1	0	0	0
1	1	1	1
1	1	0	1

3 - Simplify the circuit in the figure as much as possible and verify that the simplified circuit is equivalent to the original by showing that the truth tables are identical.



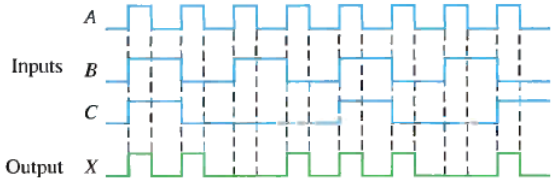
4 – Show how the following expressions can be implemented by using only NOR gates:

a) X = A + B + C' b) X = (A + B)(C + D)

5 - Show how the following expressions can be implemented by using only NAND gates:

a) X = (AB)' + (CD)' b) X = AB(C[(DE)' + (AB)'] + [BCE]')

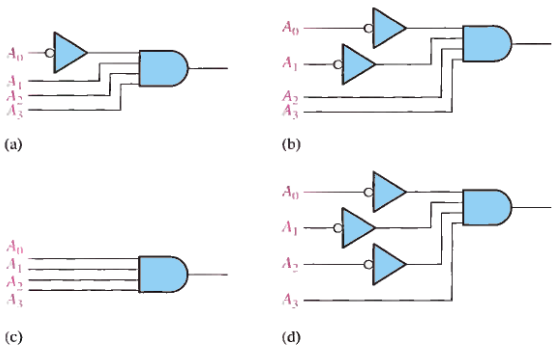
6 - For the input waveforms in the figure. What logic circuit will generate the output waveform shown?



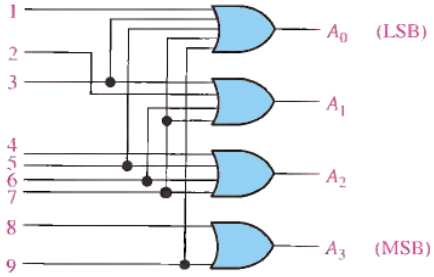
7 - What are the full-adder inputs/outputs for each of the following outputs/inputs:

a) S = 0, C_{out}=0 **b)** S = 1, C_{out}=1 **c)** A=0, B=1, C_{in}=1 **d)** A=1, B=1, C_{in}=1

8 - When a HIGH is on the output of each of the decoding gates in the following figure, what is the binary code appearing on the inputs? The MSB is A_3.



9 - For the decimal-to-BCD encoder logic of following figure, assume that the 9 input and the 3 input are both HIGH. What is the output code? Is it a valid BCD (8421) code?



10 - For the multiplexer in the figure, determine the output for the following input states:

a) D_0 = 0, D_1 = 1, D_2 = 1, D_3 = 0, S_0 =1, S_1 = 0 **b)** D_0 = 0, D_1 = 1, D_2 = 0, D_3 = 1, S_0 =0, S_1 = 1