CME 2003 Logic Design

Experiment 3

Preliminary Work

Design full adder circuit using primitive logic gates. Give the truth table and Karnaugh map of the design.

- Use Altera Max+Plus II software to implement the full adder circuit you have designed.
- Simulate your circuit and verify that it works correctly using the waveform.

This work is expected from each student individually.

Lab Work

- Implement your circuit design in the lab.

Requirements

- AND Gate (IC 7408)
- XOR Gate (IC 7486
- OR Gate (IC 7432)
- Breadboard
- Connection cables.