CME2003 Logic Design
Experiment 6

1. Frequency Divider Circuit

a. Preliminary Work

Draw truth tables, Karnaugh maps and logic diagrams of the design. Construct and test the designed circuits in MaxPlus II. Bring logic diagrams and waveforms.

b. Equipments

- Experiment kit (Y0016 – 003D) which will be given you at lab.
- Connection cables.

c. Experiment

Build a frequency divider, divide-by-2 and divide-by-4 circuit using

1. D Flip Flops
2. JK Flip Flops

You will use experiment kit (Y0016 – 003D) for the flip flops. You should build 4 circuits in total.

2. 3-bit Synchronous Counter

a. Preliminary Work

Implement your design using **VHDL** and test it in MaxPlus II. Write your code and paste the waveforms in your prelab document.

b. Equipments

- JK Flip Flops (74LS73 or 74LS76) and other necessary ICs such as Inverter, OR, AND
- Breadboard
- Connection cables

c. Experiment

Design a 3-bit synchronous counter using logic gates and JK flip flops. The circuit should output your number without repetition in MOD 8. For example, for a student number 1900510082 the circuit should output 1,0,5,2 in succession. (MOD 8 produces 1,1,0,0,5,1,0,0,0,2 and without repetition it counts 1,0,5,2)

Notes

- Come with your PreLab report and data sheets of the ICs you used in your designs.
- Prepare the PreLab report **individually**.
- You **will not be allowed** to the lab without your individual pre-lab document