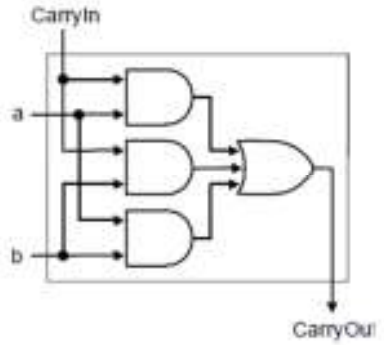
Problem (4) B.30, Answer C

Assumption:

1. a delay of gate is proportion to the number of fan-ins (inputs): **k**T (k=fanin)
2. 1bit full adder: CarryOut = 2T + 3T = 5T, Sum=3T (a xor b xor C)
3. Carry-Lookahead Unit implementation: a sum of products (**same as the textbook and lecture slides**)



a. 64bit ripple carry adder: c64=320T (5T×64), Sum_{63}= 318T (c63+3T)

b. 64bit ripple carry adder using **4 bit carry-lookahead adder**: c64 = 162T, Sum=163T

CLA4bit$_{3,0}$: c4 = 12T, $Sum_{3,0}$ = max(Sum3, Sum2, Sum1, Sum0) = max (13T, 11T, 9T, 3T) = 13T
The details of delay calculations follow:
The delay of output = gate delay + the max delay among input signals

pi = a * b = 2T, gi = a xor b = 2T from each one bit adder

Carry-lookahead unit (CLU) generates c1, c2, c3, c4
c1 = g0+p0*c0 = 2T(gate delay of 2-input or) + max(g0, 2T(gate delay of 2-input and) + max(p0,c0))
= 2T + max(2T, 2T+max(2T, 0T)) = 2T+ max(2T, 4T) = 2T+4T = 6T
c2 = g1 + p1*g0 + p1*p0*c0 = 3T + max (g1, p1*g0, p1*p0*c0) = 3T + max(2T, 2T+2T, 3T+2T) = 3T+5T = 8T
c3 = g2 + p2*g1 + p2*p1*g0 + p2*p1*p0*c0 = 4T + max(g2, p2*g1, p2*p1*g0, p2*p1*p0*c0)
= 4T + max(2T, 2T+2T, 3T+2T, 4T+2T) = 4T+max(2T, 4T, 5T, 6T) = 10T
c4 = g3+ p3*g2 + p3*p2*g1 + p3*p2*p1*g0 + p3*p2*p1*p0*c0
= 5T + max(g3, p3*g2, p3*p2*g1, p3*p2*p1*g0, p3*p2*p1*p0*c0)
= 5T + max(2T, 2T+2T, 3T+2T, 4T+2T, 5T+2T) = 5T+max(2T, 4T, 5T, 6T, 7T) = 12T

Sum = 3T (gate delay of 3-input xor) + max(Ai, Bi, Ci), but Ai and Bi are always 0T.
So, Sum = 3T+ the delay of Ci

Sum0 = 3T+ c0 = 3T+0T = 3T
Sum1 = 3T+ c1 = 3T+6T = 9T
Sum2 = 3T+ c2 = 3T+8T = 11T
Sum3 = 3T+ c3 = 3T+10T = 13T

CLA4bit$_{7,4}$: c8 = 22T, Sum$_{7,4}$ = max(Sum7, Sum6, Sum5, Sum4) = max(23T, 21T, 19T, 15T) = 23T

pi = a * b = 2T, gi = a xor b = 2T from each one bit adder

Carry-lookahead unit (CLU) generates c5, c6, c7, c8
c5 = g4+p4*c4 = 2T + max(2T, 2T+max(p4, **c4**)) = 2T + max(2T, 2T+max(2T, **12T**)) = 2T + 14T = 16T
c6 = g5 + p5*g4 + p5*p4*c4 = 3T + max (g5, p5*g4, p5*p4*c4) = 3T + max(2T, 4T, 3T+max(p5, p4, **c4**))
=3T + max(2T, 4T, 3T+max(2T, 2T, **12T**)) = 3T + max(2T, 4T, 15T) = 3T+15T= 18T
c7 = g6 + p6*g5 + p6*p5*g4 + p6*p5*p4*c4 = 4T + max(g6, p6*g5, p6*p5*g4, p6*p5*p4*c4)
= 4T + max(2T, 4T, 5T, 4T+max(p6, p5, p4, **c4**) = 4T + max(2T, 4T, 5T, 4T+max(2T, 2T, 2T, **12T**))
= 4T + max(2T, 4T, 5T, 16T) = 4T+16T= 20T
c8 = g7+ p7*g6 + p7*p6*g5 + p7*p6*p5*g4 + p7*p6*p5*p4*c4
= 5T + max(g7, p7*g6, p7*p6*g5, p7*p6*p5*g4, p7*p6*p5*p4*c4)
= 5T + max(2T, 4T, 5T, 6T, 5T+max(p7, p6, p5, p4, **c4**))
= 5T+ max(2T, 4T, 5T, 6T, 5T+max(2T, 2T, 2T, 2T, **12T**))
= 5T + max(2T, 4T, 5T, 6T, 17T) = 5T+17T = 22T

Sum4 = 3T+c4 = 3T+12T = 15T
Sum5 = 3T+c5 = 3T+16T = 19T
Sum6 = 3T+c6 = 3T+18T = 21T
Sum7 = 3T+c7 = 3T+20T = 23T

→ The delay time of **pi** and **gi** is overlapped since pi and gi are already available when the c4 arrives at 12T.
This delay overlap is applied to the **rest** of CLAs:
c(i+4) = ci+10T
Sum(i+3, i) = ci + 11T

CLA4bit$_{11,8}$: c12 = c8+10T = 22T+10T = 32T, Sum$_{11,8}$ = c8+11T = 22T+11T = 33T
CLA4bit$_{15,12}$: c16 = c12+10T= 32T+10T= 42T, Sum$_{15,12}$ = c12+11T = 32T+11T= 43T
…
CLA4bit$_{63,60}$: c64 = c60+10T = 152T+10T = 162T, Sum$_{63,60}$ = c60+11T = 152T+11T= 163T

c. 64bit ripple carry adder using **16 bit hierarchical carry-lookahead adder**: c64 = 49T, Sum=58T
HCLA16bit$_{15,0}$: c16=19T, Sum=28T

pi = a * b = 2T, gi = a xor b = 2T from each one bit adder

CLU-1level generates Gi and Pi.
G =g3+ p3*g2 + p3*p2*g1 + p3*p2*p1*g0 = 4T+ max(2T, 4T, 5T, 6T) = 10T
P = p0 * p1 * p2 * p3 = 4T + max(2T, 2T, 2T, 2T) = 6T
G0=G1=G2=G3=10T and P0=P1=P2=P3=6T

CLU-2level generates c4, c8, c12, c16
The notation of CLU-2lev is same as 1-level CLU: gi=Gi, pi=Pi
c4 = g0+p0*c0 =2T+ max(g0, 2T+ max(p0,c0)) = 2T+ max(10T, 2T+6T) = 2T+10T = 12T
c8 = g1 + p1*g0 + p1*p0*c0 = 3T + max (g1, p1*g0, p1*p0*c0) = 3T + max(10T, 12T, 3T+6T) = 3T+12T = 15T
c12 = g2 + p2*g1 + p2*p1*g0 + p2*p1*p0*c0 = 4T + max(g2, p2*g1, p2*p1*g0, p2*p1*p0*c0)

= 4T + max(10T, 12T, 13T, 4T+6T) = 4T+13T = 17T

c16 = g3+ p3*g2 + p3*p2*g1 + p3*p2*p1*g0 + p3*p2*p1*p0*c0

= 5T + max(g3, p3*g2, p3*p2*g1, p3*p2*p1*g0, p3*p2*p1*p0*c0)

= 5T + max(10T, 12T, 13T, 14T, 5T+6T) = 5T+14T = 19T

From solution b:

Sum(i+3, i) = ci + 11T

$CLA4bit_{3,0}$: …

$CLA4bit_{7,4}$: $Sum_{7,4}$ = c4+11T = 12T+11T = 23T

$CLA4bit_{11,8}$:$Sum_{11,8}$ = c8+11T = 15T+11T= 26T

$CLA4bit_{15,12}$: $Sum_{15,12}$ = c12+11T = 17T+11T = 28T

$HCLA16bit_{31,16}$: c32=29T, $Sum_{31,16}$=38T

CLU-2level generates c20, c24, c28, c32

The notation of CLU-2lev is same as 1-level CLU: gi=Gi, pi=Pi, c0=c16 (19T)

c20 = g0+p0*c16 = 2T+ max(g0, 2T+ max(p0,**c0**))= 2T + max(10T, 2T+max(6T, **19T**))

= 2T+ max(10T, max(8T, 21T)) = 2T+21T = 23T

c24 = g1 + p1*g0 + p1*p0*c0 = 3T + max (g1, p1*g0, p1*p0*c0) = 3T + max(10T, 12T, 3T+max(p1, p0, **c0**))

=3T + max(10T, 12T, 3T+max(6T, 6T, **19T**)) = 3T + max(10T, 12T, 22T) = 25T

c28 = g2 + p2*g1 + p2*p1*g0 + p2*p1*p0*c0 = 4T + max(g2, p2*g1, p2*p1*g0, 4T+max(p2,p1,p0,**c0**))

= 4T + max(10T, 12T, 13T, 4T+max(6T, 6T, 6T, **19T**)) = 4T+max(10T, 12T, 13T, 23T) = 4T+23T = 27T

c32 = g3+ p3*g2 + p3*p2*g1 + p3*p2*p1*g0 + p3*p2*p1*p0*c0

= 5T + max(g3, p3*g2, p3*p2*g1, p3*p2*p1*g0, p3*p2*p1*p0*c0)

= 5T + max(10T, 12T, 13T, 14T, 5T+ max(p3, p2, p1, p0, **c0**))

= 5T + max(10T, 12T, 13T, 14T, 5T+ max(6T, 6T, 6T, 6T, **19T**)) = 5T+24T = 29T

$CLA4bit_{19,16}$: $Sum_{19,16}$ = c16+11T = 19T+11T = 30T

$CLA4bit_{23,20}$: $Sum_{23,20}$ = c20+11T = 23T+11T = 34T

$CLA4bit_{27,24}$: $Sum_{27,24}$ = c24+11T = 25T+11T = 36T

$CLA4bit_{31,28}$: $Sum_{31,28}$ = c28+11T = 27T+11T = 38T

→ The delay time of **Pi** and **Gi** is overlapped since Pi and Gi are already available when the c16 arrives at 19T.

This delay overlap is applied to the **rest** of HCLAs:

c(i+16) = ci+10T

Sum(i+15, i) = c(i+12) + 11T = ci + 8T + 11T = ci + 19T

$HCLA16bit_{47,32}$: c48= c32+10T = 29T+10T= 39T, $Sum_{47,32}$ = c32+19T = 29T+19T= 48T

$HCLA16bit_{63,48}$: c64= c48+10T = 39T+10T= 49T, $Sum_{63,48}$ = c48+19T = 39T+19T= 58T

d. 64bit **three-level** carry-lookahead adder: c64=27T, Sum=44T

pi = a * b = 2T, gi = a xor b = 2T from each one bit adder

CLU-1level generates Gi and Pi.
G =g3+ p3*g2 + p3*p2*g1 + p3*p2*p1*g0 = 4T+ max(2T, 4T, 5T, 6T) = 10T
P = p0 * p1 * p2 * p3 = 4T + max(2T, 2T, 2T, 2T) = 6T
G0=G1=G2=G3=10T and P0=P1=P2=P3=6T

CLU-2level generates Gi_2lev and Pi_2lev
G_2lev =G3+ G3*G2 + P3*P2*G1 +P3*P2*P1*G0 = 4T+ max(10T, 12T, 13T, 14T) = 4T+14T= 18T
P_2lev = P0 * P1 * P2 * P3 = 4T + max(6T, 6T, 6T, 6T) = 10T
G0_2lev=G1_2lev=G2_2lev =G3_2lev =18T and P0_2lev =P1_2lev =P2_2lev =P3_2lev =10T

CLU-3lev generates c16, c32, c48, c64
The notation is same as 1-level CLU: **gi=Gi_2lev, pi=Pi_2lev**
c16 = g0+p0*c0 = 2T + max(g0, 2T+ max(p0,c0)) = 2T+max(18T, 2T+max(10T, 0T)) = 2T+18T= 20T
c32 = g1 + p1*g0 + p1*p0*c0 = 3T + max (g1, p1*g0, p1*p0*c0) = 3T + max(18T, 20T, 13T) = 3T+20T = 23T
c48 = g2 + p2*g1 + p2*p1*g0 + p2*p1*p0*c0 = 4T + max(g2, p2*g1, p2*p1*g0, p2*p1*p0*c0)
= 4T + max(18T, 20T, 21T, 14T) = 25T
c64 = g3+ p3*g2 + p3*p2*g1 + p3*p2*p1*g0 + p3*p2*p1*p0*c0
= 5T + max(g3, p3*g2, p3*p2*g1, p3*p2*p1*g0, p3*p2*p1*p0*c0)
= 5T + max(18T, 20T, 21T, 22T, 15T) = 5T+22T = 27T

From solution c:
Sum(i+15, i) = ci + 19T

HCLA16bit$_{15,0}$: …
HCLA16bit$_{31,16}$: Sum$_{31,16}$= c16+19T = 20T+19T= 39T
HCLA16bit$_{47,32}$: Sum$_{47,32}$= c32+19T = 23T+19T= 42T
HCLA16bit$_{63,48}$: Sum$_{63,48}$= c48+19T = 25T+19T= 44T