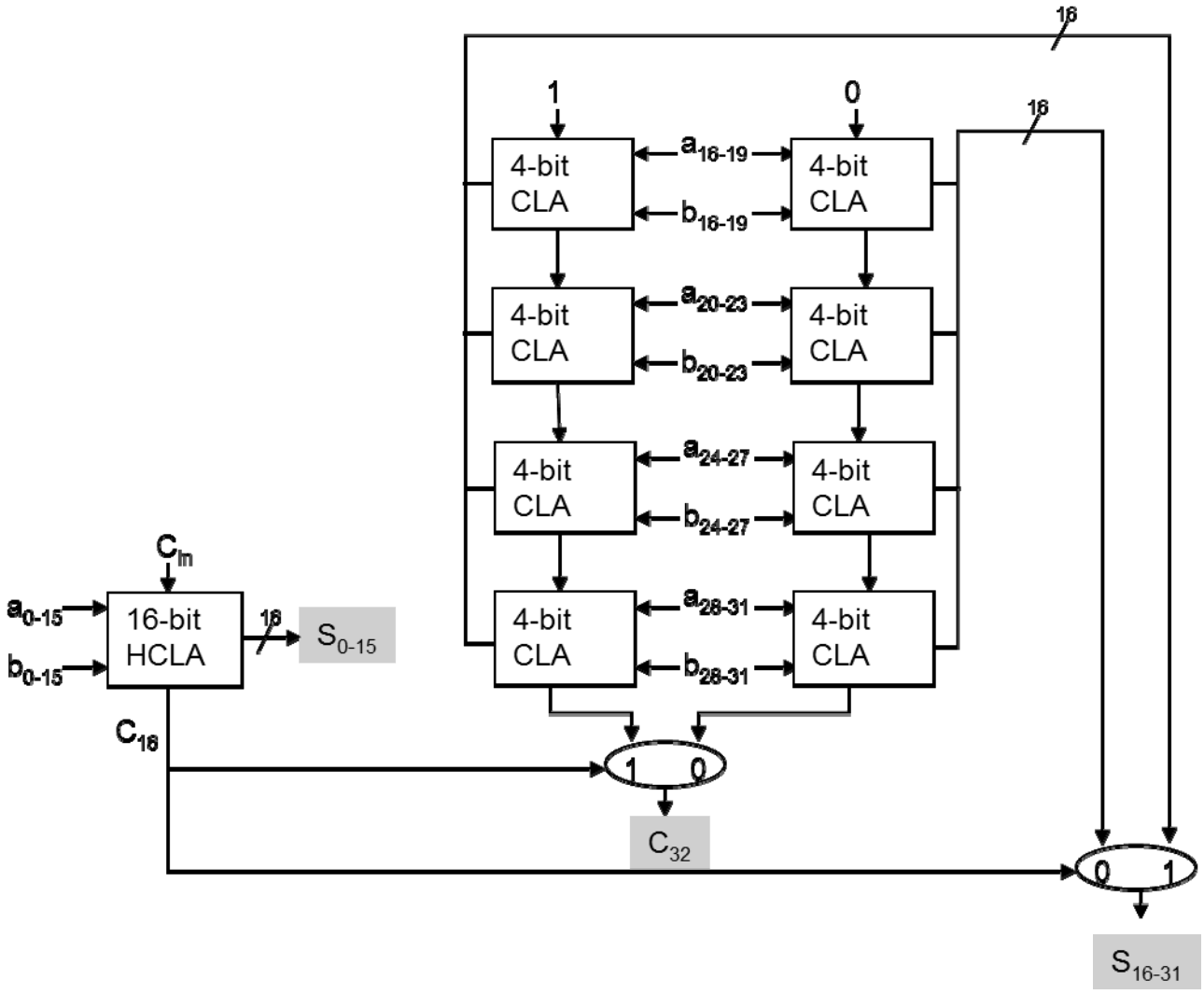
Assume for the rest of this problem that all logic gates have the following delays:

Fan In	Delay
1	5T
2	8T
3	12T
4	15T
5	20T
6	24T
7 or more	4T x fan-in

So a 2-input AND gate would have delay 8T and a 4-input OR gate would have delay 15T.

For simplicity, assume that mux's have delay 10T regardless of fan-in.

We will create a 32-bit adder out of some building blocks we've covered in class. We will use the 4-bit CLA that we covered in class as one basic building block of this design. And we will use it (as we did in class) to make 16-bit hierarchical CLAs (HCLA) which will be our other building block. But instead of connecting these in series to make a 32-bit adder, we will use carry select to speed up the 32-bit adder. The design will look as follows (be sure to note where we are using CLAs and where we are using HCLAs):

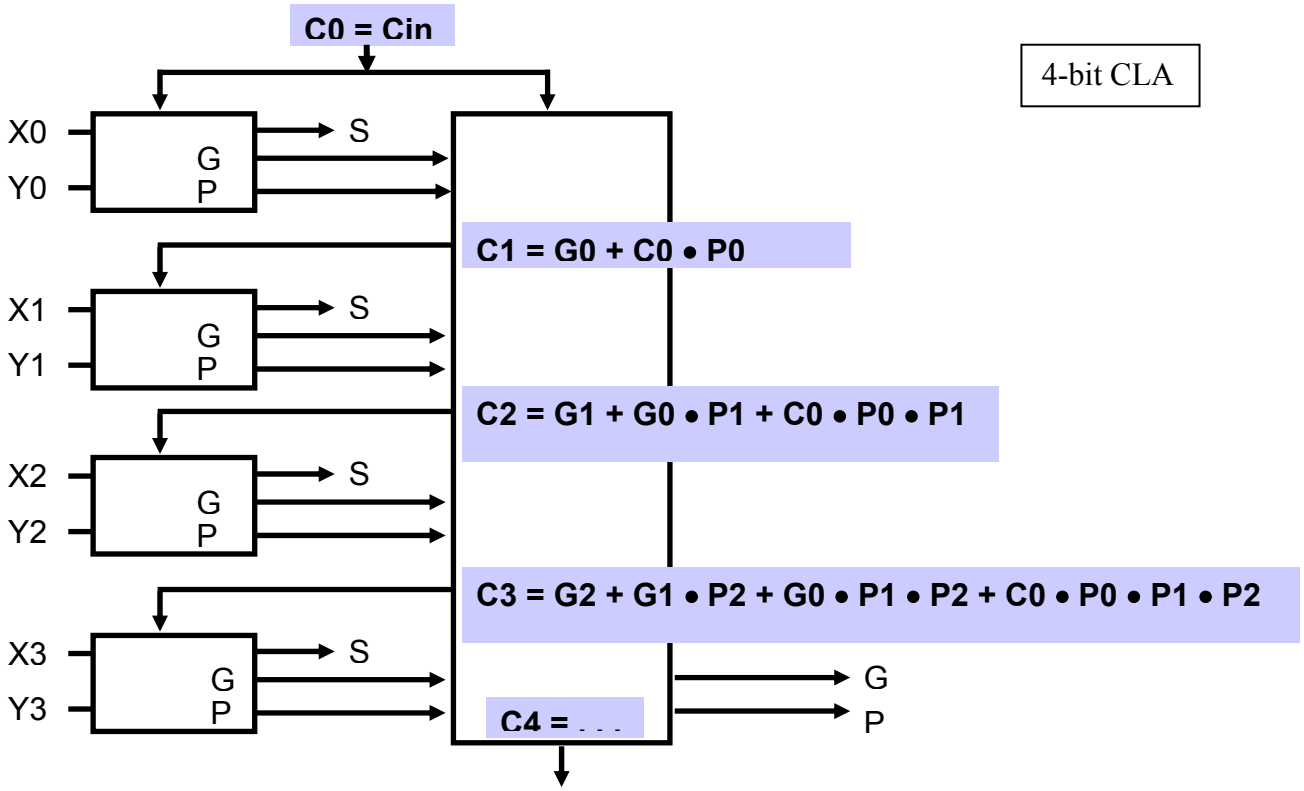

16
1
0
16
4-bit CLA
4-bit CLA
a_{16-19}
b_{16-19}
4-bit CLA
4-bit CLA
a_{20-23}
b_{20-23}
4-bit CLA
4-bit CLA
a_{24-27}
b_{24-27}
4-bit CLA
4-bit CLA
a_{28-31}
b_{28-31}
C_{in}
a_{0-15}
b_{0-15}
16-bit HCLA
16
S_{0-15}
C_{16}
1 0
C_{32}
0 1
S_{16-31}

Your task is to find the maximal delay of this design – i.e. determine the delays of $S_{0\text{-}31}$ and C_{32} – the maximal delay of these outputs will be the maximal delay of the design. Fill in the values in the table on the following page to receive full credit (and to help with possible partial credit).

Output	Delay	
G0		*(2 points)*
P0		*(2 points)*
Gα		*(2 points)*
Pα		*(2 points)*
C12		*(2 points)*
C15		*(2 points)*
C16		*(2 points)*
S15		*(2 points)*
C20		*(2 points)*
S19		*(2 points)*
C24		*(2 points)*
C31		*(2 points)*
C32 (after mux)		*(2 points)*
S31 (after mux)		*(2 points)*

Find the maximum delay **in terms of T** of the 32-bit adder – take the maximum of all output bits – including the sum bits (S_0-S_{31}) and the final carry out (C_{32}). Show your work clearly in the table above. The two figures on the following pages are taken from the class notes, if you need to refer to them.

Maximal Delay: _____ *(2 points)*


C0 = Cin
4-bit CLA
X0
Y0
G
P
S
C1 = G0 + C0 • P0
X1
Y1
G
P
S
C2 = G1 + G0 • P1 + C0 • P0 • P1
X2
Y2
G
P
S
C3 = G2 + G1 • P2 + G0 • P1 • P2 + C0 • P0 • P1 • P2
X3
Y3
G
P
S
C4 = . . .
G
P

16-bit Hierarchical CLA