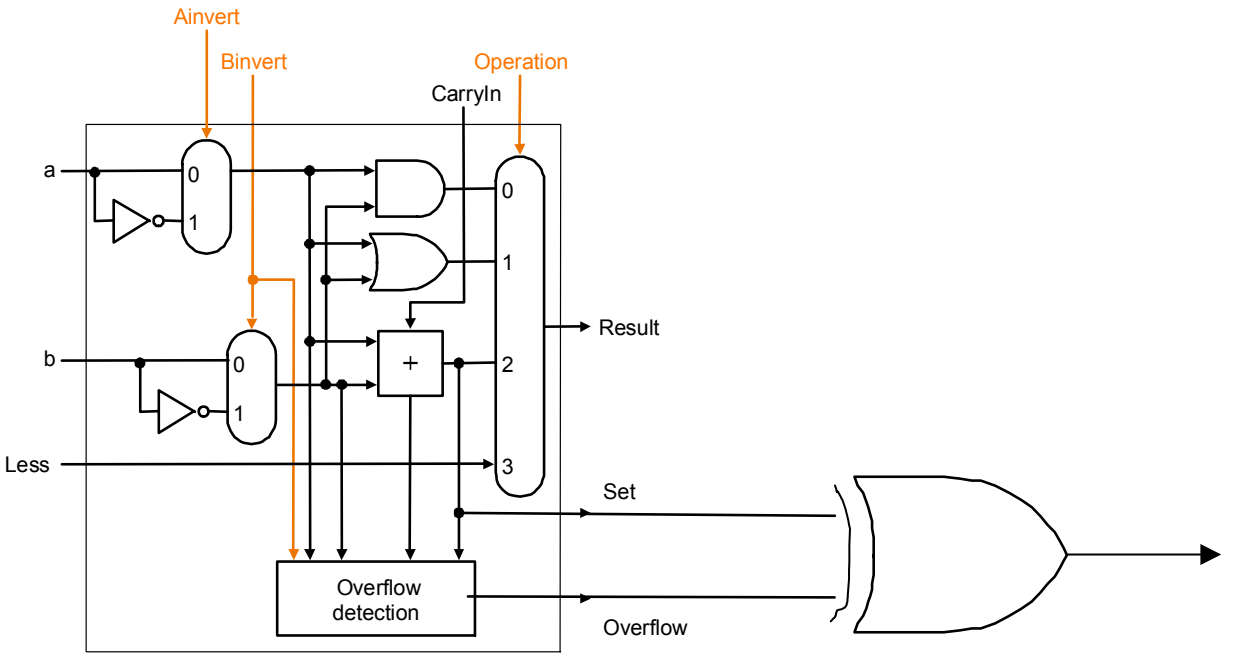
CS151B/EE116C – Solutions to Homework #2

Problem (1) B.24

If there is no overflow, the circuitry shown in Figure C.B.10 is sufficient – the "Set" output from bit 31 (the sign bit) can be used as the "Less" input for bit 0. However, if there is an overflow, the inverse of the sign bit must be used as the "Less" input for bit 0. Both cases are handled correctly by the following circuitry (replacing the bottom part – bit 31 – of Figure B.5.10):



"Less" input of bit 0

Problem (2) B.26

$c4 = G_{3,0} + (P_{3,0} \bullet c0)$
$c8 = G_{7,4} + (P_{7,4} \bullet G_{3,0}) + (P_{7,4} \bullet P_{3,0} \bullet c0)$
$c12 = G_{11,8} + (P_{11,8} \bullet G_{7,4}) + (P_{11,8} \bullet P_{7,4} \bullet G_{3,0}) + (P_{11,8} \bullet P_{7,4} \bullet P_{3,0} \bullet c0)$
$c16 = G_{15,12} + (P_{15,12} \bullet G_{11,8}) + (P_{15,12} \bullet P_{11,8} \bullet G_{7,4}) + (P_{15,12} \bullet P_{11,8} \bullet P_{7,4} \bullet G_{3,0}) + (P_{15,12} \bullet P_{11,8} \bullet P_{7,4} \bullet P_{3,0} \bullet c0)$

Problem (3) B. 27

$c16 = G_{15,0} + (P_{15,0} \bullet c0)$
$c32 = G_{31,16} + (P_{31,16} \bullet G_{15,0}) + (P_{31,16} \bullet P_{15,0} \bullet c0)$
$c48 = G_{47,32} + (P_{47,32} \bullet G_{31,16}) + (P_{47,32} \bullet P_{31,16} \bullet G_{15,0}) + (P_{47,32} \bullet P_{31,16} \bullet P_{15,0} \bullet c0)$
$c64 = G_{63,48} + (P_{63,48} \bullet G_{47,32}) + (P_{63,48} \bullet P_{47,32} \bullet G_{31,16}) + (P_{63,48} \bullet P_{47,32} \bullet P_{31,16} \bullet G_{15,0}) + (P_{63,48} \bullet P_{47,32} \bullet P_{31,16} \bullet P_{15,0} \bullet c0)$

Problem (4) B. 30

Answer A:
Assumption: any gate delay = T, regardless of the number of inputs
1-bit full adder: CarryOut =2T, Sum =2T (Both of them are sum of products)

a. 64bit ripple carry adder: c64=128T, Sum_{63}=128T since 64 × 2T = 128T

b. 64bit ripple carry of 4bit carry-lookahead adder: c64 = 35T, Sum_{63}=37T
The delay of carry-lookahead unit: c1 ~ c4 =2T, G=2T, P=1T

Thus, the delay of CLA4bit adders:
$CLA4bit_{3,0}$: pi, gi = 1T, carry-lookahead unit(CLU) = 2T, c0 = 0T → c1~c4 = 3T , $Sum_{3,0}$ = 5T
$CLA4bit_{7,4}$: pi, gi = 1T, CLU= 2T, c4 = 3T → c5~c8 = 5T , $Sum_{7,4}$ = 7T
$CLA4bit_{11,8}$: pi, gi = 1T, CLU= 2T, c8 = 5T → c9~c12 = 7T, $Sum_{11,8}$ = 9T
$CLA4bit_{15,12}$: pi, gi = 1T, CLU= 2T, c12 = 7T → c13~ c15= 9T, $Sum_{15,12}$ = 11T
…
$CLA4bit_{63,60}$: pi, gi = 1T, CLU= 2T, c60 = 33T → c61~ c64= 35T, $Sum_{15,12}$ = 37T

c. 64bit ripple carry of 16bit hierarchical carry-lookahead adder: c64 = 11T, Sum=15T
Unlike normal CLA4bit adder, each CLA4bit adder does not have the carry-out since these carry-out signals are generated in the CLU-2lev unit.

$HCLA16bit_{15,0}$: CLU-2lev generates c4, c8, c12, c16 at 5T since c0=0T
- $CLA4bit_{3,0}$: pi, gi = 1T, CLU= 2T, c0=0T → c1~c3=3T, $Sum_{3,0}$ = 5T
- $CLA4bit_{7,4}$: pi, gi = 1T, CLU= 2T, c4 = 5T→ c5~c7=7T, $Sum_{7,4}$ = 9T
- $CLA4bit_{11,8}$: pi, gi = 1T, CLU= 2T, c8 = 5T → c9~c11=7T, $Sum_{11,8}$ = 9T
- $CLA4bit_{15,12}$: pi, gi = 1T, CLU= 2T, c12 = 5T → c13~c15=7T, $Sum_{15,12}$ = 9T

$HCLA16bit_{31,16}$: CLU-2lev generates c20, c24, c28, c32 at 7T since c16=5T
- $CLA4bit_{19,16}$: pi, gi = 1T, CLU= 2T, c16=5T →c17~c19=7T, $Sum_{19,16}$ = 9T
- $CLA4bit_{23,20}$: pi, gi = 1T, CLU= 2T, c20 = 7T→ c21~c23=9T, $Sum_{23,20}$ = 11T
- $CLA4bit_{27,24}$: pi, gi = 1T, CLU= 2T, c24 = 7T → c25~c27=9T , $Sum_{27,24}$ = 11T
- $CLA4bit_{31,28}$: pi, gi = 1T, CLU= 2T, c28 = 7T → c29~c31=9T , $Sum_{31,28}$ = 11T

$HCLA16bit_{47,32}$: CLU-2lev generates c36, c40, c44, c48 at 9T since c32=7T
- …

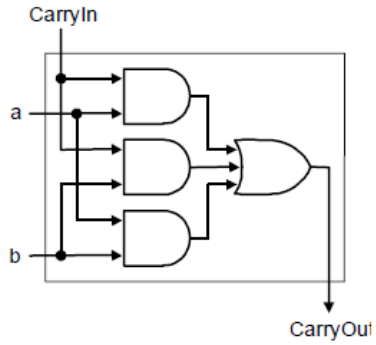
$HCLA16bit_{63,48}$: CLU-2lev generates c52, c56, c60, c64 at 11T since c48=9T
- $CLA4bit_{51,48}$: pi, gi = 1T, CLU= 2T, c48 = 9T →c49~c51=11T, $Sum_{51,48}$ = 13T
- $CLA4bit_{55,52}$: pi, gi = 1T, CLU= 2T, c52 = 11T → c52~c55=13T, $Sum_{55,52}$ = 15T
- $CLA4bit_{59,56}$: pi, gi = 1T, CLU= 2T, c56 = 11T → c56~c59=13T , $Sum_{59,56}$ = 15T
- $CLA4bit_{63,60}$: pi, gi = 1T, CLU= 2T, c60 = 11T → c60~c63=13T , $Sum_{63,60}$ = 15T

d. 64bit three-level carry-lookahead adder: c64=7T, Sum=13T
Unlike normal HCLA16bit adder, each HCLA16bit adder does not have the carry-out since these carry-out signals are generated in the CLU-3lev unit.

CLU-3lev generates c16, c32, c48, c64 at 7T since c0=0T

HCLA16bit$_{15,0}$: CLU-2lev generates c4, c8, c12 at 5T since c0=0T
HCLA16bit$_{31,16}$: CLU-2lev generates c20, c24, c28 at 9T since c16=7T
HCLA16bit$_{47,32}$: CLU-2lev generates c36, c40, c44 at 9T since c32=7T
HCLA16bit$_{63,48}$: CLU-2lev generates c52, c56, c60 at 9T since c48=7T
CLA4bit$_{51,48}$: pi, gi = 1T, CLU= 2T, c48 = 7T →c49~c51=9T, Sum$_{51,48}$ = 11T
CLA4bit$_{55,52}$: pi, gi = 1T, CLU= 2T, c52 = 9T → c52~c55=11T, Sum$_{55,52}$ = 13T
CLA4bit$_{59,56}$: pi, gi = 1T, CLU= 2T, c56 = 9T → c56~c59=11T , Sum$_{59,56}$ = 13T
CLA4bit$_{63,60}$: pi, gi = 1T, CLU= 2T, c60 = 9T → c60~c63=11T , Sum$_{63,60}$ = 13T

Answer B:
Assumption: a delay of gate is proportion to the number of inputs
1bit full adder: CarryOut = 2T+3T = 5T, Sum=3T (a xor b xor c)



a. 64bit ripple carry adder: c64=320T (5T×64), Sum$_{63}$= 318T (c63+3T)

b. 64bit ripple carry of 4bit carry-lookahead adder: c64 = 76T, Sum$_{63}$=79T
Carry-lookhead unit implementation is based on "carry-lookahead.pdf" in the courseweb.

Thus, each CLA4bit adders' delays follow:
CLA4bit$_{3,0}$: pi, gi = 2T, c0 = 0T → c1=4T, c2=8T, c3=10T, c4=12T , Sum$_{3,0}$ = 13T (c3+3T)
CLA4bit$_{7,4}$: pi, gi = 2T, c4=12T → c5=16T, c6=16T, c7=16T, c8=16T , Sum$_{7,4}$ = 19T (c7+3T)
CLA4bit$_{11,8}$: pi, gi = 2T, c8 = 16T→ c9=20T, c10=20T, c11=20T, c12=20T , Sum$_{11,8}$ = 23T (c20+3T)
CLA4bit$_{15,12}$:pi, gi = 2T, c12 = 20T→ c13=24T, c14=24T, c15=24T, c16=24T, Sum$_{15,12}$ = 27T (c15+3T)
…
CLA4bit$_{63,60}$: pi, gi = 2T, c60 = 72T → c61=76T, c62=76T, c63=76T, c64= 76T, Sum$_{15,12}$ = 79T

c. 64bit ripple carry of 16bit hierarchical carry-lookahead adder: c64 = 32T, Sum=39T
HCLA16bit$_{15,0}$: CLU-2lev generates c4=12T, c8=16T, c12=18T, c16=20T, Sum$_{15,0}$=25T (c12+7T)
HCLA16bit$_{31,16}$: CLU-2lev generates c20=24T, c24=24T, c28=24T, c32=24T, Sum$_{31,16}$=31T (c28+7T)
HCLA16bit$_{47,32}$: CLU-2lev generates c36=28T, c40=28T, c44=28T, c48=28T, Sum$_{47,32}$=35T (c44+7T)
HCLA16bit$_{63,48}$: CLU-2lev generates c52=32T, c56=32T, c60=32T, c64=32T, Sum$_{63,48}$=39T (c60+7T)

d. 64bit three-level carry-lookahead adder: c64=28T, Sum=37T
CLU-3lev generates c16=20T, c32=24T, c48=26T, c64=28T at 7T since c0=0T, Gi=18T, and Pi=10T
HCLA16bit$_{15,0}$: CLU-2lev generates c4=12T, c8=16T, c12=18T, Sum$_{15,0}$=25T (c12+7T)
HCLA16bit$_{31,16}$: CLU-2lev generates c20=24T, c24=24T, c28=24T,Sum$_{31,16}$=31T (c28+7T)
HCLA16bit$_{47,32}$: CLU-2lev generates c36=28T, c40=28T, c44=28T, Sum$_{47,32}$=35T (c44+7T)
HCLA16bit$_{63,48}$: CLU-2lev generates c52=30T, c56=30T, c60=30T, Sum$_{63,48}$=37T (c60+7T)